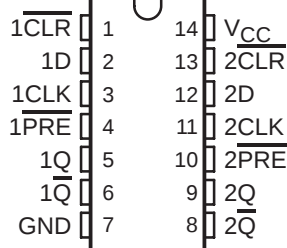


# SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

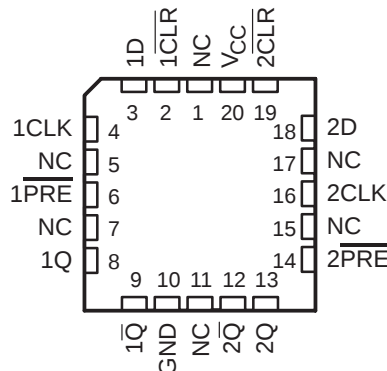
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- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 10.5 ns at 5 V
- Inputs Are TTL-Voltage Compatible

SN54ACT74 . . . J OR W PACKAGE  
SN74ACT74 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54ACT74 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'ACT74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) input sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

## ORDERING INFORMATION

| $T_A$          | PACKAGE <sup>†</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|---------------|-----------------------|------------------|
| -40°C to 85°C  | PDIP – N             | Tube          | SN74ACT74N            | SN74ACT74N       |
|                | SOIC – D             | Tube          | SN74ACT74D            | ACT74            |
|                |                      | Tape and reel | SN74ACT74DR           |                  |
|                | SOP – NS             | Tape and reel | SN74ACT74NSR          | ACT74            |
|                | SSOP – DB            | Tape and reel | SN74ACT74DBR          | AD74             |
| -55°C to 125°C | TSSOP – PW           | Tube          | SN74ACT74PW           | AD74             |
|                |                      | Tape and reel | SN74ACT74PWR          |                  |
|                | CDIP – J             | Tube          | SNJ54ACT74J           | SNJ54ACT74J      |
|                | CFP – W              | Tube          | SNJ54ACT74W           | SNJ54ACT74W      |
|                | LCCC – FK            | Tube          | SNJ54ACT74FK          | SNJ54ACT74FK     |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# SN54ACT74, SN74ACT74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH CLEAR AND PRESET

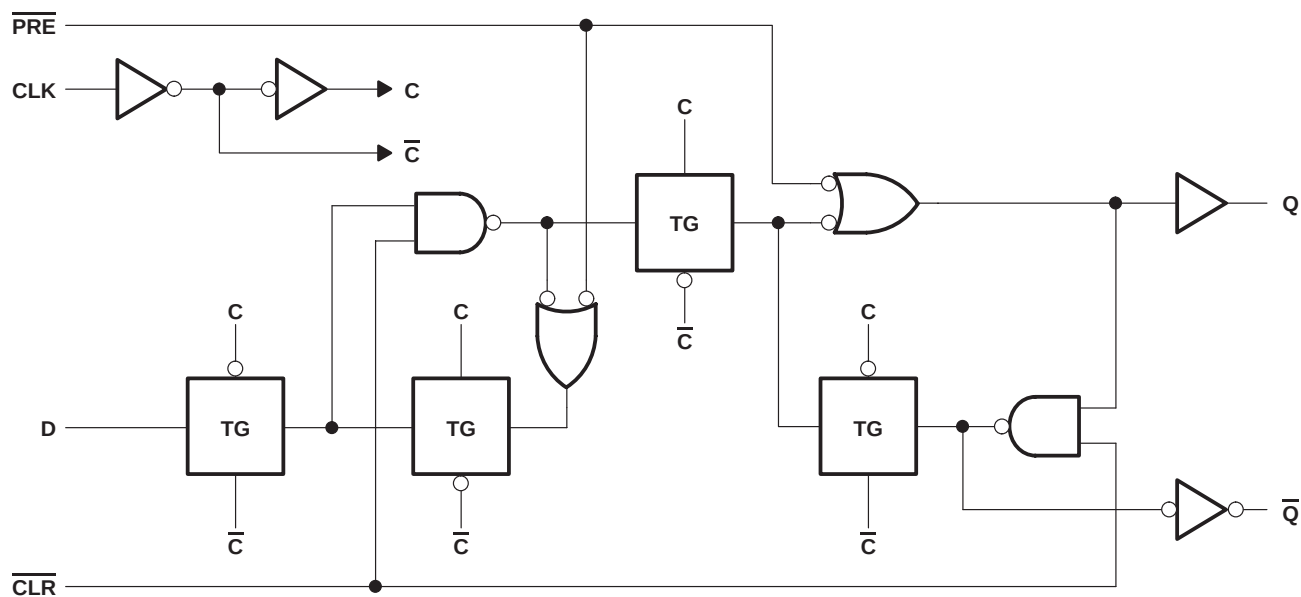
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FUNCTION TABLE  
(each flip-flop)

| INPUTS                  |                         |     |   | OUTPUTS        |                         |
|-------------------------|-------------------------|-----|---|----------------|-------------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | D | Q              | $\overline{\text{Q}}$   |
| L                       | H                       | X   | X | H              | L                       |
| H                       | L                       | X   | X | L              | H                       |
| L                       | L                       | X   | X | H <sup>†</sup> | H <sup>†</sup>          |
| H                       | H                       | ↑   | H | H              | L                       |
| H                       | H                       | ↑   | L | L              | H                       |
| H                       | H                       | L   | X | Q <sub>0</sub> | $\overline{\text{Q}}_0$ |

<sup>†</sup> This configuration is nonstable; that is, it does not persist when either  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

#### logic diagram, each flip-flop (positive logic)



# SN54ACT74, SN74ACT74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH CLEAR AND PRESET

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                  |                            |
|------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                   | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                          | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, $V_O$ (see Note 1)                         | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )    | ±20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )   | ±20 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )       | ±50 mA                     |
| Continuous current through $V_{CC}$ or GND                       | ±200 mA                    |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package | 86°C/W                     |
| DB package                                                       | 96°C/W                     |
| N package                                                        | 80°C/W                     |
| NS package                                                       | 76°C/W                     |
| PW package                                                       | 113°C/W                    |
| Storage temperature range, $T_{stg}$                             | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

|                                                        | SN54ACT74 |          | SN74ACT74 |          | UNIT |
|--------------------------------------------------------|-----------|----------|-----------|----------|------|
|                                                        | MIN       | MAX      | MIN       | MAX      |      |
| $V_{CC}$ Supply voltage                                | 4.5       | 5.5      | 4.5       | 5.5      | V    |
| $V_{IH}$ High-level input voltage                      | 2         |          | 2         |          | V    |
| $V_{IL}$ Low-level input voltage                       |           | 0.8      |           | 0.8      | V    |
| $V_I$ Input voltage                                    | 0         | $V_{CC}$ | 0         | $V_{CC}$ | V    |
| $V_O$ Output voltage                                   | 0         | $V_{CC}$ | 0         | $V_{CC}$ | V    |
| $I_{OH}$ High-level output current                     |           | –24      |           | –24      | mA   |
| $I_{OL}$ Low-level output current                      |           | 24       |           | 24       | mA   |
| $\Delta t/\Delta v$ Input transition rise or fall rate |           | 8        |           | 8        | ns/V |
| $T_A$ Operating free-air temperature                   | –55       | 125      | –40       | 85       | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54ACT74, SN74ACT74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH CLEAR AND PRESET

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER          | TEST CONDITIONS                                               | V <sub>CC</sub> | T <sub>A</sub> = 25°C |       |      | SN54ACT74 |     | SN74ACT74 |      | UNIT |
|--------------------|---------------------------------------------------------------|-----------------|-----------------------|-------|------|-----------|-----|-----------|------|------|
|                    |                                                               |                 | MIN                   | TYP   | MAX  | MIN       | MAX | MIN       | MAX  |      |
| V <sub>OH</sub>    | I <sub>OH</sub> = -50 µA                                      | 4.5 V           | 4.4                   | 4.49  |      | 4.4       |     | 4.4       |      | V    |
|                    |                                                               | 5.5 V           | 5.4                   | 5.49  |      | 5.4       |     | 5.4       |      |      |
|                    | I <sub>OH</sub> = -24 mA                                      | 4.5 V           | 3.86                  |       |      | 3.7       |     | 3.76      |      |      |
|                    |                                                               | 5.5 V           | 4.86                  |       |      | 4.7       |     | 4.76      |      |      |
|                    | I <sub>OH</sub> = -50 mA†                                     | 5.5 V           |                       |       |      | 3.86      |     |           |      |      |
|                    | I <sub>OH</sub> = -75 mA†                                     | 5.5 V           |                       |       |      |           |     | 3.85      |      |      |
| V <sub>OL</sub>    | I <sub>OL</sub> = 50 µA                                       | 4.5 V           |                       | 0.001 | 0.1  |           | 0.1 |           | 0.1  | V    |
|                    |                                                               | 5.5 V           |                       | 0.001 | 0.1  |           | 0.1 |           | 0.1  |      |
|                    | I <sub>OL</sub> = 24 mA                                       | 4.5 V           |                       |       | 0.36 |           | 0.5 |           | 0.44 |      |
|                    |                                                               | 5.5 V           |                       |       | 0.36 |           | 0.5 |           | 0.44 |      |
|                    | I <sub>OL</sub> = 50 mA†                                      | 5.5 V           |                       |       |      | 1.65      |     |           |      |      |
|                    | I <sub>OL</sub> = 75 mA†                                      | 5.5 V           |                       |       |      |           |     | 1.65      |      |      |
| I <sub>I</sub>     | V <sub>I</sub> = V <sub>CC</sub> or GND                       | 5.5 V           |                       |       | ±0.1 |           | ±1  |           | ±1   | µA   |
| I <sub>CC</sub>    | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0   | 5.5 V           |                       |       | 2    |           | 40  |           | 20   | µA   |
| ΔI <sub>CC</sub> ‡ | One input at 3.4 V,<br>Other inputs at GND or V <sub>CC</sub> | 5.5 V           |                       | 0.6   |      |           | 1.6 |           | 1.5  | mA   |
| C <sub>i</sub>     | V <sub>I</sub> = V <sub>CC</sub> or GND                       | 5 V             |                       | 3     |      |           |     |           |      | pF   |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

timing characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|                    |                              |                     | T <sub>A</sub> = 25°C |     | SN54ACT74 |     | SN74ACT74 |     | UNIT |
|--------------------|------------------------------|---------------------|-----------------------|-----|-----------|-----|-----------|-----|------|
|                    |                              |                     | MIN                   | MAX | MIN       | MAX | MIN       | MAX |      |
| f <sub>clock</sub> | Clock frequency              |                     | 145                   |     | 85        |     | 125       |     | MHz  |
| t <sub>w</sub>     | Pulse duration               | PRE or CLR low      | 5                     |     | 7         |     | 6         |     | ns   |
|                    |                              | CLK                 | 5                     |     | 7         |     | 6         |     |      |
| t <sub>su</sub>    | Setup time, data before CLK↑ | Data                | 3                     |     | 4         |     | 3.5       |     | ns   |
|                    |                              | PRE or CLR inactive | 0                     |     | 0.5       |     | 0         |     |      |
| t <sub>h</sub>     | Hold time, data after CLK↑   |                     | 1                     |     | 1         |     | 1         |     | ns   |

switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)                                    | TO<br>(OUTPUT)             | SN54ACT74             |     |     |     |      | UNIT |
|------------------|----------------------------------------------------|----------------------------|-----------------------|-----|-----|-----|------|------|
|                  |                                                    |                            | T <sub>A</sub> = 25°C |     |     | MIN | MAX  |      |
|                  |                                                    |                            | MIN                   | TYP | MAX |     |      |      |
| f <sub>max</sub> |                                                    |                            | 145                   | 210 |     | 85  |      | MHz  |
| t <sub>PLH</sub> | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | 1                     | 5.5 | 9.5 | 1   | 11.5 | ns   |
| t <sub>PHL</sub> |                                                    |                            | 1                     | 6   | 10  | 1   | 12.5 |      |
| t <sub>PLH</sub> | CLK                                                | Q or $\overline{\text{Q}}$ | 1                     | 7.5 | 11  | 1   | 14   | ns   |
| t <sub>PHL</sub> |                                                    |                            | 1                     | 6   | 10  | 1   | 12   |      |



# SN54ACT74, SN74ACT74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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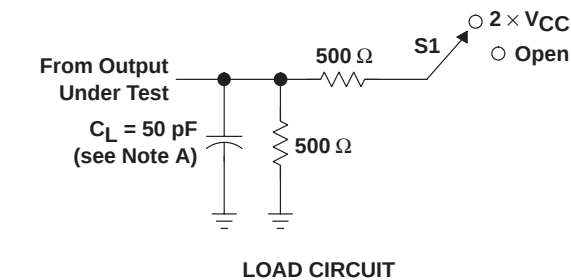
switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)                                    | TO<br>(OUTPUT)      | SN74ACT74             |     |     |     |      | UNIT |
|------------------|----------------------------------------------------|---------------------|-----------------------|-----|-----|-----|------|------|
|                  |                                                    |                     | T <sub>A</sub> = 25°C |     |     | MIN | MAX  |      |
|                  |                                                    |                     | MIN                   | TYP | MAX |     |      |      |
| f <sub>max</sub> |                                                    |                     | 145                   | 210 |     | 125 |      | MHz  |
| t <sub>PLH</sub> | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{Q}$ | 3                     | 5.5 | 9.5 | 2.5 | 10.5 | ns   |
| t <sub>PHL</sub> |                                                    |                     | 3                     | 6   | 10  | 3   | 11.5 |      |
| t <sub>PLH</sub> | CLK                                                | Q or $\overline{Q}$ | 4                     | 7.5 | 11  | 4   | 13   | ns   |
| t <sub>PHL</sub> |                                                    |                     | 3.5                   | 6   | 10  | 3   | 11.5 |      |

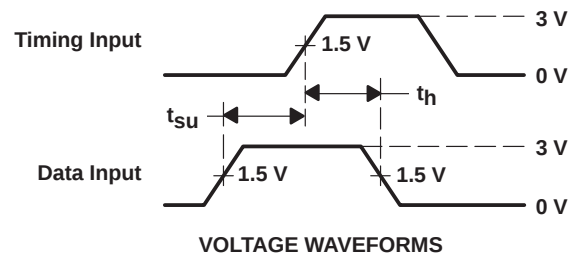
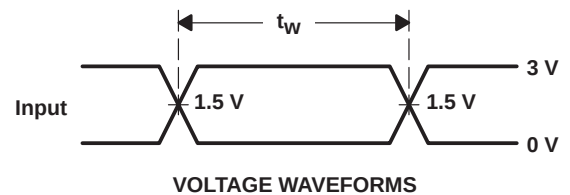
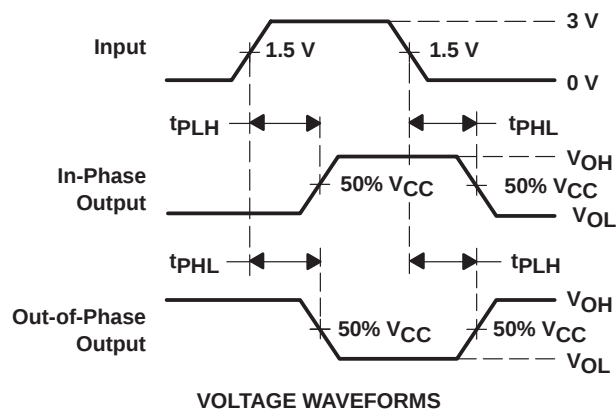
operating characteristics,  $V_{\text{CC}} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER                                     | TEST CONDITIONS                           | TYP | UNIT |
|-----------------------------------------------|-------------------------------------------|-----|------|
| $C_{\text{pd}}$ Power dissipation capacitance | $C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$ | 45  | pF   |

### PARAMETER MEASUREMENT INFORMATION



| TEST                            | S1   |
|---------------------------------|------|
| $t_{\text{PLH}}/t_{\text{PHL}}$ | Open |



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $\text{PRR} \leq 1\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                 | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-----------------------------------------|-------------------------|
| 5962-8752501M2A  | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>8752501M2A<br>SNJ54ACT<br>74FK | <a href="#">Samples</a> |
| 5962-8752501MCA  | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8752501MC<br>A<br>SNJ54ACT74J      | <a href="#">Samples</a> |
| 5962-8752501MDA  | ACTIVE        | CFP          | W                  | 14   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8752501MD<br>A<br>SNJ54ACT74W      | <a href="#">Samples</a> |
| SN74ACT74D       | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | ACT74                                   | <a href="#">Samples</a> |
| SN74ACT74DBR     | ACTIVE        | SSOP         | DB                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | AD74                                    | <a href="#">Samples</a> |
| SN74ACT74DE4     | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | ACT74                                   | <a href="#">Samples</a> |
| SN74ACT74DG4     | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | ACT74                                   | <a href="#">Samples</a> |
| SN74ACT74DR      | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | ACT74                                   | <a href="#">Samples</a> |
| SN74ACT74DRE4    | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | ACT74                                   | <a href="#">Samples</a> |
| SN74ACT74DRG4    | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | ACT74                                   | <a href="#">Samples</a> |
| SN74ACT74N       | ACTIVE        | PDIP         | N                  | 14   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | -40 to 85    | SN74ACT74N                              | <a href="#">Samples</a> |
| SN74ACT74NE4     | ACTIVE        | PDIP         | N                  | 14   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | -40 to 85    | SN74ACT74N                              | <a href="#">Samples</a> |
| SN74ACT74NSR     | ACTIVE        | SO           | NS                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | ACT74                                   | <a href="#">Samples</a> |
| SN74ACT74PW      | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | AD74                                    | <a href="#">Samples</a> |
| SN74ACT74PWR     | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | AD74                                    | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                 | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-----------------------------------------|-------------------------|
| SN74ACT74PWRE4   | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | AD74                                    | <a href="#">Samples</a> |
| SNJ54ACT74FK     | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>8752501M2A<br>SNJ54ACT<br>74FK | <a href="#">Samples</a> |
| SNJ54ACT74J      | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8752501MC<br>A<br>SNJ54ACT74J      | <a href="#">Samples</a> |
| SNJ54ACT74W      | ACTIVE        | CFP          | W                  | 14   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8752501MD<br>A<br>SNJ54ACT74W      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ACT74, SN74ACT74 :**

- Catalog: [SN74ACT74](#)
- Enhanced Product: [SN74ACT74-EP](#), [SN74ACT74-EP](#)
- Military: [SN54ACT74](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ACT74DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74ACT74NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ACT74PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



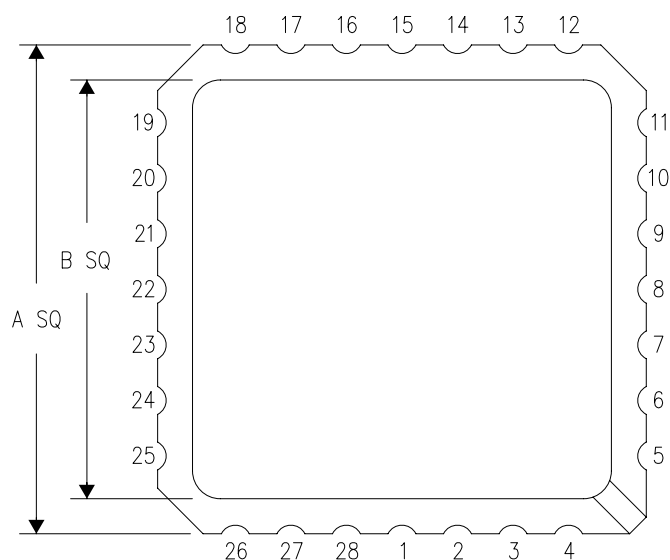
\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ACT74DR  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74ACT74NSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74ACT74PWR | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14

**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

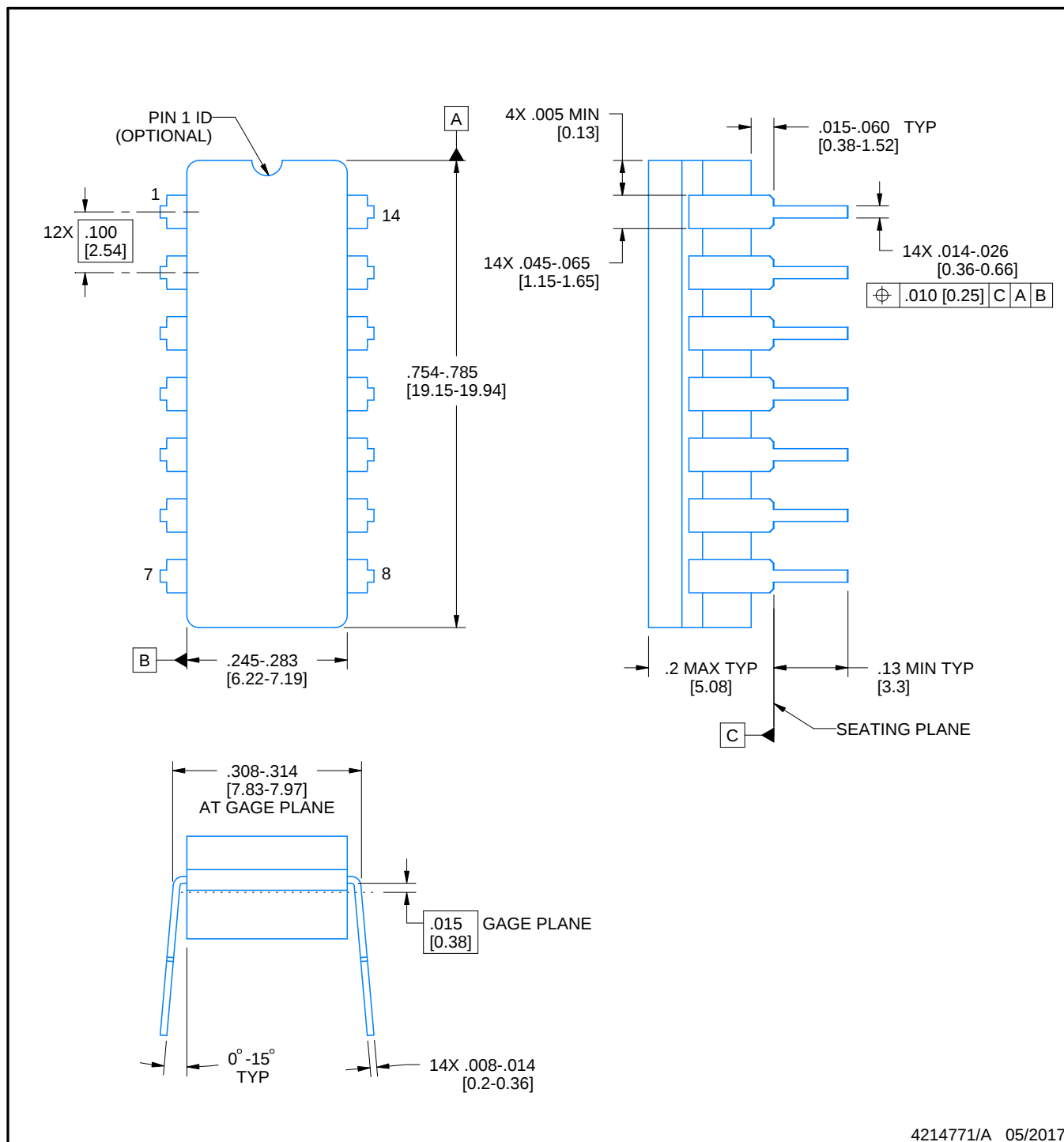


**J0014A**

## PACKAGE OUTLINE

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

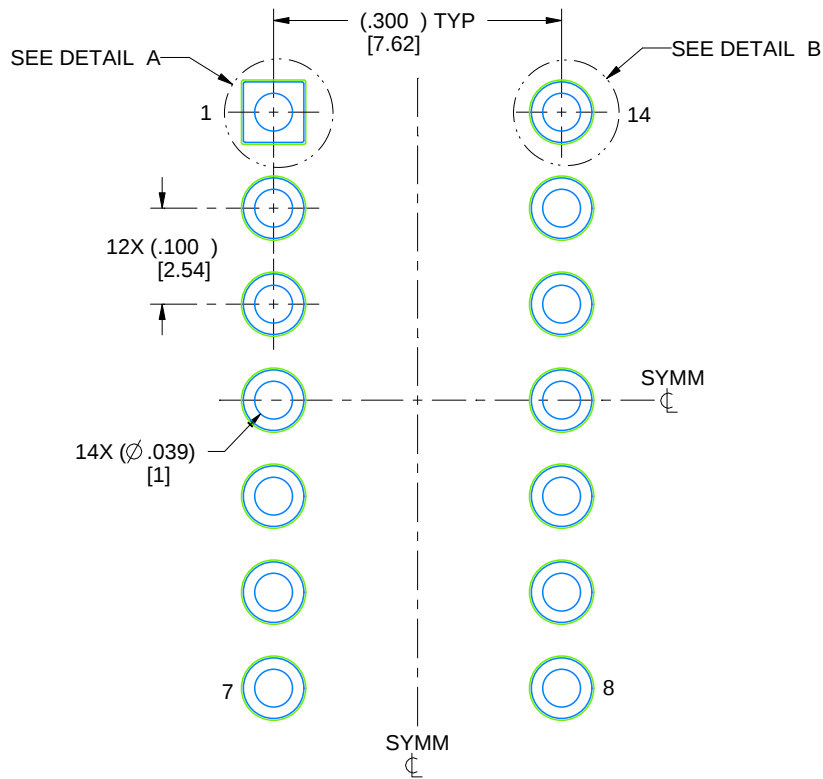
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

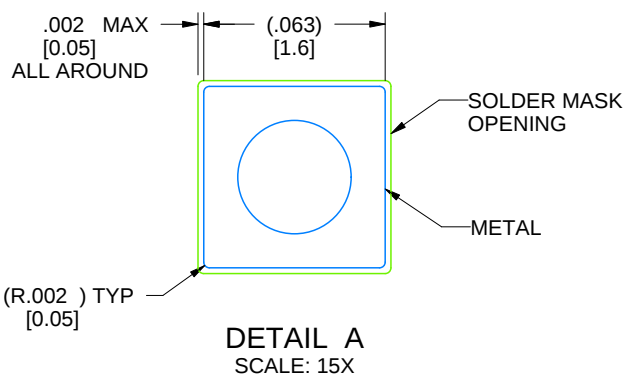
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

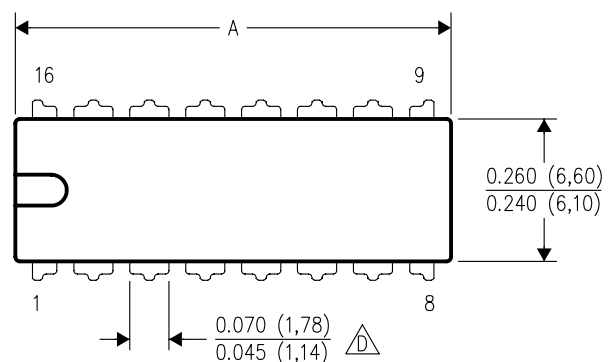


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

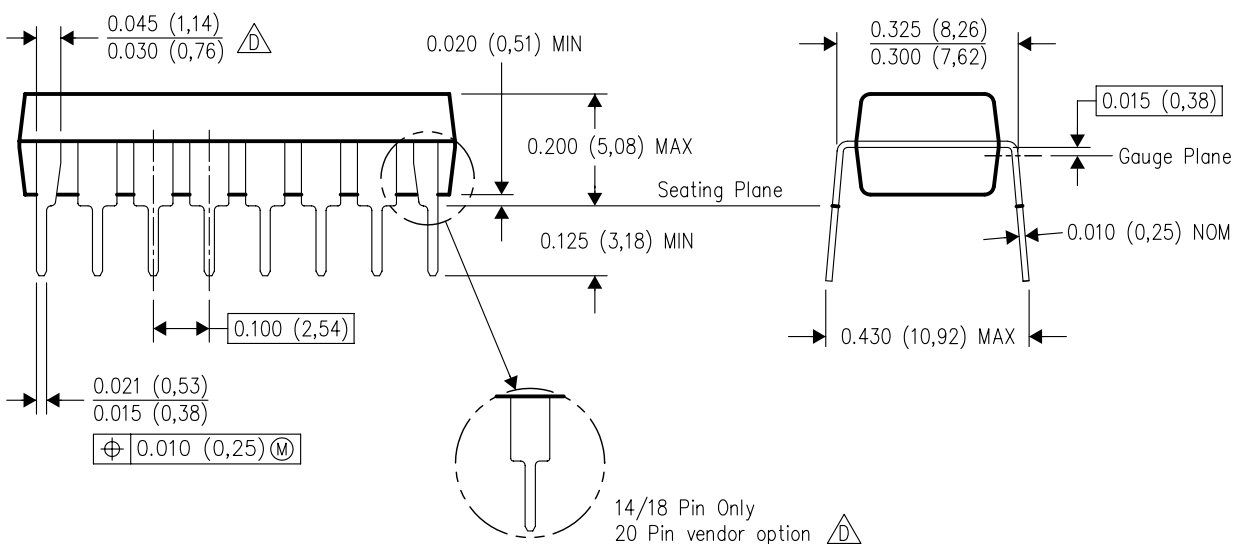
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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