CSD23202W10 12-V P-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Small Footprint 1 mm × 1 mm
- Low Profile 0.62-mm Height
- Pb Free
- Gate ESD Protection – 3 kV
- RoHS Compliant
- Halogen Free

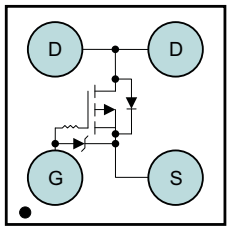
2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

This 12 V, 44 mΩ device is designed to deliver the lowest on-resistance and gate charge in a small 1 mm × 1 mm outline with excellent thermal characteristics in an ultra-low profile.

Top View



P0097-01

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–12		V
Q_g	Gate Charge Total (–4.5 V)	2.9		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.28		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.5 V	82	mΩ
		V_{GS} = –1.8 V	67	mΩ
		V_{GS} = –2.5 V	54	mΩ
		V_{GS} = –4.5 V	44	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.60		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD23202W10	3000	7-Inch Reel	1 × 1-mm Wafer Level Package	Tape and Reel
CSD23202W10T	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

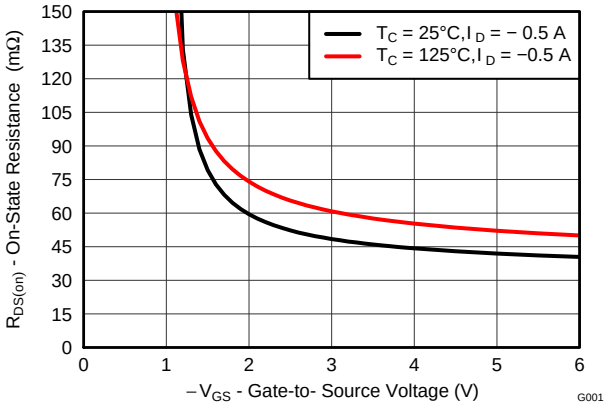
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–12	V
V_{GS}	Gate-to-Source Voltage	–6	V
I_D	Continuous Drain Current(1)	–2.2	A
I_{DM}	Pulsed Drain Current(2)	–25	A
I_G	Continuous Gate Clamp Current	–0.5	A
	Pulsed Gate Clamp Current	–7	A
P_D	Power Dissipation(1)	1	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Device operating at a temperature of 105°C

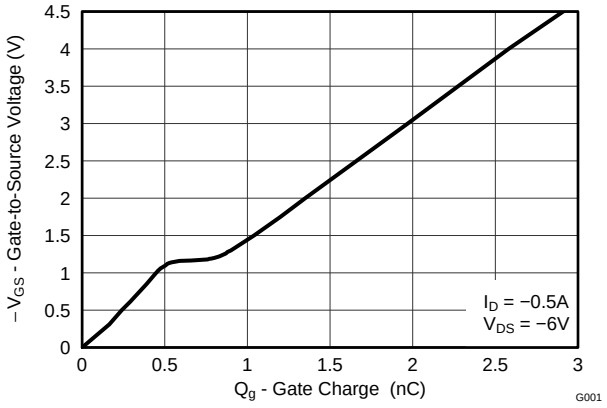
(2) Typ $R_{\theta JA}$ = 195°C/W, Pulse width ≤100 µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



G001

Gate Charge



G001

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
August 2014	*	Initial release.

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5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = –250 µA	–12			V
BV_{GSS}	Gate-to-Source Voltage;	V_{DS} = 0 V, I_G = –250 µA	–6		–7.2	V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –9.6 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.4	–0.6	–0.9	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.5 V, I_D = –0.5 A		82	123	mΩ
		V_{GS} = –1.8 V, I_D = –0.5 A		67	92	mΩ
		V_{GS} = –2.5 V, I_D = –0.5 A		54	66	mΩ
		V_{GS} = –4.5 V, I_D = –0.5 A		44	53	mΩ
g_{fs}	Transconductance	V_{DS} = –1.2 V, I_D = –0.5 A		5.6		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –6.0 V, f = 1 MHz		394	512	pF
C_{OSS}	Output Capacitance			238	310	pF
C_{RSS}	Reverse Transfer Capacitance			29	37	pF
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –6 V, I_D = –0.5 A		2.9	3.8	nC
Q_{gd}	Gate Charge Gate-to-Drain			0.28		nC
Q_{gs}	Gate Charge Gate-to-Source			0.55		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.29		nC
Q_{OSS}	Output Charge	V_{DS} = –6 V, V_{GS} = 0 V		2.0		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –0.5 A R_G = 0 Ω		9		ns
t_r	Rise Time			4		ns
$t_{d(off)}$	Turn Off Delay Time			58		ns
t_f	Fall Time			21		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = –0.5 A, V_{GS} = 0 V		–0.66	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= –6 V, I_F = –0.5 A, di/dt = 100 A/µs		3.7		nC
t_{rr}	Reverse Recovery Time			12		ns

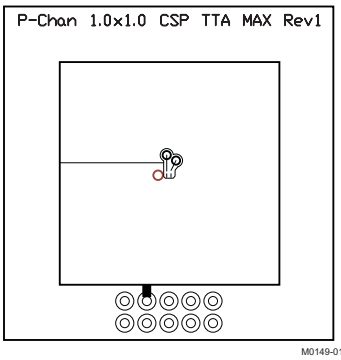
5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

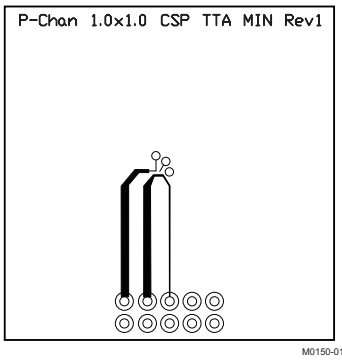
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)		195		°C/W
	Junction-to-Ambient Thermal Resistance(2)		65		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

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Typical $R_{\theta JA}$ = 65°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Typical $R_{\theta JA}$ = 195°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

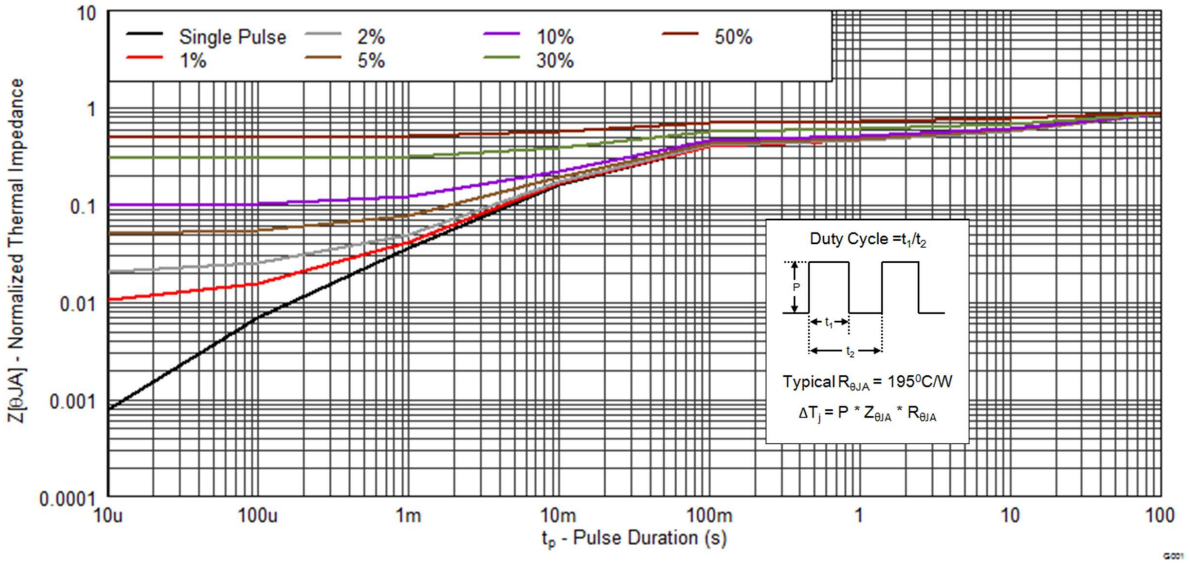


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

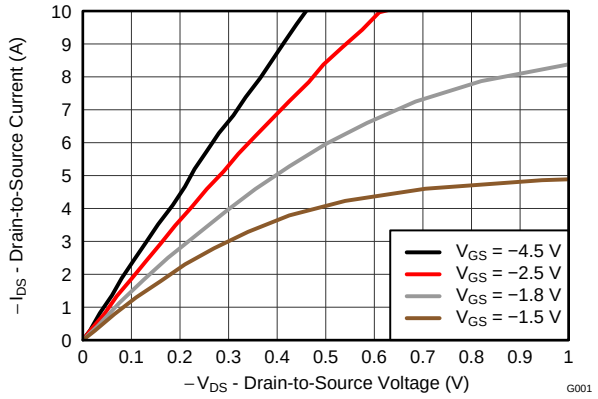


Figure 2. Saturation Characteristics

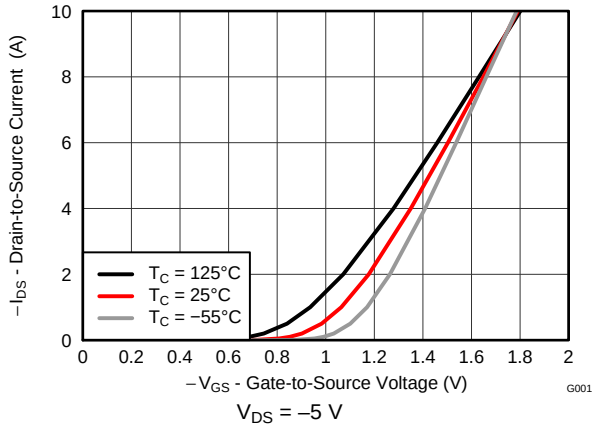


Figure 3. Transfer Characteristics

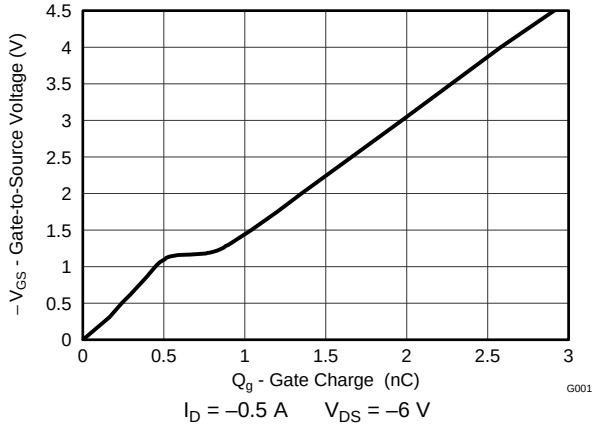


Figure 4. Gate Charge

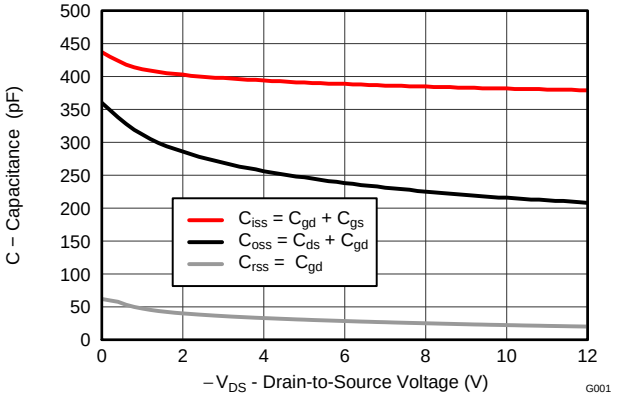


Figure 5. Capacitance

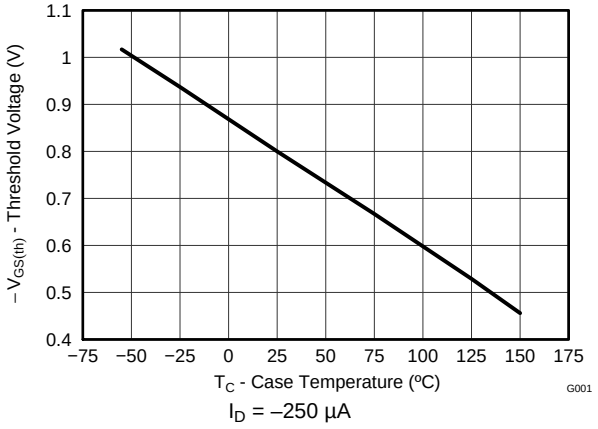


Figure 6. Threshold Voltage vs Temperature

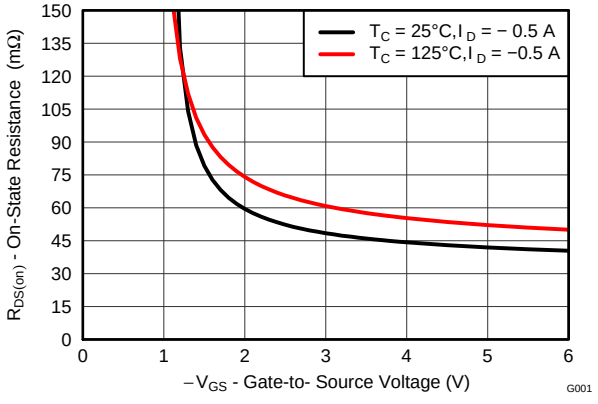


Figure 7. On-State Drain-to-Source Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

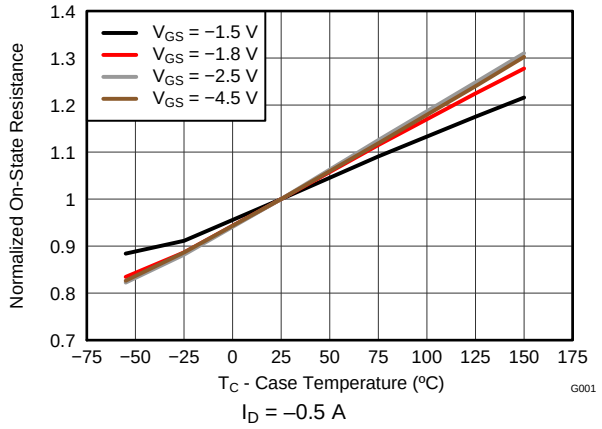


Figure 8. Normalized On-State Resistance vs Temperature

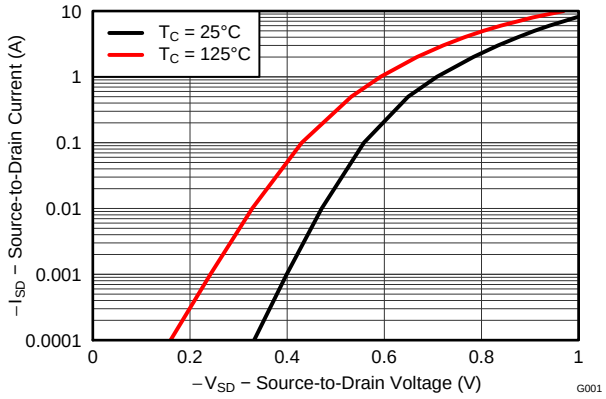


Figure 9. Typical Diode Forward Voltage

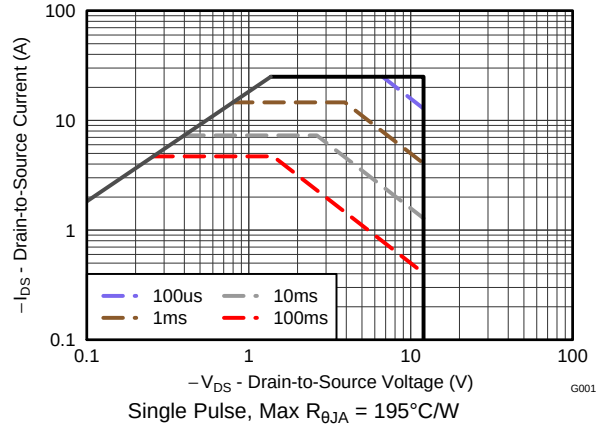


Figure 10. Maximum Safe Operating Area

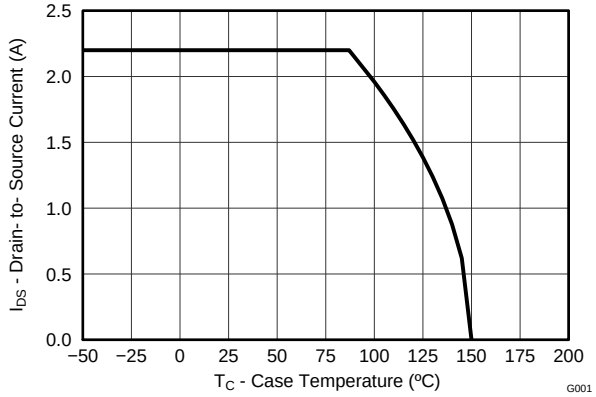


Figure 11. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

SLYZ022 — *TI Glossary*.

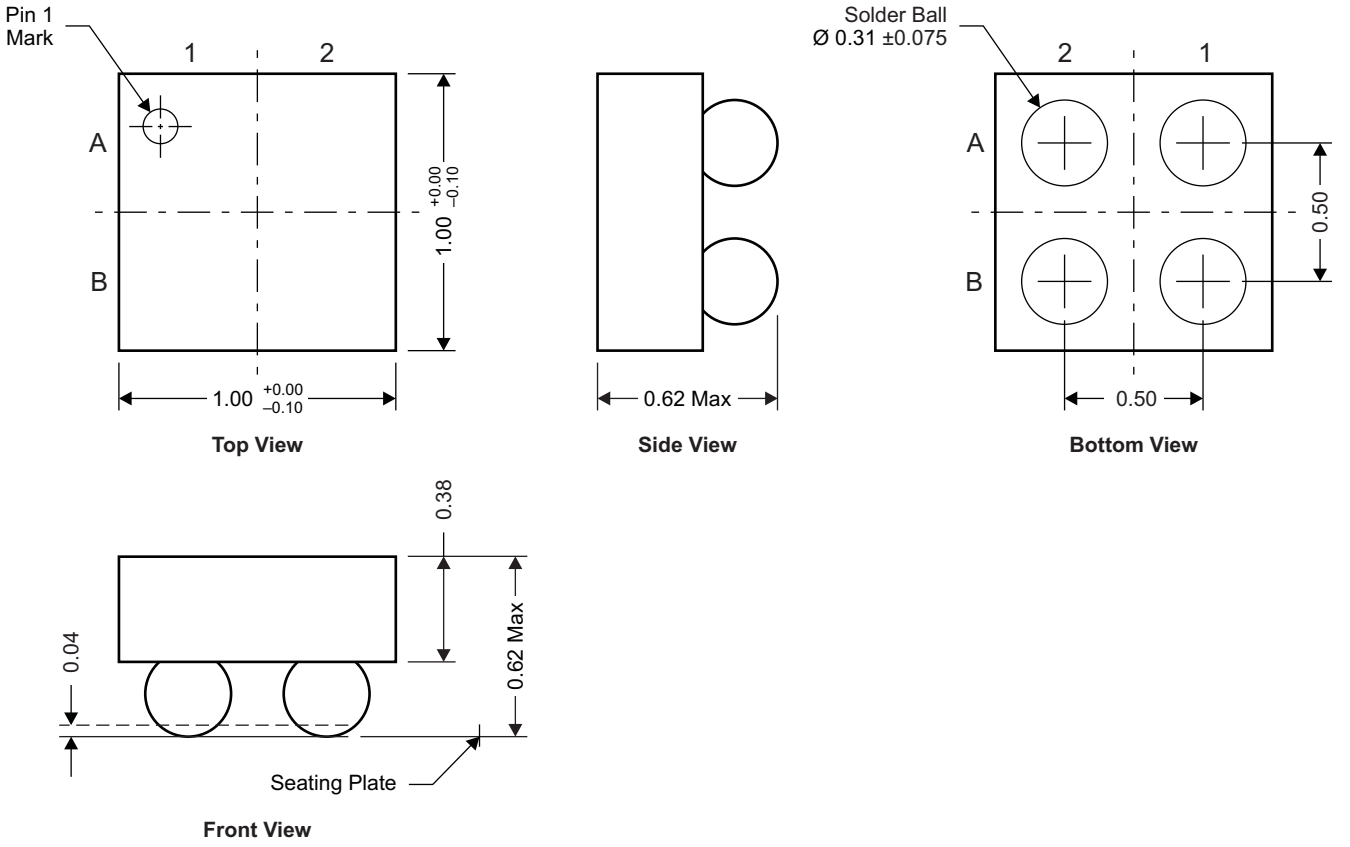
This glossary lists and explains terms, acronyms, and definitions.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD23202W10 Package Dimensions



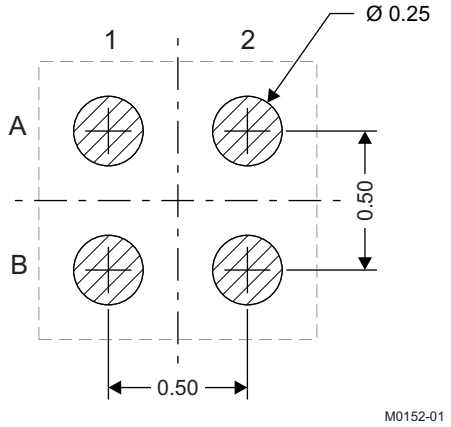
NOTE: All dimensions are in mm (unless otherwise specified).

Pin Configuration Table

POSITION	DESIGNATION
B1	Source
A1	Gate
A2, B2	Drain

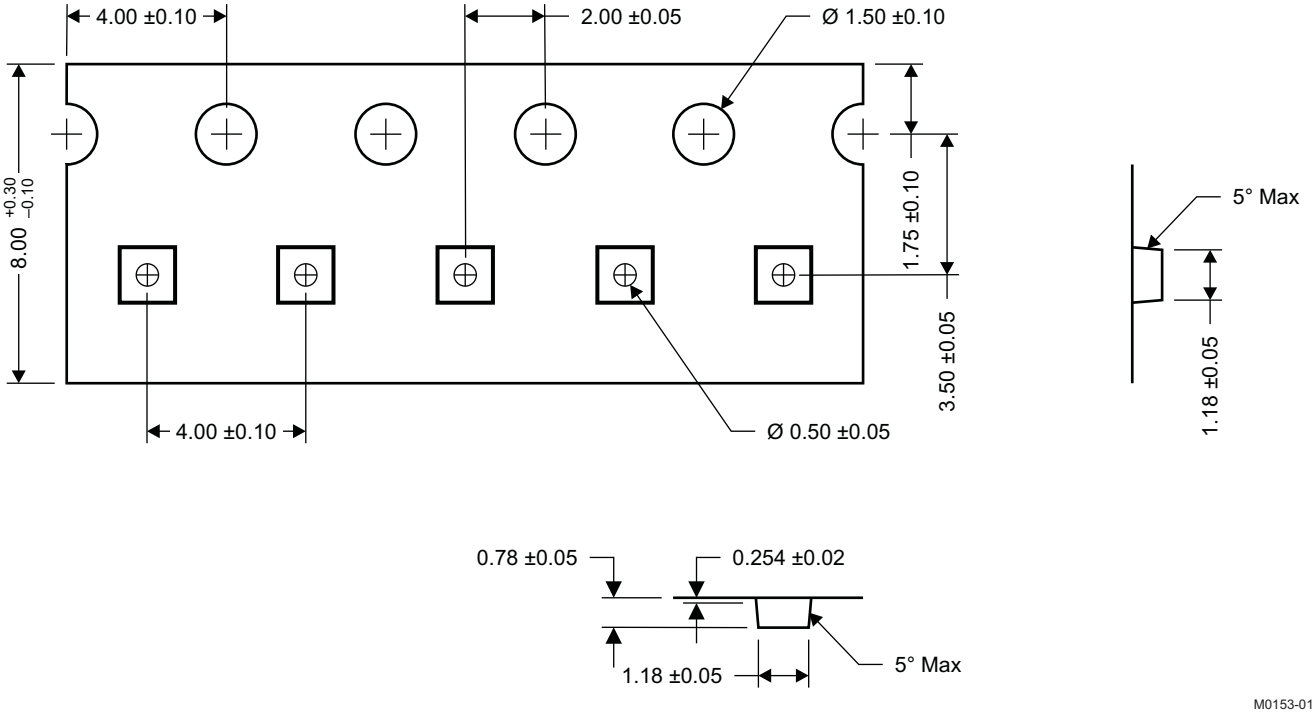
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7.2 Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified).

7.3 Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23202W10	ACTIVE	DSBGA	YZB	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		202	Samples
CSD23202W10T	ACTIVE	DSBGA	YZB	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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