9.5 GHz to 13.5 GHz, GaAs MMIC I/Q Upconverter

Preliminary Technical Data

HMC9059

FEATURES

- Conversion gain: 15 dB typical
- Sideband rejection: 22 dB typical
- Input power for 1 dB compression (P1dB): 5 dBm typical
- Output third-order intercept (OIP3): 30 dBm typical
- LO leakage at the RF output: −10 dBm typical
- LO leakage at the IF input: −40 dBm typical
- RF return loss: 15dB typical
- LO return loss: 10 dB typical
- 32-lead, 5 mm × 5 mm LFCSP package

APPLICATIONS

- Point to point and point to multipoint radios
- Military radars, electronic warfare (EW) and electronic intelligence (ELINT)
- Satellite communications
- Sensors

GENERAL DESCRIPTION

The HMC9059 is a compact gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC) upconverter in a RoHS compliant, low stress injection molded plastic LFCSP package that operates from 9.5 GHz to 13.5 GHz. This device provides a small signal conversion gain of 15 dB with 22 dBc of sideband rejection. The HMC9059 uses a radio frequency (RF) amplifier preceded by an in-phase/quadrature (I/Q) mixer, where the local oscillator (LO) is driven by a driver amplifier. IF1 and IF2 mixer inputs are provided, and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces the need for filtering of the unwanted sideband. The HMC9059 is a much smaller alternative to hybrid style single-sideband (SSB) upconverter assemblies, and it eliminates the need for wire bonding by allowing the use of surface-mount manufacturing techniques.

FUNCTIONAL BLOCK DIAGRAM

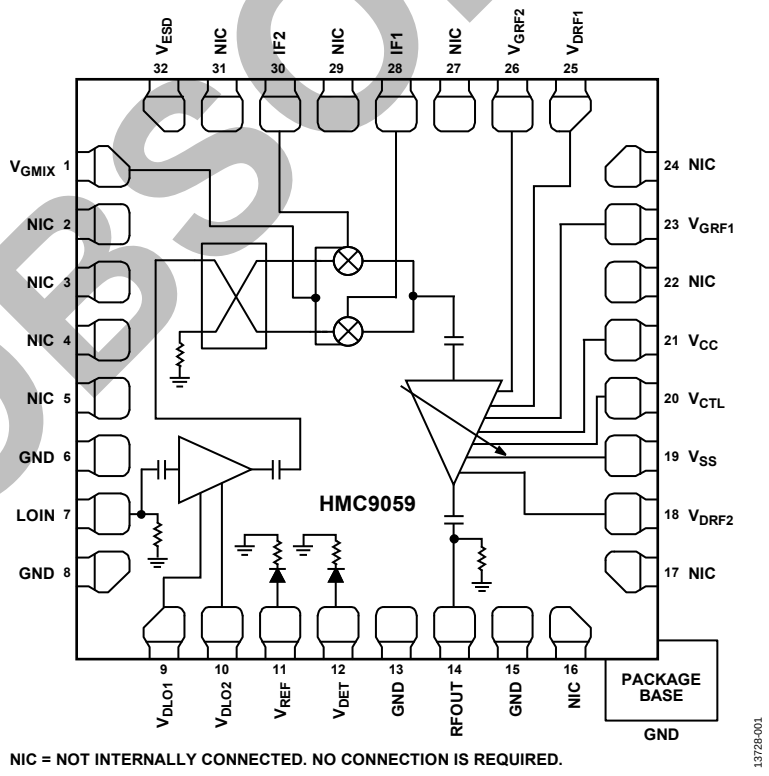

Figure 1.

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SPECIFICATIONS

T_A = 25°C, IF = 1 GHz, V_{DLOx} = 2.4 V, V_{DRFx} = 5 V, V_{CC} = 5 V, V_{CTL} = −6 V, V_{ESD} = −5 V, V_{SS} = −5 V, V_{GMIX} = −0.5 V, LO = 2 dBm. Measurements performed with upper sideband selected and external 90° hybrid at the IF ports, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
Frequency Range				
RF	9.5		13.5	GHz
LO	6		17	GHz
Intermediate Frequency (IF)	DC		3.5	GHz
LO Drive Range	2		8	dBm
PERFORMANCE				
Conversion Gain	12	15		dB
Sideband Rejection	18	22		dBc
Input Power for 1 dB Compression (P1dB)		5		dBm
Output Third-Order Intercept (OIP3) at Maximum Gain	27	30		dBm
LO Leakage at RFOUT[1]		−10		dBm
LO Leakage at IFx[2]		−40		dBm
Noise Figure		12		dB
Return Loss				
RF		15		dB
LO		10		dB
IFx[2]		15		dB
POWER SUPPLY				
Total Supply Current				
LO Amplifier		100		mA
RF Amplifier[3]		240		mA

[1] The LO signal level at the RF output port is not calibrated.
[2] Measurement taken without 90° hybrid at the IF ports.
[3] Adjust V_{GRF1} and V_{GRF2} between −2 V and 0 V to achieve the total quiescent current, I_{DRF1} + I_{DRF2} = 240 mA.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage	
V_{DRFx}, V_{DLOx}, V_{CC}, V_{REF}, V_{DET}	5.5 V
Gate Bias Voltage	
V_{GRFx}	−3 V to 0 V
V_{CTL}, V_{ESD}, V_{SS}	−7 V to 0 V
V_{GMIX}	−2 V to 0 V
LO Input Power	10 dBm
IF Input Power	10 dBm
Maximum Junction Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity, Human Body Model (HBM)	250 V (Class 1A)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA} value in Table 3 assumes a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	43.1	27.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

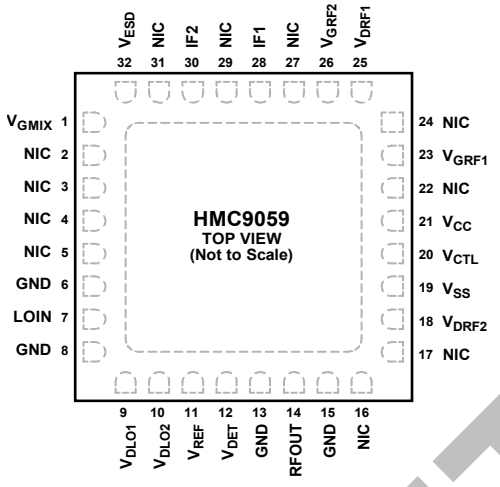


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{GMIX}	Gate Voltage for the FET Mixer (see Figure 3). Refer to the typical application circuit for the required external components (see Figure 170).
2 to 5, 16, 17, 22, 24, 27, 29, 31	NIC	Not Internally Connected. No connection is required. These pins are not connected internally. However, all data shown herein was measured with these pins connected to RF/dc ground externally.
6, 8, 13, 15	GND	Ground Connect (see Figure 4). These pins and package bottom must be connected to RF/dc ground.
7	LOIN	Local Oscillator Input (see Figure 5). This pin is dc-coupled and matched to 50 Ω.
9, 10	V_{DLO1}, V_{DLO2}	Power Supply Voltage for LO Amplifier (see Figure 6). Refer to the typical application circuit for the required external components (see Figure 170).
11	V_{REF}	Reference Voltage for the Power Detector (see Figure 7). V_{REF} is the dc bias of the diode biased through the external resistor used for temperature compensation of V_{DET}. Refer to the typical application circuit for the required external components (see Figure 170).
12	V_{DET}	Detector Voltage for the Power Detector (see Figure 8). V_{DET} is the dc voltage representing the RF output power rectified by the diode, which is biased through an external resistor. Refer to the typical application circuit for the required external components (see Figure 170).
14	RFOUT	Radio Frequency Output (see Figure 9). This pin is dc-coupled and matched to 50 Ω.
18, 25	V_{DRF2}, V_{DRF1}	Power Supply Voltage for RF Amplifier (see Figure 11). Refer to the typical application circuit for the required external components (see Figure 170).
19	V_{SS}	Gate Voltage for Gain Control Circuitry (see Figure 11). Refer to the typical application circuit for the required external components (see Figure 170).
20	V_{CTL}	Gain Control Voltage for RF Amplifier (see Figure 11). Refer to the typical application circuit for the required external components (see Figure 170).
21	V_{CC}	DC Voltage for Gain Control Circuitry (see Figure 11). Refer to the typical application circuit for the required external components (see Figure 170).
23, 26	V_{GRF1}, V_{GRF2}	Gate Voltage for RF Amplifier (see Figure 12). Refer to the typical application circuit for the required external components (see Figure 170).
28, 30	IF1, IF2	Quadrature IF Inputs (see Figure 13). For applications not requiring operation to dc, use an off-chip dc blocking capacitor. For operation to dc, these pins must not source/sink more than 3 mA of current or device malfunction and failure may result.
32	V_{ESD}	DC Voltage for ESD Protection (see Figure 14). Refer to the typical application circuit for the required external components (see Figure 170).
	EPAD	Exposed Pad. Connect the exposed pad to a low impedance thermal and electrical ground plane.

INTERFACE SCHEMATICS

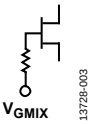


Figure 3. V_{GMIX} Interface

Figure 4. GND Interface

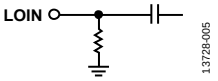


Figure 5. LOIN Interface

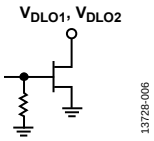


Figure 6. V_{DLO1}, V_{DLO2} Interface

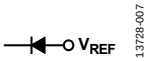


Figure 7. V_{REF} Interface

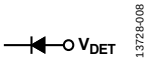


Figure 8. V_{DET} Interface

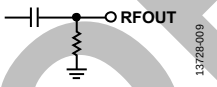


Figure 9. RFOUT Interface

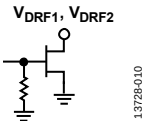


Figure 10. V_{DRF1}, V_{DRF2} Interface

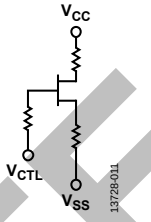


Figure 11. V_{SS}, V_{CTL}, V_{CC} Interface

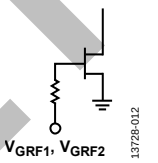


Figure 12. V_{GRF1}, V_{GRF2} Interface

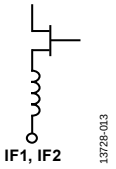


Figure 13. IF1, IF2 Interface

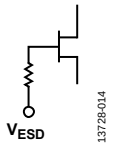


Figure 14. V_{ESD} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

UPPER SIDEBAND SELECTED

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

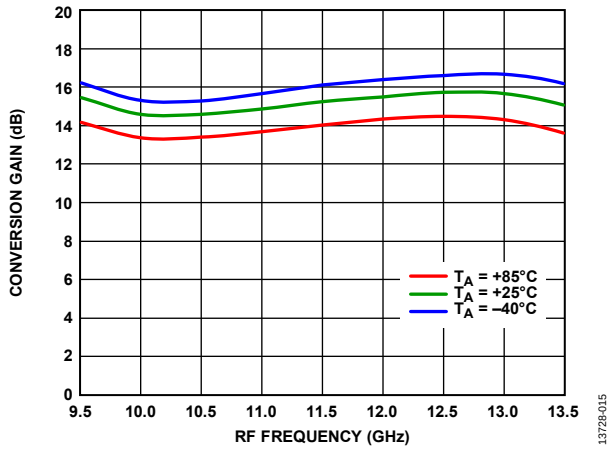


Figure 15. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

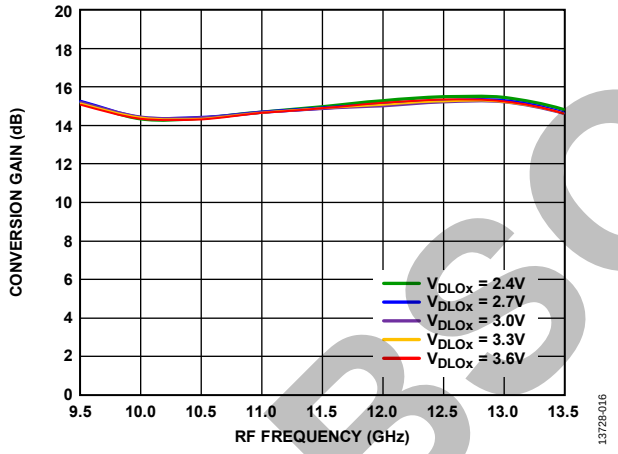


Figure 16. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

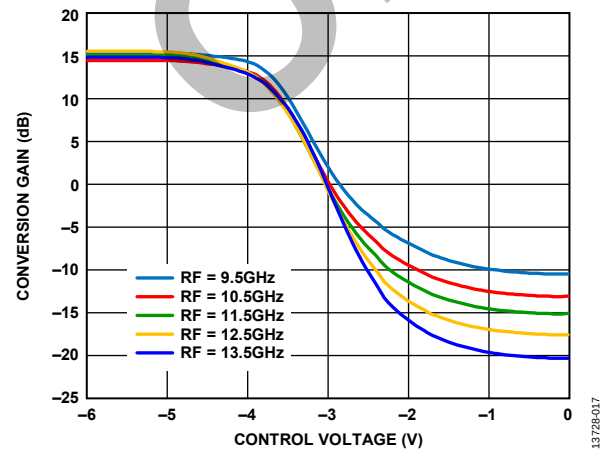


Figure 17. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

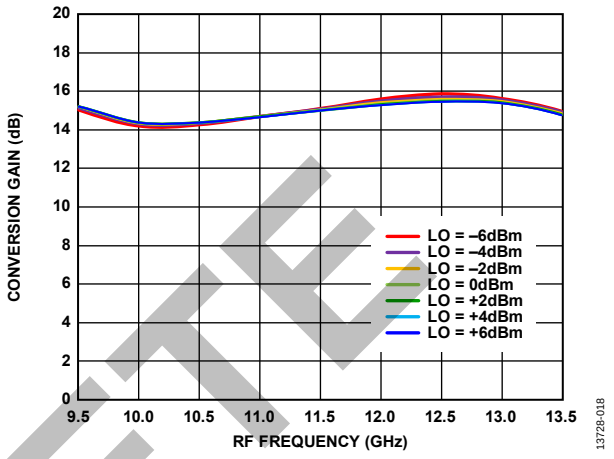


Figure 18. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

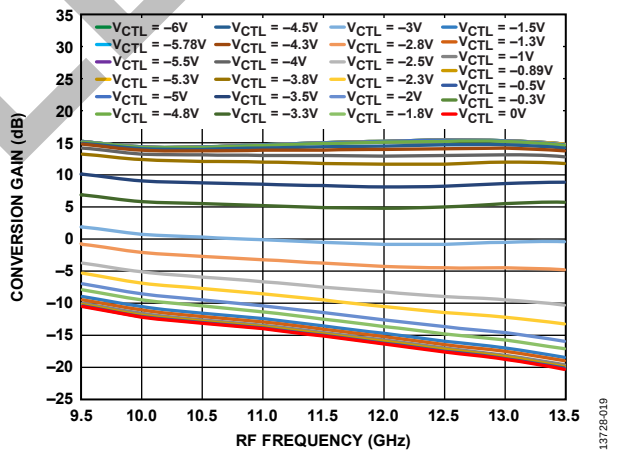


Figure 19. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

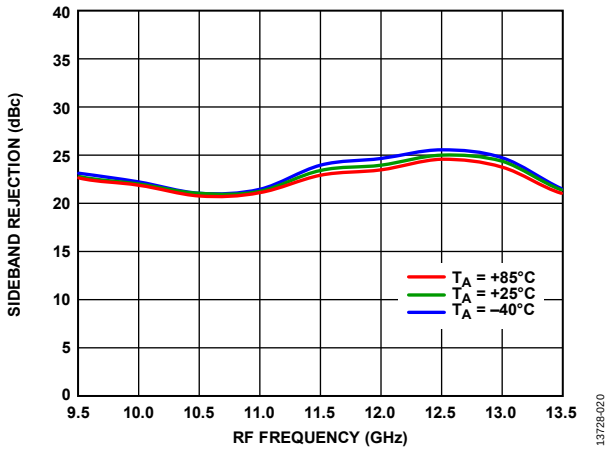


Figure 20. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

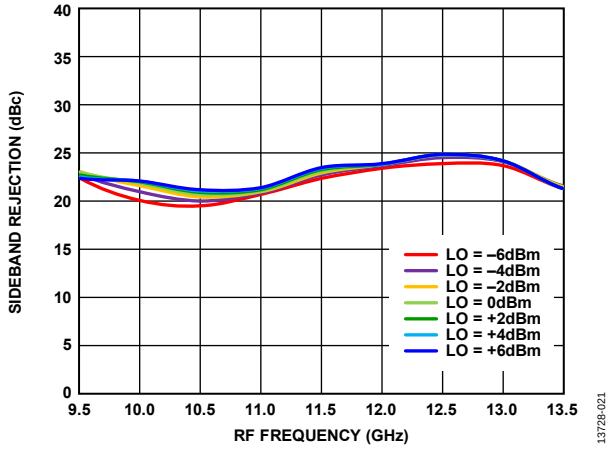


Figure 21. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

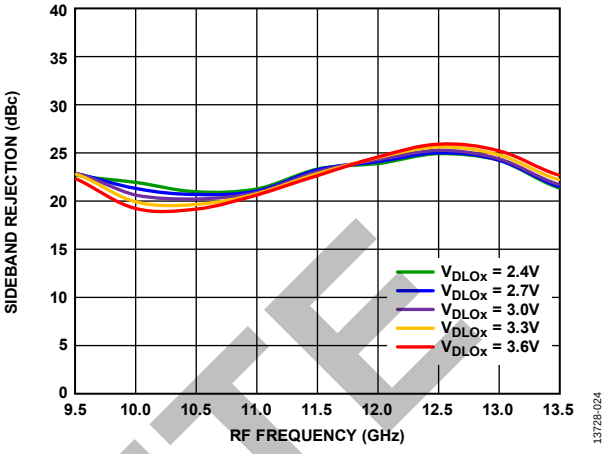


Figure 24. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

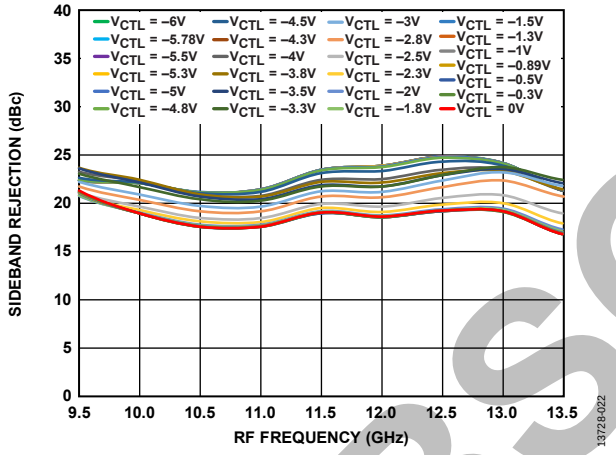


Figure 22. Sideband Rejection vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

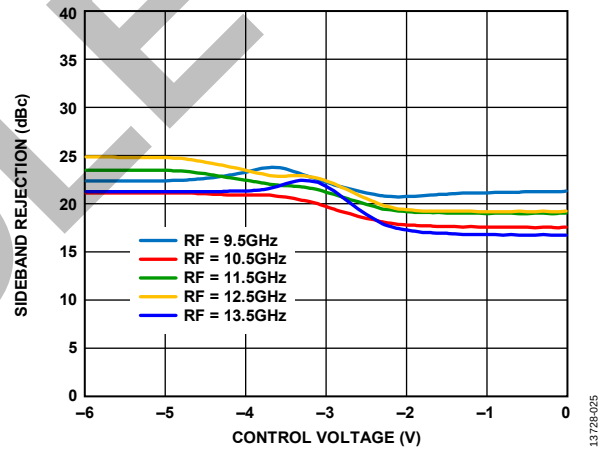


Figure 25. Sideband Rejection vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

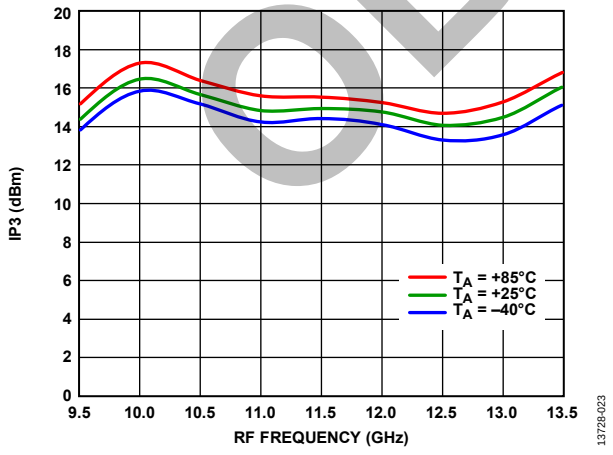


Figure 23. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

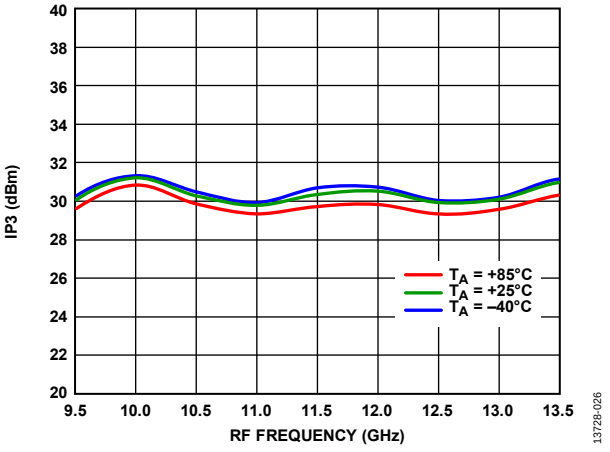


Figure 26. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

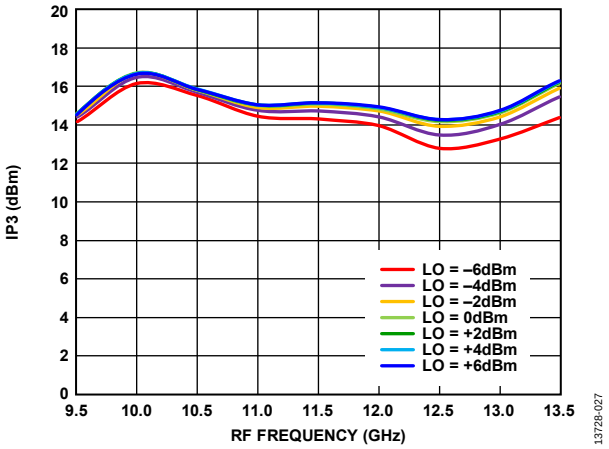


Figure 27. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

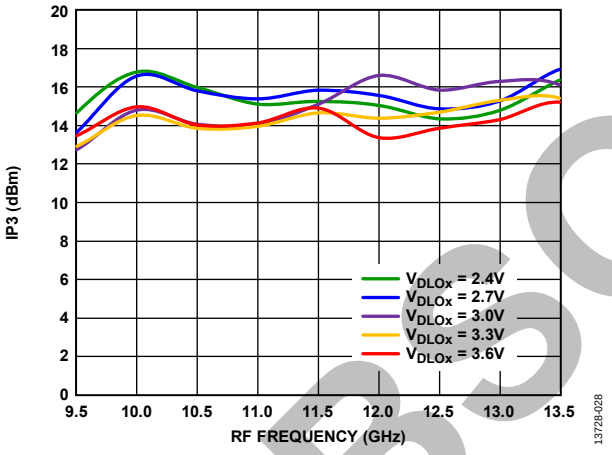


Figure 28. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

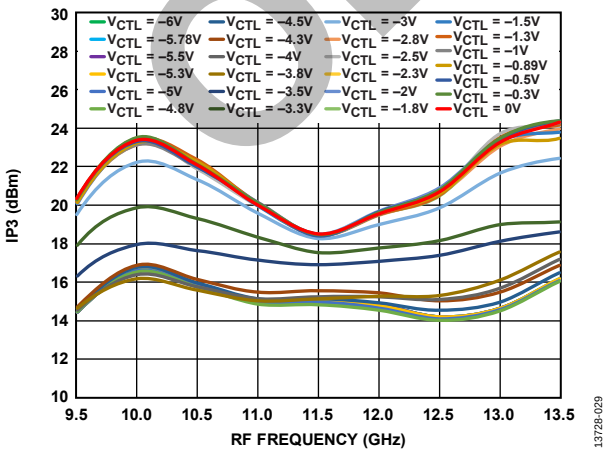


Figure 29. Input IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

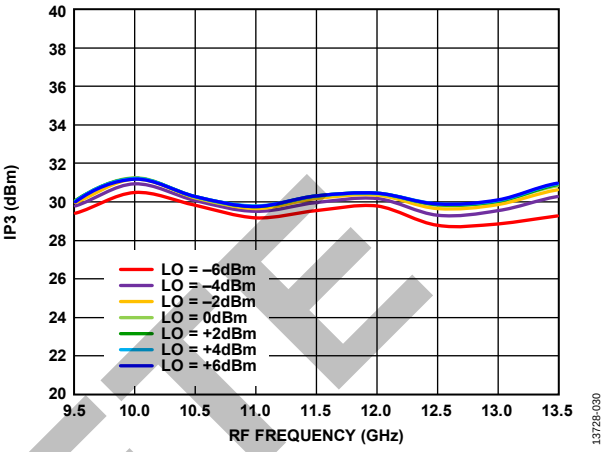


Figure 30. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

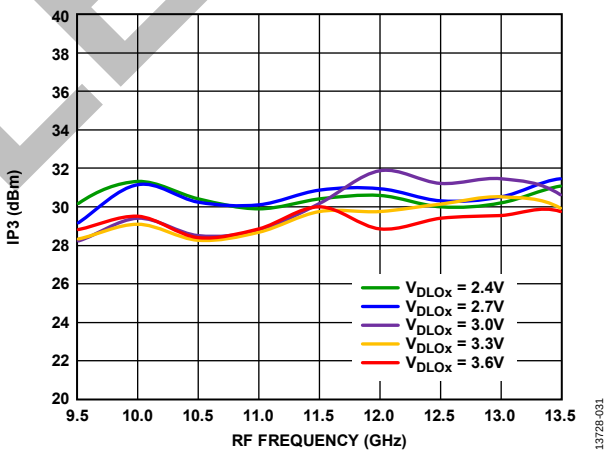


Figure 31. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

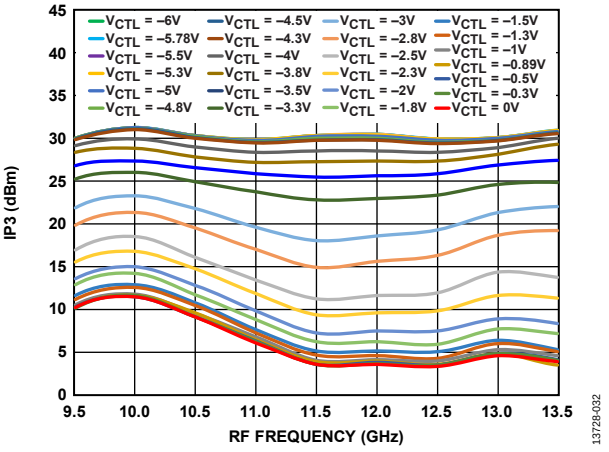


Figure 32. Output IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

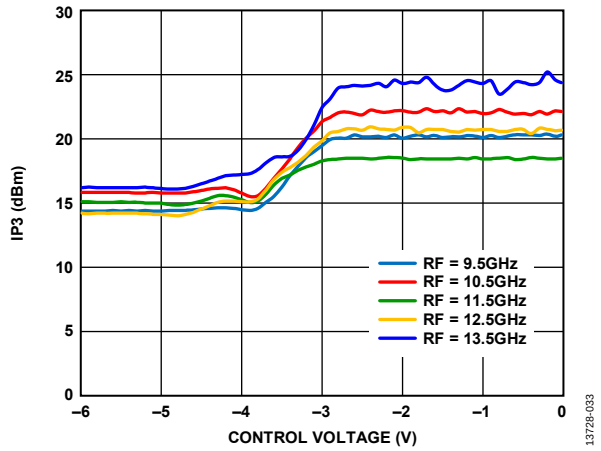


Figure 33. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

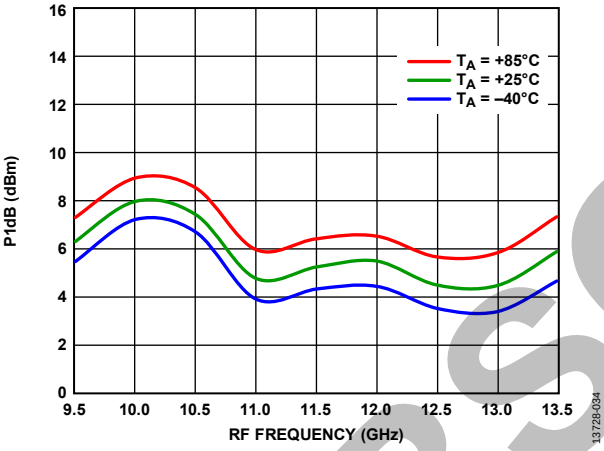


Figure 34. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm

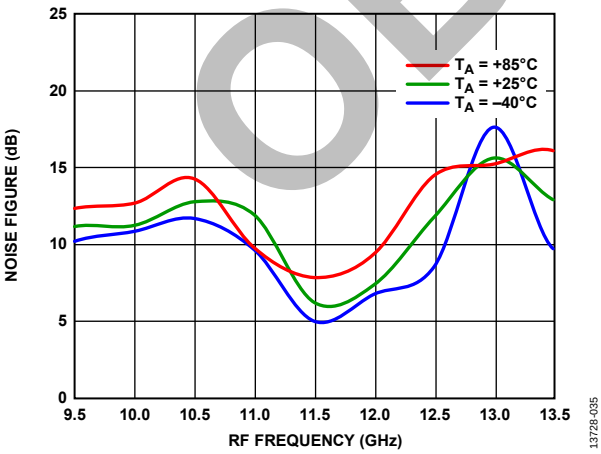


Figure 35. Noise Figure vs. RF Frequency at Various Temperatures,

LO = 2 dBm, V_{DLOx} = 2.4 V

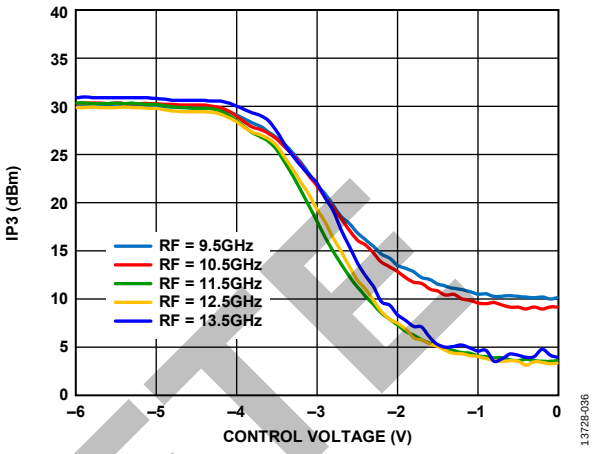


Figure 36. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

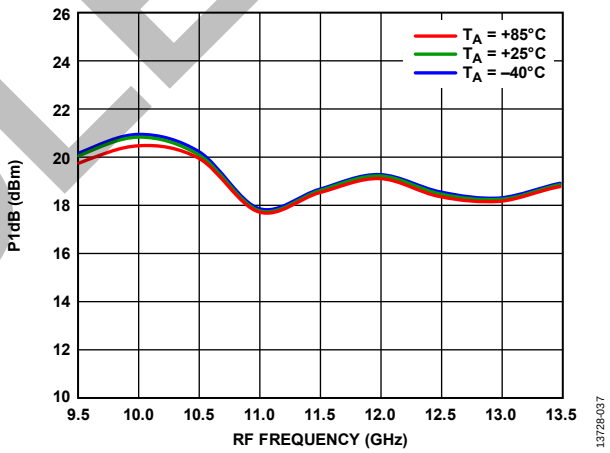


Figure 37. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

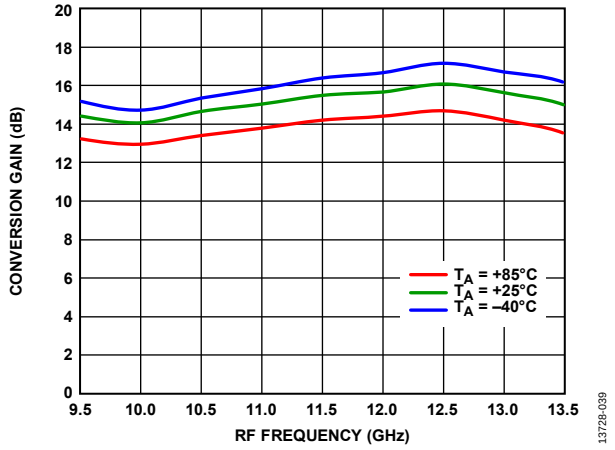


Figure 38. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

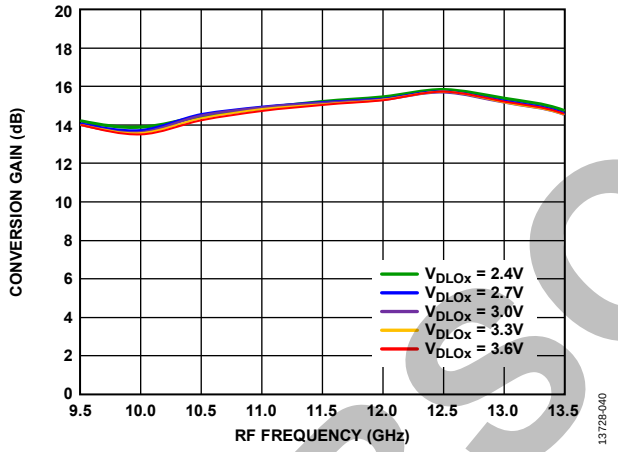


Figure 39. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

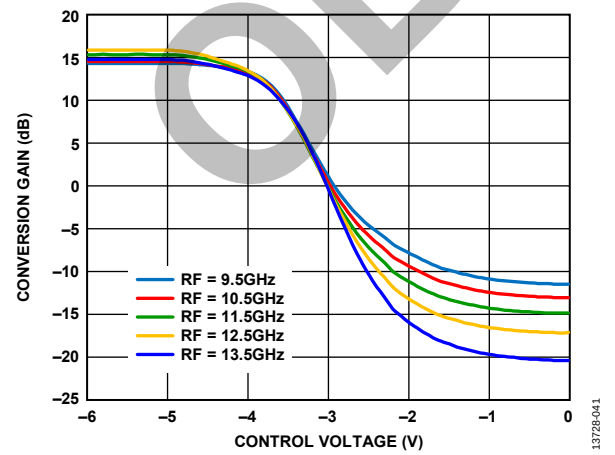


Figure 40. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

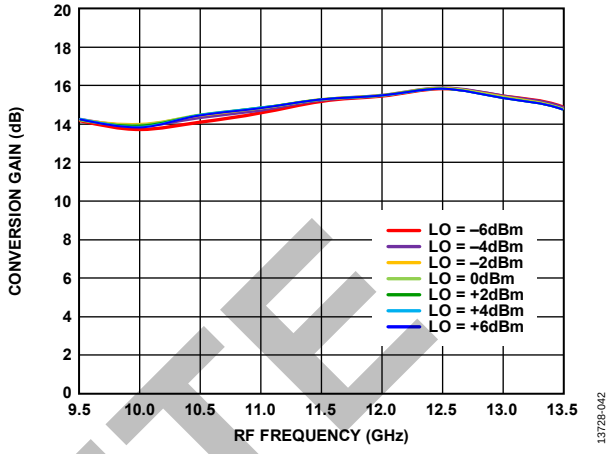


Figure 41. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

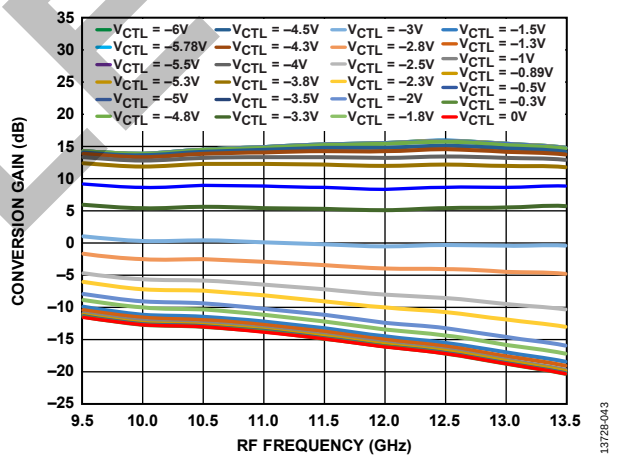


Figure 42. Conversion Gain vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

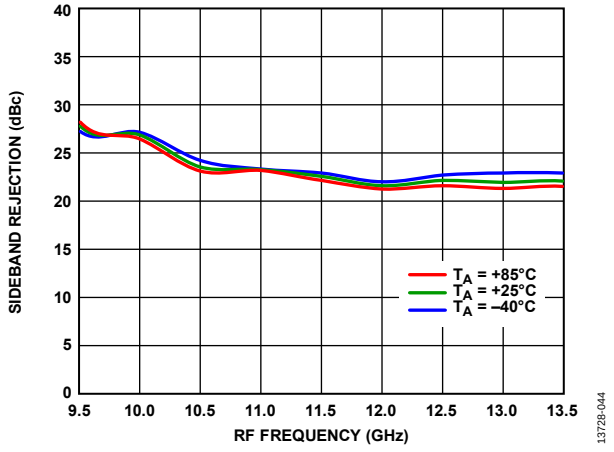


Figure 43. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

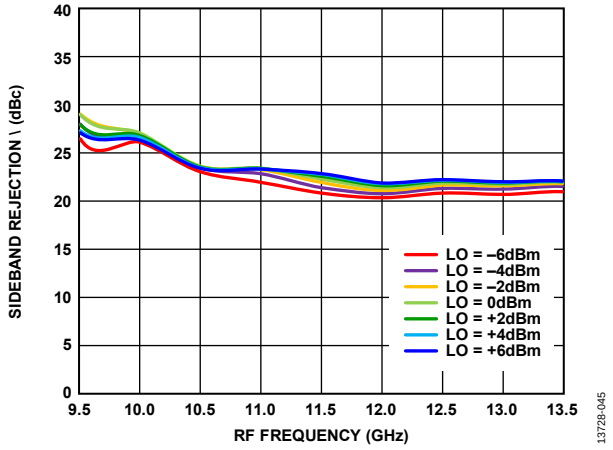


Figure 44. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

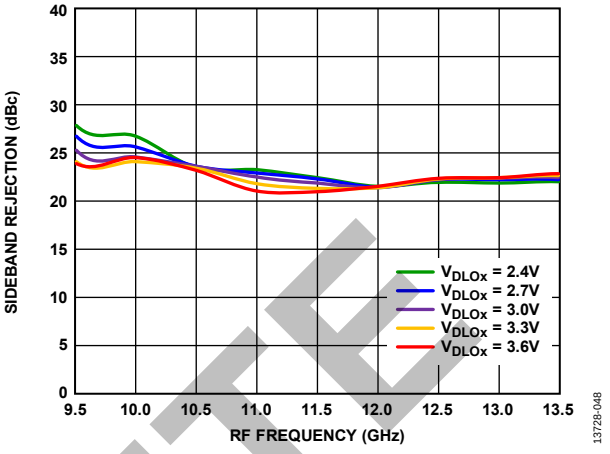


Figure 47. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

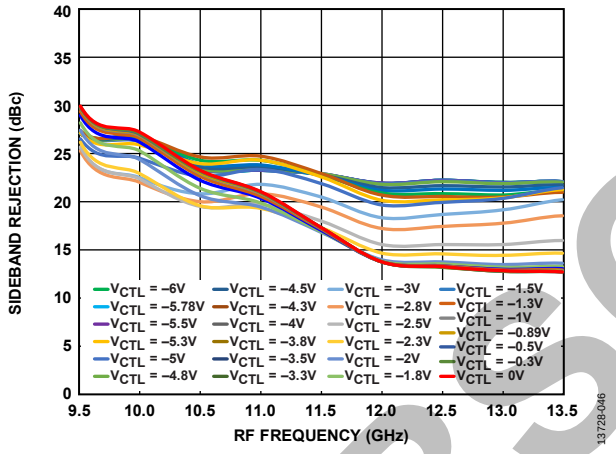


Figure 45. Sideband Rejection vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

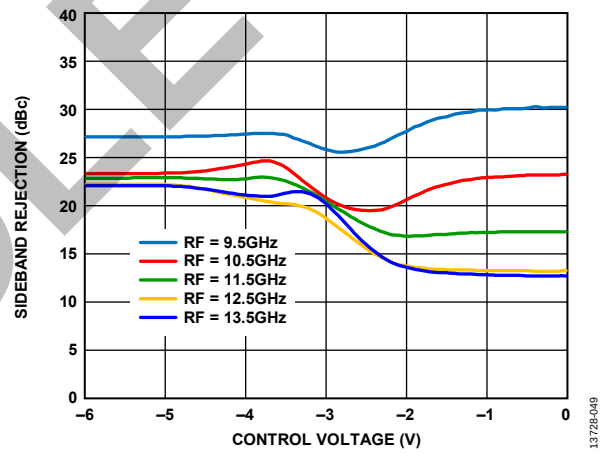


Figure 48. Sideband Rejection vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

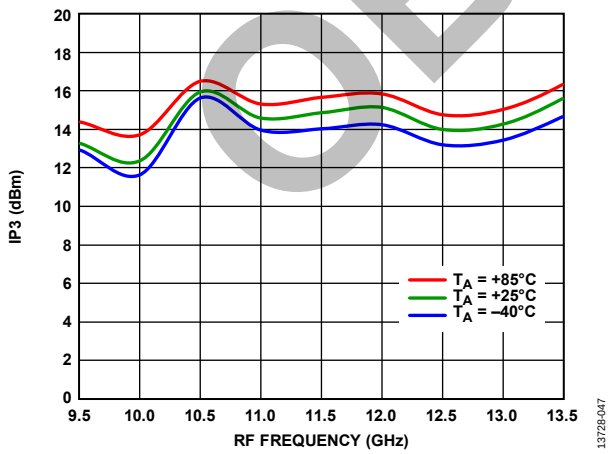


Figure 46. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

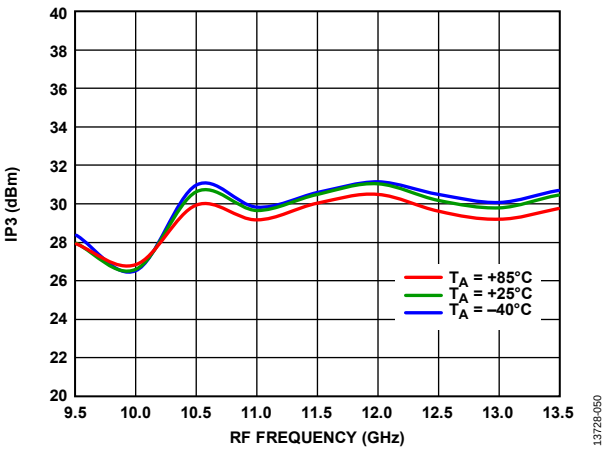


Figure 49. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

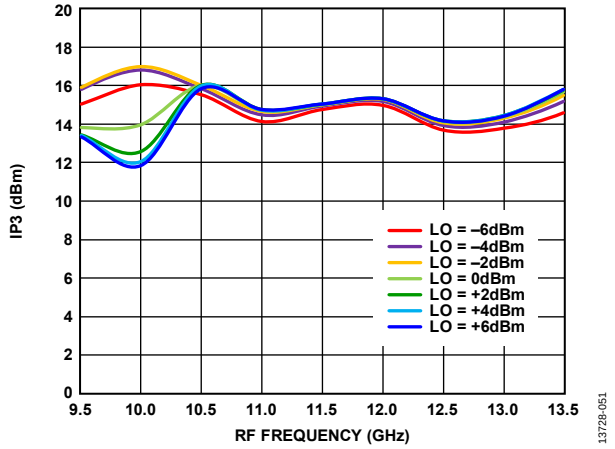


Figure 50. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

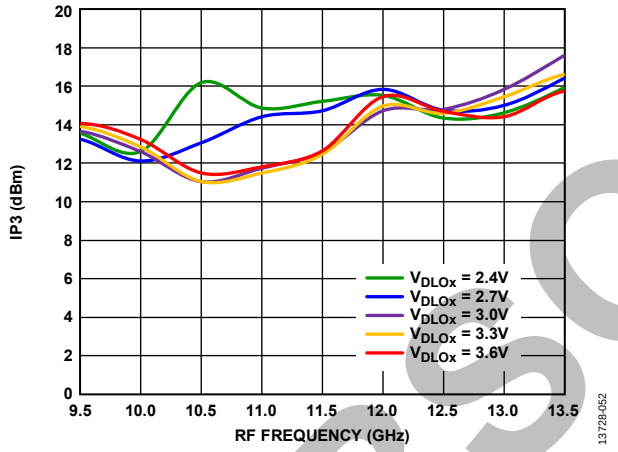


Figure 51. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

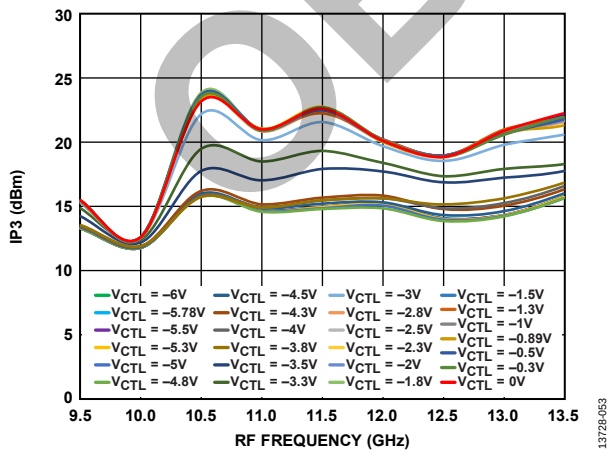


Figure 52. Input IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

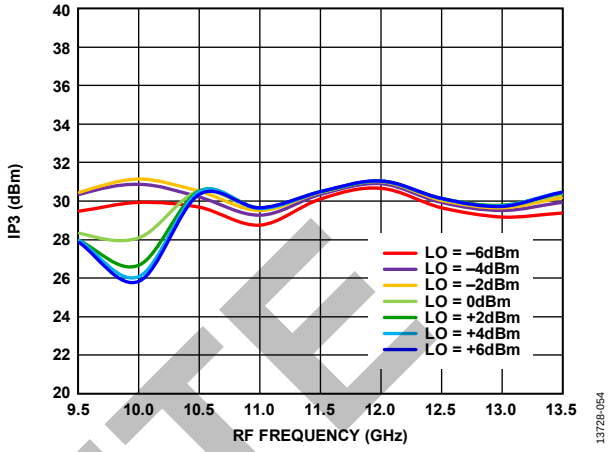


Figure 53. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

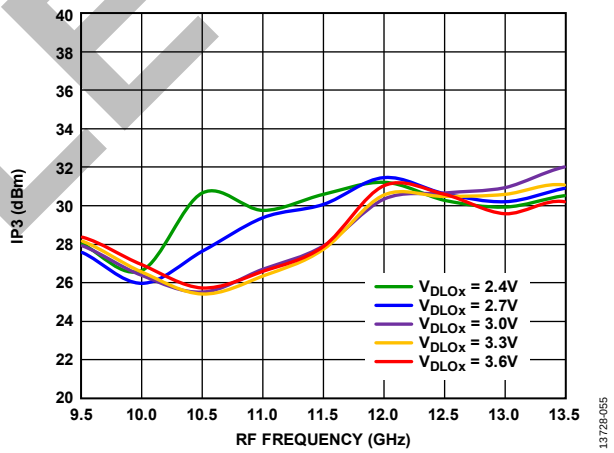


Figure 54. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

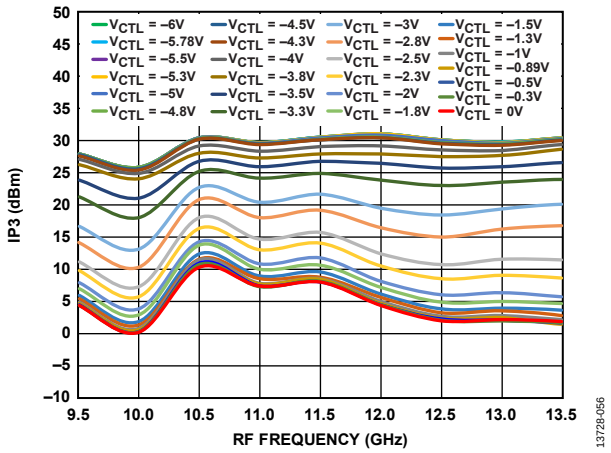


Figure 55. Output IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

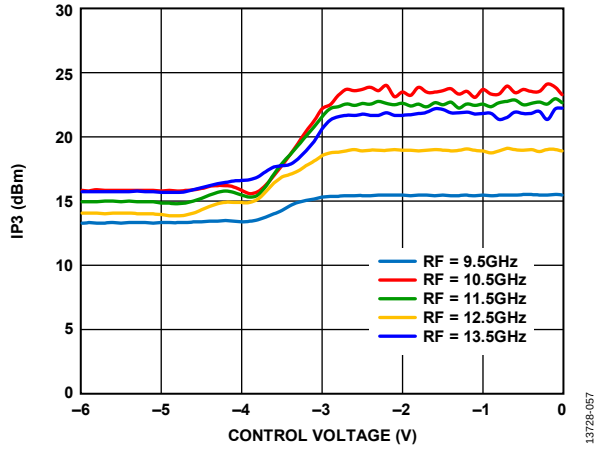


Figure 56. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

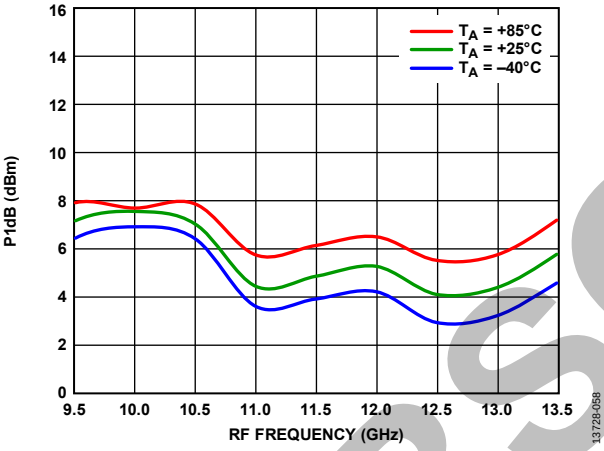


Figure 57. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

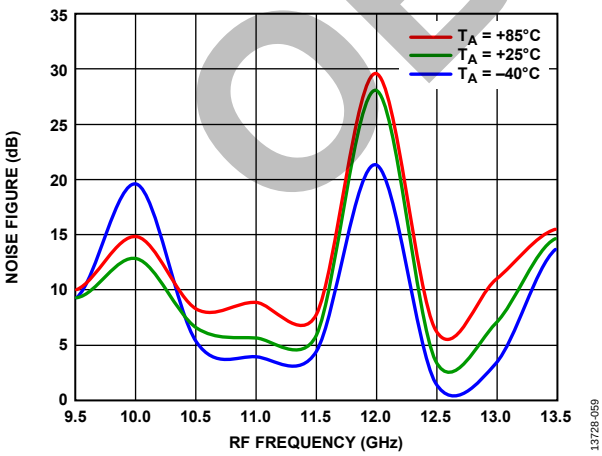


Figure 58. Noise Figure vs. RF Frequency at Various Temperatures,

LO = 2 dBm, V_{DLOx} = 2.4 V

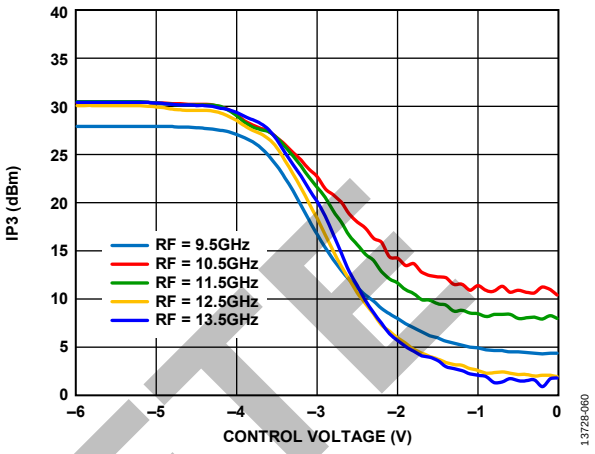


Figure 59. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

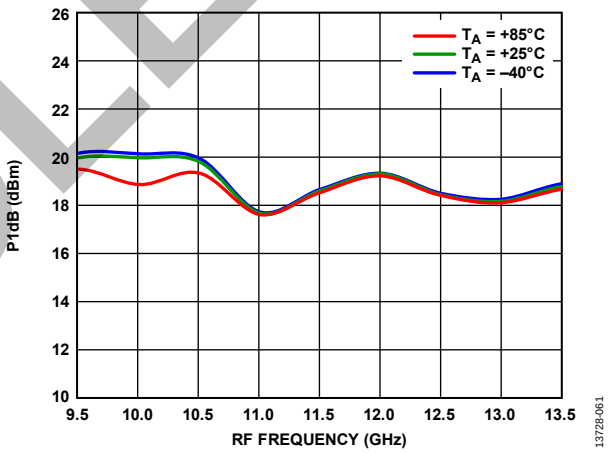


Figure 60. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

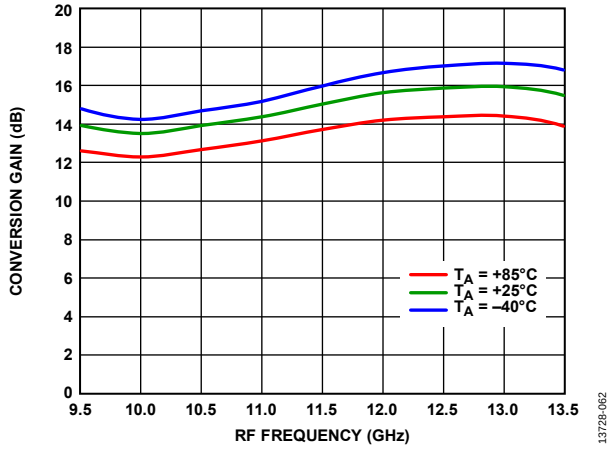


Figure 61. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

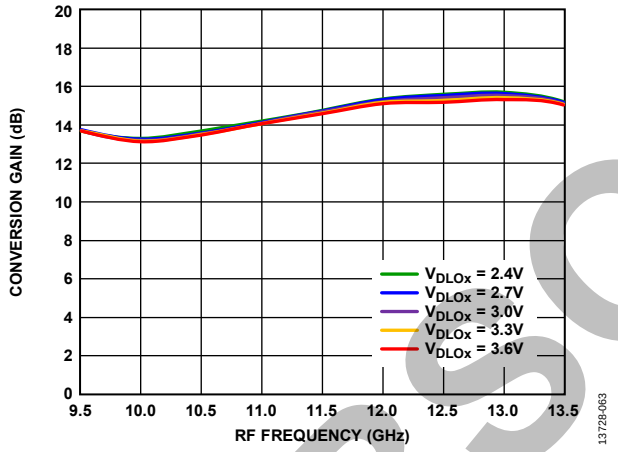


Figure 62. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

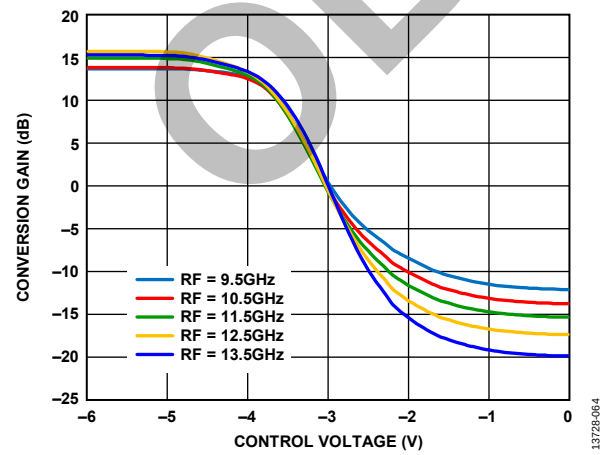


Figure 63. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

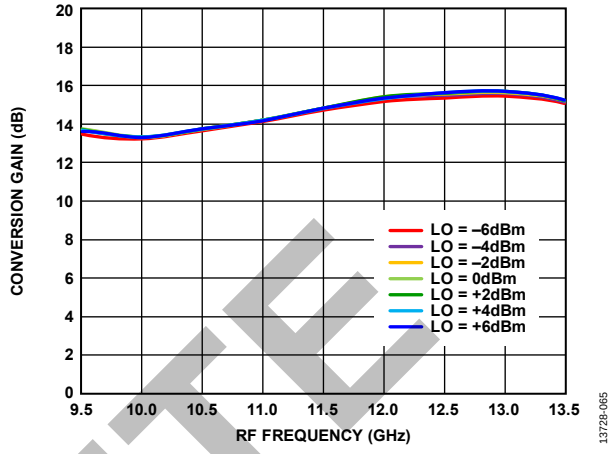


Figure 64. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

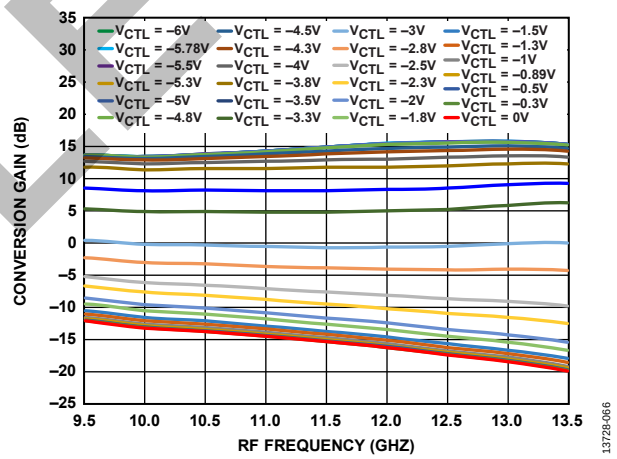


Figure 65. Conversion Gain vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

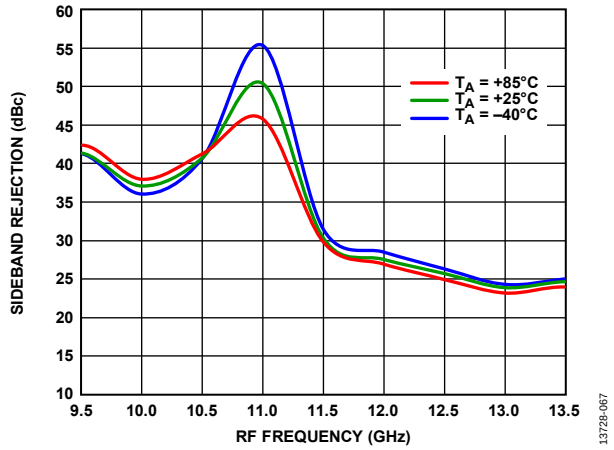


Figure 66. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

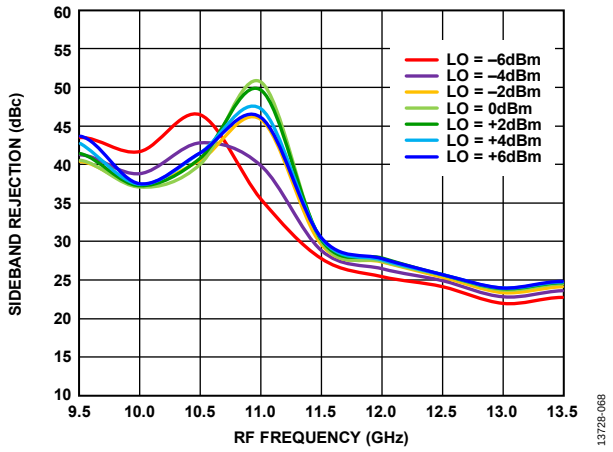


Figure 67. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

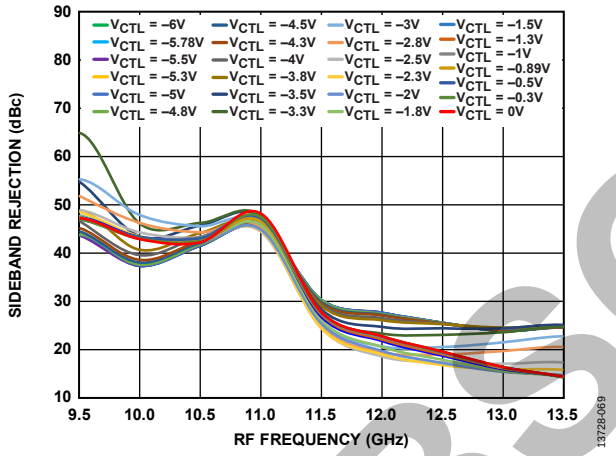


Figure 68. Sideband Rejection vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

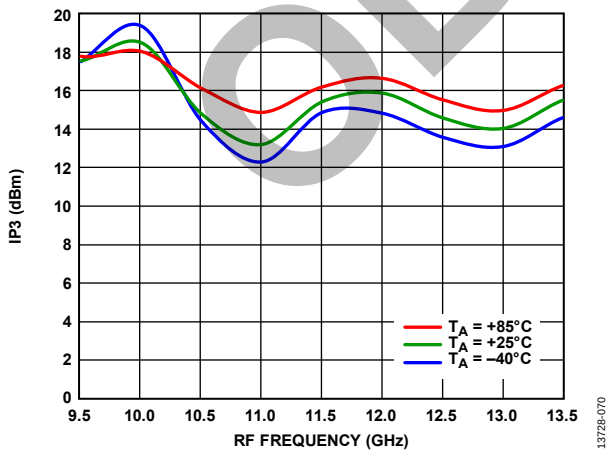


Figure 69. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

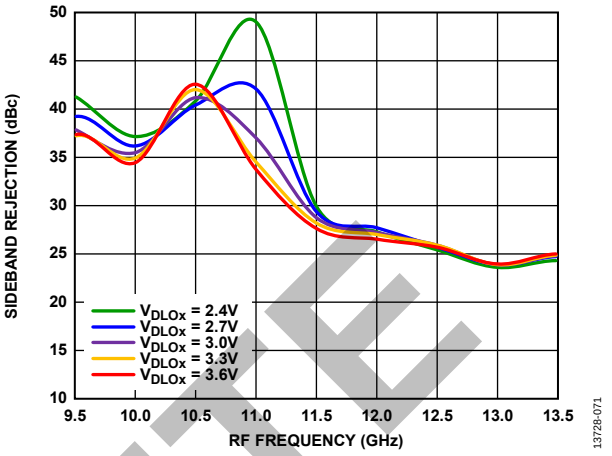


Figure 70. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

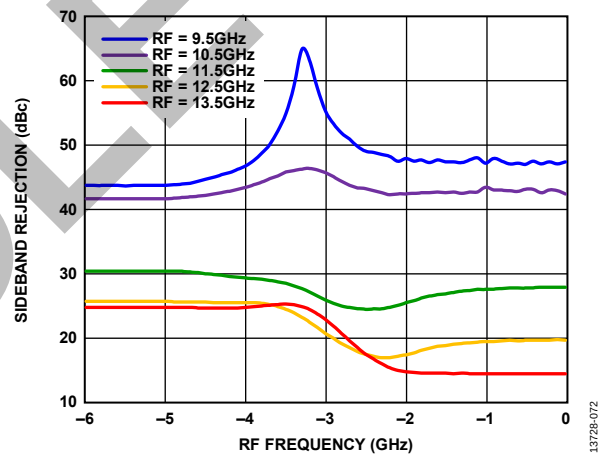


Figure 71. Sideband Rejection vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

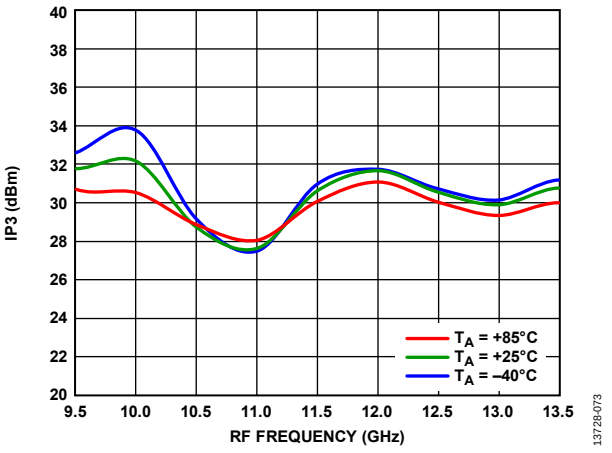


Figure 72. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

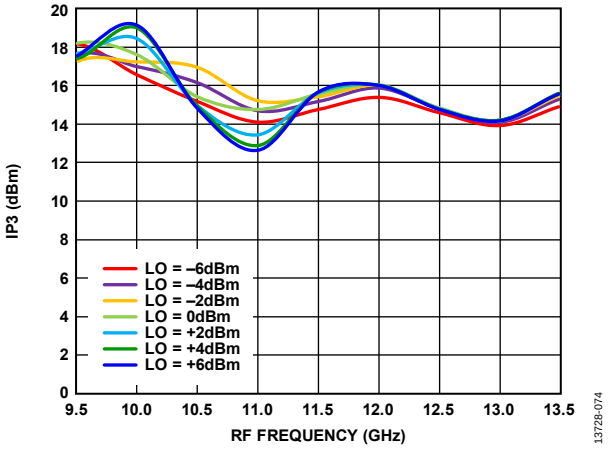


Figure 73. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

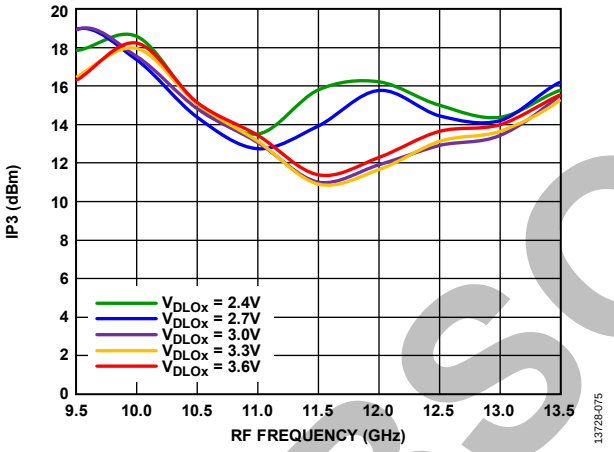


Figure 74. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

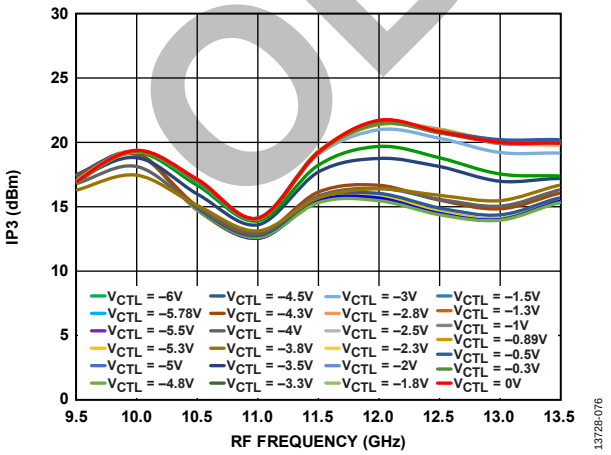


Figure 75. Input IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

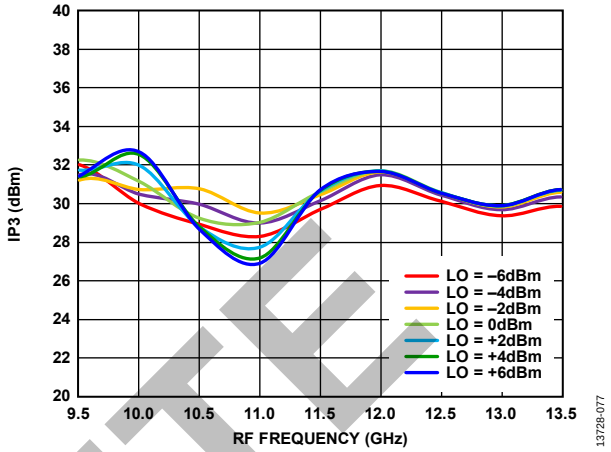


Figure 76. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

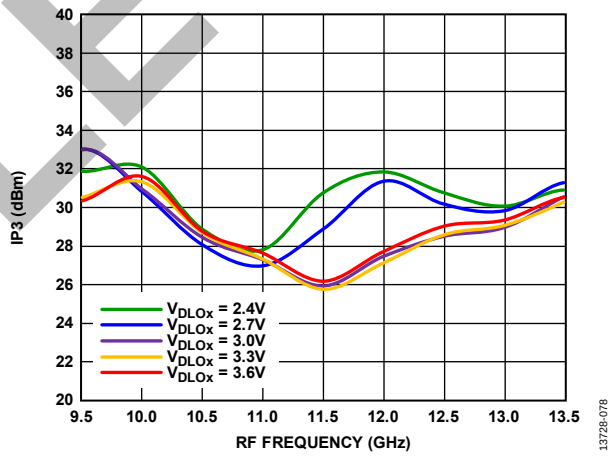


Figure 77. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

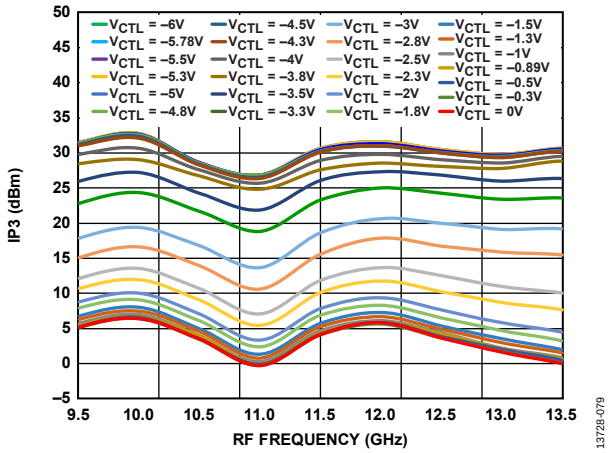


Figure 78. Output IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

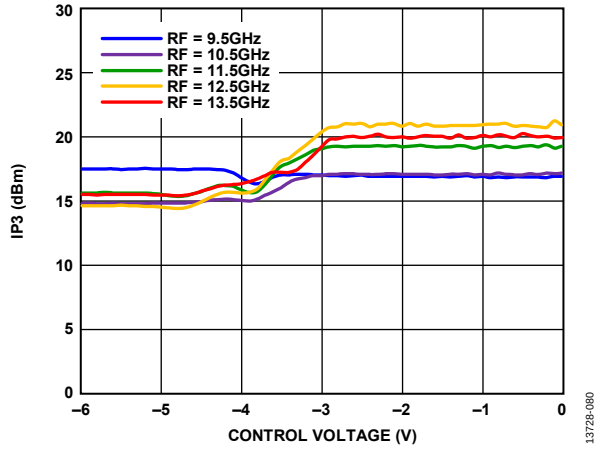


Figure 79. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

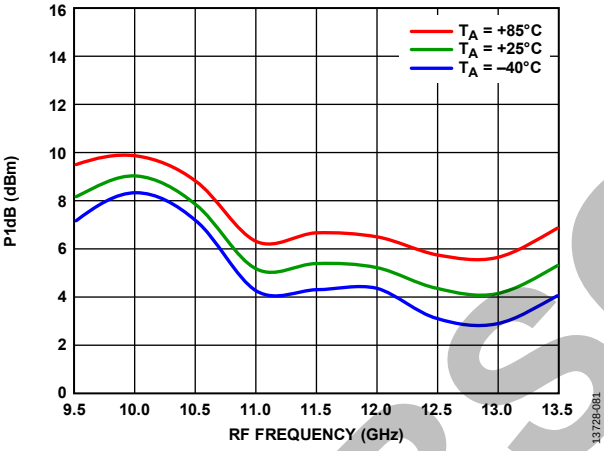


Figure 80. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

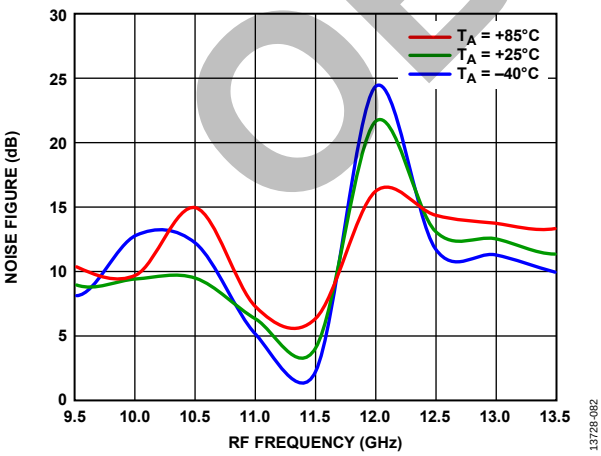


Figure 81. Noise Figure vs. RF Frequency at Various Temperatures,

LO = 2 dBm, V_{DLOx} = 2.4 V

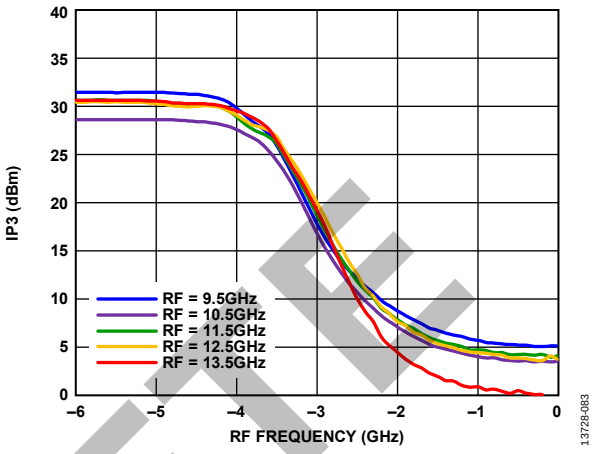


Figure 82. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

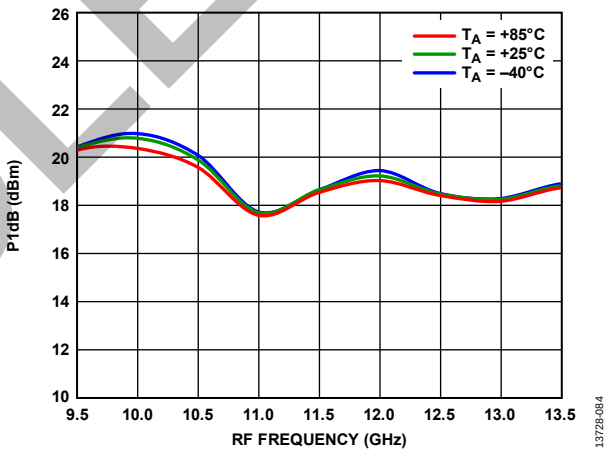


Figure 83. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

LOWER SIDEBAND SELECTED

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

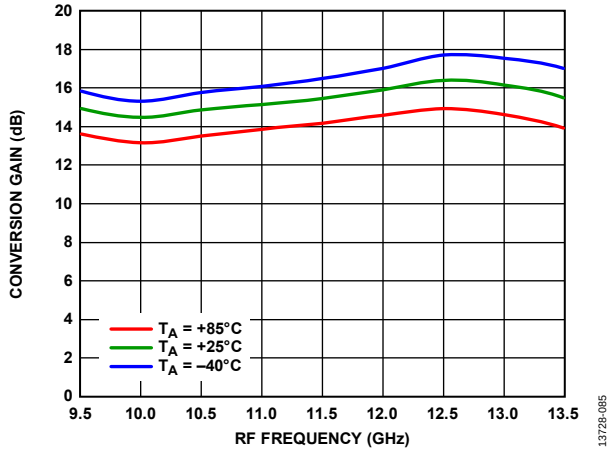


Figure 84. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

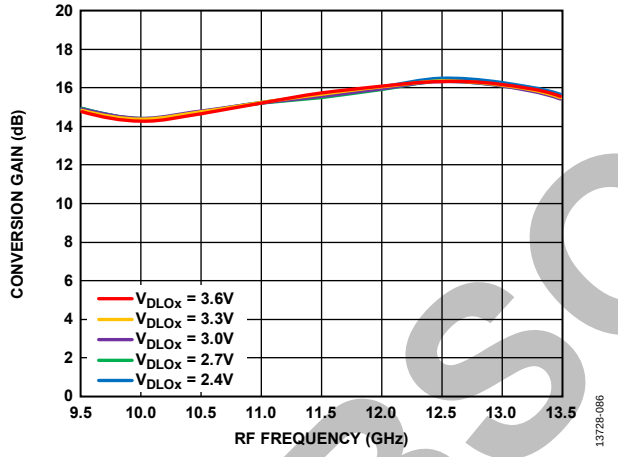


Figure 85. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

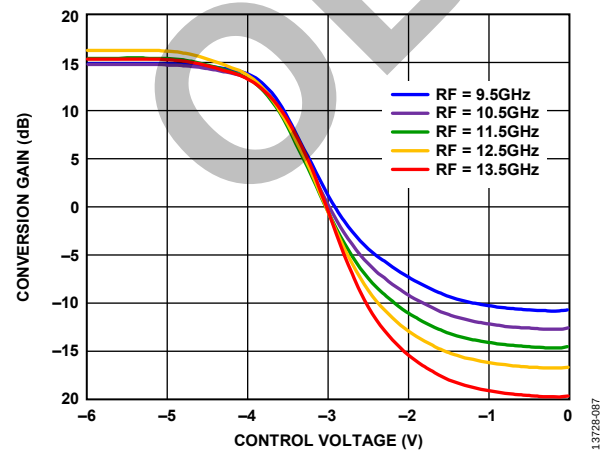


Figure 86. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

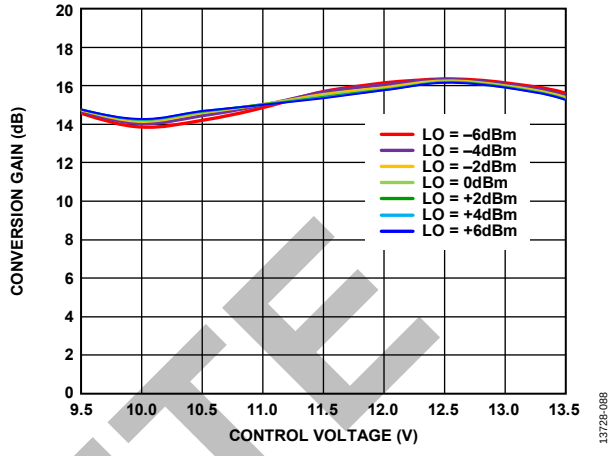


Figure 87. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

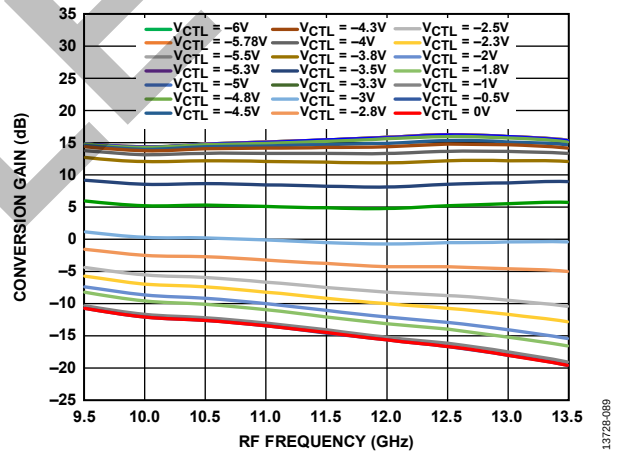


Figure 88. Conversion Gain vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

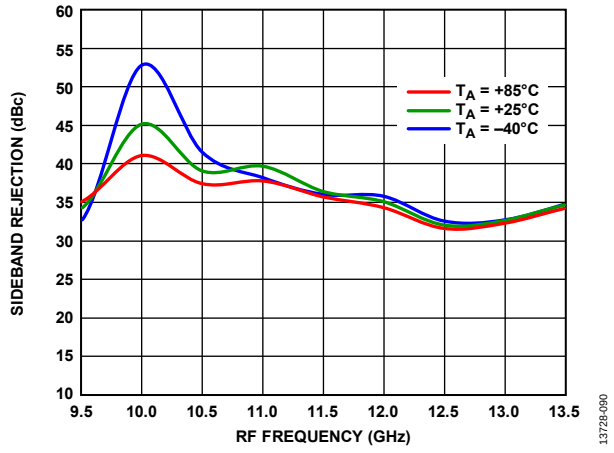


Figure 89. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

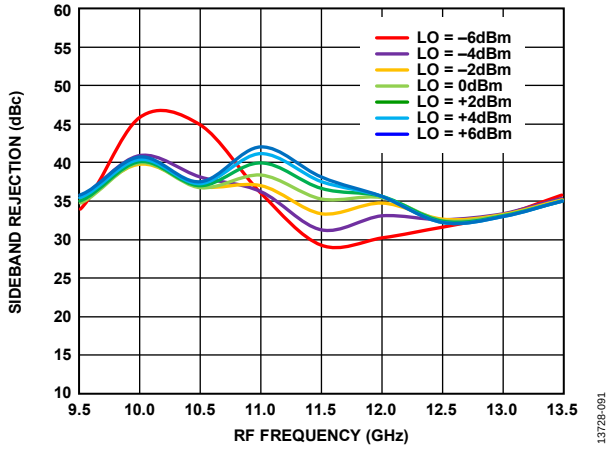


Figure 90. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

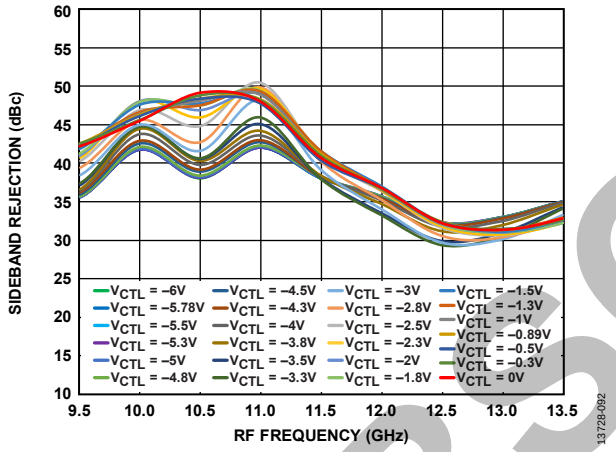


Figure 91. Sideband Rejection vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

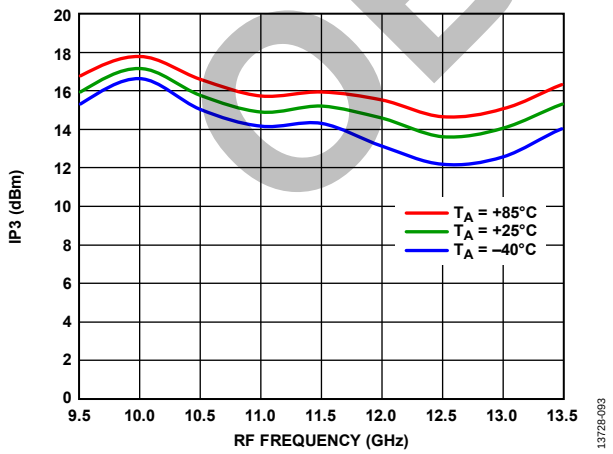


Figure 92. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

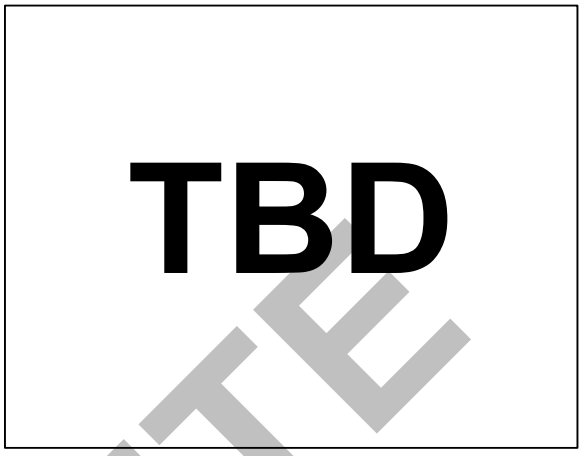


Figure 93. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

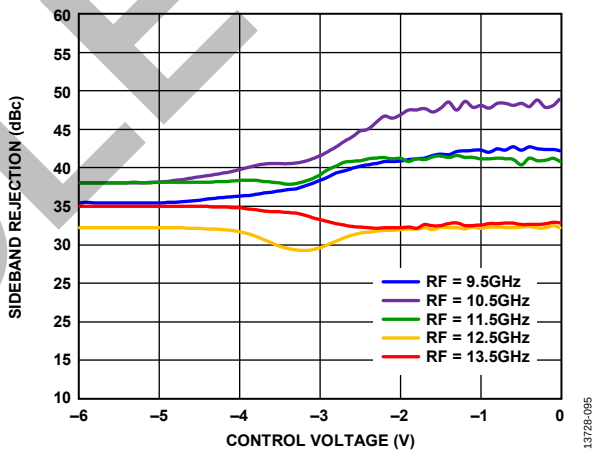


Figure 94. Sideband Rejection vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

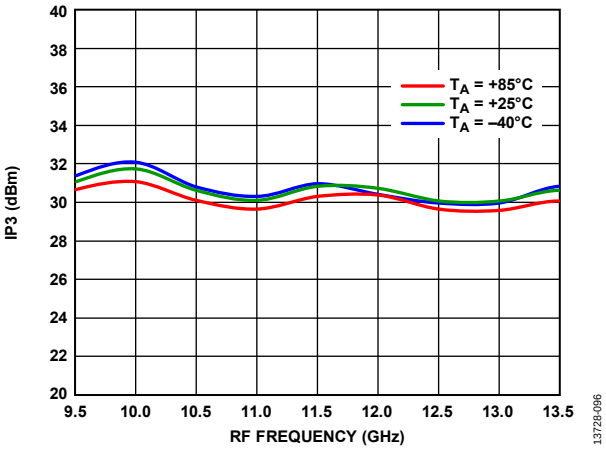


Figure 95. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

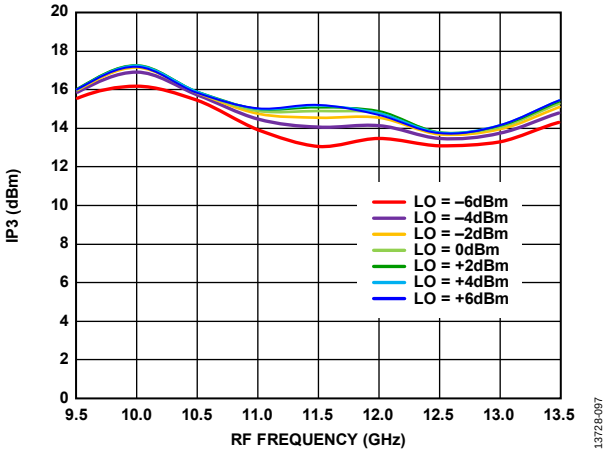


Figure 96. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

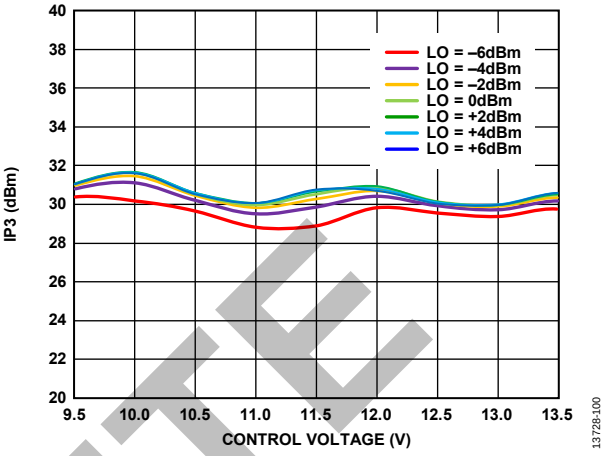


Figure 99. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

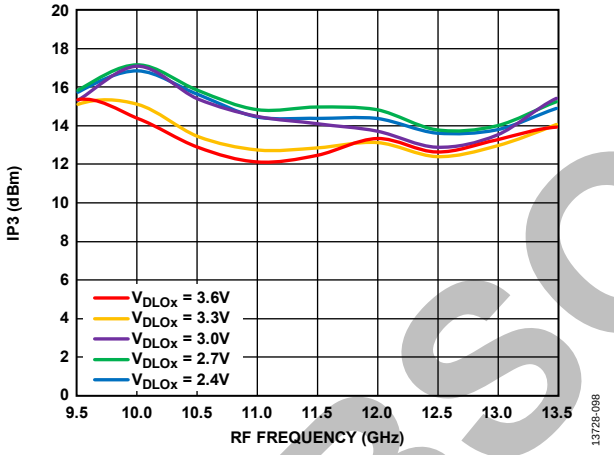


Figure 97. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

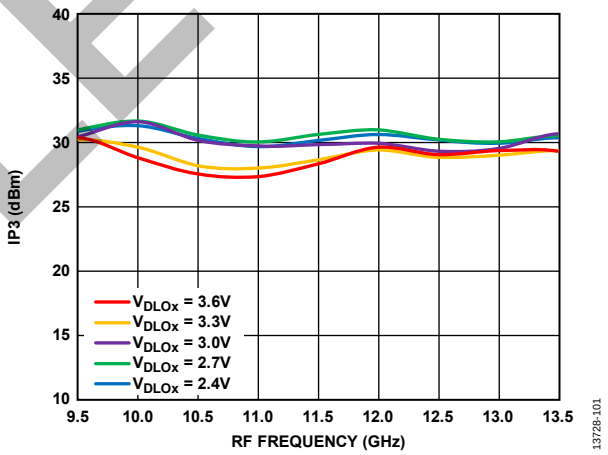


Figure 100. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

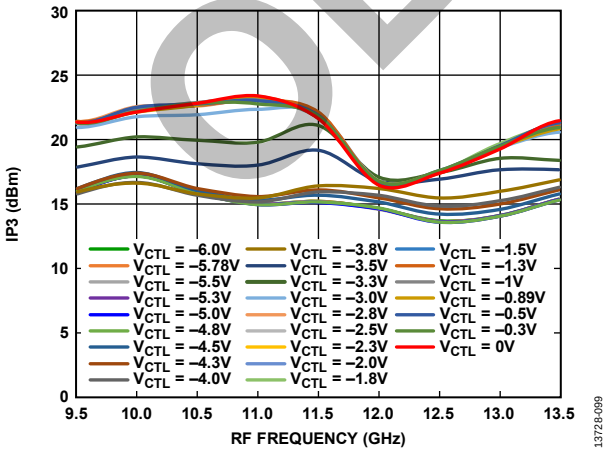


Figure 98. Input IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

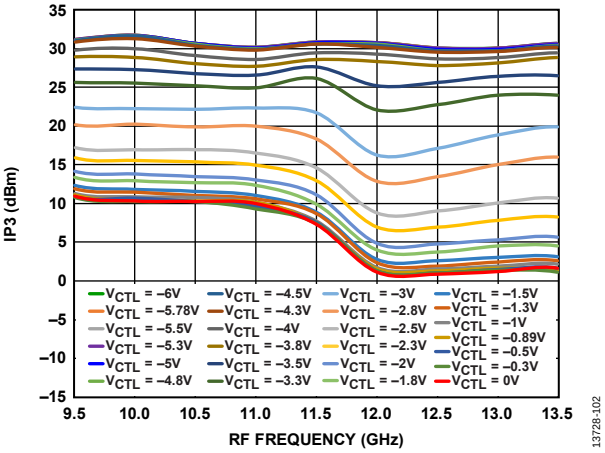


Figure 101. Output IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

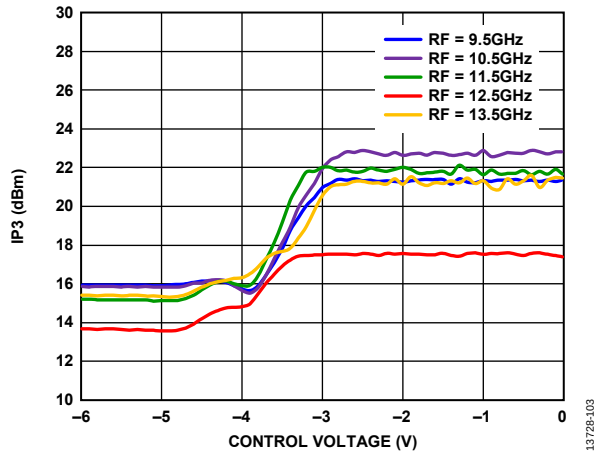


Figure 102. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

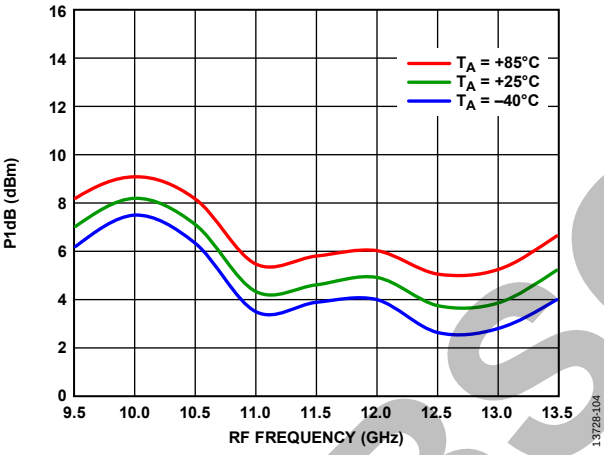


Figure 103. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm

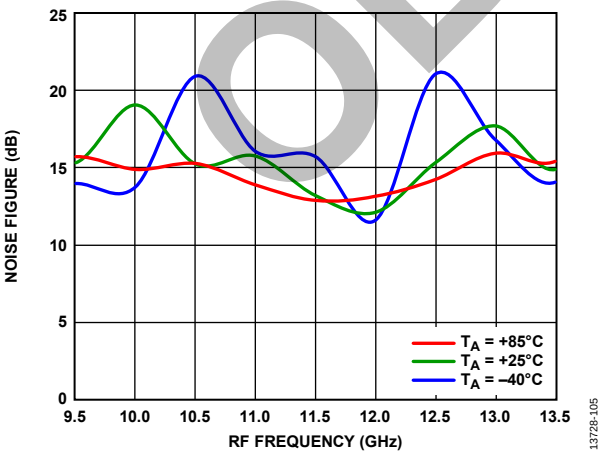


Figure 104. Noise Figure vs. RF Frequency at Various Temperatures,

LO = 2 dBm, V_{DLOx} = 2.7 V

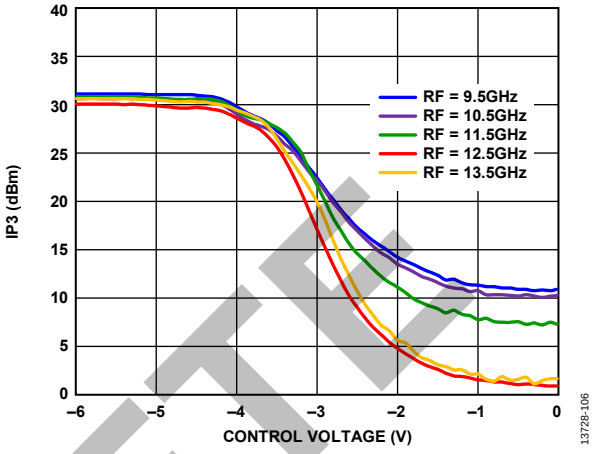


Figure 105. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

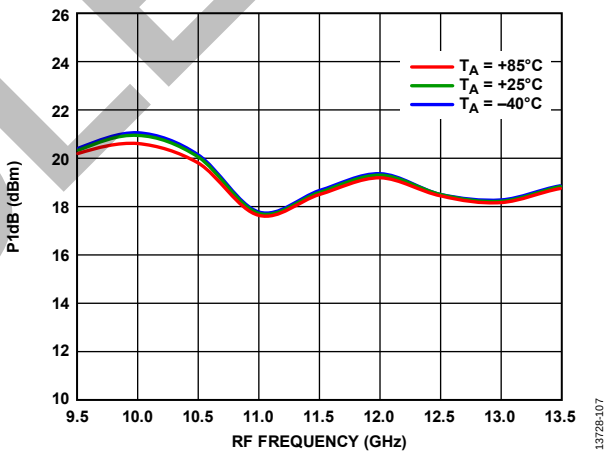


Figure 106. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

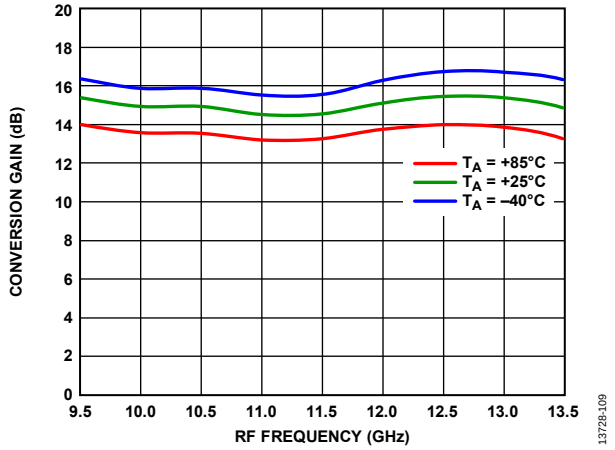


Figure 107. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

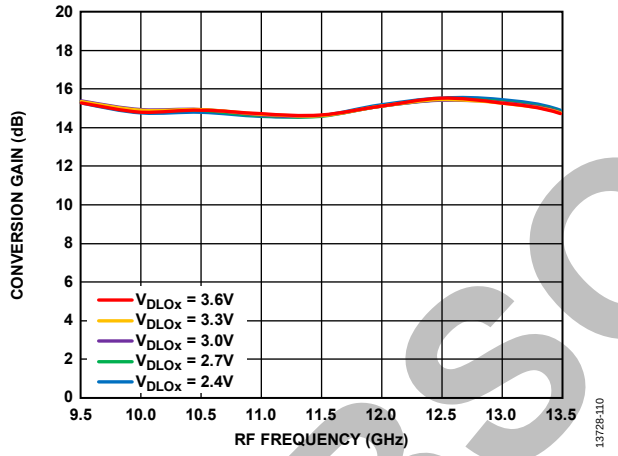


Figure 108. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

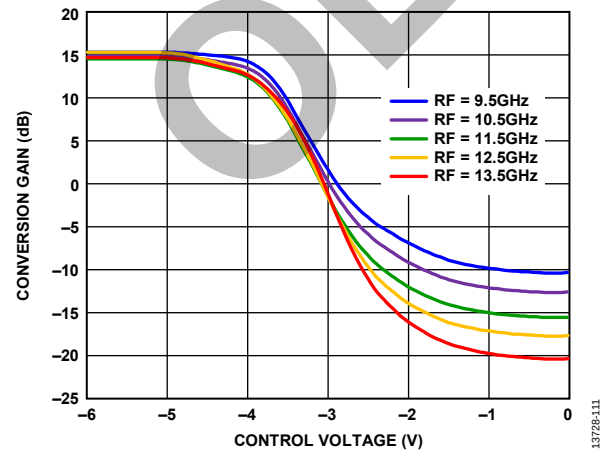


Figure 109. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

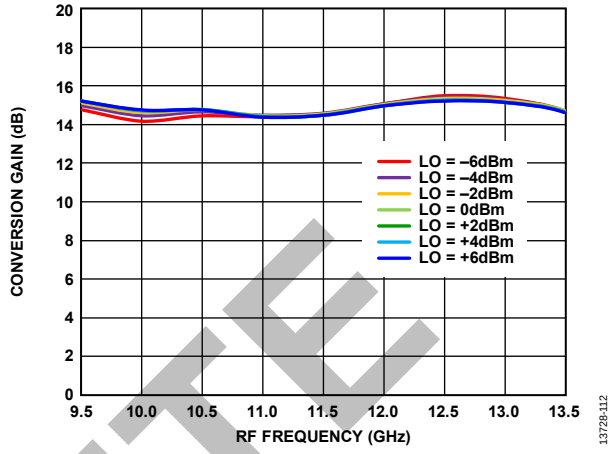


Figure 110. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

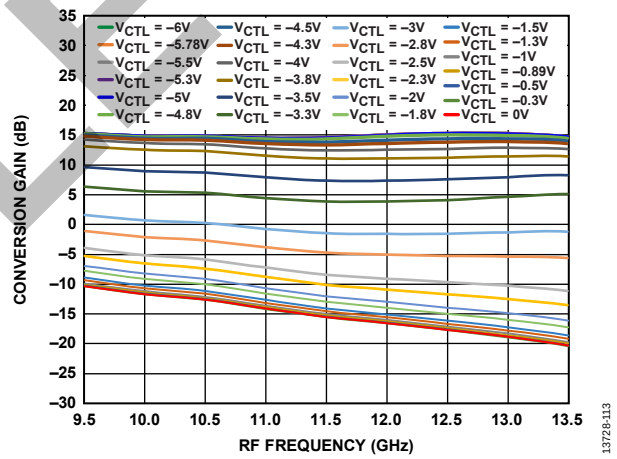


Figure 111. Conversion Gain vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

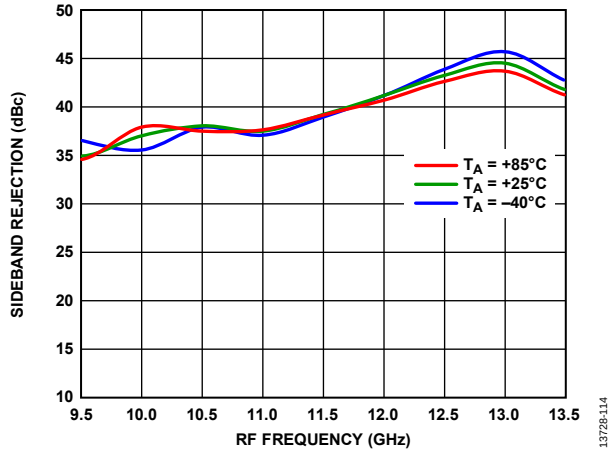


Figure 112. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

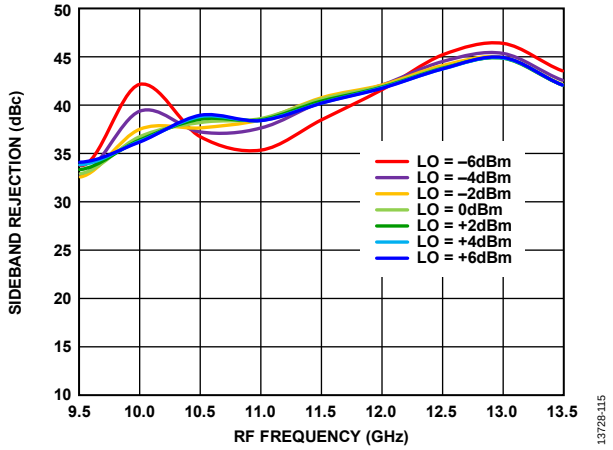


Figure 113. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

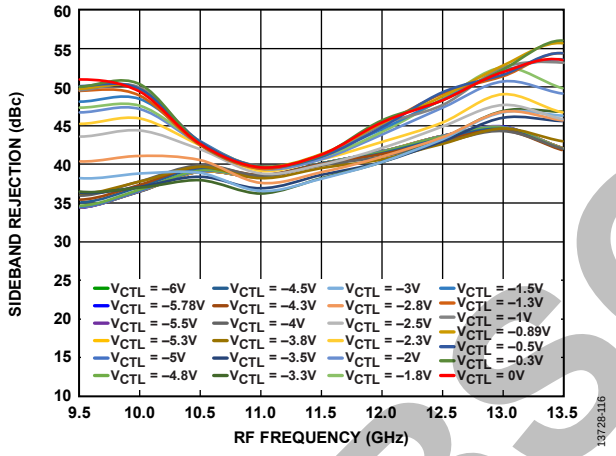


Figure 114. Sideband Rejection vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

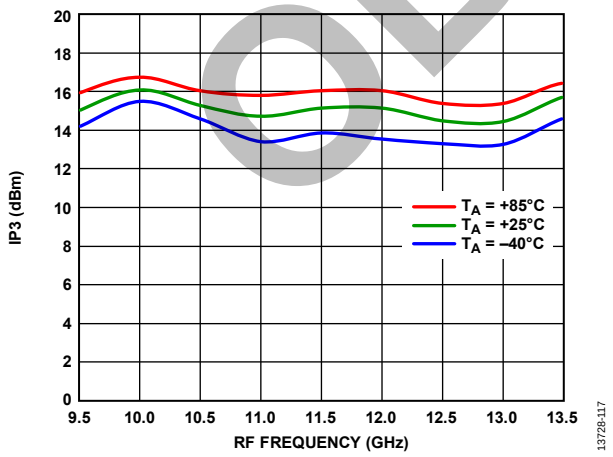


Figure 115. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

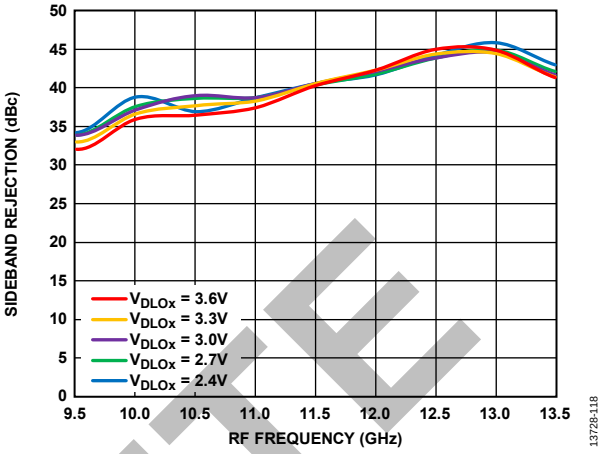


Figure 116. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

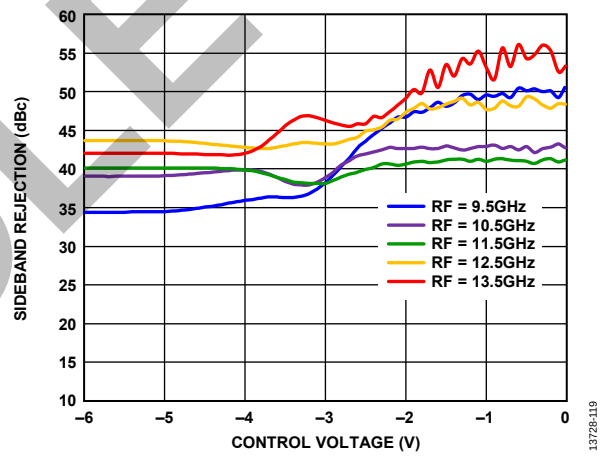


Figure 117. Sideband Rejection vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

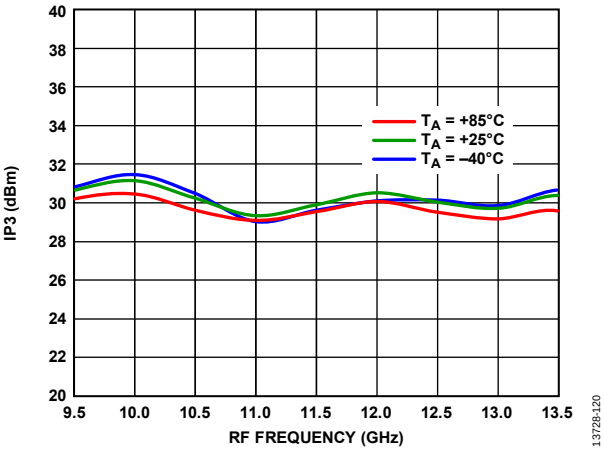


Figure 118. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

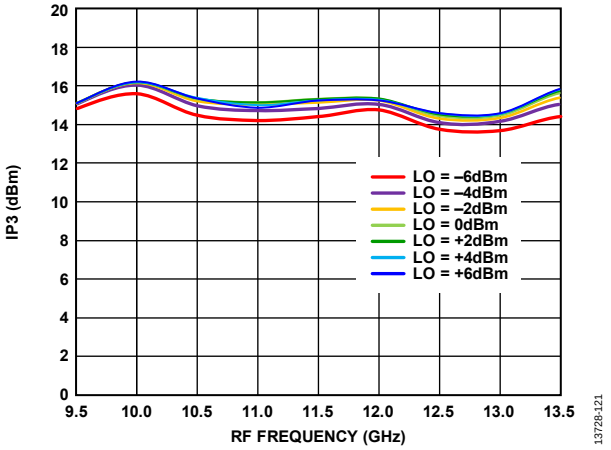


Figure 119. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

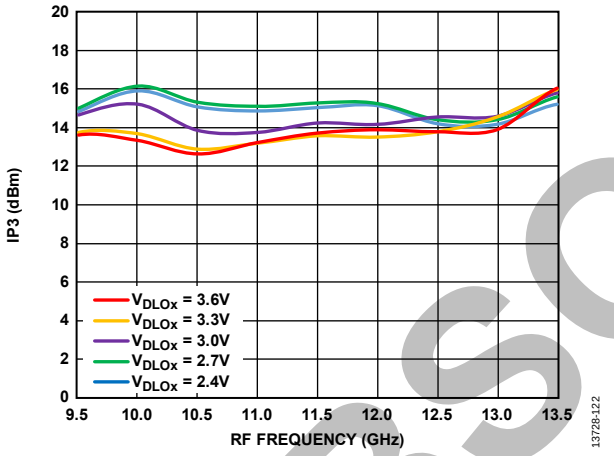


Figure 120. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

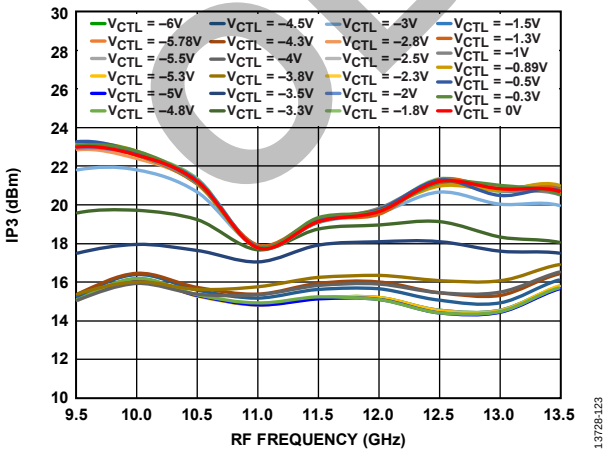


Figure 121. Input IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

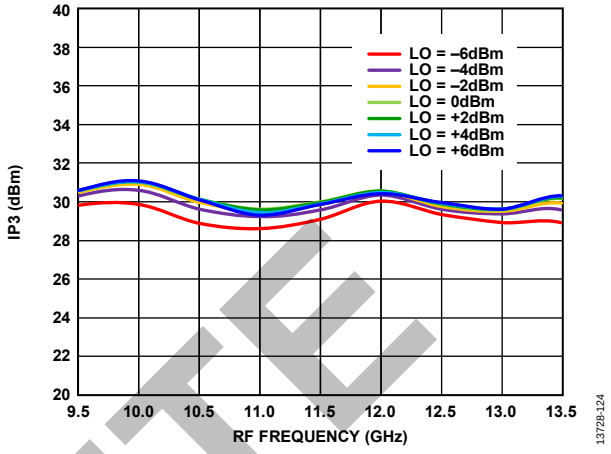


Figure 122. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

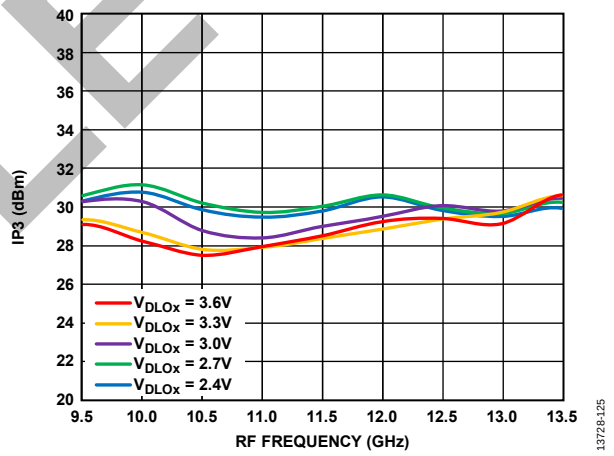


Figure 123. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

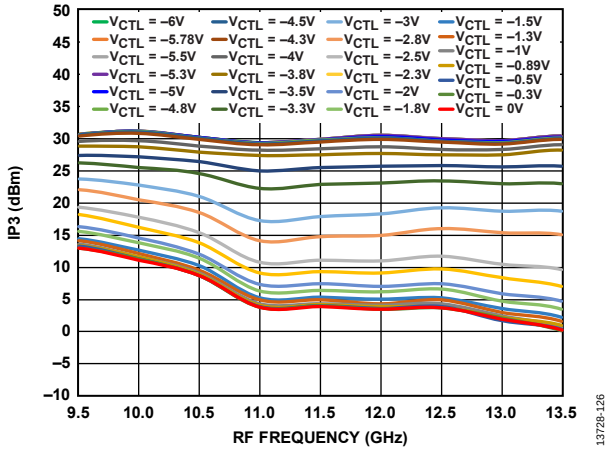


Figure 124. Output IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

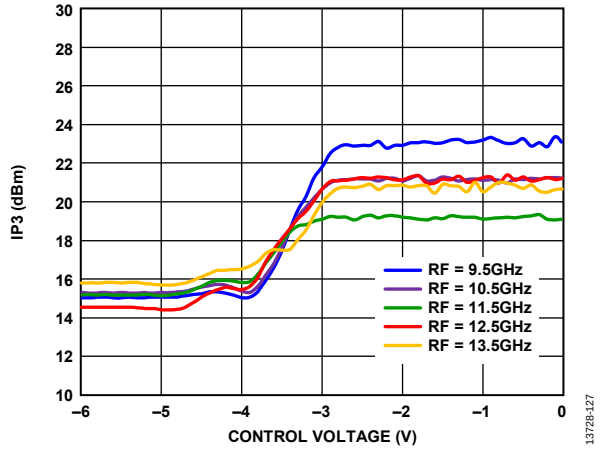


Figure 125. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

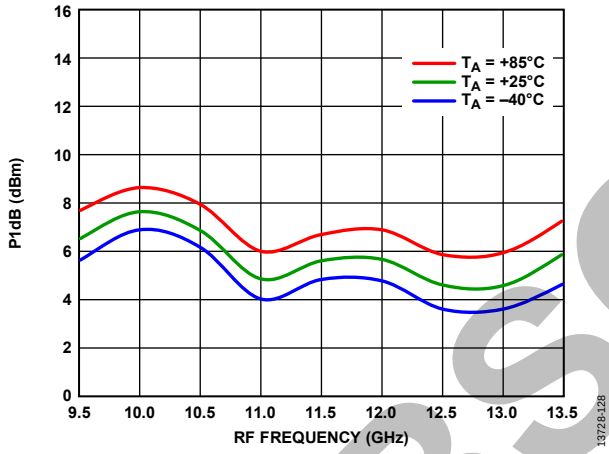


Figure 126. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

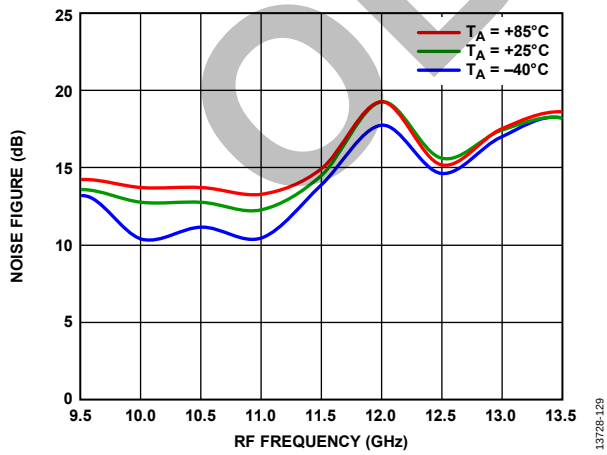


Figure 127. Noise Figure vs. RF Frequency at Various Temperatures,

LO = 2 dBm, V_{DLOx} = 2.7 V

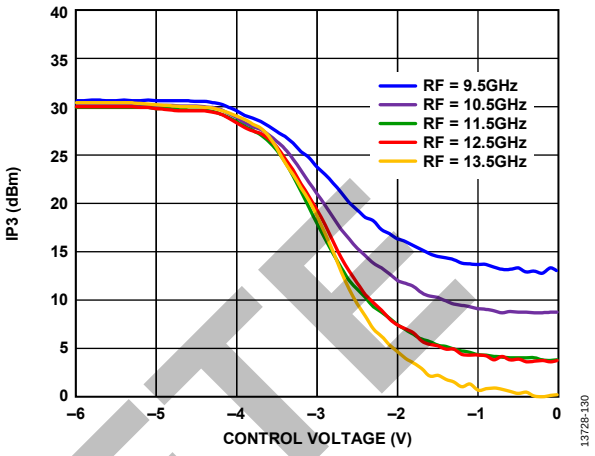


Figure 128. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

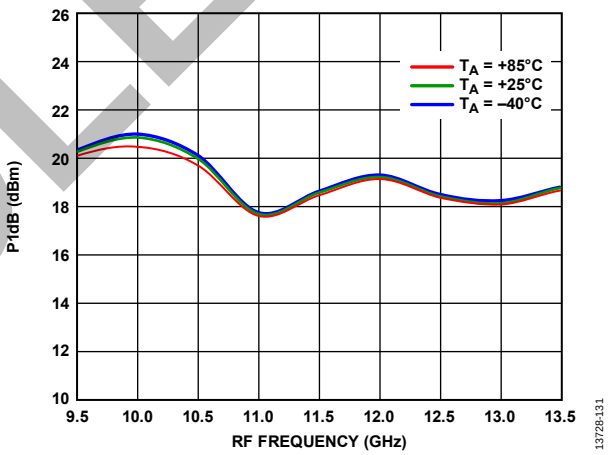


Figure 129. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

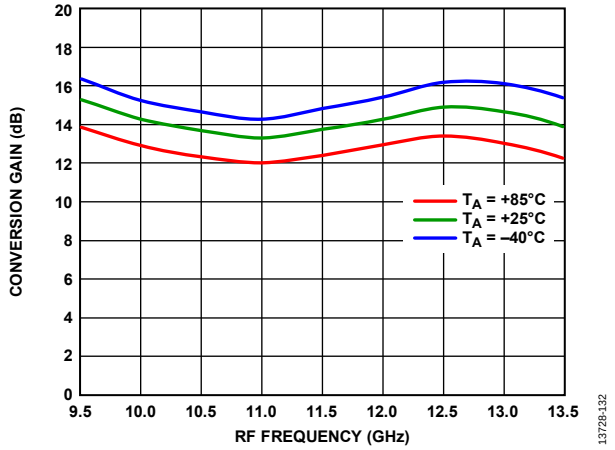


Figure 130. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

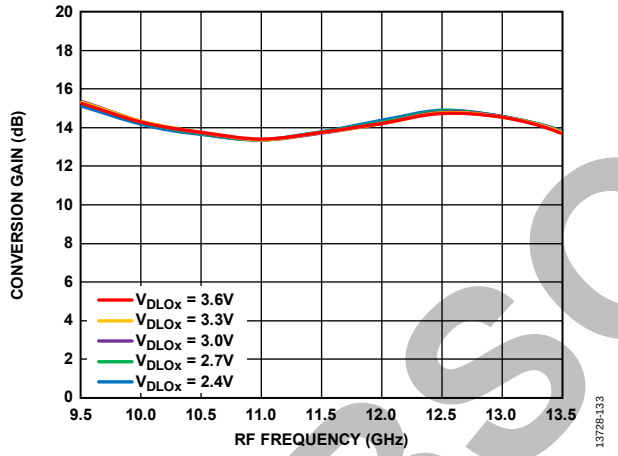


Figure 131. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

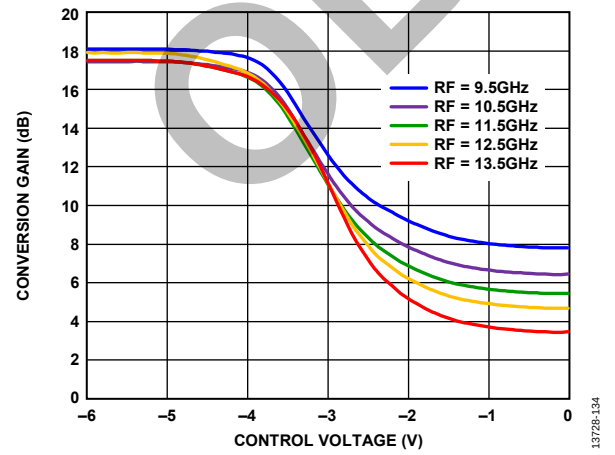


Figure 132. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

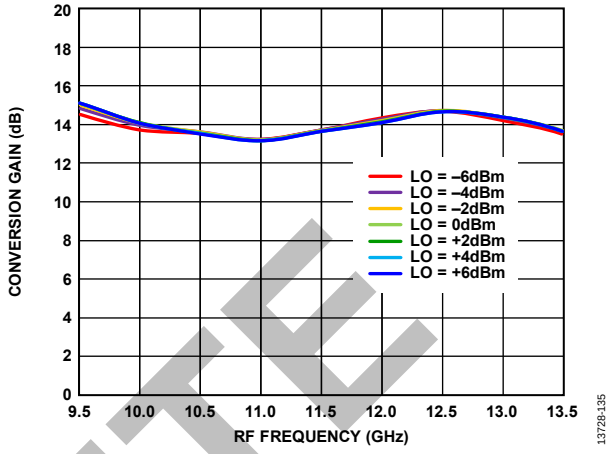


Figure 133. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

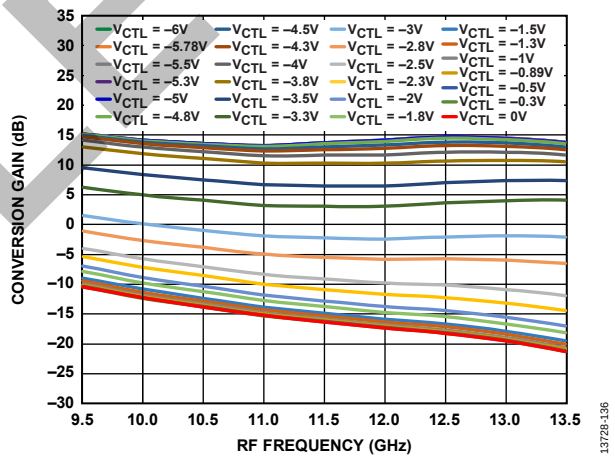


Figure 134. Conversion Gain vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

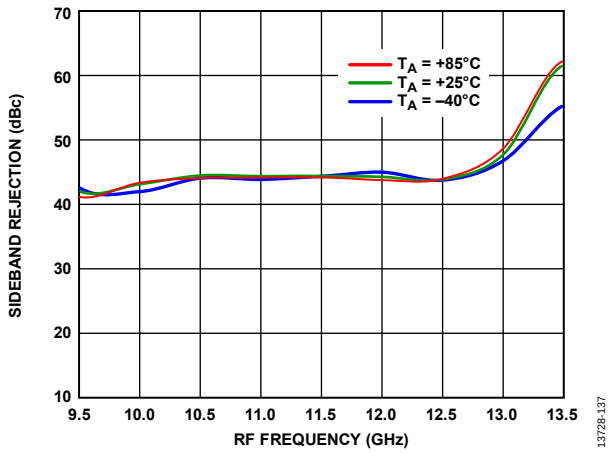


Figure 135. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

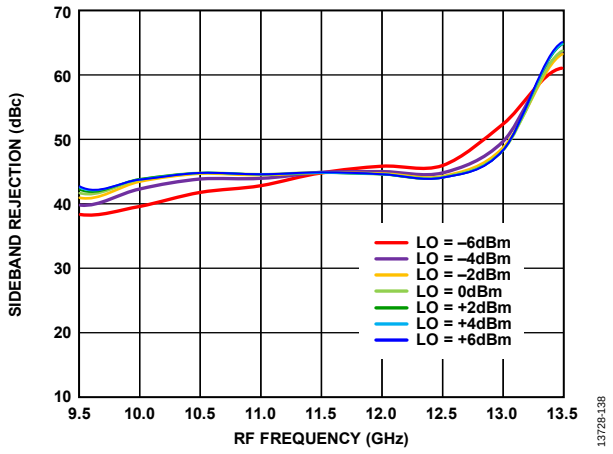


Figure 136. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

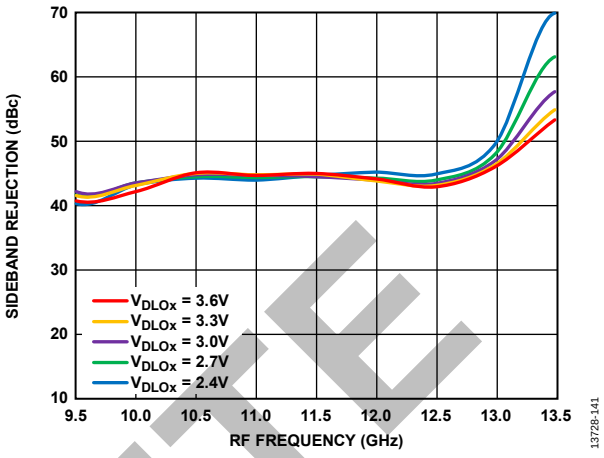


Figure 139. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

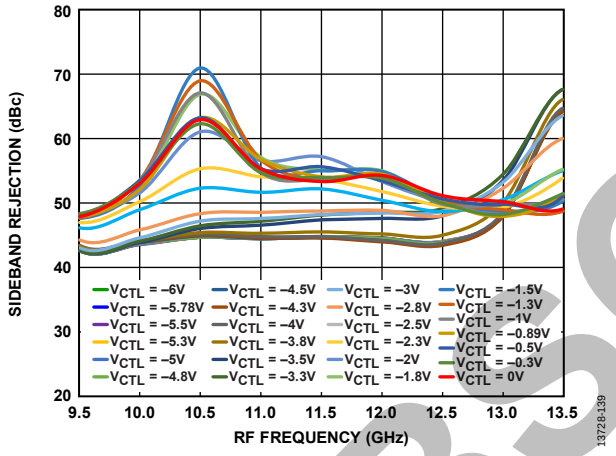


Figure 137. Sideband Rejection vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

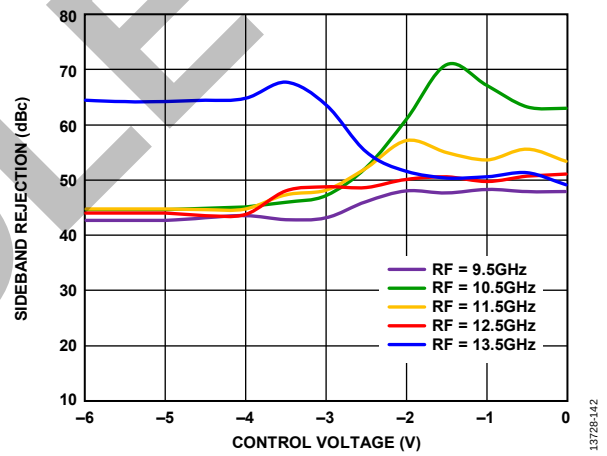


Figure 140. Sideband Rejection vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

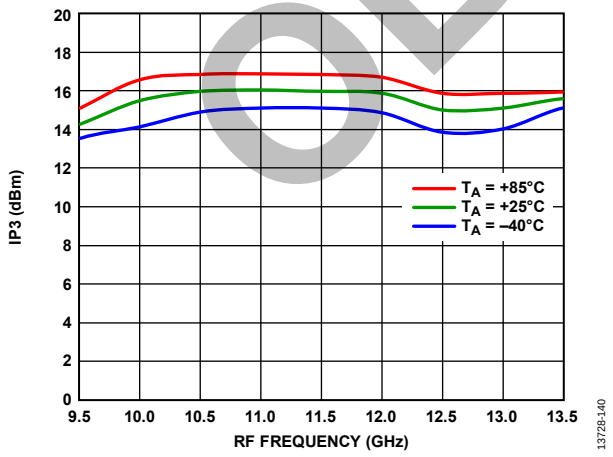


Figure 138. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

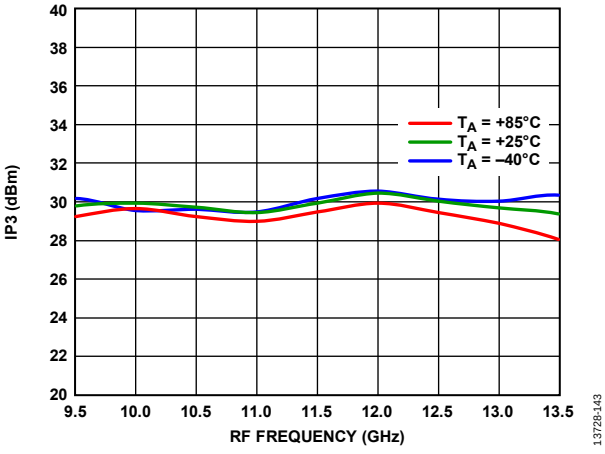


Figure 141. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

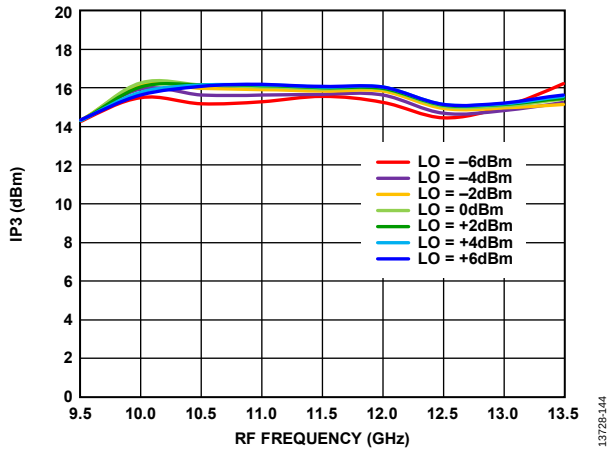


Figure 142. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

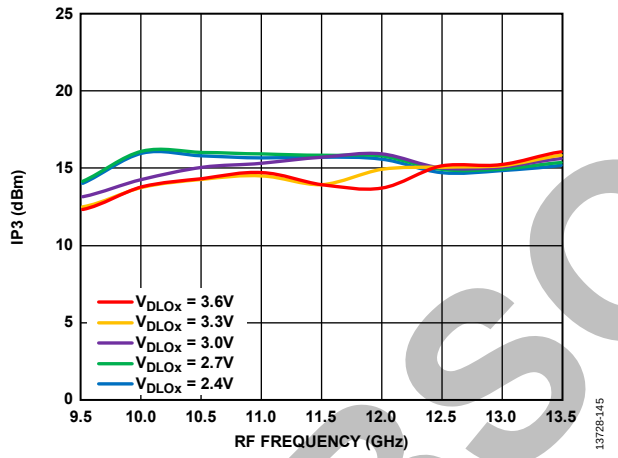


Figure 143. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

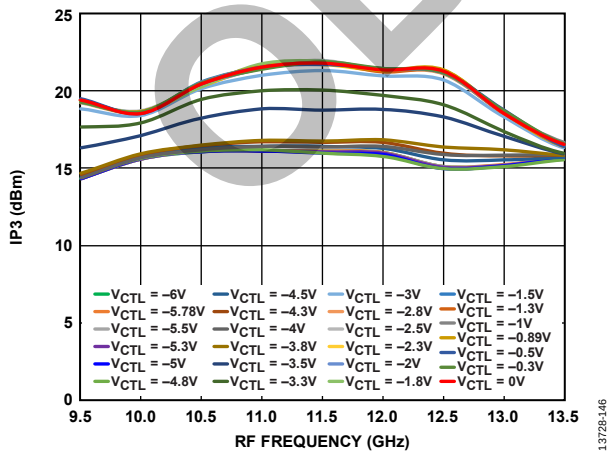


Figure 144. Input IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

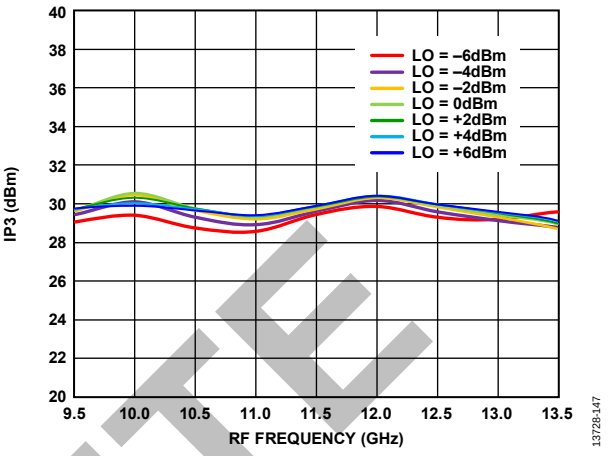


Figure 145. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.7 V

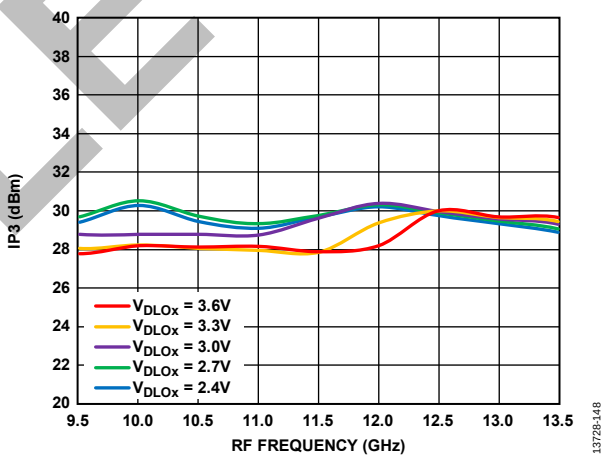


Figure 146. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

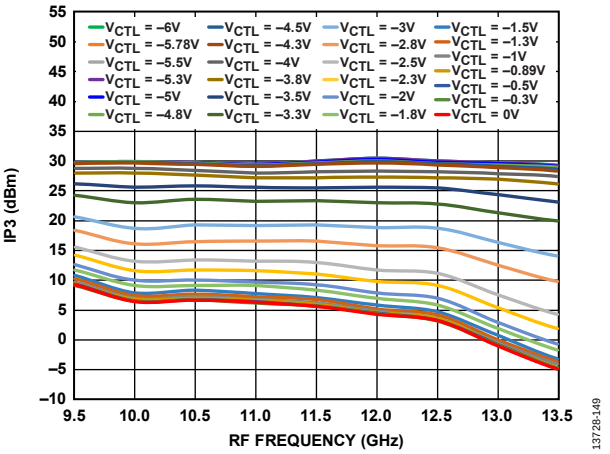


Figure 147. Output IP3 vs. RF Frequency at Various Control Voltages (V_{CTL}), LO = 2 dBm, V_{DLOx} = 2.7 V

Data taken as an SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

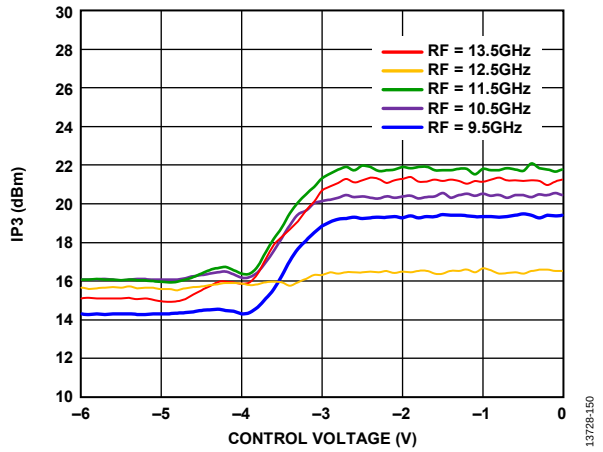


Figure 148. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

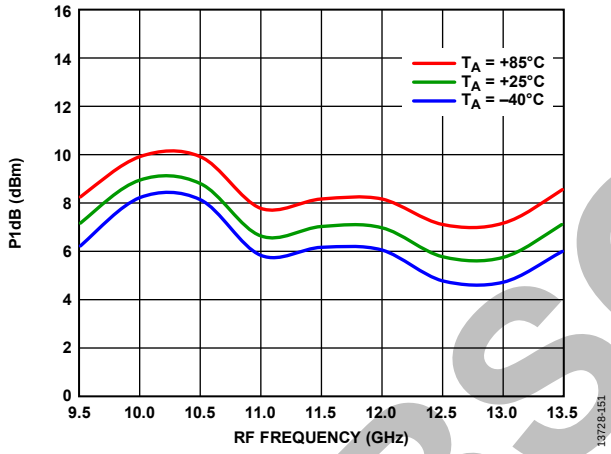


Figure 149. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

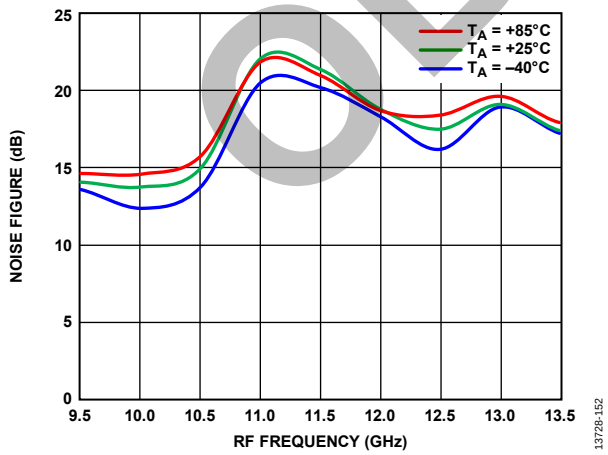


Figure 150. Noise Figure vs. RF Frequency at Various Temperatures,

LO = 2 dBm, V_{DLOx} = 2.7 V

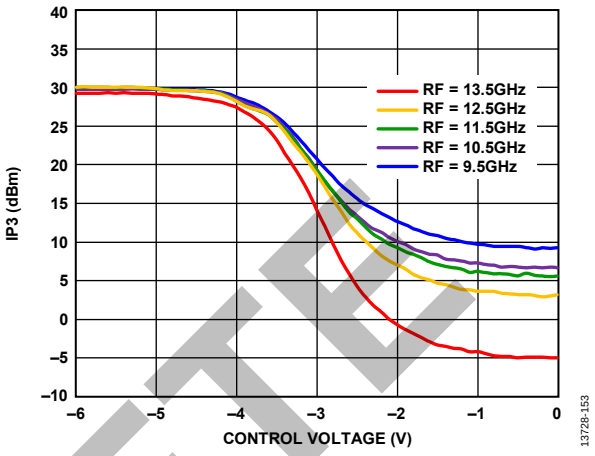


Figure 151. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.7 V

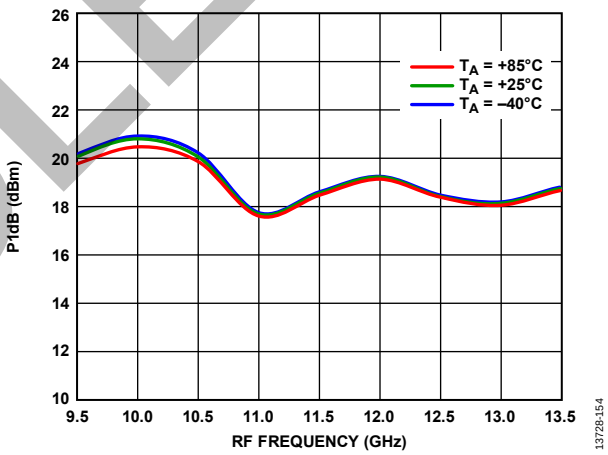


Figure 152. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.7 V

LEAKAGE PERFORMANCE

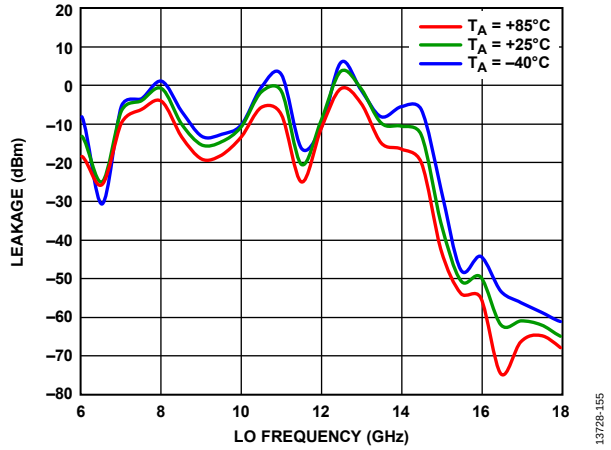


Figure 153. LO Leakage at RFOUT vs. Frequency at Various Temperatures, LO = 2 dBm

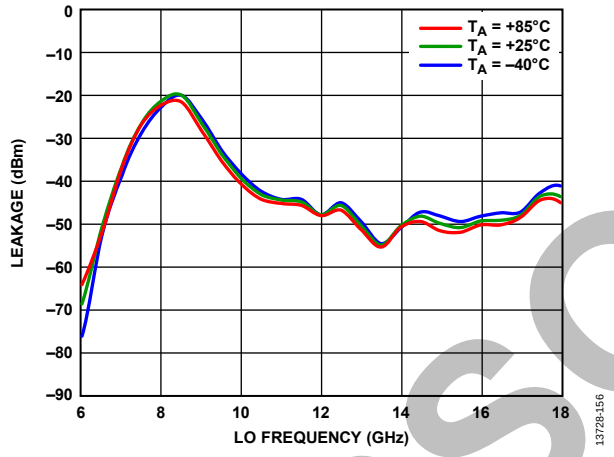


Figure 154. LO Leakage at IF2 vs. Frequency at Various Temperatures, LO = 2 dBm

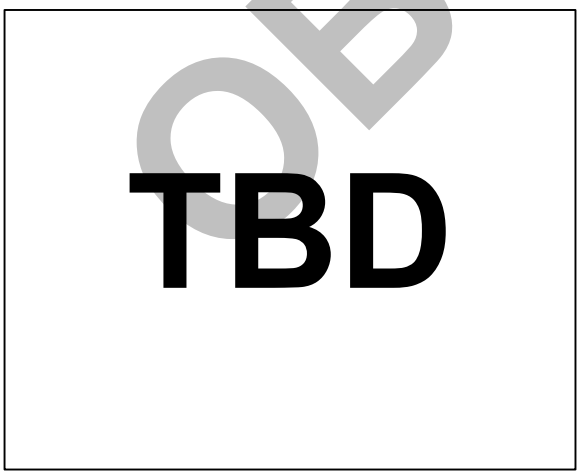


Figure 155. IF2 Leakage at RFOUT vs. Frequency at Various Temperatures, LO = 2 dBm

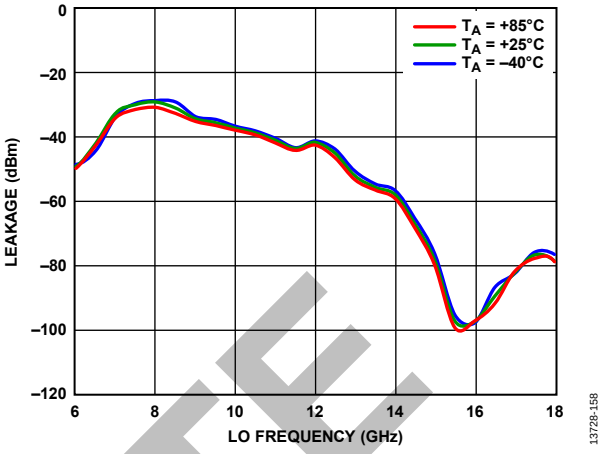


Figure 156. LO Leakage at IF1 vs. Frequency at Various Temperatures, LO = 2 dBm

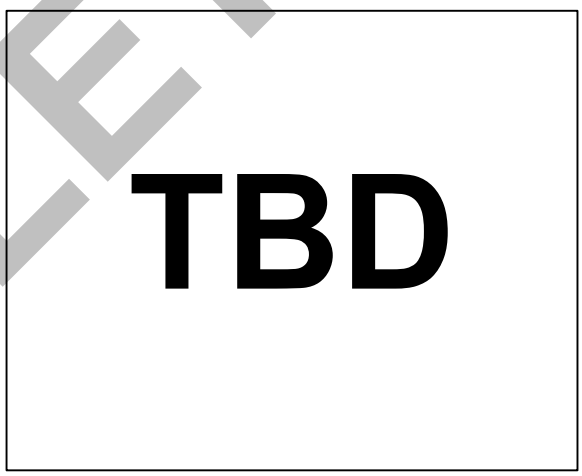


Figure 157. IF1 Leakage at RFOUT vs. Frequency at Various Temperatures, LO = 2 dBm

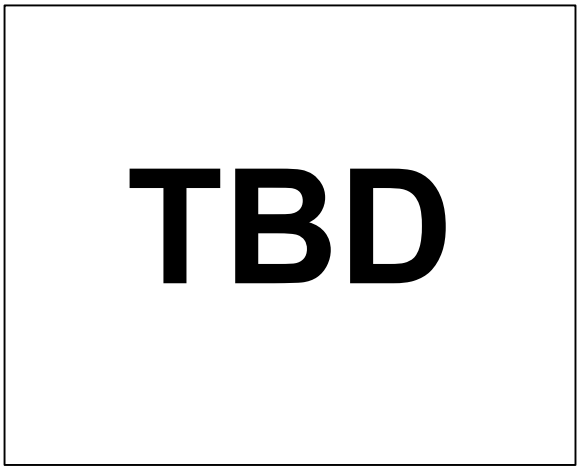


Figure 158. LO to RF Rejection vs. Frequency at Various Temperatures, LO = 2 dBm

RETURN LOSS PERFORMANCE

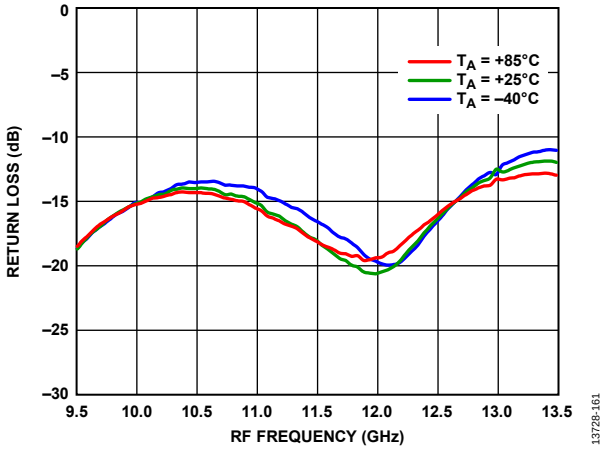


Figure 159. RF Return Loss vs. RF Frequency at Various Temperatures, LO = 2 dBm at LO = 15 GHz

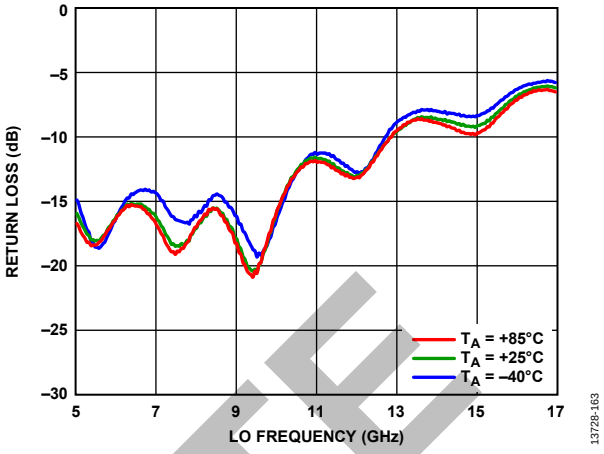


Figure 161. LO Return Loss vs. LO Frequency at Various Temperatures, LO = 2 dBm

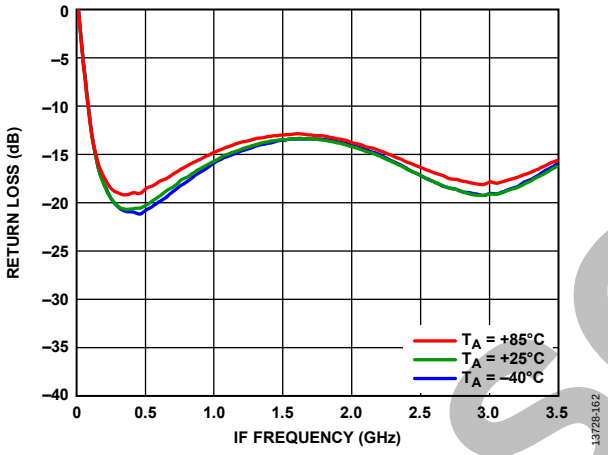


Figure 160. IF1 Return Loss vs. IF Frequency at Various Temperatures, LO = 2 dBm at LO = 15 GHz

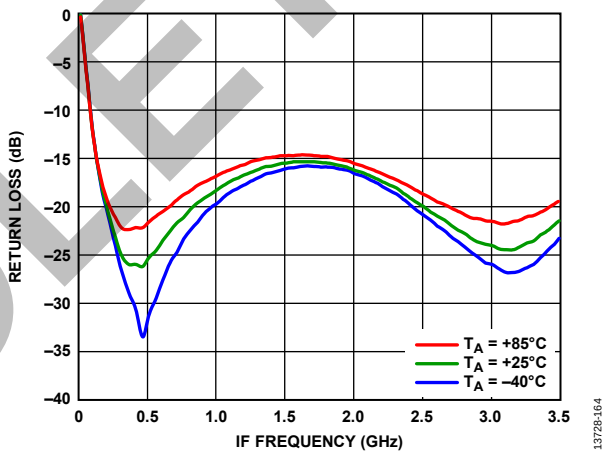


Figure 162. IF2 Return Loss vs. IF Frequency at Various Temperatures, LO = 2 dBm at LO = 15 GHz

POWER DETECTOR PERFORMANCE

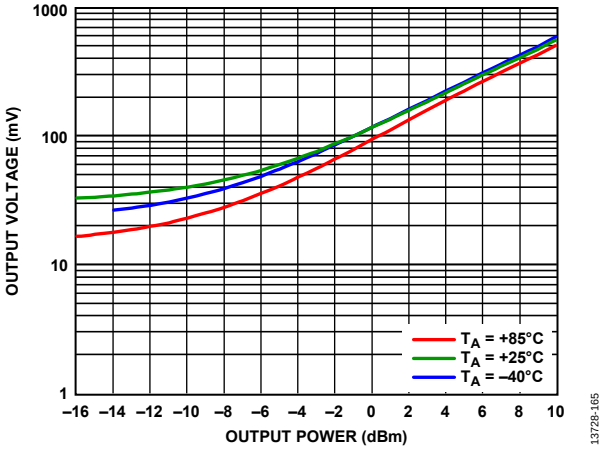


Figure 163. Detector Output Voltage ($V_{REF} - V_{DET}$) vs. Output Power at Various Temperatures, LO = 6 GHz

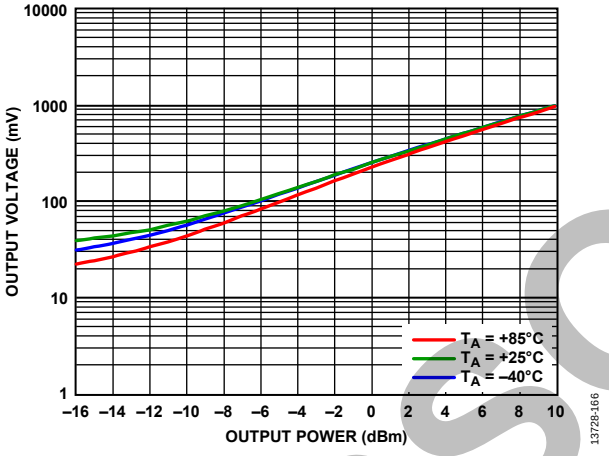


Figure 164. Detector Output Voltage ($V_{REF} - V_{DET}$) vs. Output Power at Various Temperatures, LO = 12 GHz

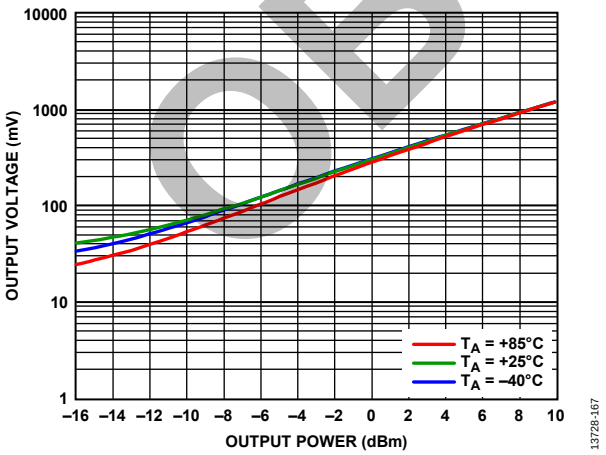


Figure 165. Detector Output Voltage ($V_{REF} - V_{DET}$) vs. Output Power at Various Temperatures, LO = 17 GHz

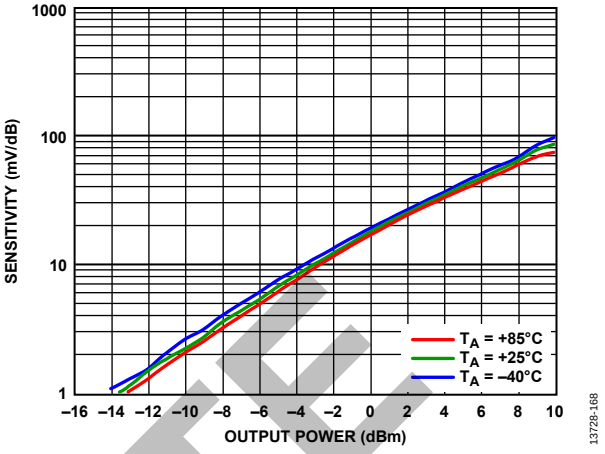


Figure 166. Detector Sensitivity vs. Output Power at Various Temperatures, LO = 6 GHz

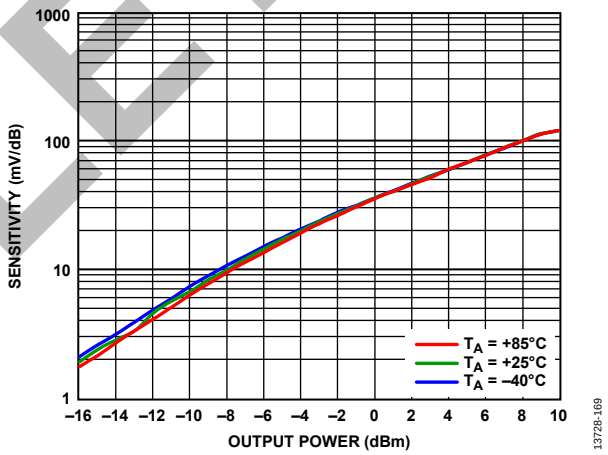


Figure 167. Detector Sensitivity vs. Output Power at Various Temperatures, LO = 12 GHz

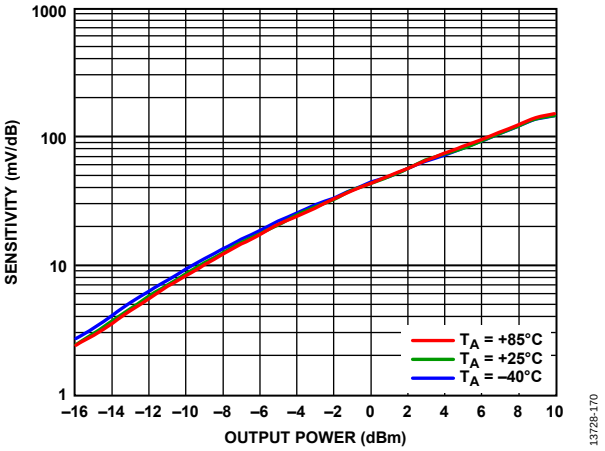


Figure 168. Detector Sensitivity vs. Output Power at Various Temperatures, LO = 17 GHz

UPPER SIDEBAND SPURIOUS PERFORMANCE

T_A = 25°C, IF = 1 GHz, V_{DLOx} = 2.4 V, V_{DREx} = 5 V, V_{CC} = 5 V, V_{CTL} = −6 V, V_{ESD} = −5 V, V_{SS} = −5 V, V_{GMIX} = −0.5 V.

Mixer spurious products are measured in dBc from the RF output power level. Spur values are (M × IF) + (N × LO). N/A means not applicable.

M × N Spurious Outputs, RF = 10 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 9 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	16	38	71	77	70
	1	64	0	38	86	92	90
	2	65	42	41	82	93	111
	3	74	64	77	66	85	105
	4	114	91	99	98	82	111
	5	94	84	113	115	101	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 8 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	7	22	62	90	74
	1	53	0	43	65	78	92
	2	52	33	41	72	77	90
	3	26	23	66	66	86	104
	4	23	22	62	90	74	77
	5	23	43	65	78	92	N/A

IF = 3 GHz at IF input power = −6 dBm, LO frequency = 7 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	5	23	45	55	75
	1	41	0	38	45	67	65
	2	45	38	42	73	64	74
	3	58	74	77	68	80	85
	4	71	75	92	99	87	114
	5	48	79	91	101	93	N/A

M × N Spurious Output, RF = 13 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 12 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**		16	75	75	72	N/A
	1	64	0	57	85	91	N/A
	2	69	46	47	69	N/A	N/A
	3	84	75	86	72	N/A	N/A
	4	98	105	104	92	N/A	N/A
	5	117	122	108	99	N/A	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 11 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	7	57	80	63	N/A
	1	52	0	48	71	89	N/A
	2	56	46	47	65	89	N/A
	3	84	76	80	71	N/A	N/A
	4	81	94	99	79	N/A	N/A
	5	99	102	106	89	N/A	N/A

IF = 3 GHz at IF input power = −6 dBm, LO frequency = 10 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	7	50	80	73	N/A
	1	42	0	45	69	87	N/A
	2	56	56	46	62	82	N/A
	3	69	73	77	69	79	N/A
	4	90	93	107	77	N/A	N/A
	5	103	103	118	98	N/A	N/A

LOWER SIDEBAND SPURIOUS PERFORMANCE

T_A = 25°C, IF = 1 GHz, V_{DLOx} = 2.7 V, V_{DREx} = 5 V, V_{CC} = 5 V, V_{CTL} = −6 V, V_{ESD} = −5 V, V_{SS} = −5 V, V_{GMIX} = −0.5 V.

Mixer spurious products are measured in dBc from the RF output power level. Spur values are (M × IF) − (N × LO). N/A means not applicable.

M × N Spurious Outputs, RF = 10 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 11 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	7	56	77	63	N/A
	1	54	0	44	71	93	N/A
	2	83	43	41	64	84	N/A
	3	84	71	73	66	77	N/A
	4	99	85	104	93	81	N/A
	5	112	111	116	107	108	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 12 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	15	69	74	72	N/A
	1	60	0	55	88	93	N/A
	2	73	45	40	72	99	N/A
	3	70	69	75	65	88	N/A
	4	45	73	62	98	80	N/A
	5	24	60	37	92	105	N/A

IF = 3 GHz at IF input power = −6 dBm, LO frequency = 13 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	11	70	71	N/A	N/A
	1	46	0	52	79	91	N/A
	2	59	34	40	70	104	N/A
	3	95	91	68	66	82	N/A
	4	90	126	95	97	81	N/A
	5	124	129	117	112	109	N/A

M × N Spurious Output, RF = 13 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 14 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	13	68	62	N/A	N/A
	1	60	0	55	81	N/A	N/A
	2	79	49	47	71	N/A	N/A
	3	97	85	88	71	N/A	N/A
	4	116	87	98	85	N/A	N/A
	5	122	114	106	116	N/A	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 15 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	33	71	64	N/A	N/A
	1	70	0	74	91	N/A	N/A
	2	75	44	48	83	N/A	N/A
	3	80	72	86	73	N/A	N/A
	4	88	84	106	103	N/A	N/A
	5	107	115	115	123	N/A	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 16 GHz at LO input power = 2 dBm.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	27	63	63	N/A	N/A
	1	67	0	71	92	N/A	N/A
	2	54	45	49	75	N/A	N/A
	3	73	73	85	75	N/A	N/A
	4	86	107	103	102	N/A	N/A
	5	116	135	126	123	117	N/A

THEORY OF OPERATION

The HMC9059 is a GaAs MMIC I/Q upconverter with an integrated LO buffer that upconverts intermediate frequencies (IF) between dc and 3.5 GHz to radio frequencies (RF) between 9.5 GHz and 13.5 GHz. LO buffer amplifiers are included on-chip to allow a LO drive level of only 2 dBm for full performance. The LO path feeds a quadrature splitter followed by on-chip baluns that drive the in phase (I) and quadrature (Q) singly balanced cores of the passive mixer. The RF output of the I and Q mixers are then summed through an on-chip Wilkinson power combiner and relatively matched to provide a single-ended 50 Ω output signal.

This output signal is amplified by RF amplifiers to produce a dc-coupled and 50 Ω matched radio frequency output signal at the RFOUT port. A voltage attenuator precedes the RF amplifiers for desired gain control.

The power detector feature provides LO cancellation capability to the level of −10 dBm (see Figure 169 for a functional block diagram of the circuit architecture).

The optimum output IP3 performance at a given LO power level is obtained when a 2.4 V power supply is used for V_{DLOx} with upper sideband selection. Alternatively, 2.7 V V_{DLOx} is recommended for lower sideband selection for optimum performance.

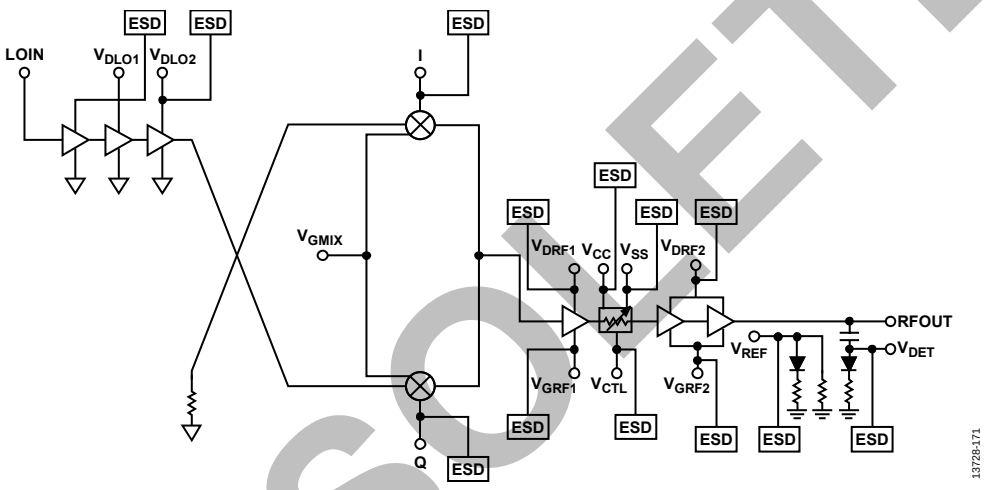


Figure 169. Upconverter Circuit Architecture

APPLICATIONS INFORMATION

A typical single-sideband upconversion circuit is shown in Figure 170. For single-sideband upconversion, an external 90° hybrid splits the IF signal into I and Q inputs. The LO to RF leakage can be improved by applying a small dc offsets to the I/Q mixer cores via the IF V_{DC_IF1} and V_{DC_IF2} inputs (where V_{DC_IFx} is the dc voltage at the IFx pins). However, it is important to limit the applied dc bias to avoid sourcing or sinking more than ±3 mA of bias current. Depending on the bias sources used, it may be prudent to add series resistance to ensure the applied bias current does not exceed ±3 mA.

BIASING SEQUENCE

The HMC9059 uses buffer amplifiers in the LO and RF paths. These active stages all use depletion mode pseudomorphic high electron mobility transistors (pHEMTs). To ensure that transistor damage does not occur, use the following power-up bias sequence:

1. Apply a −5 V bias to Pin 32 (V_{ESD}) and Pin 19 (V_{SS}).
2. Apply a −2 V bias to Pin 23 (V_{GRF1}), and Pin 26 (V_{GRF2}) (pinched off state).
3. Apply a −0.5 V bias to Pin 1 (V_{GMIX}). This bias can be adjusted from −1 V to +0.5 V depending on the LO power and V_{DLOx} used to provide the optimum IP3 response of the mixer.
4. Apply 2.4 V or 2.7 V to Pin 9 (V_{DLO1}) and Pin 10 (V_{DLO2}), depending on the sideband selection.
5. Apply −6 V to Pin 20 (V_{CTL}). Adjust V_{CTL} from −6 V to 0 V depending on amount of attenuation desired.
6. Apply 5 V to V_{DRF1}, V_{DRF2}, and V_{CC}.
7. Adjust V_{GRF1} and V_{GRF2} between −2 V and 0 V to achieve a total amplifier quiescent drain current of 240 mA.

LOCAL OSCILLATOR NULLING

Broad LO nulling may be required to achieve optimum IP3 and LO to RF isolation performance, which is achieved by applying dc voltages between −0.2 V and +0.2 V to the I and Q ports to suppress the LO signal across the RF frequency band by approximately 5 dBc to 10 dBc. To suppress the LO signal at the RF port, use the following nulling sequence:

1. Adjust the V_{DC_IF1} input between −0.2 V and +0.2 V and monitor the LO leakage on the RF port. As soon as the desired or maximum level of suppression is achieved, proceed to Step 2.
2. Adjust the V_{DC_IF2} input between −0.2 V and +0.2 V and monitor the LO leakage on the RF port until either the desired or maximum level of suppression is achieved.
3. If the desired level of the LO signal on the RF port is still not achieved, further tune each V_{DC_IF1} or V_{DC_IF2} input independently to achieve the desired LO leakage. Ensure that the voltage resolution changed on the voltage of the V_{DC_IFi} or V_{DC_IF2} inputs is in the millivolt range.

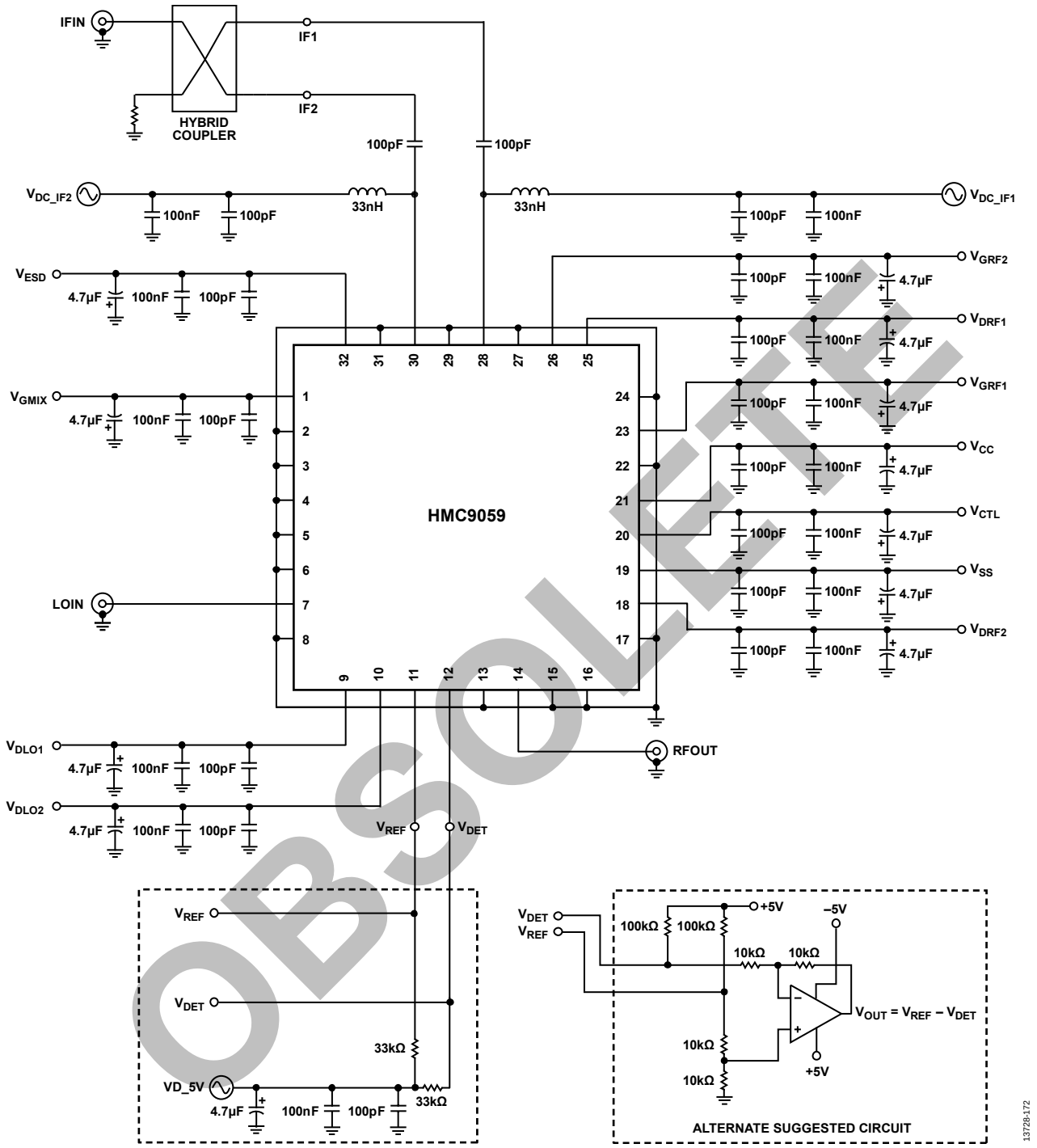


Figure 170. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD

The circuit board used in the application must use RF circuit design techniques. Signal lines must have 50 Ω impedance, and the package ground leads and exposed pad must be connected directly to the ground plane similarly to that shown in Figure 171. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 171 is available from Analog Devices, Inc., upon request.

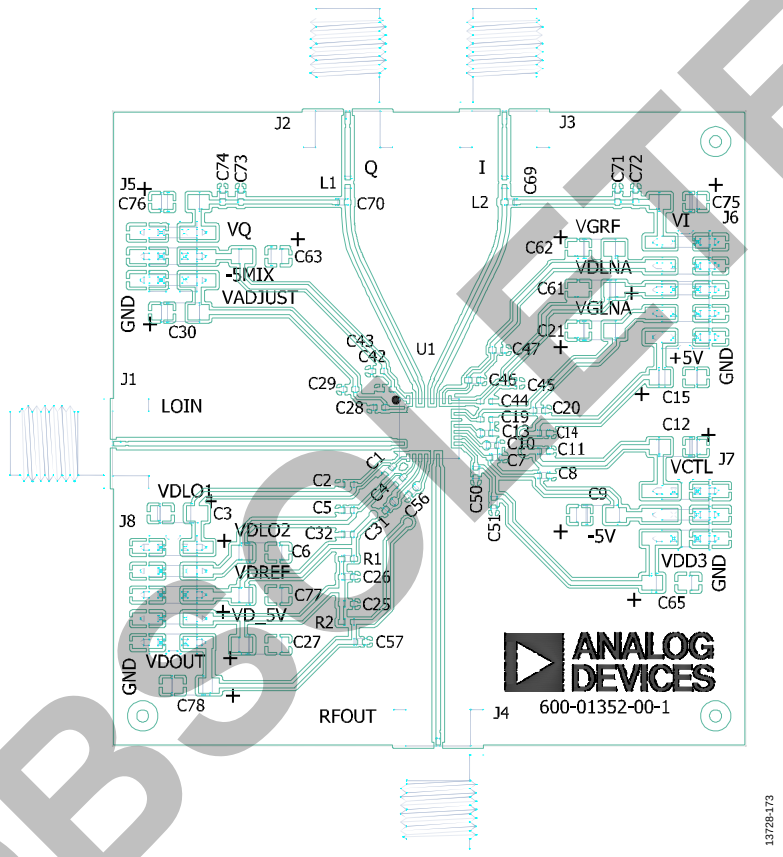
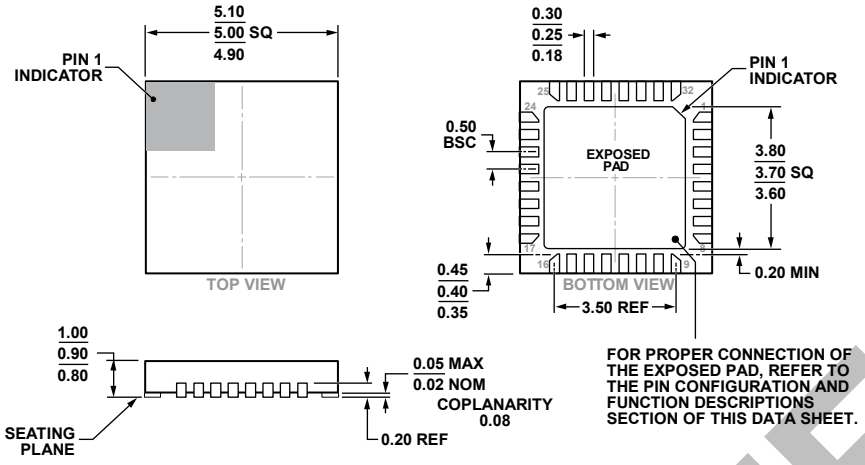


Figure 171. Evaluation Board Top Layer

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-4.

Figure 172. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body, Very Thin Quad
(HCP-32-3)
Dimensions shown in millimeters

PR13728-0-3/16(PrB)