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APPLICATION NOTE 5659

Step-by-Step Design Process for the MAX16833 High-Voltage High-Brightness LED Driver, Part 2

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Abstract: This application note details a step-by-step design process for the MAX16833 high-voltage high-brightness LED driver. This process can speed up prototyping and increase the chance for first-pass success. A typical design scenario is presented, along with example calculations based on the design constraints. Component selection trade-offs are discussed. A spreadsheet calculator (XLS) is included to help calculate external component values. This application note focuses on the buck-boost converter topology. However, the same process can be applied to other topologies as long as the underlying equations are understood. For a boost converter design example, see application note 5571, "Step-by-Step Design Process for the MAX16833 High-Voltage High-Brightness LED Driver, Part 1."

Introduction

This application note is the second in a series that details a step-by-step design process for the MAX16833 high-voltage high-brightness LED driver to speed up prototyping and increase the chance for first-pass success. The MAX16833 is a peak current-mode-controlled LED driver, capable of driving an LED string in several different architectures: boost, buck-boost, SEPIC, flyback, and high-side buck topologies. The first application note in the series, application note 5571, "Step-by-Step Design Process for the MAX16833 High-Voltage High-Brightness LED Driver, Part 1," focuses on the boost converter topology. This application note, Part 2, focuses on the buck-boost topology.

The MAX16833 offers several features: a dimming driver designed to drive an external p-channel MOSFET, extremely fast PWM current switching to the LEDs without transient overvoltage or undervoltage, analog dimming, programmable switching frequency between 100kHz and 1MHz, and the option of either a ramp output for frequency dithering or a voltage reference for precisely setting the LED current with few external components.

For the design example here in Part 2, a 4 LED string is driven with a constant current of 1A. Assume that each LED has a typical forward voltage drop of 3V and a dynamic resistance of 0.2Ω. Also assume that the LED driver circuit is running directly off of the car battery, which has a typical voltage of 12V but can vary from 6V to 16V. Since the LED string voltage is inside the input voltage range, the buck-boost configuration is chosen.
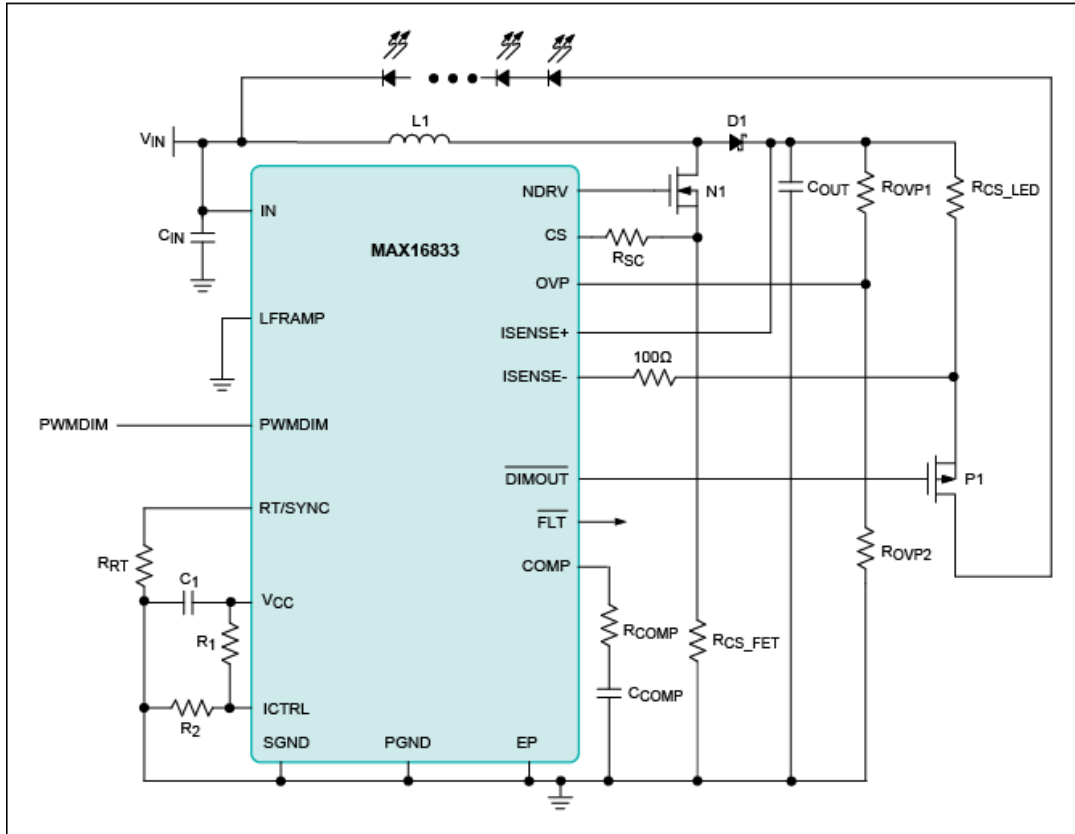
Figure 1. Typical operating circuit.

Inductor Selection (Buck-Boost)

In order to select the right inductor value, the maximum duty cycle must first be calculated:

$$D_{MAX} = \frac{V_{LED} + V_D}{V_{LED} + V_D + V_{INMIN} - V_{FET}}$$

(Eq. 1)

Where V_{LED} is the forward voltage of the LED string in volts, V_D is the forward drop of the rectifying diode (approximately 0.6V), V_{INMIN} is the minimum input-supply voltage in volts, and V_{FET} is the average drain-to-source voltage of the switching MOSFET in volts when it is on (assume 0.2V initially).

The maximum duty cycle and LED current determine the average inductor current.

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

(Eq. 2)

The peak inductor current is defined as follows:

$$IL_P = IL_{AVG} + \frac{\Delta I_L}{2}$$

(Eq. 3)

Where ΔI_L is the peak-to-peak inductor current ripple in amperes.

Finally, the minimum inductor value can be calculated:

$$L_{MIN} = \frac{(V_{INMIN} - V_{FET}) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

(Eq. 4)

Below is a numerical example based on the design problem outlined in the Introduction. Choose an inductor current ripple of 50%. Lower ripple current would require a larger (and typically more expensive) inductor. Higher ripple current requires more slope compensation and increased input capacitance.

$$D_{MAX} = \frac{12 + 0.6}{12 + 0.6 + 6.0 - 0.2} = 0.685 \tag{Eq. 5}$$

$$IL_{AVG} = \frac{1}{1 - 0.685} = 3.17A \tag{Eq. 6}$$

$$IL_P = 3.17 + \frac{1.59}{2} = 3.97A \tag{Eq. 7}$$

$$L_{MIN} = \frac{(6.0 - 0.6) \times 0.685}{3E^5 \times 1.59} = 7.75\mu H \tag{Eq. 8}$$

Once the minimum inductor value has been determined, a real inductor value must be chosen that is as close to L_{MIN} as possible without going under. Recalculate the peak inductor current and ripple using the chosen inductor value. These numbers are necessary for additional calculations going forward.

$$L_{ACTUAL} = 8.2\mu H \tag{Eq. 9}$$

$$\Delta I_L = \frac{(6.0 - 0.6) \times 0.685}{3E^5 \times 8.2E^{-6}} = 1.5A \tag{Eq. 10}$$

$$IL_P = 3.17 + \frac{1.5}{2} = 3.92A \tag{Eq. 11}$$

Ensure that the chosen inductor has a current rating higher than IL_P. Typically, 20% headroom is used for inductor peak current.

Switching MOSFET Selection

Choose a switching MOSFET that is rated to withstand the maximum output voltage.

$$V_{DS} = (V_{LED} + V_{INMAX} + V_D) \times 1.2 \tag{Eq. 12}$$

The factor of 1.2 is included for margin.

The switching MOSFET must also be rated to handle the maximum RMS current.

$$I_{DRMS} = 1.3 \times \sqrt{(IL_{AVG})^2 \times D_{MAX}} \tag{Eq. 13}$$

Where I_{DRMS} is the switching MOSFET's drain RMS current in amperes.

Rectifier Diode Selection

The rectifier diode can be a major contributor to overall power loss. Choose a Schottky diode with low forward voltage drop that is rated to handle the average LED current.

$$I_D = IL_{AVG} \times (1 - D_{MAX}) \times 1.2 \tag{Eq. 14}$$

The factor of 1.2 is included for margin.

Also, ensure that the Schottky diode has a reverse voltage rating 20% higher than ($V_{LED} + V_{INMAX}$), the maximum expected reverse voltage across the diode.

Dimming MOSFET Selection

Select a dimming MOSFET with a continuous current rating at an operating temperature 30% higher than the LED current. The drain-to-source voltage rating of the dimming MOSFET must be 20% higher than V_{LED}.

Input Capacitor Selection

In a buck-boost converter, the input current is continuous (assuming the output capacitor is connected to ground; see the Output Capacitor Connection section), so the RMS ripple current is low. Both bulk capacitance and ESR contribute to the input ripple. Assume equal ripple contributions from bulk capacitance and ESR if both aluminum electrolytic and ceramic capacitors are used in parallel. If only ceramic capacitors are used, most of the input ripple comes from the bulk capacitance (since ceramic capacitors have very low ESR). Use Equations 15 and 16 to calculate the minimum input bulk capacitance and maximum ESR:

$$C_{IN} \geq \frac{\Delta I_L \times D_{MAX}}{4 \times \Delta V_{Q\_IN} \times f_{SW}}$$ (Eq. 15)

Where ΔV_{Q_IN} is the portion of input ripple due to the capacitor discharge.

$$ESR_{CIN} < \frac{\Delta V_{ESR\_IN}}{\Delta I_L}$$ (Eq. 16)

Where ΔV_{ESR_IN} is the input ripple due to ESR.

Assume that a maximum of 120mV of input ripple can be tolerated (2% of V_{INMIN}). Also, assume that 95% of this input ripple comes from the bulk capacitance. This assumption may need to be revisited if the calculated values are not easily attained with actual components. Based on the stated design specifications, the input capacitor is calculated as follows:

$$C_{IN} \geq \frac{1.5 \times 0.685}{4 \times 0.114 \times 3E5} = 7.5\mu F$$ (Eq. 17)

$$ESR_{CIN} < \frac{0.006}{1.5} = 4m\Omega$$ (Eq. 18)

Use two 4.7µF capacitors in parallel to achieve the 7.5µF minimum bulk capacitance. Ensure that the chosen capacitors meet the minimum bulk capacitance requirement *at the operating voltage* (capacitance can decrease substantially with a change in voltage in ceramic capacitors).

Output Capacitor Selection

The purpose of the output capacitor is to reduce the output ripple and source current to the LEDs when the switching MOSFET is on. Both bulk capacitance and ESR contribute to the total output voltage ripple. If ceramic capacitors are used, a majority of the ripple comes from the bulk capacitance. Use Equation 19 to calculate the required bulk capacitance:

$$C_{OUT} \geq \frac{I_{LED} \times D_{MAX}}{\Delta V_{Q\_OUT} \times f_{SW}}$$ (Eq. 19)

Where ΔV_{Q_OUT} is the portion of output ripple due to the capacitor discharge.

The remaining ripple, ΔV_{ESR_OUT}, comes from the output capacitor ESR, which can be calculated as follows:

$$ESR_{COUT} < \frac{\Delta V_{ESR\_OUT}}{I_{LP}}$$ (Eq. 20)

To determine the total allowed output ripple, multiply the allowed LED current ripple by the dynamic impedance of the LED string. The dynamic impedance of an LED is defined as $\Delta V/\Delta I$ at the operating LED current and can be determined from the I-V curve in the LED data sheet. If an I-V curve is not provided in the LED data sheet, then it must be measured manually.

Use multiple ceramic capacitors in parallel to reduce the effective ESR and ESL of the bulk output capacitance.

During PWM dimming, the ceramic output capacitors might cause some audible noise. To reduce this noise, use an electrolytic or tantalum capacitor in conjunction with the ceramic capacitors to provide most of the bulk capacitance necessary. A low acoustic noise ceramic capacitor can also be used.[1]

Assume a maximum LED current ripple of 0.1 × I_{LED}. Also, assume that the dynamic impedance of the chosen LED is 0.2Ω (0.8Ω total for the 4 LED string). The total output voltage ripple is then calculated as follows:

$$V_{OUTRIPPLE} = 0.1A \times 0.8\Omega = 80mV \qquad \text{(Eq. 21)}$$

Assuming a ripple contribution of 95% from bulk capacitance, the output capacitor is calculated as follows:

$$C_{OUT} \geq \frac{1 \times 0.685}{0.076 \times 3E^5} = 30\mu F \qquad \text{(Eq. 22)}$$

$$ESR_{COUT} < \frac{0.004}{3.92} = 1.0m\Omega \qquad \text{(Eq. 23)}$$

Use three 10µF capacitors and one 4.7µF capacitor in parallel to achieve the minimum output capacitance of 30µF. Ensure that the chosen capacitors meet the minimum bulk capacitance requirement *at the operating voltage* (capacitance can decrease substantially with a change in voltage in ceramic capacitors).

Overvoltage Protection

If the LEDs are open, the converter tries to increase the output voltage to achieve the desired LED current. This means that the output voltage could approach unsafe levels. The OVP input is provided to sense an overvoltage condition and limit the output voltage. In the event that V_{OVP} exceeds 1.23V, NDRV is forced low until V_{OVP} discharges to 1.16V.

For a buck-boost configuration, the output voltage is equal to the input voltage plus the LED voltage. The V_{OV} trip point chosen should be above the maximum output voltage expected during normal operation.

$$V_{OV} > V_{INMAX} + V_{LEDMAX} \qquad \text{(Eq. 24)}$$

$$V_{OV} = 1.23V \times \frac{R_{OVP1} + R_{OVP2}}{R_{OVP2}} \qquad \text{(Eq. 25)}$$

For this design example, assume that a V_{OV} of 42V is desired. Choose R_{OVP2} to be 10kΩ, then

$$R_{OVP1} = \frac{(42 - 1) \times 10,000}{1.23V} \cong 330k\Omega \qquad \text{(Eq. 26)}$$

Current Sensing

The MAX16833 is a current-mode-controlled LED driver, which means that information about the inductor current and LED current is fed back into the loop.

LED Current Sensing

The LED current is programmed by either a series high-side current-sense resistor or the voltage applied to the ICTRL input.

If $V_{ICTRL} > 1.23V$, the internal reference regulates the voltage across R_{CS_LED} ($V_{ISENSE+}$ - $V_{ISENSE-}$) to 200mV. Therefore, the current-sense resistor R_{CS_LED} sets the LED current.

$$I_{LED} = \frac{200mV}{R_{CS\_LED}} \qquad \text{(Eq. 27)}$$

If $V_{ICTRL} < 1.23V$, then the LED current is determined by R_{CS_LED} and V_{ICTRL}. This allows the LEDs to be dimmed with an analog voltage.

$$I_{LED} = \frac{V_{ICTRL}}{R_{CS\_LED} \times 6.15} \qquad \text{(Eq. 28)}$$

Notice that when $V_{ICTRL} = 1.23V$, both equations are the same.

Switching FET Current Sensing and Slope Compensation

At duty cycles greater than 50%, a load transient can cause subharmonic oscillation and loop instability without slope compensation. To keep the loop stable, add a resistor (R_{SC} from CS to the source of the switching MOSFET). Internal to the MAX16833, there is a current source that feeds current through R_{SC} to create a voltage V_{SC}. This voltage is added to the voltage across R_{CS_FET} and the result is compared to a reference.

$$V_{CS} = V_{SC} + V_{CS\_FET} \qquad \text{(Eq. 29)}$$

The minimum amount of slope-compensation voltage needed to maintain stability is:

$$V_{SCMIN} = 0.5 \times (\text{inductor current downslope - inductor current upslope}) \times R_{CS\_FET} \qquad \text{(Eq. 30)}$$

The FET current-sense resistor, R_{CS_FET}, has both the switching MOSFET current and the slope compensation current flowing through it.
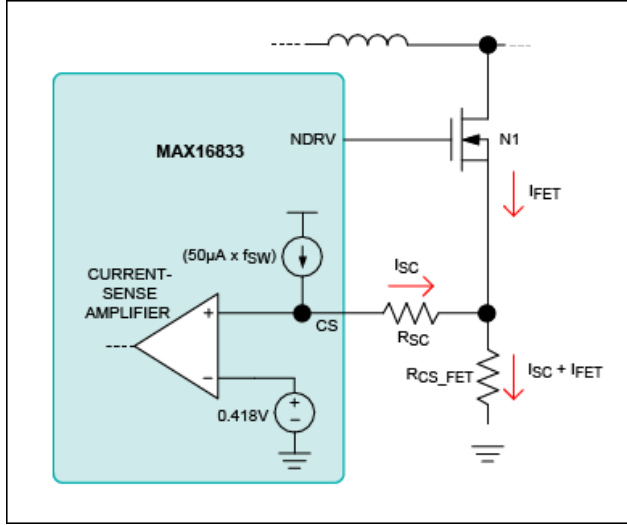

Figure 2. Slope compensation.

The slope-compensation voltage is defined as follows:

$$\frac{dV_{SC}}{dt} = \frac{R_{SC} \times 50\mu A}{T_{SW}} \qquad \text{(Eq. 31)}$$

In order to calculate the minimum necessary slope-compensation voltage, assume the minimum supply voltage and minimum inductor value:

$$\text{inductor current upslope} = \frac{V_{INMIN}}{L_{MIN}} \qquad \text{(Eq. 32)}$$

$$\text{inductor current downslope} = \frac{V_{LED}}{L_{MIN}} \qquad \text{(Eq. 33)}$$

Therefore:

$$V_{SCMIN} = \frac{D_{MAX} \times (V_{LED} - V_{INMIN}) \times R_{CS\_FET} \times 1.5}{2 \times L_{MIN} \times f_{SW}} \qquad \text{(Eq. 34)}$$

The factor of 1.5 is included to provide adequate margin.

$$R_{CS\_FET} = \frac{0.418V}{I_{LP} + 0.75 D_{MAX} \frac{V_{LED} - V_{INMIN}}{L_{MIN} \times f_{SW}}} \qquad \text{(Eq. 35)}$$

Once R_{CS_FET} has been determined, R_{SC} can be calculated as follows:

$$R_{SC} = \frac{(V_{LED} - V_{INMIN}) \times R_{CS\_FET} \times 1.5}{2 \times L_{MIN} \times f_{SW} \times 50\mu A} \qquad \text{(Eq. 36)}$$

Based on the stated design specifications, the slope compensation and current-sense resistors are calculated as follows:

$$R_{CS\_LED} = \frac{200mV}{1A} = 200m\Omega \qquad \text{(Eq. 37)}$$

$$R_{CS\_FET} = \frac{0.418V}{3.97 + 0.51\frac{12 - 6}{8.2E^{-6} \times 3E^{5}}} = 80m\Omega \qquad \text{(Eq. 38)}$$

The closest standard resistor value without going over is 75mΩ.

$$R_{SC} = \frac{(12 - 6) \times 0.075 \times 1.5}{2 \times 8.2E^{-6} \times 3E^{5} \times 50E^{-6}} \cong 2.7k\Omega \qquad \text{(Eq. 39)}$$

Error Amplifier Compensation

In the buck-boost configuration, the switching converter has a right-half-plane (RHP) zero that causes the loop to be unstable. The goal of loop compensation is to ensure that there is less than 180° of phase shift for loop gains > 0dB (and adequate phase margin). By adding a left-half-plane (LHP) pole, the loop gain can be rolled off to 0dB at approximately 1/5 f_{ZRHP} and the instability caused by the RHP zero can be avoided. The error amplifier must be compensated to ensure loop stability over all expected variations in operating conditions. The worst case RHP zero frequency is calculated as follows:

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^{2}}{2\pi \times L \times I_{LED} \times D_{MAX}} \qquad \text{(Eq. 40)}$$

There is also a pole at the output of the switching converter. The output pole, f_{P2}, can be calculated as follows:

$$f_{P2} = \frac{1}{2\pi \times C_{OUT} \times R_{OUT}} \qquad \text{(Eq. 41)}$$

Where C_{OUT} is the bulk output capacitance calculated above and R_{OUT} is the effective output impedance.

$$R_{OUT} = \frac{(R_{LED} + R_{CS\_LED}) \times V_{LED}}{(R_{LED} + R_{CS\_LED}) \times I_{LED} \times D_{MAX} + V_{LED}} \qquad \text{(Eq. 42)}$$

Where R_{LED} is the dynamic impedance of the LED string at the operating current in ohms.

The loop is compensated by adding a series resistor and capacitor (R_{COMP} and C_{COMP}) from COMP to SGND. R_{COMP} sets the crossover frequency and C_{COMP} sets the integrator zero frequency. For optimum performance, use the following equations:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS\_FET}}{5 \times f_{P2} \times (1 - D_{MAX}) \times R_{CS\_LED} \times 6.15 \times GM_{COMP}} \qquad \text{(Eq. 43)}$$

$$C_{COMP} = \frac{1}{2\pi \times R_{COMP} \times f_{P2}} \qquad \text{(Eq. 44)}$$

C_{COMP} and the output impedance of the error amplifier set the dominant pole frequency according to the following equation:

$$f_{P1} = \frac{1}{2\pi \times ROUT_{EA} \times C_{COMP}} \qquad \text{(Eq. 45)}$$

It is assumed that $ROUT_{EA}$ is much greater than R_{COMP}. $ROUT_{EA}$ is not specified in the MAX16833 data sheet, but it can be calculated from the transconductance and open-loop gain of the error amplifier. First, convert the open-loop gain of 75dB from decibels to volt/volt.

$$AV_{OTA} \left(\frac{V}{V}\right) = 10^{\left(\frac{75dB}{20}\right)} = 5623 \left(\frac{V}{V}\right) \qquad \text{(Eq. 46)}$$

Then $ROUT_{EA}$ can be calculated as follows:

$$ROUT_{EA} = \frac{AV_{OTA}}{GM_{COMP}} = \frac{5623}{3500E^{-6}} = 1.6M\Omega \qquad \text{(Eq. 47)}$$

Following the design example:

$$f_{ZRHP} = \frac{12 \times (1 - 0.685)^2}{2\pi \times 8.2E^{-6} \times 1 \times 0.685} = 33.7kHz \qquad \text{(Eq. 48)}$$

$$R_{OUT} = \frac{(0.8 + 0.2) \times 12}{(0.8 + 0.2) \times 1 \times 0.685 + 12} = 0.95\Omega \qquad \text{(Eq. 49)}$$

$$f_{P2} = \frac{1}{2\pi \times 3.47E^{-5} \times 0.95} = 4.8kHz \qquad \text{(Eq. 50)}$$

$$R_{COMP} = \frac{33700 \times 0.075}{5 \times 4800 \times (1 - 0.685) \times 0.2 \times 6.15 \times 3.5E^{-3}} = 78\Omega \qquad \text{(Eq. 51)}$$

The closest standard resistor value without going under is 82Ω.

$$C_{COMP} = \frac{1}{2\pi \times 82 \times 4800} = 0.40\mu F \qquad \text{(Eq. 52)}$$

The closest standard capacitor value without going under is 0.47µF.

$$f_{P1} = \frac{1}{2\pi \times 1.6E^{6} \times 0.47E^{-6}} = 0.2Hz \qquad \text{(Eq. 53)}$$

Loop Response and Phase Margin

We can approximate the phase margin (Φ_M) as follows:

$$\phi_M = 180° - \tan^{-1}\left(\frac{f_C}{f_{P1}}\right) - \tan^{-1}\left(\frac{f_C}{f_{P2}}\right) + \tan^{-1}\left(\frac{f_C}{f_{ZI}}\right) - \tan^{-1}\left(\frac{f_C}{f_{ZRHP}}\right) \qquad \text{(Eq. 54)}$$

By setting the crossover frequency at 1/5 of f_{ZRHP}, setting the integrator zero (f_{ZI}) at f_{P2}, and assuming f_{P1} is much less than f_C, the equation simplifies to the following:

$$\Phi_M = 90° - \tan^{-1}(0.2) = 79° \qquad \text{(Eq. 55)}$$

Figure 3 shows a simulated Bode plot based on the above external component choices. The crossover frequency is 5.5kHz and the phase margin is 79°. The crossover frequency is slightly below the hand calculated value but well within the expected range.
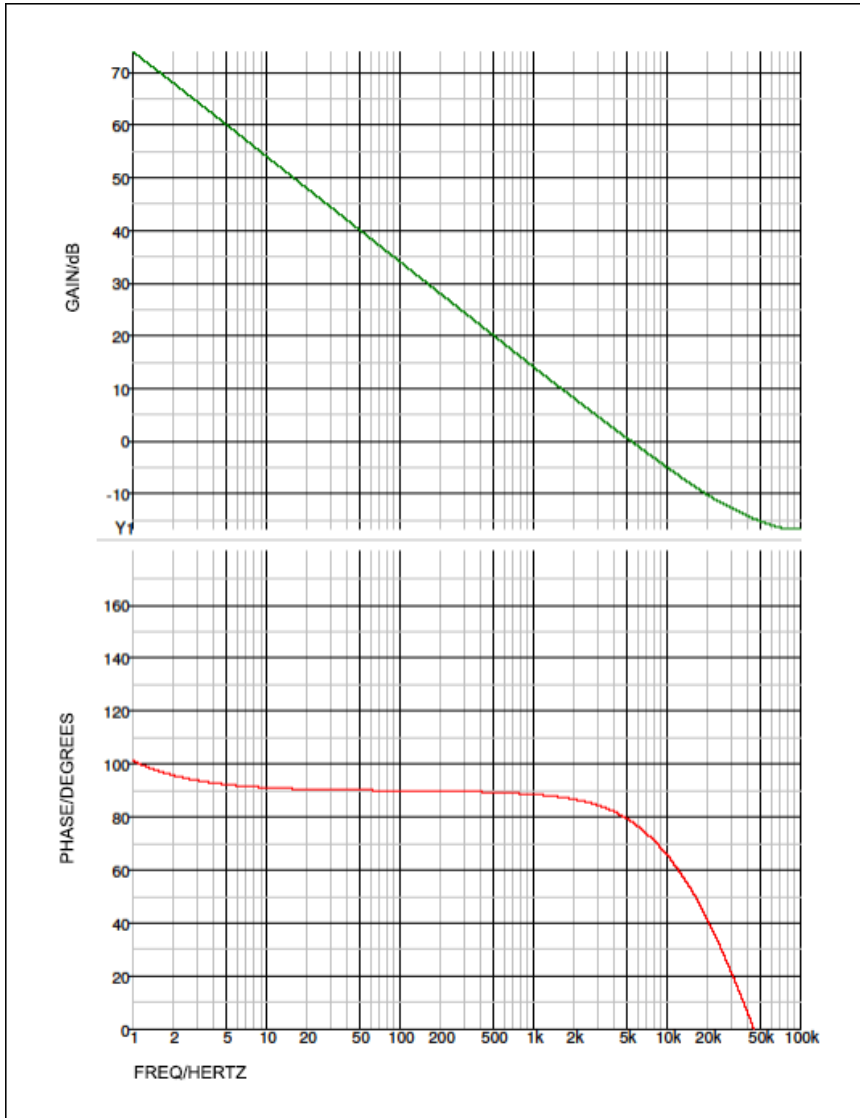
Figure 3. Bode plot simulation.

Calculating and simulating the loop response are both good ideas and important steps in designing a prototype HB LED driver. However, the loop response should also be verified in the lab *after* the prototype has been assembled.

Use a network analyzer and a transformer to inject a small signal into the loop and measure the response. Refer to **Figure 4** for a typical gain and phase measurement setup.
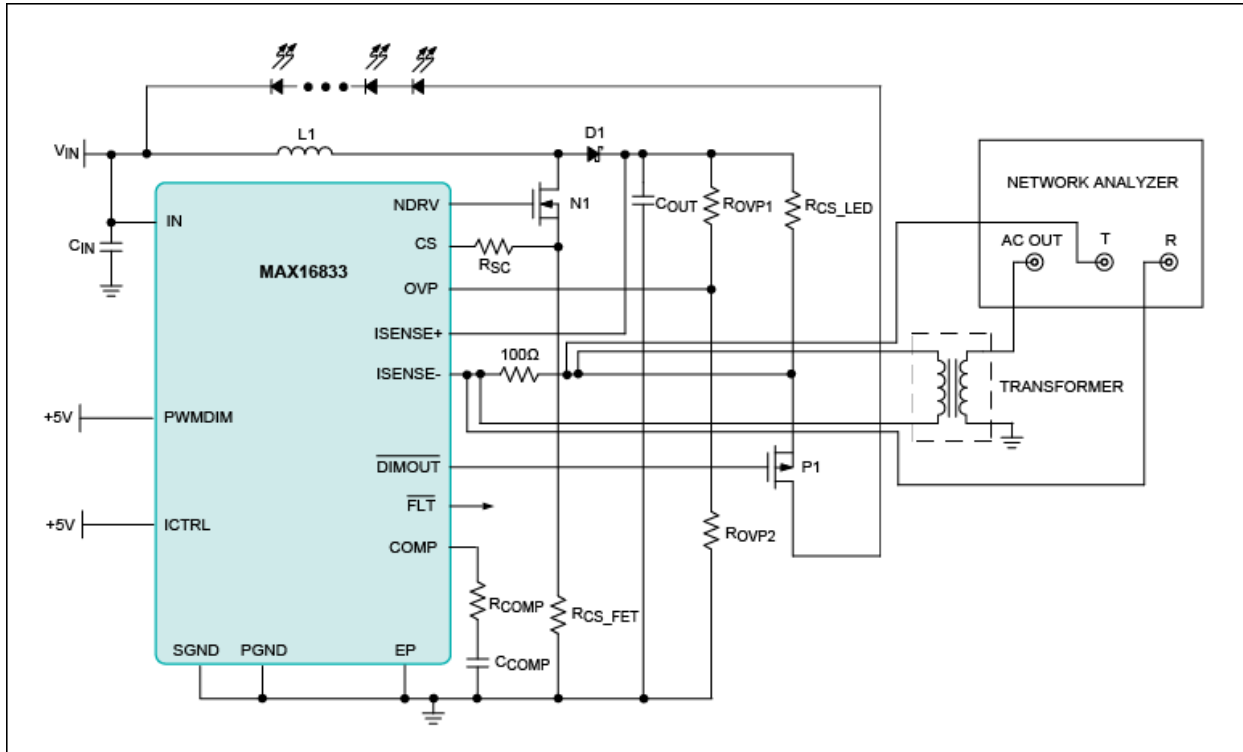
Figure 4. Setup for measuring the gain and phase response of the loop.

The AC signal needs to be injected into the feedback path across a small resistor and measured on both sides of the resistor. Since the design already has a 100Ω resistor in series with the ISENSE- input, there is no need to break the loop. The AC signal can be injected across the 100Ω resistor.

The loop response should be taken with full load current and no analog or PWM dimming, so make sure that PWMDIM and ICTRL are both high during the test. Also, the measurement should be performed with the minimum expected input voltage.

Check to make sure that the crossover frequency and phase margin measured by the network analyzer are close to the calculated values.

Designing a Circuit to Accommodate Multiple Applications

Often times, it is undesirable to do a new design for every application. If the differences between two applications are minimal, a system designer may choose to use the same circuit in both applications and accept the accompanying trade-offs in performance.

It is recommended that the designer evaluate and understand the behavior of their circuit under all varying conditions. These conditions include the minimum and maximum input voltage range, the minimum and maximum number of LEDs being driven, whether the cathode of the LED string is connected to GND (boost) or IN (buck-boost), etc.

Using the spreadsheet calculator (XLS) provided, it is easy to plug in the above scenarios and see which one dictates the minimum component values.
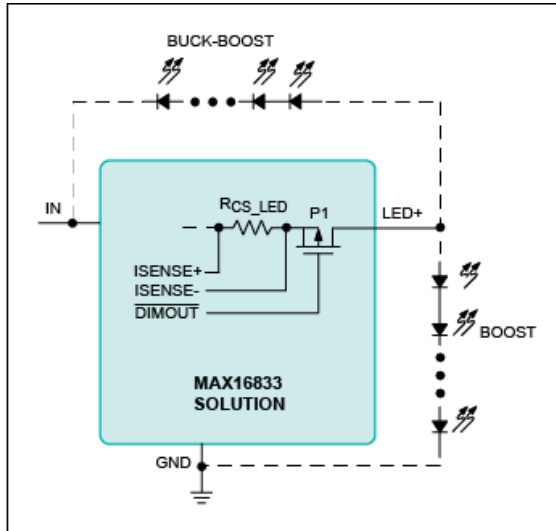
Figure 5. Generic MAX16833 solution allowing boost or buck-boost configuration.

Output Capacitor Connection

The output capacitor of the buck-boost LED driver is typically connected from the cathode of the Schottky diode to PGND. However, the output capacitor may also be connected from the cathode of the Schottky diode to V_{IN}. **Figure 6** shows both options for connecting the output capacitor of a buck-boost LED driver. Option A is the standard method and will usually provide the best EMI performance. However, because the LED cathode is connected to the input, the LED voltage is vulnerable to line-transient conditions. By connecting the output capacitor across the LEDs, the line-transient vulnerability is reduced. Option B has the drawback of changing the input current from continuous to discontinuous, increasing voltage ripple on the input and hurting EMI performance.
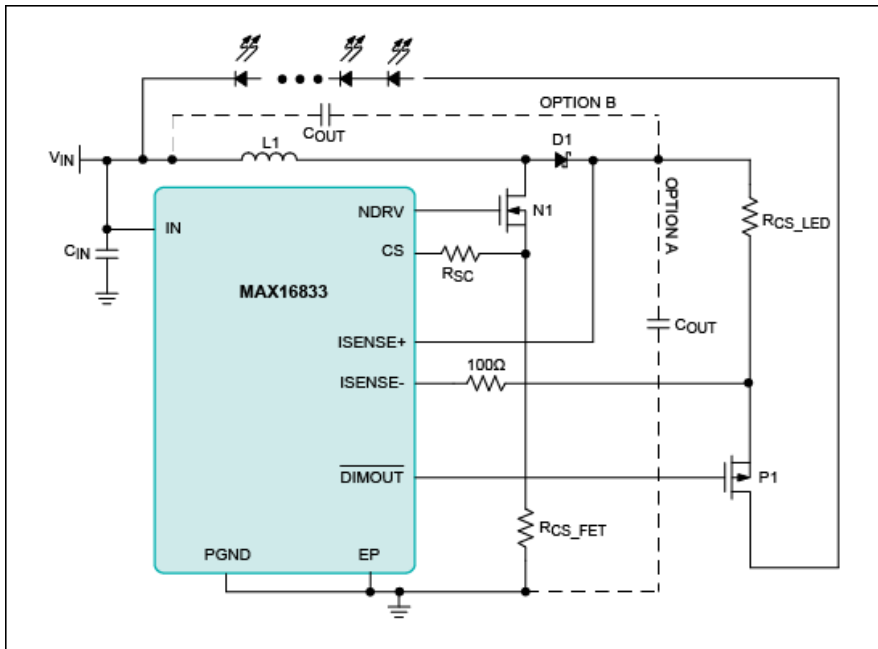

Figure 6. Two different options for connecting the output capacitor of a buck-boost LED driver.

Conclusion

The complete buck-boost LED driver schematic is shown in **Figure 7**. By following the step-by-step design process outlined in this

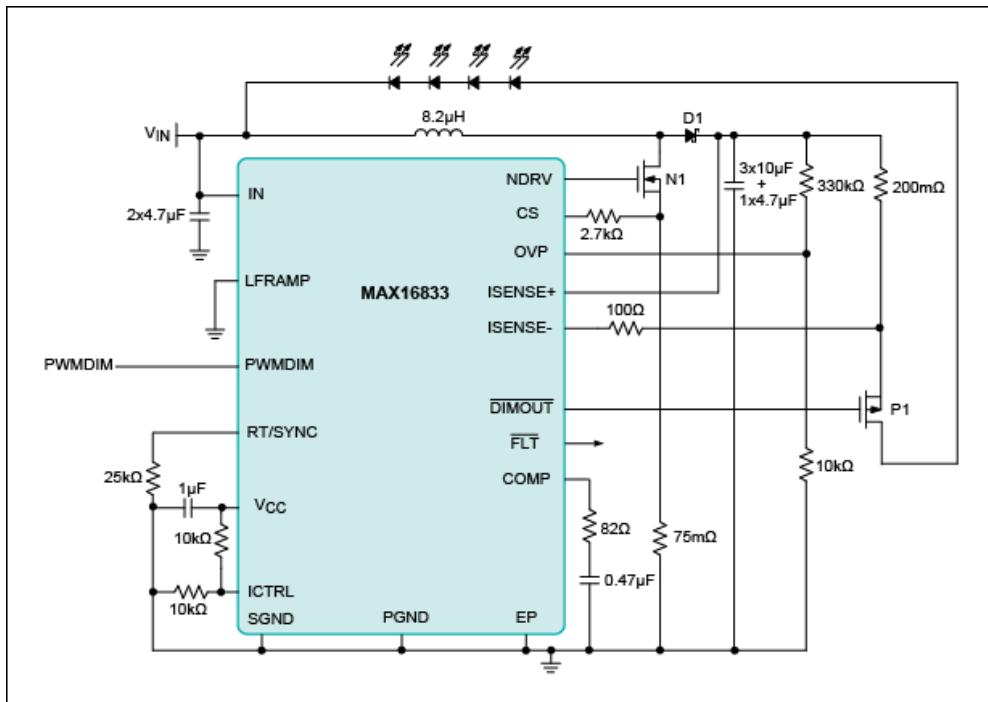application note, significant time can be saved during the debug and test phase of the project.

Figure 7. Typical application circuit based on example calculations.

For additional details, refer to the MAX16833 data sheet and the MAX16833EVKIT data sheet.

For information on the design process focused on the boost converter topology of the MAX16833, see application note 5571, "Step-by-Step Design Process for the MAX16833 High-Voltage High-Brightness LED Driver, Part 1."

References

1. For information on acoustic noise and capacitors for acoustic noise reduction, see www.murata.com/products/capacitor/solution/naki.html.

Related Parts		
MAX16833	High-Voltage HB LED Drivers with Integrated High-Side Current Sense	Free Samples
MAX16833B	High-Voltage HB LED Drivers with Integrated High-Side Current Sense	Free Samples
MAX16833C	High-Voltage HB LED Drivers with Integrated High-Side Current Sense	Free Samples
MAX16833D	High-Voltage HB LED Drivers with Integrated High-Side Current Sense	Free Samples
MAX16833EVKIT	Evaluation Kit for the MAX16833	

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