TS3L4892
16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LED SWITCH

SCDS251–MARCH 2008

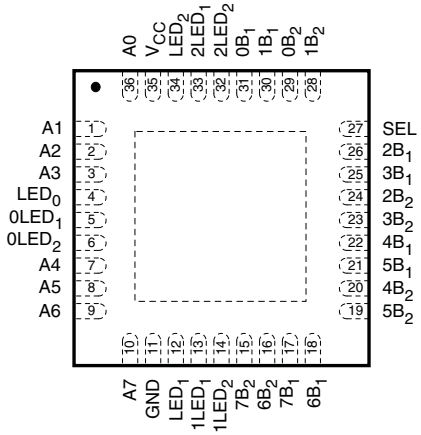
FEATURES

- **Wide Bandwidth (BW = 1100 MHz Typ)**
- **Low Crosstalk (X_{TALK} = –37 dB Typ)**
- **Low Bit-to-Bit Skew ($t_{sk(o)}$ = 100 ps Max)**
- **Low and Flat ON-State Resistance (r_{ON} = 4 Ω Typ, $r_{ON(flat)}$ = 0.5 Ω Typ)**
- **Low Input/Output Capacitance (C_{ON} = 8 pF Typ)**
- **Rail-to-Rail Switching on Data I/O Ports (0 to 5 V)**
- **V_{CC} Operating Range From 3 V to 3.6 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

APPLICATIONS

- **10/100/1000 Base-T Signal Switching**
- **Differential (LVDS, LVPECL) Signal Switching**
- **Audio/Video Switching**
- **Hub and Router Signal Switching**

RHH PACKAGE
(TOP VIEW)



PIN DESCRIPTION

NAME	DESCRIPTION
A_n	Data I/O
nB_m	Data I/O
SEL	Select input
LED_x	LED I/O port
$XLED_m$	LED I/O port

DESCRIPTION/ORDERING INFORMATION

The TS3L4892 is a 16-bit to 8-bit multiplexer/demultiplexer LAN switch with a single select (SEL) input. SEL controls the data path of the multiplexer/demultiplexer. The device provides additional I/Os for switching status indicating LED signals.

The device provides a low and flat ON-state resistance (r_{ON}) and an excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various LAN applications, such as 10/100/1000 Base-T.

This device can be used to replace mechanical relays in LAN applications. It also can be used to route signals from a 10/100 Base-T ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RHH	Tape and reel	TS3L4892RHHR	TK4892

(1) Package drawings, standard packing quantities, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE

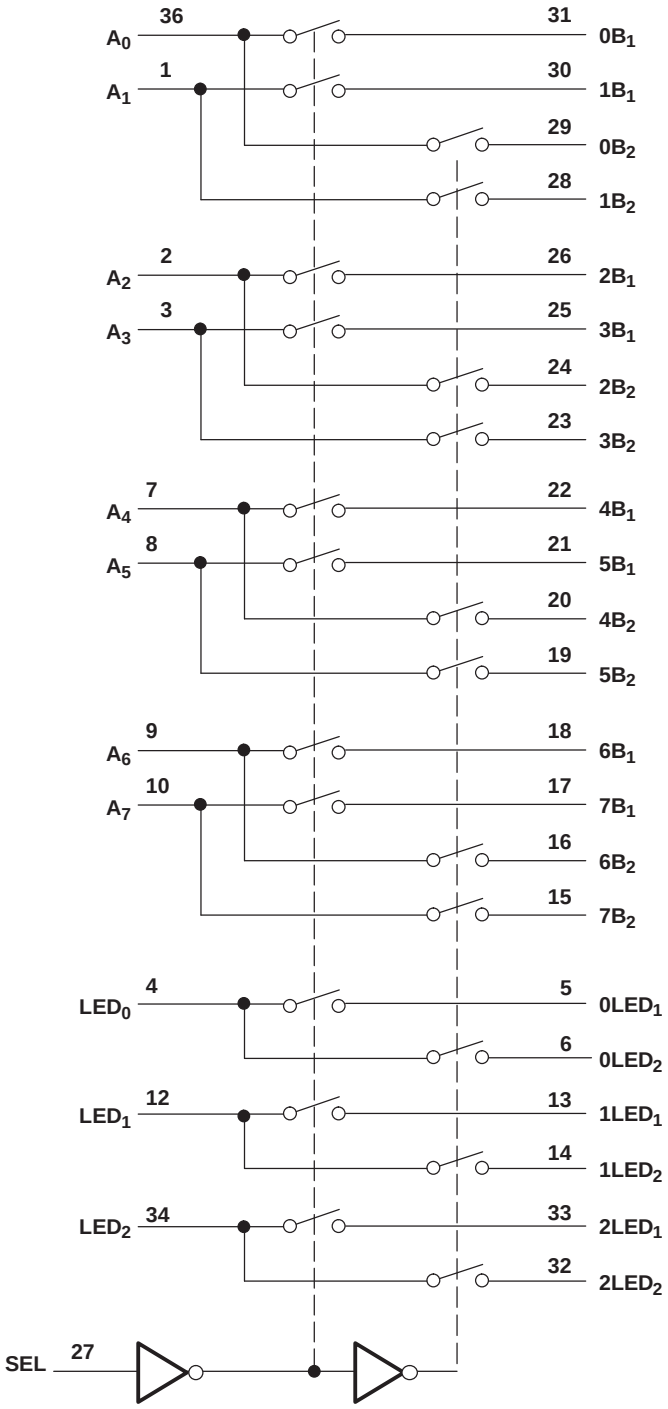
INPUT SEL	INPUT/OUTPUT A_n	FUNCTION
L	nB_1	$A_n = nB_1$, $LED_x = XLED_1$
H	nB_2	$A_n = nB_2$, $LED_x = XLED_2$

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LOGIC DIAGRAM (POSITIVE LOGIC)



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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±128	mA
	Continuous current through V_{DD} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)			31.8	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage (SEL)	2	5.5	V
V_{IL}	Low-level control input voltage (SEL)	0	0.8	V
V_I	Input voltage (SEL)	0	5.5	V
$V_{I/O}$	Input/output voltage	0	V_{CC}	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS

for 1000 Base-T Ethernet switching over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)				MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{CC} = 3.6 V,	I_{IN} = –18 mA				–0.7	–1.2	V
I_{IH}	SEL	V_{CC} = 3.6 V,	V_{IN} = V_{CC}					±1	µA
I_{IL}	SEL	V_{CC} = 3.6 V,	V_{IN} = GND					±1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF			250	500	µA
C_{IN}	SEL	f = 1 M Hz,	V_{IN} = 0				2	2.5	pF
C_{OFF}	B port	V_I = 0,	f = 1 MHz,	Outputs open,	Switch OFF		2.5	4	pF
C_{ON}		V_I = 0,	f = 1 MHz,	Outputs open,	Switch ON		8	9	pF
r_{ON}		V_{CC} = 3 V,	1.5 V ≤ V_I ≤ V_{CC},	I_O = –40 mA			4	6	Ω
$r_{ON(flat)}$(3)		V_{CC} = 3 V,	V_I = 1.5 V and V_{CC},	I_O = –40 mA			0.5		Ω
Δr_{ON}(4)		V_{CC} = 3 V,	1.5 V ≤ V_I ≤ V_{CC},	I_O = –40 mA			0.4	1	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{ON(flat)}$ is the difference of r_{ON} in a given channel at specified voltages.
(4) Δr_{ON} is the difference of r_{ON} from center (A_4, A_5) ports to any other port.

ELECTRICAL CHARACTERISTICS

for 10/100 Base-T Ethernet switching over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)				MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{CC} = 3.6 V,	I_{IN} = –18 mA				–0.7	–1.2	V
I_{IH}	SEL	V_{CC} = 3.6 V,	V_{IN} = V_{CC}					±1	µA
I_{IL}	SEL	V_{CC} = 3.6 V,	V_{IN} = GND					±1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF			250	500	µA
C_{IN}	SEL	f = 1 MHz,	V_{IN} = 0				2	2.5	pF
C_{OFF}	B port	V_I = 0,	f = 1 MHz,	Outputs open,	Switch OFF		2.5	4	pF
C_{ON}		V_I = 0,	f = 1 MHz,	Outputs open,	Switch ON		8		pF
r_{ON}		V_{CC} = 3 V,	1.25 V ≤ V_I ≤ V_{CC},	I_O = –10 mA to –30 mA			4	6	Ω
$r_{ON(flat)}$(3)		V_{CC} = 3 V,	V_I = 1.25 V and V_{CC},	I_O = –10 mA to –30 mA			0.5		Ω
Δr_{ON}(4)		V_{CC} = 3 V,	1.25 V ≤ V_I ≤ V_{CC},	I_O = –10 mA to –30 mA			0.4	1	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{ON(flat)}$ is the difference of r_{ON} in a given channel at specified voltages.
(4) Δr_{ON} is the difference of r_{ON} from center (A_4, A_5) ports to any other port.

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	A or B	B or A		40		ps
t_{PZH}, t_{PZL}	SEL	A or B	0.5		15	ns
t_{PHZ}, t_{PLZ}	SEL	A or B	0.9		9	ns
$t_{sk(o)}$(3)	A or B	B or A		50	100	ps
$t_{sk(p)}$(4)				50	150	ps

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port (A_4 to A_5) to any other port
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP(1)	UNIT
X_{TALK}	R_L = 100 Ω,	f = 250 MHz,	See Figure 8	–37	dB
O_{IRR}	R_L = 100 Ω,	f = 250 MHz,	See Figure 9	–37	dB
BW	R_L = 100 Ω,	See Figure 7		1100	MHz

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

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OPERATING CHARACTERISTICS

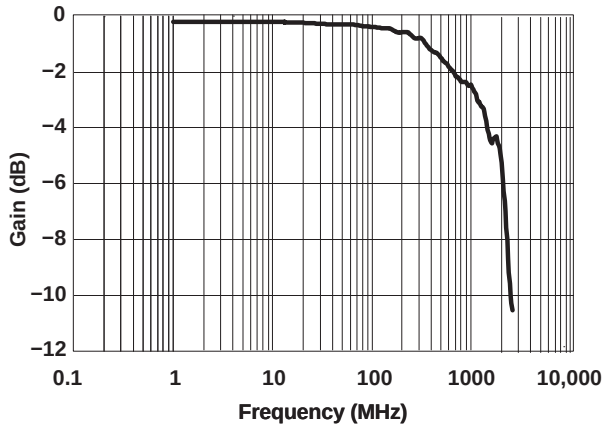


Figure 1. Gain vs Frequency

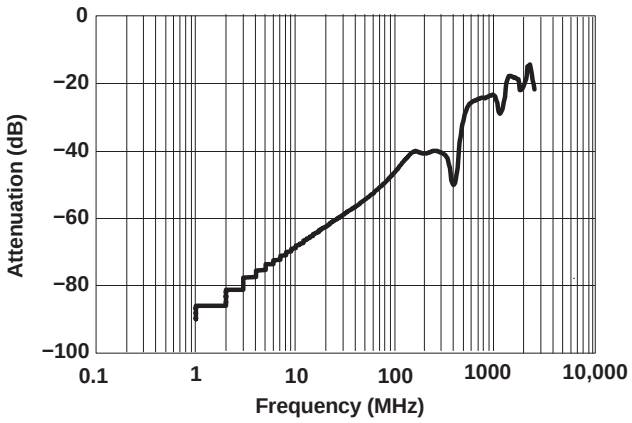


Figure 2. OFF Isolation vs Frequency

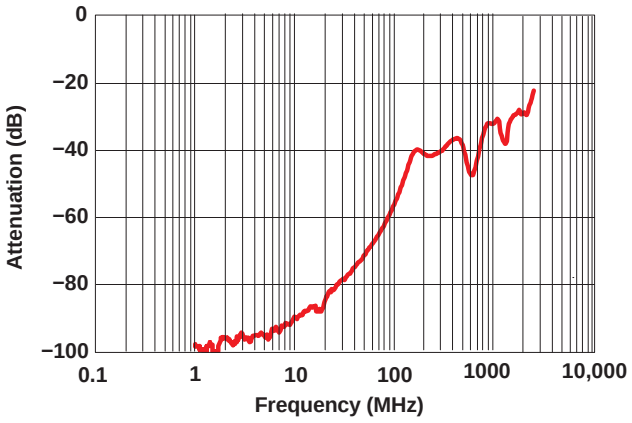


Figure 3. Crosstalk vs Frequency

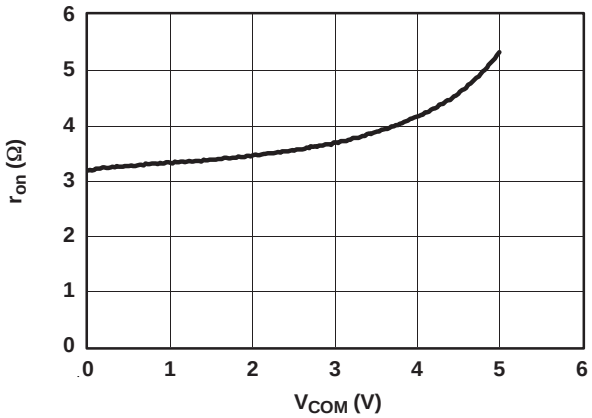
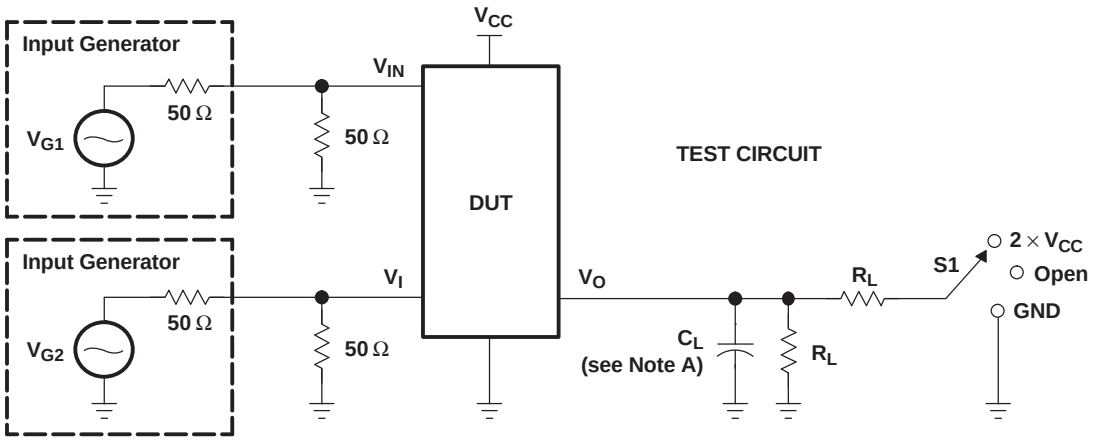


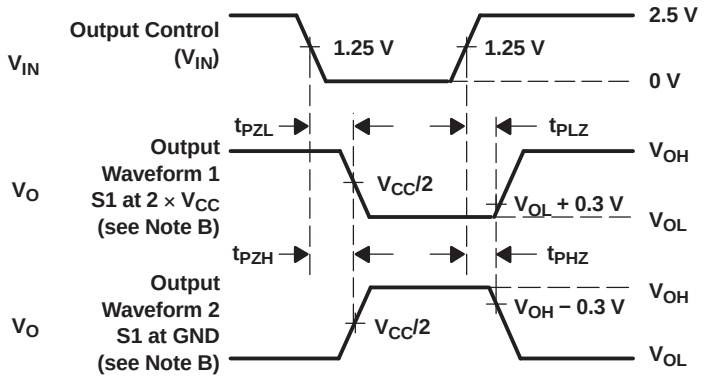
Figure 4. r_{ON} (Ω) vs V_{com} (V)

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PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 × V_{CC}	200 Ω	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V_{CC}	10 pF	0.3 V



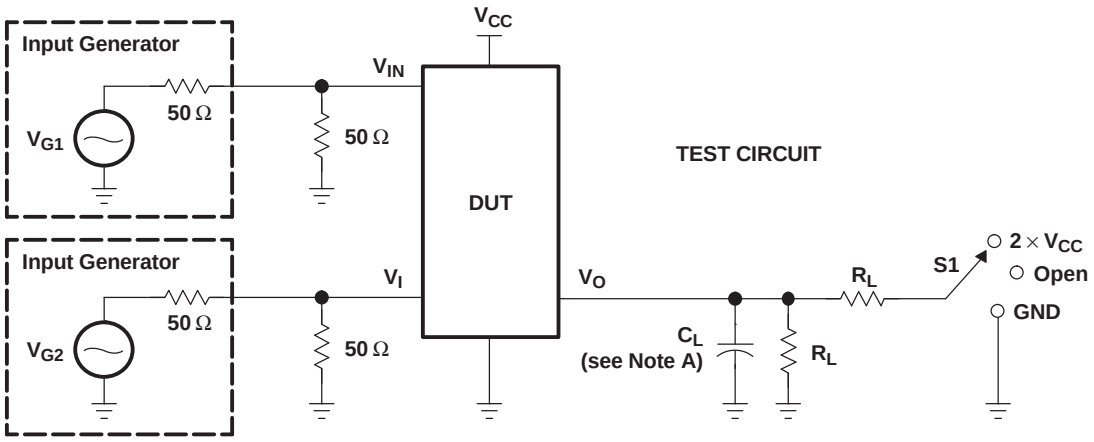
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

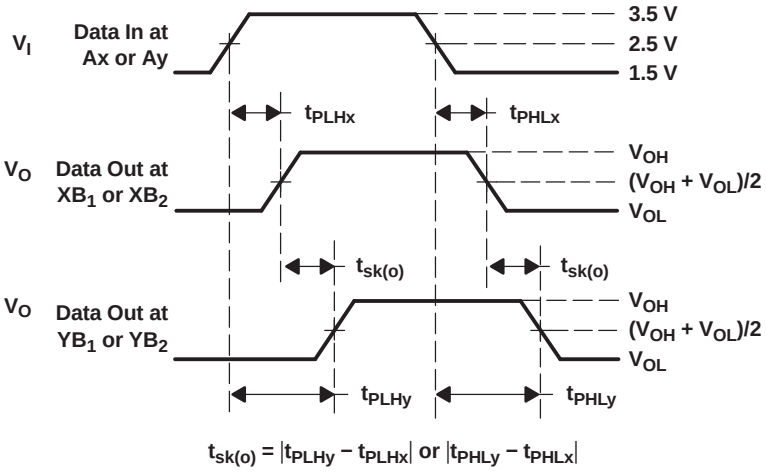
Figure 5. Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION (Skew)

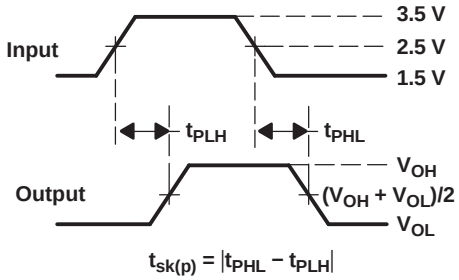


TEST	V_{CC}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{CC} or GND	10 pF
$t_{sk(p)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{CC} or GND	10 pF



$t_{sk(o)} = |t_{PLHy} - t_{PLHx}|$ or $|t_{PHLy} - t_{PHLx}|$

VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



$t_{sk(p)} = |t_{PHL} - t_{PLH}|$

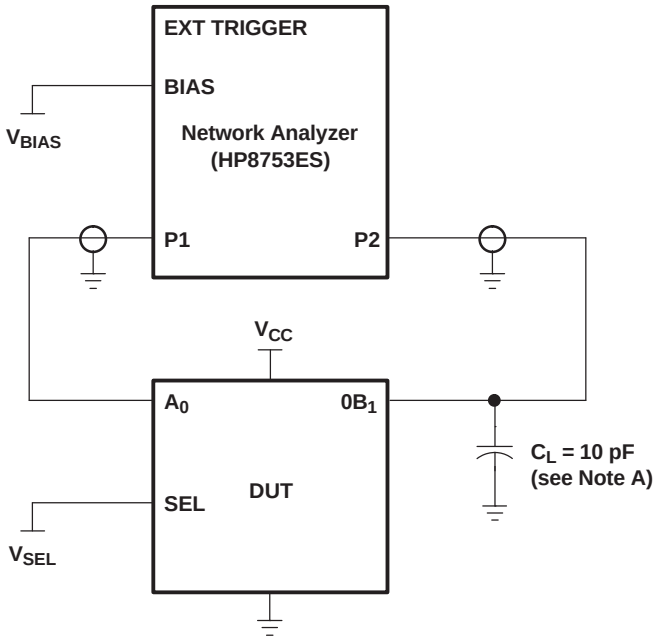
VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 6. Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

Figure 7. Test Circuit for Frequency Response (BW)

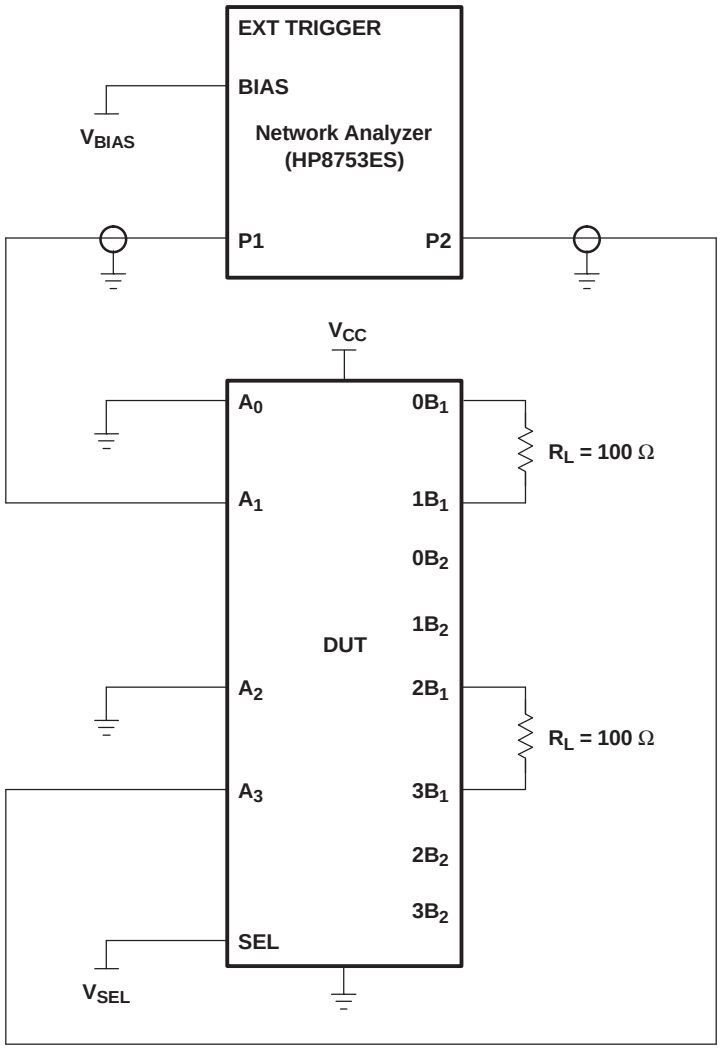
Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

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PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 8. Test Circuit for Crosstalk (X_{TALK})

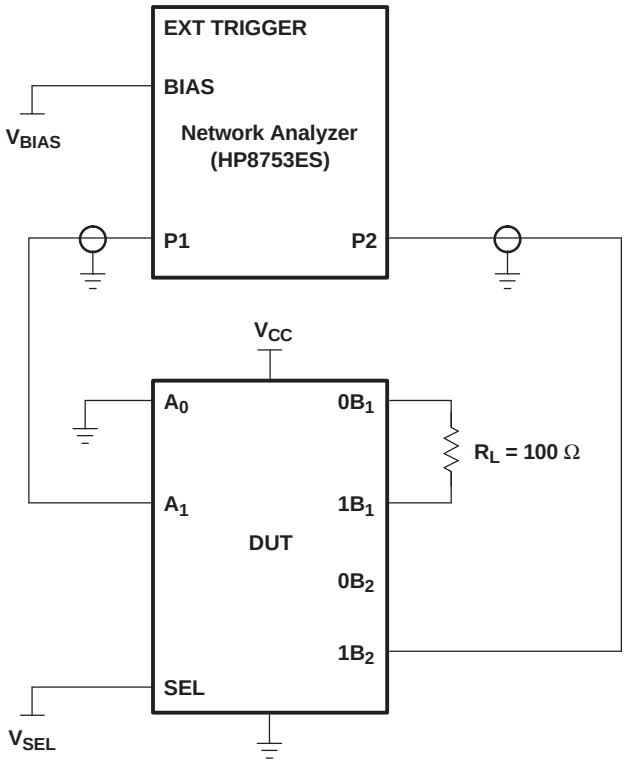
Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $1B_1$. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

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PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 9. Test Circuit for Off Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when VSEL = V_{CC} and A_0 is the input, the output is measured at $0B_2$. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3L4892RHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	TK4892	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

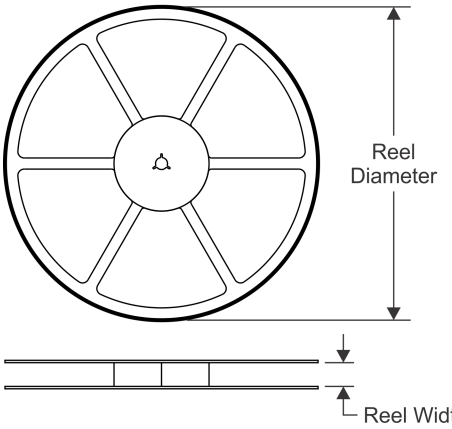
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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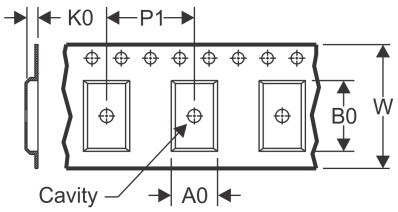
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

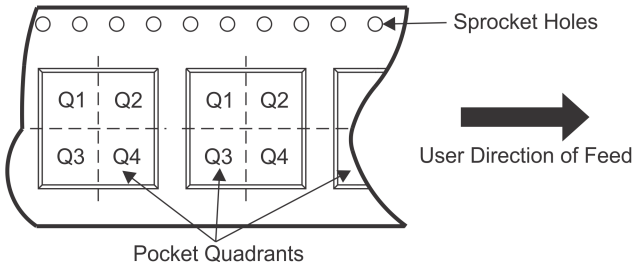


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

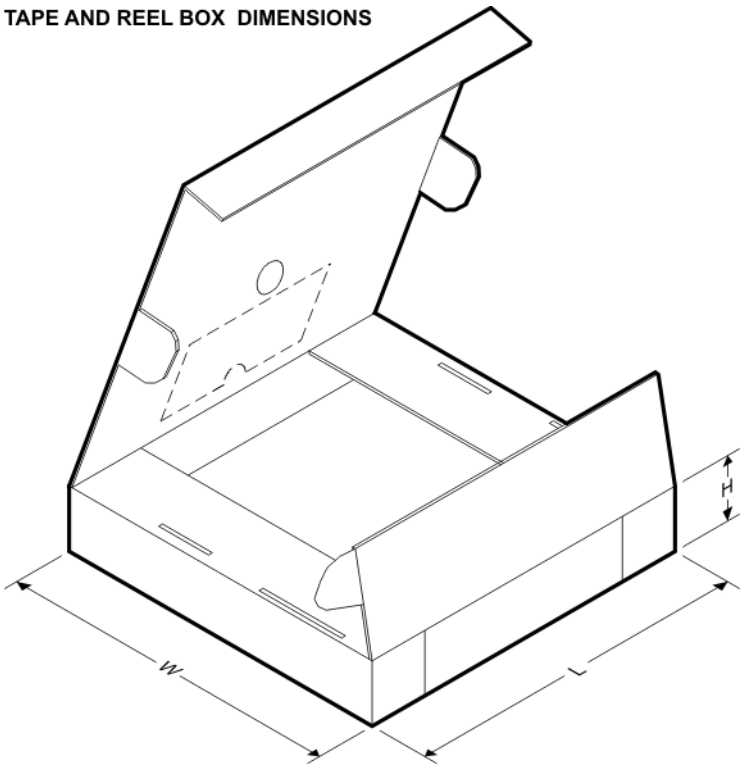
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L4892RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L4892RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0

GENERIC PACKAGE VIEW

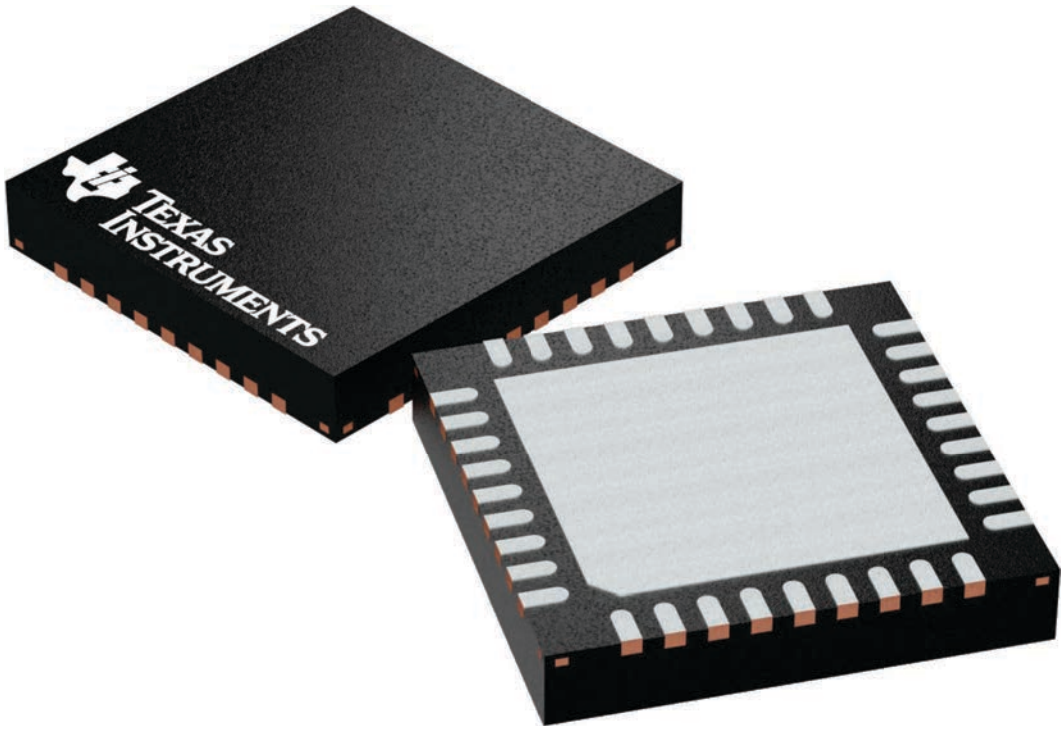
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



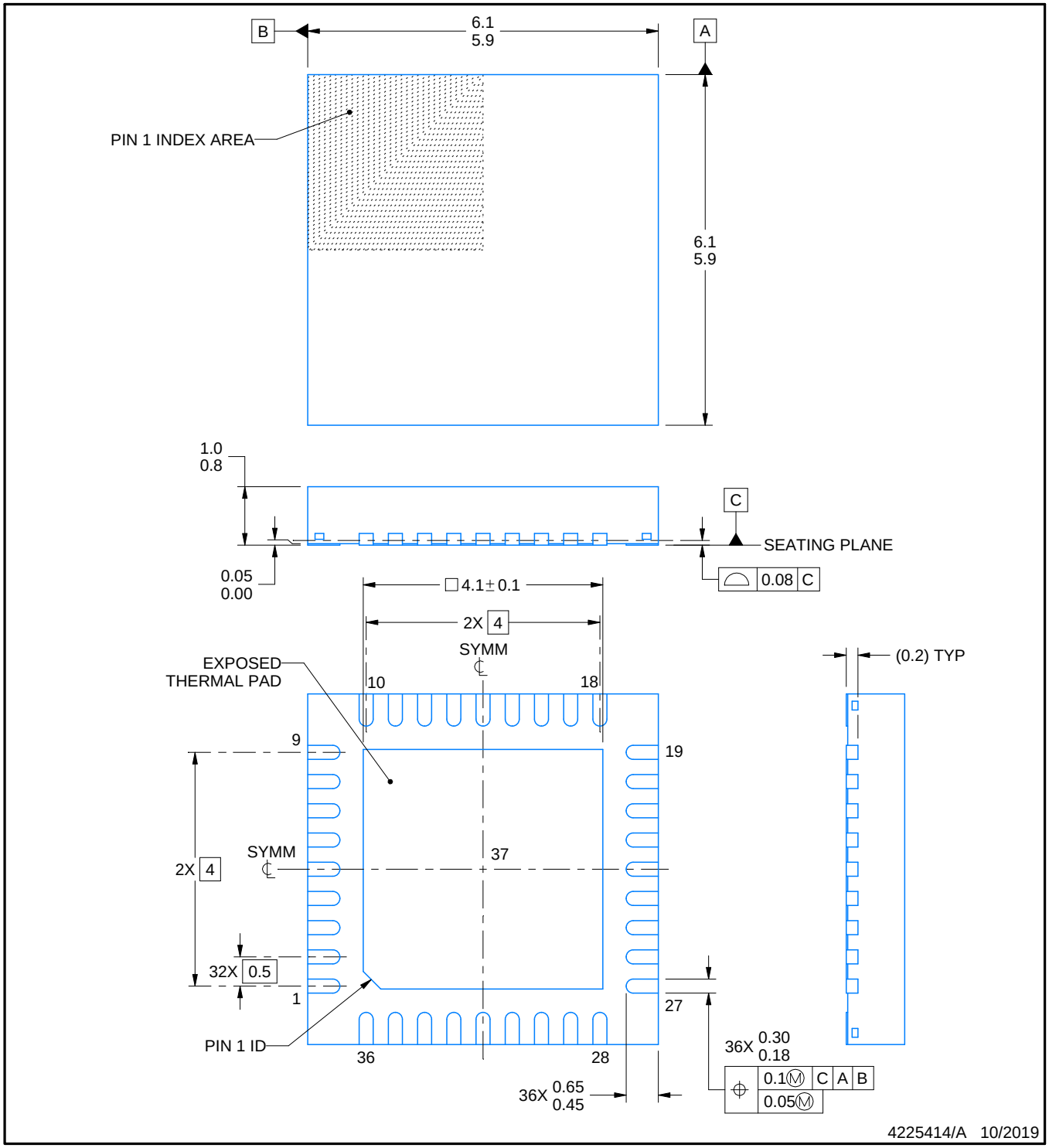
4225440/A

RHH0036B

PACKAGE OUTLINE

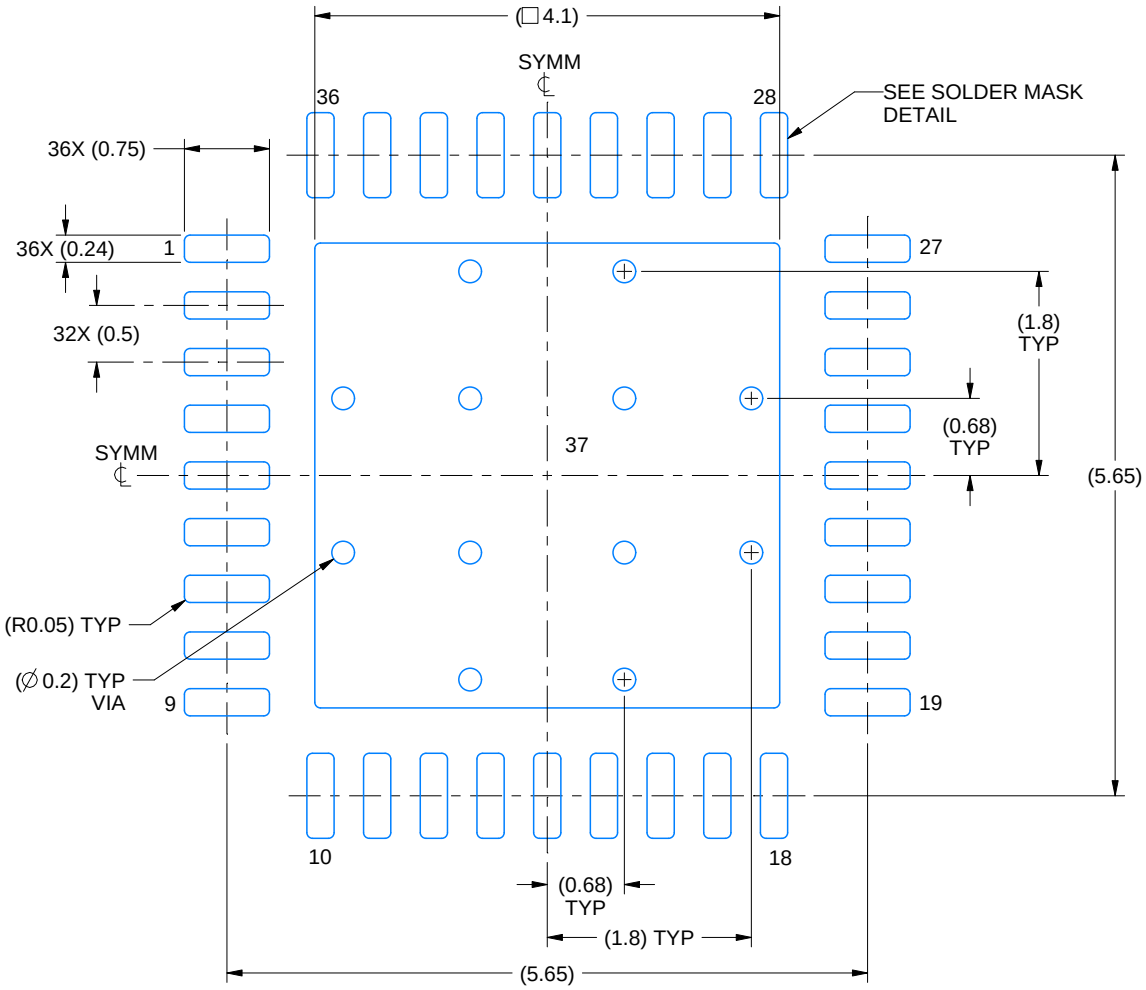
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

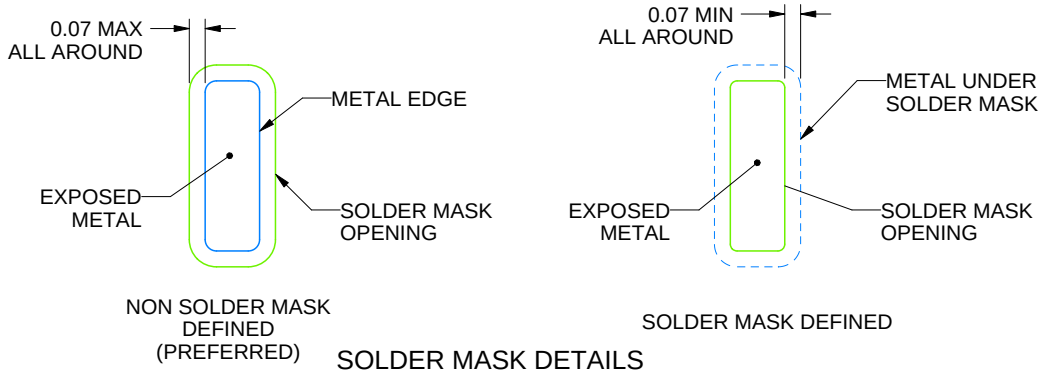


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

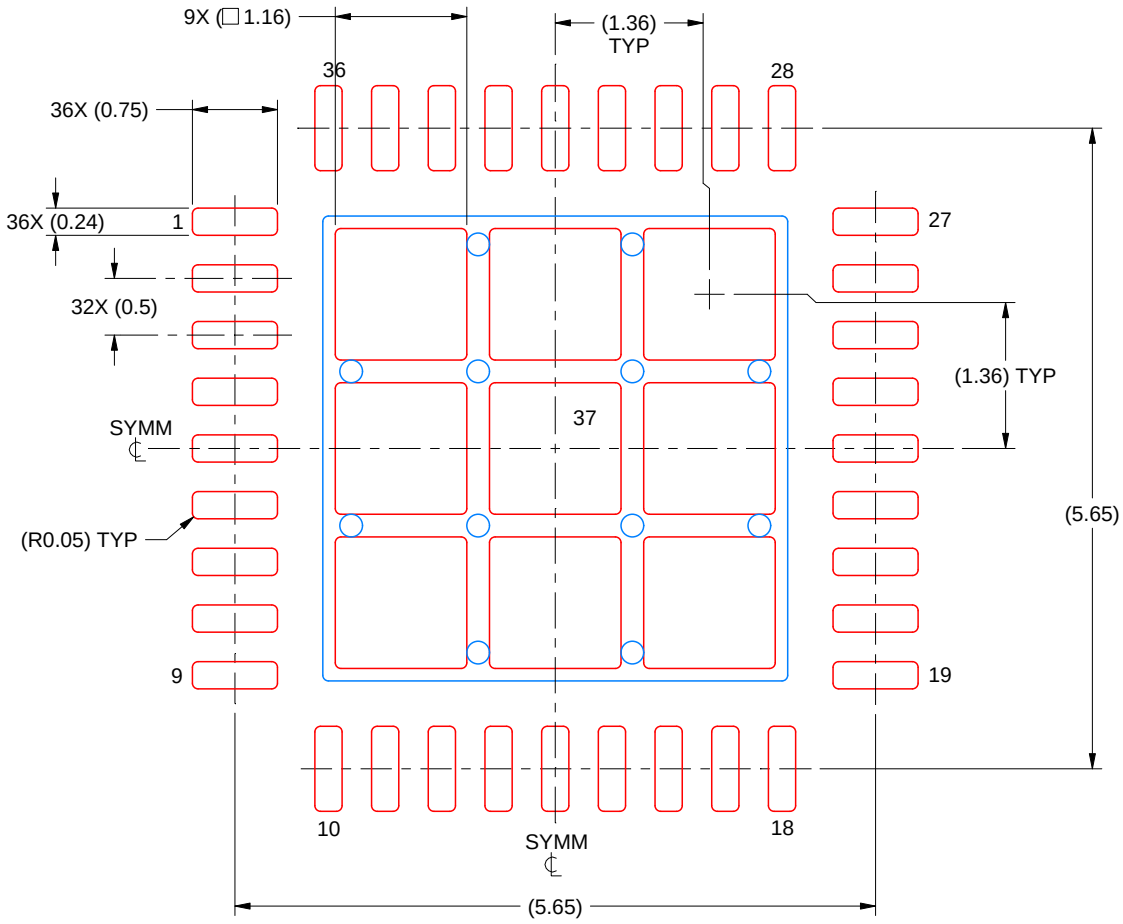


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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