



# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## General Description

The MAX9672/MAX9673/MAX9674 output 12/14/16 voltage references for gamma correction in TFT LCDs and one voltage reference for VCOM. Each gamma reference voltage has its own 10-bit DAC and buffer to ensure a stable voltage. The VCOM reference voltage has its own 10-bit DAC and an amplifier to ensure a stable voltage when critical levels and patterns are displayed. The MAX9672/MAX9673/MAX9674 feature integrated multiple-time programmable (MTP) memory to store gamma and VCOM values on the chip, eliminating the need for external EEPROM. The MAX9672/MAX9673/MAX9674 support up to 300 write operations to the on-chip nonvolatile memory.

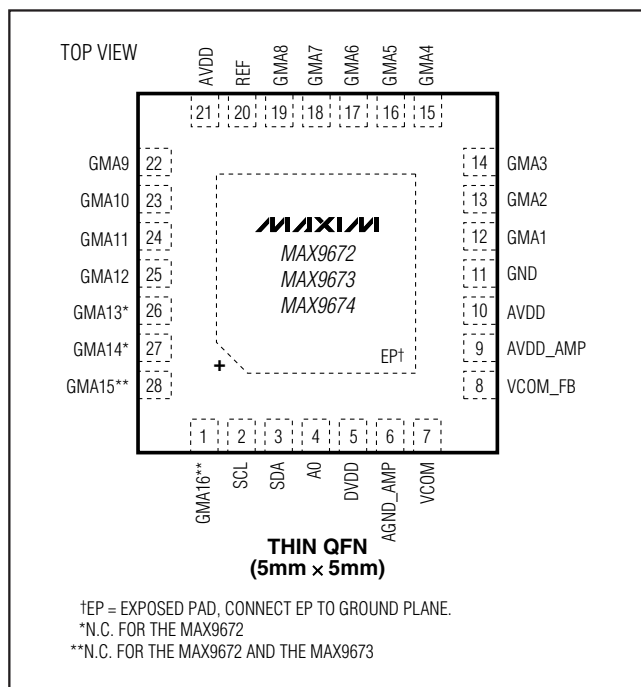
The gamma outputs can drive 200mA peak transient current and settle within 1 $\mu$ s. The VCOM output can provide 600mA peak transient current and also settles within 1 $\mu$ s. The analog supply voltage range extends from 9V to 20V, and the digital supply voltage range extends from 2.7V to 3.6V.

Gamma values and the VCOM value are programmed into registers through the I<sup>2</sup>C interface.

## Applications

TFT LCDs

## Pin Configuration



## Features

- ◆ DAC Reference Input
- ◆ 12/14/16-Channel Gamma Correction, 10-Bit Resolution
- ◆ VCOM Driver
- ◆ Integrated MTP Memory
- ◆ Programmable VCOM Limits
- ◆ 200mA Peak Current on Gamma Channels
- ◆ 600mA Peak Current on VCOM Channel

## Ordering Information

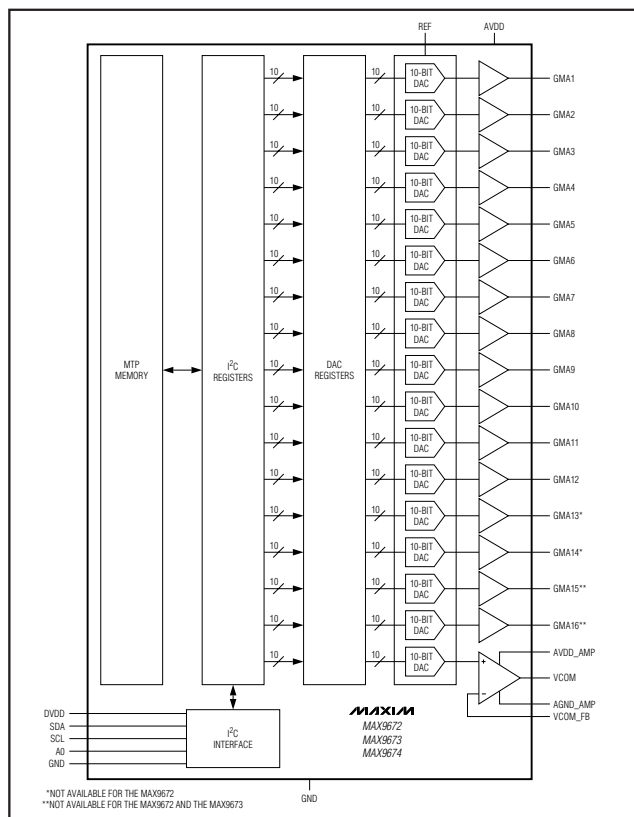
| PART        | GAMMA CHANNELS | PIN-PACKAGE |
|-------------|----------------|-------------|
| MAX9672ETI+ | 12             | 28 TQFN-EP* |
| MAX9673ETI+ | 14             | 28 TQFN-EP* |
| MAX9674ETI+ | 16             | 28 TQFN-EP* |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

**Note:** All devices are specified over the -40°C to +85°C temperature range.

## Functional Diagram



# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## ABSOLUTE MAXIMUM RATINGS

### Supply Voltages

|                      |                |
|----------------------|----------------|
| AVDD, REF to GND     | -0.3V to +22V  |
| AVDD_AMP to AGND_AMP | -0.3V to +22V  |
| AVDD to AVDD_AMP     | -0.3V to +0.3V |
| DVDD to GND          | -0.3V to +4V   |
| AGND_AMP to GND      | -0.1V to +0.1V |

### Outputs

|            |                                         |
|------------|-----------------------------------------|
| GMA1–GMA16 | -0.3V to (V <sub>AVDD</sub> + 0.3V)     |
| VCOM       | -0.3V to (V <sub>AVDD_AMP</sub> + 0.3V) |

### Inputs

|          |                                         |
|----------|-----------------------------------------|
| SDA, SCL | -0.3V to +6V                            |
| VCOM_FB  | -0.3V to (V <sub>AVDD_AMP</sub> + 0.3V) |

|                                                       |                 |
|-------------------------------------------------------|-----------------|
| SDA, SCL                                              | ±20mA           |
| GMA1–GMA16                                            | ±200mA          |
| VCOM                                                  | ±600mA          |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C) |                 |
| 28-Pin TQFN-EP (derate 28.6mW/°C above +70°C)         | 2285.7mW        |
| Operating Temperature Range                           | -40°C to +85°C  |
| Junction Temperature                                  | +150°C          |
| Storage Temperature Range                             | -65°C to +150°C |
| Lead Temperature (soldering, 10s)                     | +300°C          |
| Soldering Temperature (reflow)                        | +260°C          |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>AVDD</sub> = 18V, V<sub>AVDD\_AMP</sub> = V<sub>REF</sub> = 18V, V<sub>DVDD</sub> = 3.3V, V<sub>GND</sub> = V<sub>AGND\_AMP</sub> = 0, VCOM = VCOM\_FB, no load, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                       | SYMBOL                                       | CONDITIONS                                                             | MIN | TYP   | MAX  | UNITS |
|-------------------------------------------------|----------------------------------------------|------------------------------------------------------------------------|-----|-------|------|-------|
| <b>SUPPLIES</b>                                 |                                              |                                                                        |     |       |      |       |
| Analog Supply Voltage Range                     | V <sub>AVDD</sub> ,<br>V <sub>AVDD_AMP</sub> | Guaranteed by total output error                                       | 9   |       | 20   | V     |
| Analog Supply Voltage Range for Programming MTP | V <sub>AVDD_MTP</sub>                        |                                                                        | 15  |       | 20   | V     |
| Digital Supply Voltage Range                    | V <sub>DVDD</sub>                            |                                                                        | 2.7 |       | 3.6  | V     |
| Analog Quiescent Current                        | I <sub>AVDD</sub>                            |                                                                        |     | 20    | 35   | mA    |
| VCOM Quiescent Current                          | I <sub>AVDD_AMP</sub>                        |                                                                        |     | 2.7   | 5.6  | mA    |
| Digital Quiescent Current                       | I <sub>DVDD</sub>                            | During a register mode load event                                      |     | 400   |      | μA    |
|                                                 |                                              | No SCL or SDA transitions                                              |     | 260   | 600  |       |
| Thermal Shutdown                                |                                              |                                                                        |     | +160  |      | °C    |
| Thermal-Shutdown Hysteresis                     |                                              |                                                                        |     | 15    |      | °C    |
| Undervoltage Lockout Threshold                  | UVLO                                         | DVDD undervoltage lockout voltage threshold                            |     | 2.3   | 2.6  | V     |
| REF Input Resistance                            |                                              |                                                                        |     | 384   |      | kΩ    |
| <b>VCOM OUTPUT (VCOM)</b>                       |                                              |                                                                        |     |       |      |       |
| Resolution                                      | RES                                          |                                                                        | 10  |       |      | Bits  |
| Integral Nonlinearity Error                     | INL                                          |                                                                        |     | 0.125 | 1    | LSB   |
| Differential Nonlinearity Error                 | DNL                                          |                                                                        |     | 0.125 | 1    | LSB   |
| Total Output Error                              | V <sub>ERR</sub>                             | Code = 512, V <sub>AVDD_AMP</sub> = 9V and 20V, T <sub>A</sub> = +25°C | -40 |       | +40  | mV    |
| Total Output-Error Drift                        | ΔV <sub>ERR</sub>                            | Code = 512                                                             |     | 15    |      | μV/°C |
| Output-Voltage Low                              | V <sub>OUT</sub>                             | T <sub>A</sub> = +25°C, sinking 100mA                                  |     | 0.4   | 0.85 | V     |

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MAX9672/MAX9673/MAX9674

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{AVDD} = 18V$ ,  $V_{AVDD\_AMP} = V_{REF} = 18V$ ,  $V_{DVDD} = 3.3V$ ,  $V_{GND} = V_{AGND\_AMP} = 0$ ,  $V_{COM} = V_{COM\_FB}$ , no load,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                       | SYMBOL    | CONDITIONS                                                                               | MIN                   | TYP                   | MAX  | UNITS      |
|---------------------------------|-----------|------------------------------------------------------------------------------------------|-----------------------|-----------------------|------|------------|
| Output-Voltage High             | $V_{OUT}$ | $T_A = +25^\circ C$ , sourcing 100mA                                                     | $V_{AVDD\_AMP} - 1.1$ | $V_{AVDD\_AMP} - 0.6$ |      | V          |
| Power-Supply Rejection Ratio    | PSRR      | To AVDD_AMP, $f = 60kHz$ , REF shorted to $V_{AVDD\_AMP}$                                |                       | 40                    |      | dB         |
|                                 |           | $9V \leq V_{AVDD\_AMP} \leq 20V$                                                         | 60                    | 90                    |      |            |
| Output Load Regulation          | LR        | Transient -80mA to +80mA, code = 512                                                     |                       | $\pm 0.1$             |      | mV/mA      |
| Continuous Output Current       | $I_O$     | Code = 512 (Note 2)                                                                      |                       | 80                    |      | mA         |
| Short-Circuit Current           |           | $9V \leq V_{AVDD\_AMP} \leq 20V$                                                         |                       | 600                   |      | mA         |
| Slew Rate                       | SR        | Swing 4Vp-p at VCOM, 10% to 90%, $R_L = 10k\Omega$ , $C_L = 50pF$ (Note 3)               |                       | 100                   |      | V/ $\mu s$ |
| Program to Output Delay         | $t_D$     | From SCL rising edge for ACK bit after programming VCOM to 50% voltage change at output  |                       | 0.8                   |      | $\mu s$    |
| Bandwidth                       | BW        | $R_S = 10k\Omega$ , $C_L = 50pF$ (Note 3)                                                |                       | 60                    |      | MHz        |
| Noise                           | $e_N$     | RMS noise voltage (10MHz BW)                                                             |                       | 375                   |      | $\mu V$    |
| <b>DAC OUTPUTS (GMA1–GMA16)</b> |           |                                                                                          |                       |                       |      |            |
| Resolution                      | RES       | Guaranteed monotonic                                                                     | 10                    |                       |      | Bits       |
| Integral Nonlinearity Error     | INL       |                                                                                          |                       | 0.125                 | 1    | LSB        |
| Differential Nonlinearity Error | DNL       |                                                                                          |                       | 0.125                 | 1    | LSB        |
| Total Output Error              | $V_{ERR}$ | Code = 512, $V_{AVDD} = 9V$ and $20V$ , $T_A = +25^\circ C$                              | -40                   |                       | +40  | mV         |
| Output-Voltage Low              | $V_{OUT}$ | $T_A = +25^\circ C$ , sinking 10mA                                                       |                       | 0.15                  | 0.28 | V          |
| Output-Voltage High             | $V_{OUT}$ | $T_A = +25^\circ C$ , sourcing 10mA                                                      | $V_{AVDD} - 0.38$     | $V_{AVDD} - 0.25$     |      | V          |
| Power-Supply Rejection Ratio    | PSRR      | To AVDD, $f = 60kHz$ , REF shorted to AVDD                                               |                       | 40                    |      | dB         |
|                                 |           | $9V \leq V_{AVDD} \leq 20V$                                                              | 60                    | 90                    |      |            |
| Load Regulation                 | LR        | -12mA to +12mA                                                                           |                       | 0.5                   |      | mV/mA      |
| Short-Circuit Current           | $I_{SC}$  | Outputs to AVDD or GND                                                                   |                       | 200                   |      | mA         |
| Output Impedance                | $Z_O$     | Output resistance when output is disabled                                                |                       | 84                    |      | $k\Omega$  |
| Slew Rate                       | SR        | Swing 5Vp-p at input, 10% to 90% measurement on output                                   |                       | 22                    |      | V/ $\mu s$ |
| Program to Output Delay         | $t_D$     | From SCL rising edge for ACK bit after programming gamma to 50% voltage change at output |                       | 0.8                   |      | $\mu s$    |
| Noise                           | $e_N$     | RMS noise voltage at any output (10MHz BW)                                               |                       | 375                   |      | $\mu V$    |
| Channel-to-Channel Isolation    | CXTLK     | $f = 5MHz$ , all channels to all channels                                                |                       | 80                    |      | dB         |

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{AVDD} = 18V$ ,  $V_{AVDD\_AMP} = V_{REF} = 18V$ ,  $V_{DVDD} = 3.3V$ ,  $V_{GND} = V_{AGND\_AMP} = 0$ ,  $V_{COM} = V_{COM\_FB}$ , no load,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                                               | SYMBOL           | CONDITIONS                      | MIN                   | TYP   | MAX | UNITS   |
|---------------------------------------------------------|------------------|---------------------------------|-----------------------|-------|-----|---------|
| <b>LOGIC INPUTS (SDA, SCL)</b>                          |                  |                                 |                       |       |     |         |
| Input High Voltage                                      | $V_{IH}$         |                                 | $0.7 \times V_{DVDD}$ |       |     | V       |
| Input Low Voltage                                       | $V_{IL}$         |                                 | $0.3 \times V_{DVDD}$ |       |     | V       |
| Input Leakage Current                                   | $I_{IH}, I_{IL}$ | $V_{IN} = 0V$ or $V_{DVDD}$     | -1                    | +0.01 | +1  | $\mu A$ |
| Input Capacitance                                       |                  |                                 | 5                     |       |     | pF      |
| Power-Down Input Current                                | $I_{IN}$         | $V_{DVDD} = 0V$ , $V_{IN} = 2V$ | -10                   |       | +10 | $\mu A$ |
| SDA Output Low Voltage                                  | $V_{OL}$         | $I_{SINK} = 6mA$                |                       |       | 0.4 | V       |
| <b>I<sup>2</sup>C TIMING CHARACTERISTICS (Figure 1)</b> |                  |                                 |                       |       |     |         |
| Serial-Clock Frequency                                  | $f_{SCL}$        |                                 | 0                     |       | 400 | kHz     |
| Bus Free Time Between STOP and START Conditions         | $t_{BUF}$        |                                 | 1.3                   |       |     | $\mu s$ |
| Hold Time (REPEATED) START Condition                    | $t_{HD,STA}$     |                                 | 0.6                   |       |     | $\mu s$ |
| SCL Pulse-Width Low                                     | $t_{LOW}$        |                                 | 1.3                   |       |     | $\mu s$ |
| SCL Pulse-Width High                                    | $t_{HIGH}$       |                                 | 0.6                   |       |     | $\mu s$ |
| Setup Time for a REPEATED START Condition               | $t_{SU,STA}$     |                                 | 0.6                   |       |     | $\mu s$ |
| Data Hold Time                                          | $t_{HD,DAT}$     |                                 | 0                     |       | 900 | ns      |
| Data Setup Time                                         | $t_{SU,DAT}$     |                                 | 100                   |       |     | ns      |
| SDA and SCL Receiving Rise Time                         | $t_R$            | (Note 4)                        | $20 + 0.1C_B$         |       | 300 | ns      |
| SDA and SCL Receiving Fall Time                         | $t_F$            | (Note 4)                        | $20 + 0.1C_B$         |       | 300 | ns      |
| SDA Transmitting Fall Time                              | $t_{F,TX}$       | (Note 4)                        | $20 + 0.1C_B$         |       | 250 | ns      |
| Setup Time for STOP Condition                           | $t_{SU,STO}$     |                                 | 0.6                   |       |     | $\mu s$ |
| Bus Capacitance                                         | $C_B$            |                                 |                       |       | 400 | pF      |
| Pulse Width of Suppressed Spike                         | $t_{SP}$         |                                 | 0                     |       | 50  | ns      |

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ C$ . All temperature limits are guaranteed by design.

**Note 2:** Thermal pad attached to multilayered board. Exceeding this limit may cause the thermal shutdown to trip.

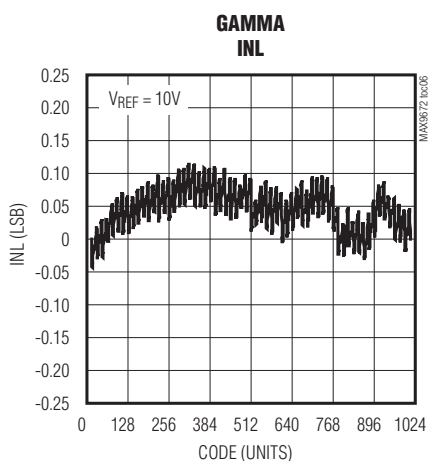
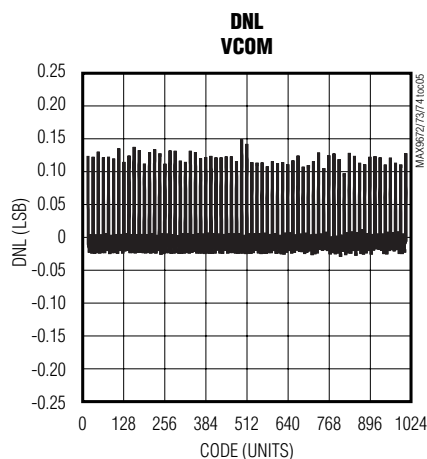
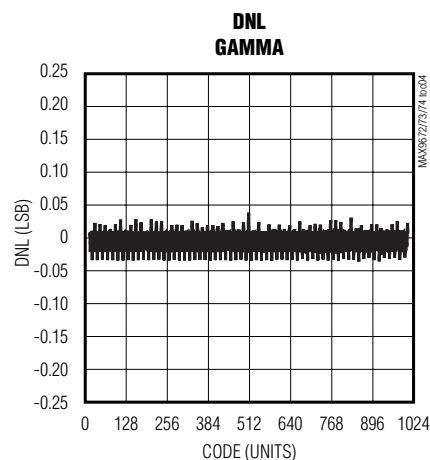
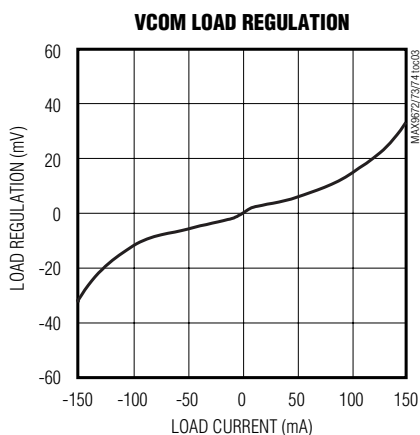
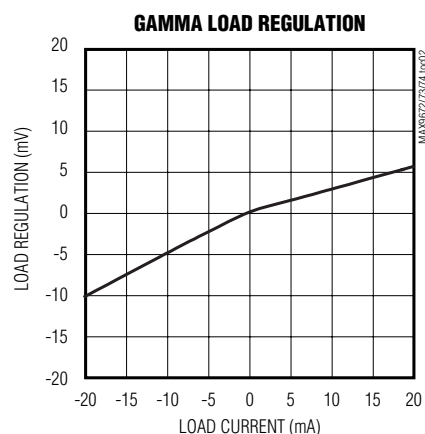
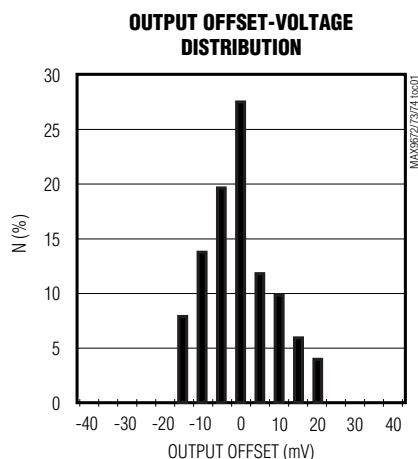
**Note 3:** Measured with the VCOM amplifier configured as an inverting unity-gain amplifier ( $R_S = R_F = 1k\Omega$ ).

**Note 4:**  $C_B$  is in pF.

# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## Typical Operating Characteristics

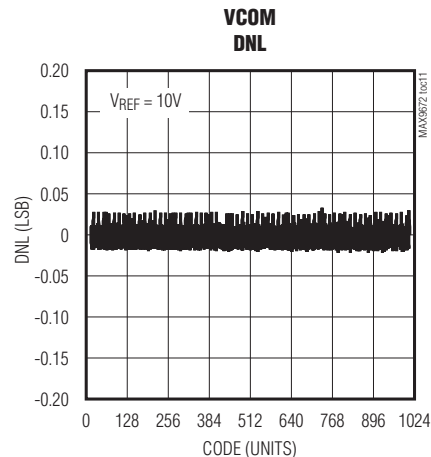
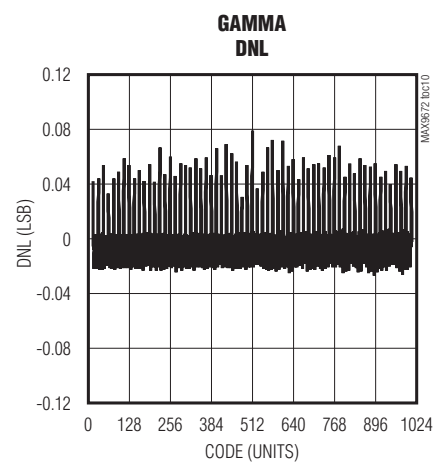
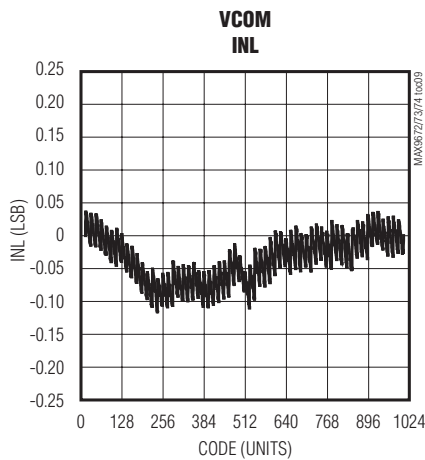
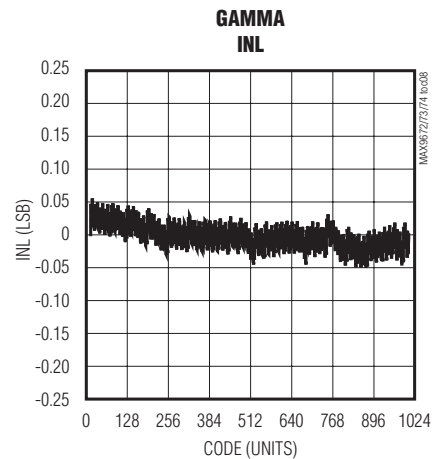
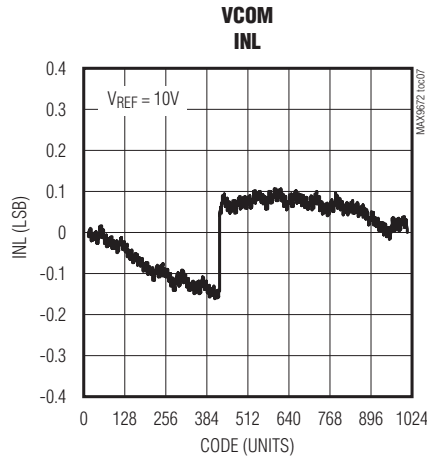
( $V_{AVDD} = V_{AVDD\_AMP} = V_{REF} = 18V$ ,  $V_{DVDD} = 3.3V$ ,  $V_{GND} = V_{AGND\_AMP} = 0$ , no load, unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)



# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## Typical Operating Characteristics (continued)

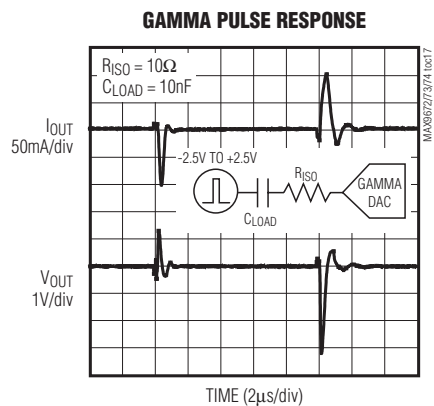
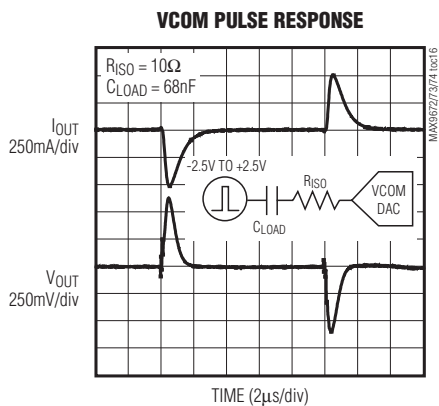
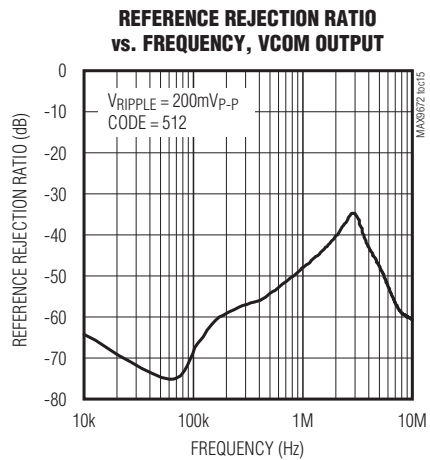
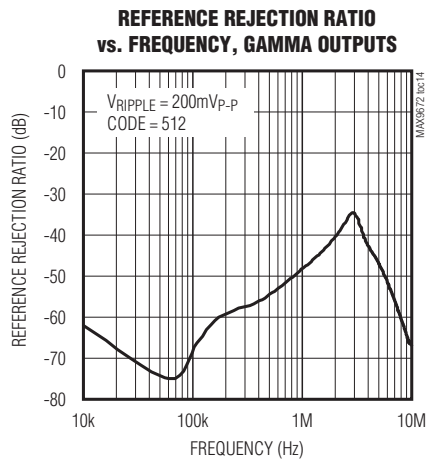
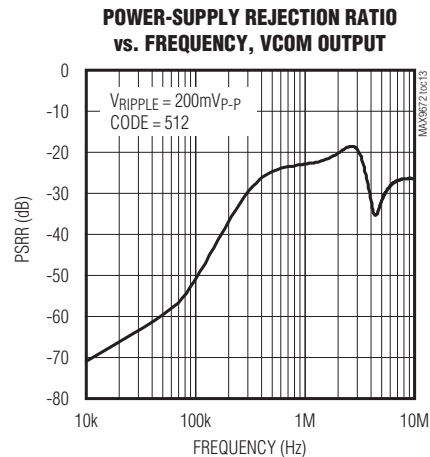
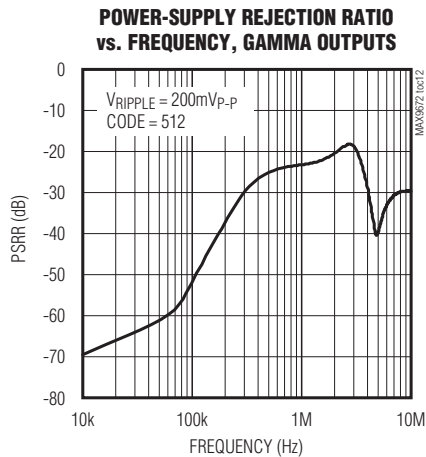
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# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## Typical Operating Characteristics (continued)

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# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## Pin Description

| PIN           |         |         | NAME     | FUNCTION                                                                                                                      |
|---------------|---------|---------|----------|-------------------------------------------------------------------------------------------------------------------------------|
| MAX9672       | MAX9673 | MAX9674 |          |                                                                                                                               |
| 1, 26, 27, 28 | 1, 28   | —       | N.C.     | No Connection. Not internally connected.                                                                                      |
| —             | —       | 1       | GMA16    | Gamma DAC Analog Output 16                                                                                                    |
| 2             | 2       | 2       | SCL      | I <sup>2</sup> C-Compatible Serial-Clock Input                                                                                |
| 3             | 3       | 3       | SDA      | I <sup>2</sup> C-Compatible Serial-Data Input/Output                                                                          |
| 4             | 4       | 4       | A0       | I <sup>2</sup> C-Compatible Device Address Bit 0                                                                              |
| 5             | 5       | 5       | DVDD     | Digital Power Supply. Bypass DVDD with a 0.1μF capacitor to GND.                                                              |
| 6             | 6       | 6       | AGND_AMP | Ground for VCOM Amplifier                                                                                                     |
| 7             | 7       | 7       | VCOM     | VCOM Output                                                                                                                   |
| 8             | 8       | 8       | VCOM_FB  | Feedback for VCOM Amplifier                                                                                                   |
| 9             | 9       | 9       | AVDD_AMP | Power Supply for VCOM Amplifier. Bypass AVDD_AMP with a 0.1μF capacitor to AGND_AMP.                                          |
| 10, 21        | 10, 21  | 10, 21  | AVDD     | Analog Power Supply. Bypass AVDD with a 0.1μF capacitor to GND.                                                               |
| 11            | 11      | 11      | GND      | Analog Ground                                                                                                                 |
| 12            | 12      | 12      | GMA1     | Gamma DAC Analog Output 1                                                                                                     |
| 13            | 13      | 13      | GMA2     | Gamma DAC Analog Output 2                                                                                                     |
| 14            | 14      | 14      | GMA3     | Gamma DAC Analog Output 3                                                                                                     |
| 15            | 15      | 15      | GMA4     | Gamma DAC Analog Output 4                                                                                                     |
| 16            | 16      | 16      | GMA5     | Gamma DAC Analog Output 5                                                                                                     |
| 17            | 17      | 17      | GMA6     | Gamma DAC Analog Output 6                                                                                                     |
| 18            | 18      | 18      | GMA7     | Gamma DAC Analog Output 7                                                                                                     |
| 19            | 19      | 19      | GMA8     | Gamma DAC Analog Output 8                                                                                                     |
| 20            | 20      | 20      | REF      | DAC Reference Input                                                                                                           |
| 22            | 22      | 22      | GMA9     | Gamma DAC Analog Output 9                                                                                                     |
| 23            | 23      | 23      | GMA10    | Gamma DAC Analog Output 10                                                                                                    |
| 24            | 24      | 24      | GMA11    | Gamma DAC Analog Output 11                                                                                                    |
| 25            | 25      | 25      | GMA12    | Gamma DAC Analog Output 12                                                                                                    |
| —             | 26      | 26      | GMA13    | Gamma DAC Analog Output 13                                                                                                    |
| —             | 27      | 27      | GMA14    | Gamma DAC Analog Output 14                                                                                                    |
| —             | —       | 28      | GMA15    | Gamma DAC Analog Output 15                                                                                                    |
| —             | —       | —       | EP       | Exposed Pad. EP is internally connected to the analog ground and digital ground. EP must be connected to the system's ground. |

## Detailed Description

The MAX9672/MAX9673/MAX9674 feature 13/15/17 total programmable reference voltage channels. Each channel has a 10-bit DAC to create the reference voltage. One channel has an amplifier that follows the DAC while all other channels have a buffer after the DAC. The MAX9672/MAX9673/MAX9674 feature integrated

MTP memory to store gamma and VCOM values on the chip, eliminating the need for external EEPROM. The MAX9672/MAX9673/MAX9674 support up to 300 write operations to the on-chip nonvolatile memory.

The MAX9672/MAX9673/MAX9674 can provide the gamma, VCOM, and possibly level-shifter reference voltages for an LCD panel that can potentially replace a discrete digital variable resistor (DVR), VCOM amplifier,



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gamma buffers, high-voltage linear regulator, and resistor strings. The high-voltage linear regulator can be eliminated because the DAC contains a lowpass filter that reduces horizontal line frequency noise by 50dB. Power sequencing is well controlled since a single chip generates all the various reference voltages needed for the LCD panel.

Each part has an I<sup>2</sup>C interface for programming both the MTP memory and the I<sup>2</sup>C registers.

With the MTP memory and the I<sup>2</sup>C interface, the MAX9672/MAX9673/MAX9674 enable automatic gamma and automatic flicker calibration on a panel-by-panel basis on the production line. Contact your Maxim representative for more details.

## 10-Bit DACs

The voltage at REF sets the full-scale output of the DACs. Determine the output voltage using the following equation:

$$V_{OUT} = (V_{REF} \times \text{CODE})/2^N$$

where CODE is the numeric value of the DAC's binary input code and N is the bits of resolution. For the MAX9672/MAX9673/MAX9674, N = 10 and CODE ranges from 0 to 1023.

The DAC can never output REF because the maximum value of CODE is always 1 least significant bit (LSB) less than the reference. For example, if V<sub>REF</sub> = 16V and CODE = 1023, then the output voltage is:

$$\begin{aligned} V_{OUT} &= (16V \times 1023)/2^{10} \\ &= 15.98438V \end{aligned}$$

## Gamma Buffers

The gamma buffers are guaranteed to source or sink 10mA of DC current within 200mV of the supplies.

The source drivers can kick back a great deal of current to the buffer outputs during a horizontal line change or a polarity switch. The DAC output buffers can source/sink 200mA of peak current to reduce the recovery time of the output voltages when critical levels and patterns are displayed.

## VCOM Amplifier

The operational amplifier attached to the VCOM DAC holds the VCOM voltage stable while providing the ability to source and sink 600mA into the backplane of a TFT LCD panel. The operational amplifier can directly drive the capacitive load of the TFT LCD backplane without the need for a series resistor in most cases. The VCOM amplifier has current limiting on its output to protect its bond wires.

If the application requires more than 600mA, buffer the output of the VCOM amplifier with a MAX9650, a VCOM power amplifier. The MAX9650 can source or sink 1A of current.

## Thermal Shutdown

The MAX9672/MAX9673/MAX9674 feature thermal-shutdown protection with temperature hysteresis. When the die temperature reaches +165°C, all of the gamma outputs are disabled. When the die cools down by 15°C, the outputs are enabled again.

## I<sup>2</sup>C Serial Interface

The MAX9672/MAX9673/MAX9674 feature an I<sup>2</sup>C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9672/MAX9673/MAX9674 and the master at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the MAX9672/MAX9673/MAX9674 by transmitting the

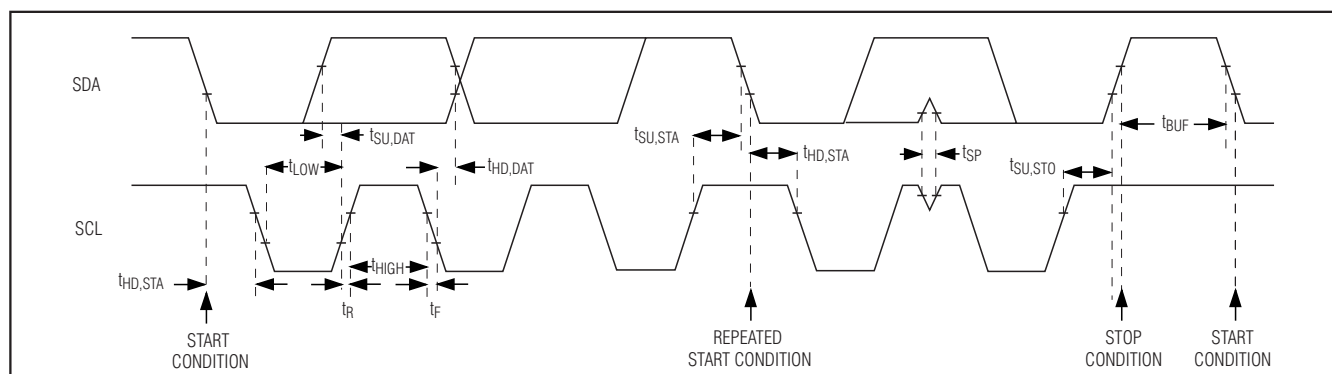


Figure 1. I<sup>2</sup>C Serial-Interface Timing Diagram

SMBus is a trademark of Intel Corp.

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proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each byte is serially transmitted to the MAX9672/MAX9673/MAX9674 as 8 bits and is followed by an acknowledge clock pulse. A master reading data from the MAX9672/MAX9673/MAX9674 transmit the proper slave address followed by a series of nine SCL pulses. The MAX9672/MAX9673/MAX9674 transmit data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9672/MAX9673/MAX9674 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

## Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I<sup>2</sup>C bus is not busy.

## START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START condition from the master signals the beginning of a transmission to the MAX9672/MAX9673/MAX9674. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

## Early STOP Conditions

The MAX9672/MAX9673/MAX9674 use a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Table 1. Slave Address

| A0   | READ ADDRESS | WRITE ADDRESS |
|------|--------------|---------------|
| GND  | E9h          | E8h           |
| DVDD | EBh          | EAh           |

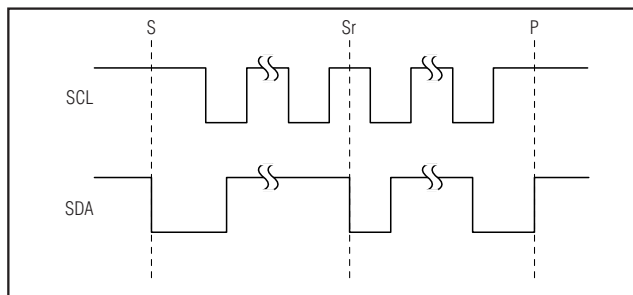


Figure 2. START, STOP, and REPEATED START Conditions

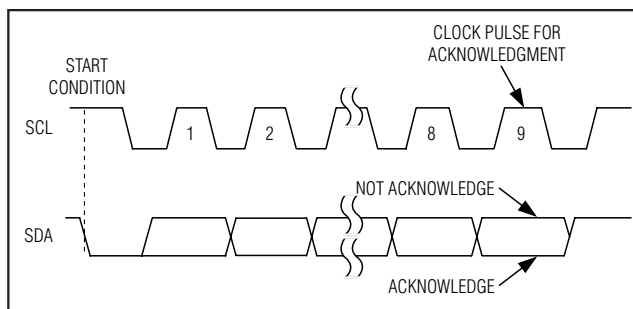


Figure 3. Acknowledge

## Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/W) bit. Set the R/W bit to 1 to configure the MAX9672/MAX9673/MAX9674 to read mode. Set the R/W bit to 0 to configure the MAX9672/MAX9673/MAX9674 to write mode. The address is the first byte of information sent to the MAX9672/MAX9673/MAX9674 after the START condition. The MAX9672/MAX9673/MAX9674 slave address is configured with A0. Table 1 shows the possible addresses for the MAX9672/MAX9673/MAX9674.

## Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9672/MAX9673/MAX9674 use to handshake receipt of each byte of data when in write mode (see Figure 3). The MAX9672/MAX9673/MAX9674 pull down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if

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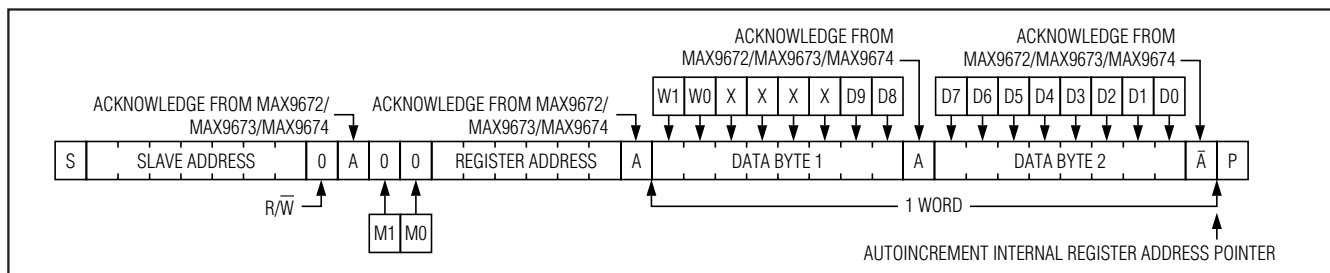


Figure 4. Writing a Word of Data to the MAX9672/MAX9673/MAX9674

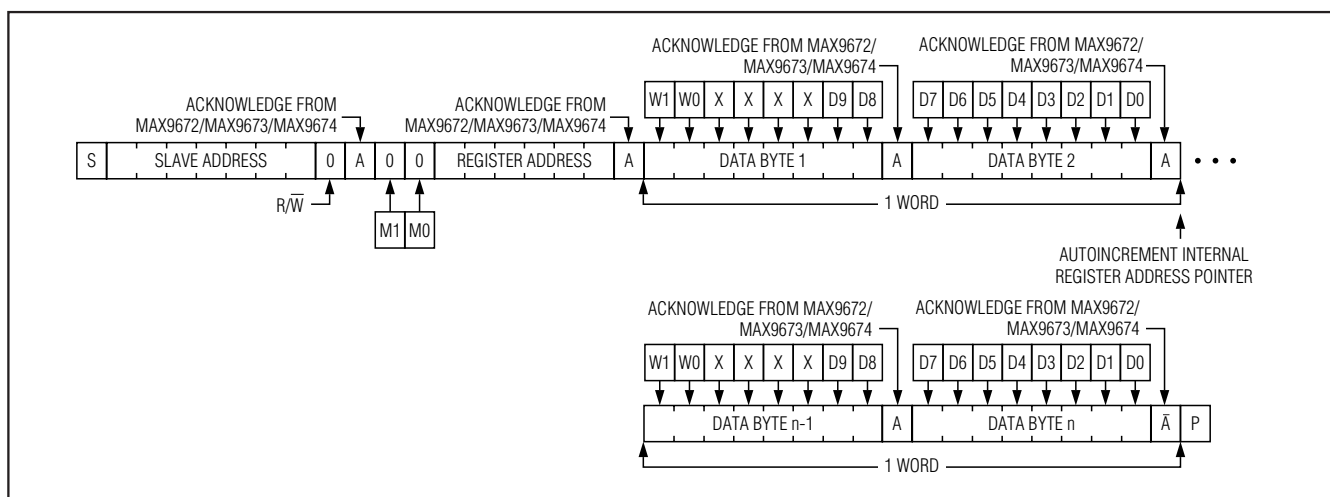


Figure 5. Writing n Bytes of Data to the MAX9672/MAX9673/MAX9674

a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the MAX9672/MAX9673/MAX9674 are in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9672/MAX9673/MAX9674, followed by a STOP condition.

## Write Data Format

A write to the MAX9672/MAX9673/MAX9674 consists of transmitting a START condition, the slave address with the R/W bit set to 0, one data byte of data to configure the internal register address pointer, one word (two bytes) of data or more, and a STOP condition. Figure 4 illustrates the proper frame format for writing one word of data to the MAX9672/MAX9673/MAX9674. Figure 5 illustrates the frame format for writing n-bytes of data to the MAX9672/MAX9673/MAX9674.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the MAX9672/MAX9673/MAX9674. The MAX9672/MAX9673/MAX9674 acknowledge receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the MAX9672/MAX9673/MAX9674's internal register address pointer. The MAX9672/MAX9673/MAX9674's internal address pointer consists of the 6 LSBs of the second byte. The 2 MSBs of the second byte (M1 and M0) are set to 00b when writing to the internal registers. See the *Memory* section for more details. The pointer tells the MAX9672/MAX9673/MAX9674 where to write the next byte of data. An acknowledge pulse is sent by the MAX9672/MAX9673/MAX9674 upon receipt of the address pointer data.

The third and fourth bytes sent to the MAX9672/MAX9673/MAX9674 contain the data that is written to the chosen register and which type of register it writes to, volatile (DAC) or nonvolatile memory (MTP). See the *Registers* section for more details. An acknowledge pulse

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Table 2. Register Map

| REGISTER ADDRESS | REGISTER NAME             | REGISTER DESCRIPTION | MTP FACTORY INITIALIZATION VALUE |         |         | READ/ WRITE    |
|------------------|---------------------------|----------------------|----------------------------------|---------|---------|----------------|
|                  |                           |                      | MAX9672                          | MAX9673 | MAX9674 |                |
| 0x00             | GMA1                      | Gamma 1              | 0x3B0                            | 0x3BA   | 0x3C2   | Read and write |
| 0x01             | GMA2                      | Gamma 2              | 0x361                            | 0x376   | 0x386   | Read and write |
| 0x02             | GMA3                      | Gamma 3              | 0x312                            | 0x332   | 0x34A   | Read and write |
| 0x03             | GMA4                      | Gamma 4              | 0x2C4                            | 0x2EE   | 0x30E   | Read and write |
| 0x04             | GMA5                      | Gamma 5              | 0x275                            | 0x2AA   | 0x2D2   | Read and write |
| 0x05             | GMA6                      | Gamma 6              | 0x226                            | 0x265   | 0x295   | Read and write |
| 0x06             | GMA7                      | Gamma 7              | 0x1D8                            | 0x221   | 0x259   | Read and write |
| 0x07             | GMA8                      | Gamma 8              | 0x189                            | 0x1DD   | 0x21D   | Read and write |
| 0x08             | GMA9                      | Gamma 9              | 0x13A                            | 0x199   | 0x1E1   | Read and write |
| 0x09             | GMA10                     | Gamma 10             | 0x0EC                            | 0x155   | 0x1A5   | Read and write |
| 0x0A             | GMA11                     | Gamma 11             | 0x09D                            | 0x110   | 0x169   | Read and write |
| 0x0B             | GMA12                     | Gamma 12             | 0x04E                            | 0x0CC   | 0x12C   | Read and write |
| 0x0C             | GMA13                     | Gamma 13             | —                                | 0x088   | 0X0F0   | Read and write |
| 0x0D             | GMA14                     | Gamma 14             | —                                | 0x044   | 0x0B4   | Read and write |
| 0x0E             | GMA15                     | Gamma 15             | —                                | —       | 0x078   | Read and write |
| 0x0F             | GMA16                     | Gamma 16             | —                                | —       | 0x03C   | Read and write |
| 0x10             | Reserved                  | —                    | —                                | —       | —       | —              |
| 0x11             | Reserved                  | —                    | —                                | —       | —       | —              |
| 0x12             | VCOM                      | Common voltage       | 0x193                            | 0x193   | 0x193   | Read and write |
| 0x13             | Reserved                  | —                    | —                                | —       | —       | —              |
| 0x14             | Reserved                  | —                    | —                                | —       | —       | —              |
| 0x15             | Reserved                  | —                    | —                                | —       | —       | —              |
| 0x16             | Reserved                  | —                    | —                                | —       | —       | —              |
| 0x17             | Reserved                  | —                    | —                                | —       | —       | —              |
| 0x18             | VCOMMIN                   | Minimum VCOM value   | 0x10D                            | 0x10D   | 0x10D   | Read and write |
| 0x19             | VCOMMAX                   | Maximum VCOM value   | 0x21A                            | 0x21A   | 0x21A   | Read and write |
| 0x1D             | Reserved,<br>DO NOT WRITE | —                    | —                                | —       | —       | —              |
| 0x1E             | Reserved,<br>DO NOT WRITE | —                    | —                                | —       | —       | —              |

from the MAX9672/MAX9673/MAX9674 signals receipt of each data byte. The address pointer autoincrements to the next register address after receiving every other data byte. This autoincrement feature allows a master to write to sequential register address locations within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

If data is written into register address 0x1E, the address pointer autoincrements to 0xFF and stays at 0xFF until the master writes a new value into the register address pointer.

## Read Data Format

The master presets the address pointer by first sending the MAX9672/MAX9673/MAX9674's slave address with the R/W bit set to 0 followed by the register address

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Table 3. Register Description

| REG                         | REG ADDR | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----------------------------|----------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| GMA1                        | 0x00     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA2                        | 0x01     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA3                        | 0x02     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA4                        | 0x03     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA5                        | 0x04     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA6                        | 0x05     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA7                        | 0x06     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA8                        | 0x07     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA9                        | 0x08     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA10                       | 0x09     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA11                       | 0x0A     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA12                       | 0x0B     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA13*                      | 0x0C     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA14*                      | 0x0D     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA15**                     | 0x0E     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| GMA16**                     | 0x0F     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Reserved                    | 0x10     | —   | —   | —   | —   | —   | —   | —  | —  | —  | —  | —  | —  | —  | —  | —  | —  |
| Reserved                    | 0x11     | —   | —   | —   | —   | —   | —   | —  | —  | —  | —  | —  | —  | —  | —  | —  | —  |
| VCOM                        | 0x12     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Reserved                    | 0x13     | —   | —   | —   | —   | —   | —   | —  | —  | —  | —  | —  | —  | —  | —  | —  | —  |
| Reserved                    | 0x14     | —   | —   | —   | —   | —   | —   | —  | —  | —  | —  | —  | —  | —  | —  | —  | —  |
| Reserved                    | 0x15     | —   | —   | —   | —   | —   | —   | —  | —  | —  | —  | —  | —  | —  | —  | —  | —  |
| Reserved                    | 0x16     | —   | —   | —   | —   | —   | —   | —  | —  | —  | —  | —  | —  | —  | —  | —  | —  |
| Reserved                    | 0x17     | —   | —   | —   | —   | —   | —   | —  | —  | —  | —  | —  | —  | —  | —  | —  | —  |
| VCOMM IN                    | 0x18     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| VCOMM AX                    | 0x19     | W1  | W0  | X   | X   | X   | X   | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Reserved<br>DO NOT<br>WRITE | 0x1D     | —   | —   | —   | —   | —   | —   | —  | —  | —  | —  | —  | —  | —  | —  | —  | —  |
| Reserved<br>DO NOT<br>WRITE | 0x1E     | —   | —   | —   | —   | —   | —   | —  | —  | —  | —  | —  | —  | —  | —  | —  | —  |

\*Reserved for the MAX9672.

\*\*Reserved for the MAX9672/MAX9673.

with M1 and M0 set to 00 after a START condition. The MAX9672/MAX9673/MAX9674 acknowledge receipt of its slave address and the register address by pulling SDA low during the ninth SCL clock pulse. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The MAX9672/MAX9673/MAX9674 transmit the contents of the specified register. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after every other read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous

frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from the register address location set by the previous transaction and not 0x00. Subsequent reads autoincrement the address pointer until the next STOP condition. Attempting to read from register addresses higher than 0x1E results in repeated reads from a dummy register containing all one data. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the

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**Table 4. Write Control Bits**

| W1 | W0 | ACTION                                                                                                      |
|----|----|-------------------------------------------------------------------------------------------------------------|
| 0  | 0  | No update.                                                                                                  |
| 0  | 1  | All MTP registers get updated when the current I <sup>2</sup> C register has finished updating (end of B0). |
| 1  | 0  | All DAC registers get updated when the current I <sup>2</sup> C register has finished updating (end of B0). |
| 1  | 1  | No update.                                                                                                  |

**Table 5. Memory Write Bits**

| M1 | M0 | ACTION                                                                                     |
|----|----|--------------------------------------------------------------------------------------------|
| 0  | 0  | None.                                                                                      |
| 0  | 1  | Only the addressed I <sup>2</sup> C registers and DAC registers get set to the MTP values. |
| 1  | 0  | All I <sup>2</sup> C registers and DAC registers get set to the MTP values.                |
| 1  | 1  | None.                                                                                      |

last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figures 6 and 7 illustrate the frame format for reading data from the MAX9672/MAX9673/MAX9674.

## Registers

### Register Map

The MAX9672/MAX9673/MAX9674 have a bank of non-volatile MTP memory and two banks of volatile memory comprised of I<sup>2</sup>C registers and DAC registers. Each memory location whether in nonvolatile or volatile memory holds a 10-bit word. Two bytes must be read or written through the I<sup>2</sup>C interface for every 10-bit word.

Table 2 shows the register map. The same register address and register name exists in the MTP memory bank, I<sup>2</sup>C register bank, and the DAC register bank. The write control bits determine which memory location the data is stored into.

### Register Description

Only the 10 LSBs are written to the registers (see Table 3). During a write operation, the write control bits (the 2 MSBs) are stripped from the incoming data stream and are used to determine whether the MTP or DAC registers are updated (see Table 4).

### VCOM Programmable Range

The MAX9672/MAX9673/MAX9674 feature the programmable range for VCOM. VCOMMIN and VCOMMAX registers provide low and high limits for the VCOM DAC register. At the factory, VCOMMIN is set to 0 and VCOMMAX is set to 1023 (default values) to provide the

full rail-to-rail programmable range for VCOM. Later, users can define their own limits by programming VCOMMIN and VCOMMAX registers and MTP.

VCOM register values are limited to the defined range. This means if the VCOM register accidentally gets programmed with a value higher than VCOMMAX, it automatically gets locked to the VCOMMAX value. The I<sup>2</sup>C bus does acknowledge and receive the data sent on the bus. However, internally the part recognizes that the value is outside of the range and adjusts it accordingly. The same scenario is true if the value programming VCOM is below VCOMMIN.

## Memory

The MAX9672/MAX9673/MAX9674 include both volatile memory (I<sup>2</sup>C and DAC) and nonvolatile memory (MTP). It is possible to write to each single DAC memory location from an MTP memory location individually or to write to all at once. This is done with memory write bits (M1, M0) that are the 2 MSBs of the register address byte. Table 5 shows the memory write bits. Set both M1 and M0 to low or high when writing to or reading from the register values through the I<sup>2</sup>C bus.

### Volatile Memory

The MAX9672/MAX9673/MAX9674 feature a double-buffered register structure. The volatile (DAC) memory can be updated without updating the output voltage. Figure 8 shows how to program a single DAC. The output voltage is updated after sending the LSB (D0).



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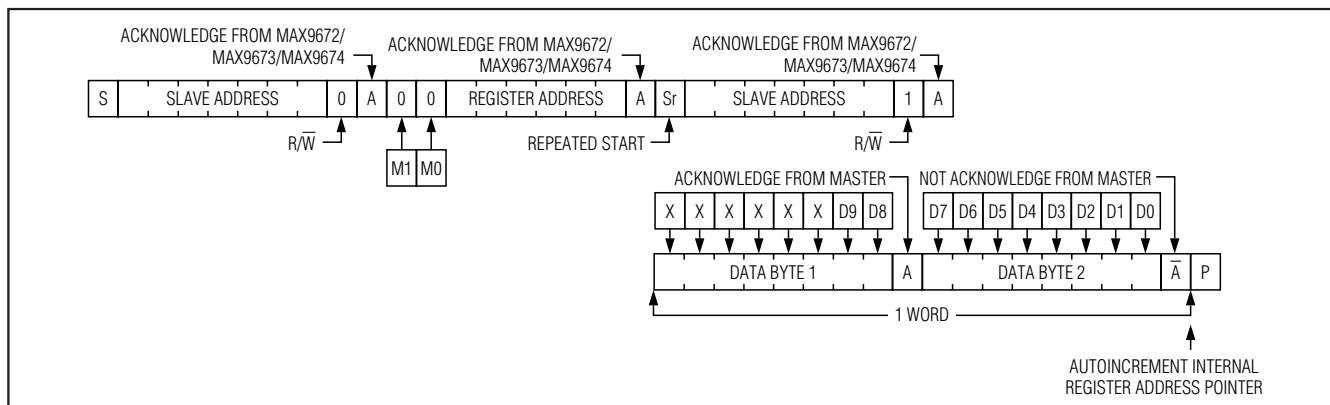


Figure 6. Reading One Indexed Word of Data from the MAX9672/MAX9673/MAX9674

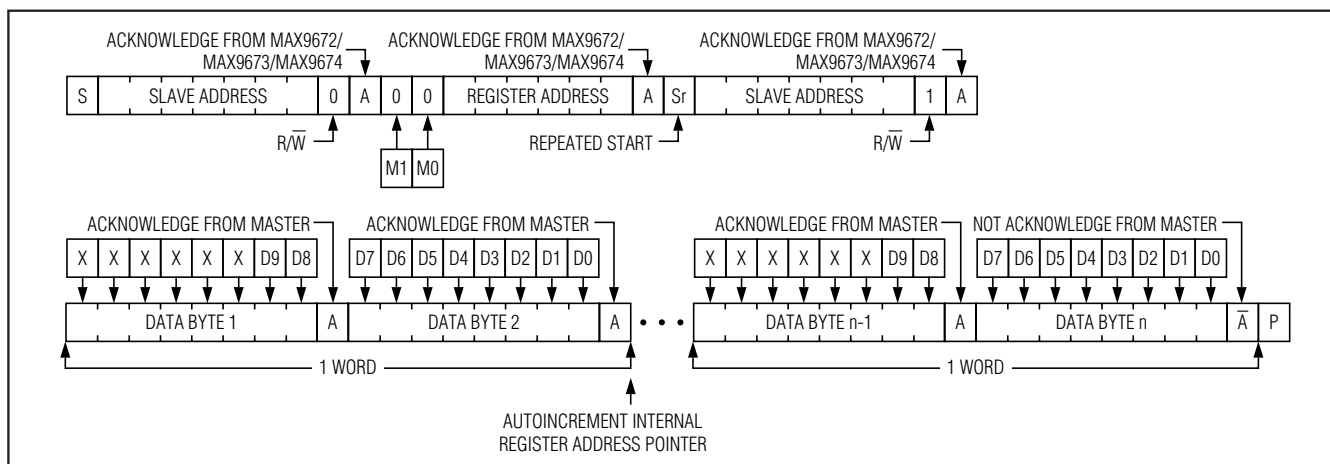


Figure 7. Reading n Bytes of Indexed Data from the MAX9672/MAX9673/MAX9674

# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

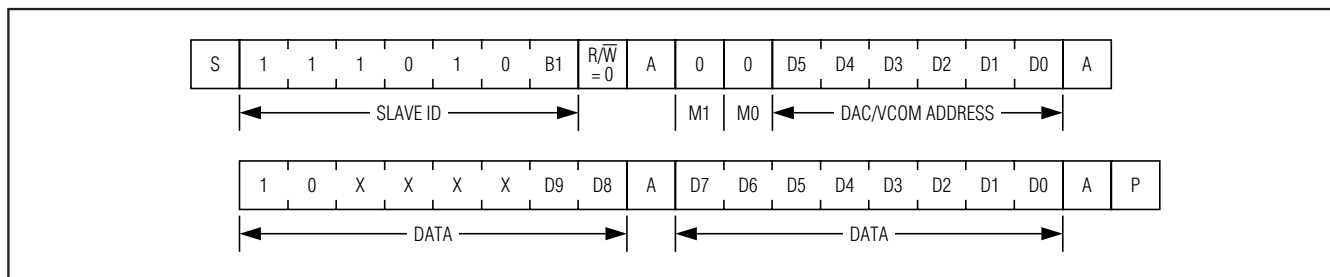


Figure 8. Single DAC Programming

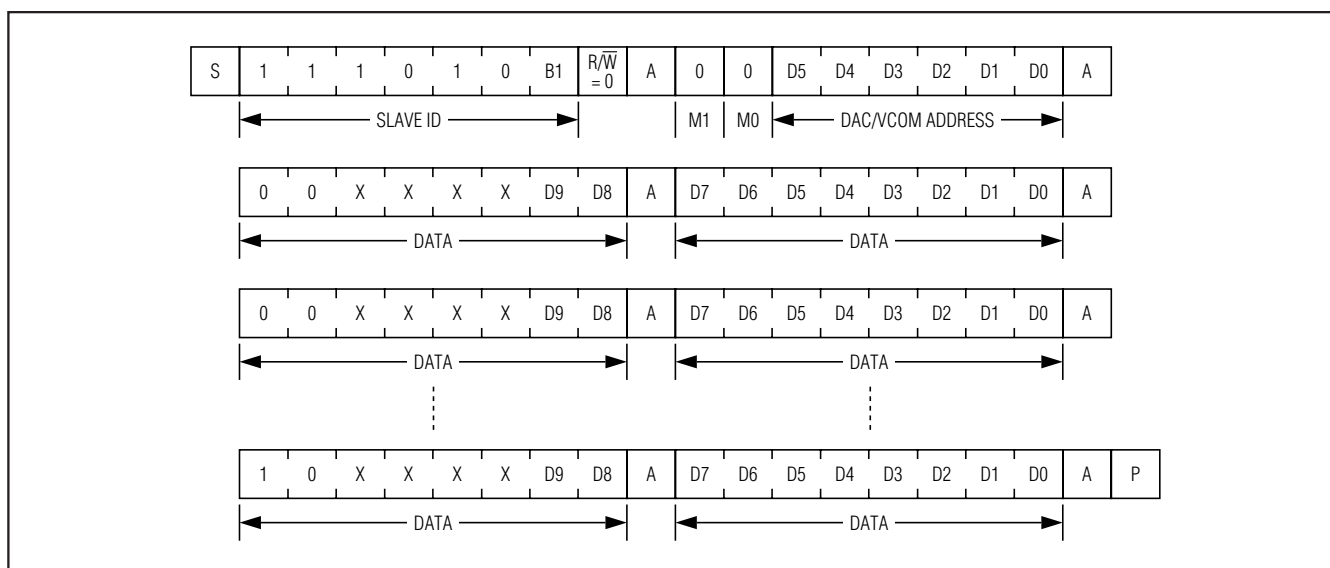


Figure 9. Multiple (or All) DACs Programming

It is possible to write to multiple DACs first then update the output voltage of all channels simultaneously, as shown in Figure 9. In this mode, it is possible for the I<sup>2</sup>C master to write to all registers of the MAX9672/MAX9673/MAX9674 (Gamma and VCOM) in one communication. In that case, the value programmed on addresses 0x10, 0x11, and 0x13 through 0x17 are meaningless. However, the MAX9672/MAX9673/MAX9674 send an acknowledge bit for each of the 2 bytes on any of these addresses. The control bits (W1, W0) shown in Figure 9 are set in a way that all DACs are programmed to their desired value with no changes to the output voltages until the LSB of the last DAC is received and then all the channels are updated simultaneously.

## Nonvolatile Memory

The MAX9672/MAX9673/MAX9674 are able to write to nonvolatile memory (MTP) of any single DAC/VCOM register in a single or burst I<sup>2</sup>C transaction. This memory

can be written to at least 300 times. Figure 10 shows a single write to a MTP address. The control bits on Figure 10 set in a way that the MTP register is updated at the end of the LSB (D0).

Figure 11 shows how to program multiple MTP registers in one communication transition. Similar to programming the volatile memory, the first 2 bytes of data correspond to the DAC/VCOM address specified by the master on the previous byte and the following 2 bytes of data correspond to the next address and so on. In this configuration all the MTP registers are programmed at the same time following the LSB of the last set of data bytes. (The last set of data bytes is different than the previous bytes as it is bits 15 and 14.) If for some reason the master issues a STOP condition before sending the last 2 bytes of the data with appropriate values of bits 15 and 14 (01), then none of the MTP registers are updated.



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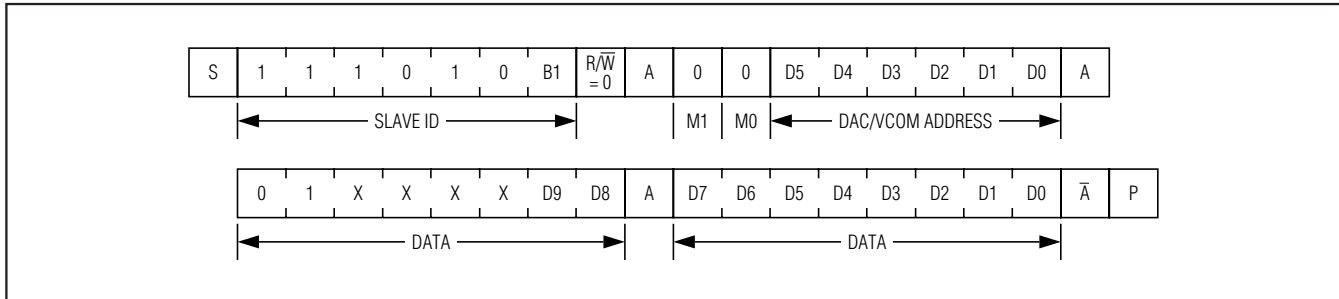


Figure 10. Single MTP Programming

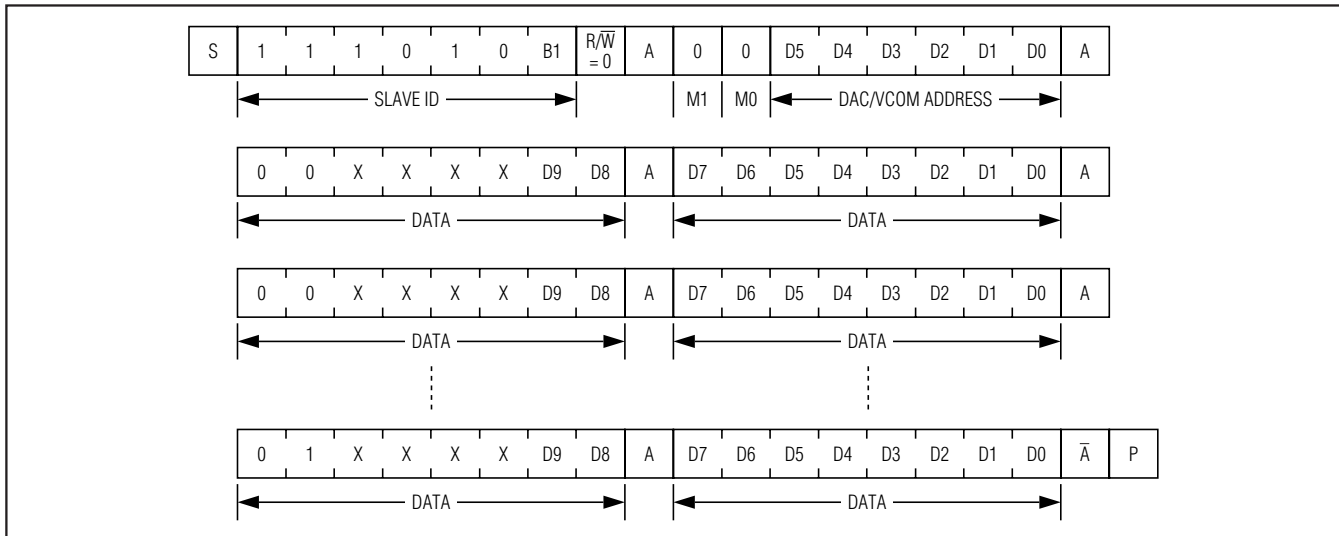


Figure 11. Multiple MTP Programming

Programming the MTP registers also updates the DACs/VCOM volatile memory as well as the output voltages. Similar to multiple volatile memory programming, the update only occurs after the LSB of the last byte is received. All the outputs are programmed and updated simultaneously. However, depending on the number of MTP registers, it takes 31ms to 500ms to store the values into the nonvolatile memory. During this time, the MAX9672/MAX9673/MAX9674 are not available on the I<sup>2</sup>C and any communication from the master should be delayed until the MTP is programmed. Any attempt from the I<sup>2</sup>C master to talk to the MAX9672/MAX9673/MAX9674 is not acknowledged.

## General and Single Acquire Commands

It is possible to update all the DAC outputs to the previously stored MTP values with one special command. Set the 2 MSBs (M1 and M0) of the DAC/VCOM

address to 10 to set all the DACs and the output voltages to the values of MTP (as shown in Figure 12). The MAX9672/MAX9673/MAX9674 ignore the DAC/VCOM address in this case.

It is also possible to update the DAC and output voltage of only one channel from the MTP. Set the 2 MSBs (M1 and M0) of the DAC/VCOM address to 01 (as shown in Figure 13) to move a specific value from MTP into the DAC and output voltage of a single channel.

The MAX9672/MAX9673/MAX9674 feature a double-buffered register structure. It is important to note that updating the volatile (DAC) memory is not the same as updating the output voltage. It is possible to write to multiple DACs first then update the output voltage of all channels simultaneously.

# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

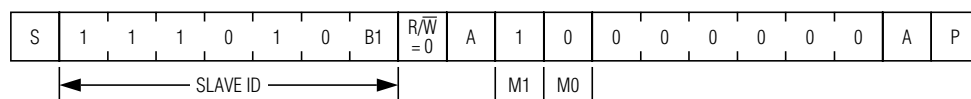


Figure 12. General Acquire Command to Update All Outputs with MTP

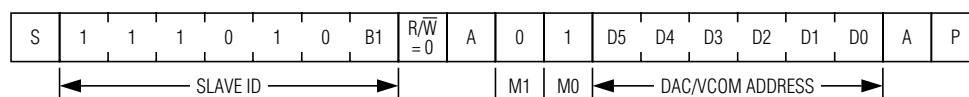


Figure 13. Single Acquire Command to Update One Output with MTP

## Applications Information

### Driving the Resistor Ladders with More Current

If the gamma buffers cannot provide enough current to drive the ends of the resistor ladders, then attach an additional resistor from the nearest supply. For example, at the very top of the resistor ladder, attach an additional resistor to AVDD. At the very bottom of the resistor ladder, attach an additional resistor to GND. The MAX9672/MAX9673/MAX9674 greatly diminish any noise from AVDD supply through the discrete resistor because the high-frequency noise from AVDD has been attenuated, and the buffers have excellent AC PSRR. See Figure 14.

### VCOM Operational Amplifier with Feedback Resistors

The output (VCOM) and negative input (VCOM\_FB) of the operational amplifier would usually be connected together, resulting in a unity-gain configuration. If a higher, closed-loop gain is desired, add feedback resistors as shown in Figure 15.

### Power-Up and Power-Down

Figures 16 and 17 show the proper startup sequence of the MAX9672/MAX9673/MAX9674. The digital supply must be powered up first. The analog supply should not be powered up for at least 250μs (typ) after the digital supply has been powered up. During this time, the MTP register values are overwriting the default values in the I<sup>2</sup>C registers. Once AVDD is above approximately 8V, the output buffers have enough headroom to power up.

If REF is powered up after AVDD, then the outputs track REF. If REF is powered up before AVDD, then the outputs track AVDD.

For power-down, AVDD and REF must be powered down first to 0V, and then DVDD can safely be powered down.

### Power Supplies and Bypass Capacitors

The MAX9672/MAX9673/MAX9674 operate from a single 9V to 20V analog supply (AVDD) and a 2.7V to 3.6V digital supply (DVDD). Bypass AVDD to GND with 0.1μF and 10μF capacitors in parallel. Use an extensive ground plane to ensure optimum performance. Bypass DVDD to GND with a 0.1μF capacitor. The 0.1μF bypass capacitors should be as close as possible to the device.

Refer to the MAX9672/MAX9673/MAX9674 evaluation kit for a proven PCB layout.

### Layout and Grounding

#### Exposed Pad

If the MAX9672/MAX9673/MAX9674 are mounted using reflow soldering or wave soldering, the ground via(s) for the exposed pad should have a finished hole size of at least 14 mils to insure adequate wicking of soldering onto the exposed pad. If the MAX9672/MAX9673/MAX9674 are mounted using the solder mask technique, the via requirement does not apply. In either case, the exposed pad must be connected to both digital and analog grounds through a low thermal resistance path to ensure adequate heat dissipation. Do not route traces under these packages.

# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

MAX9672/MAX9673/MAX9674

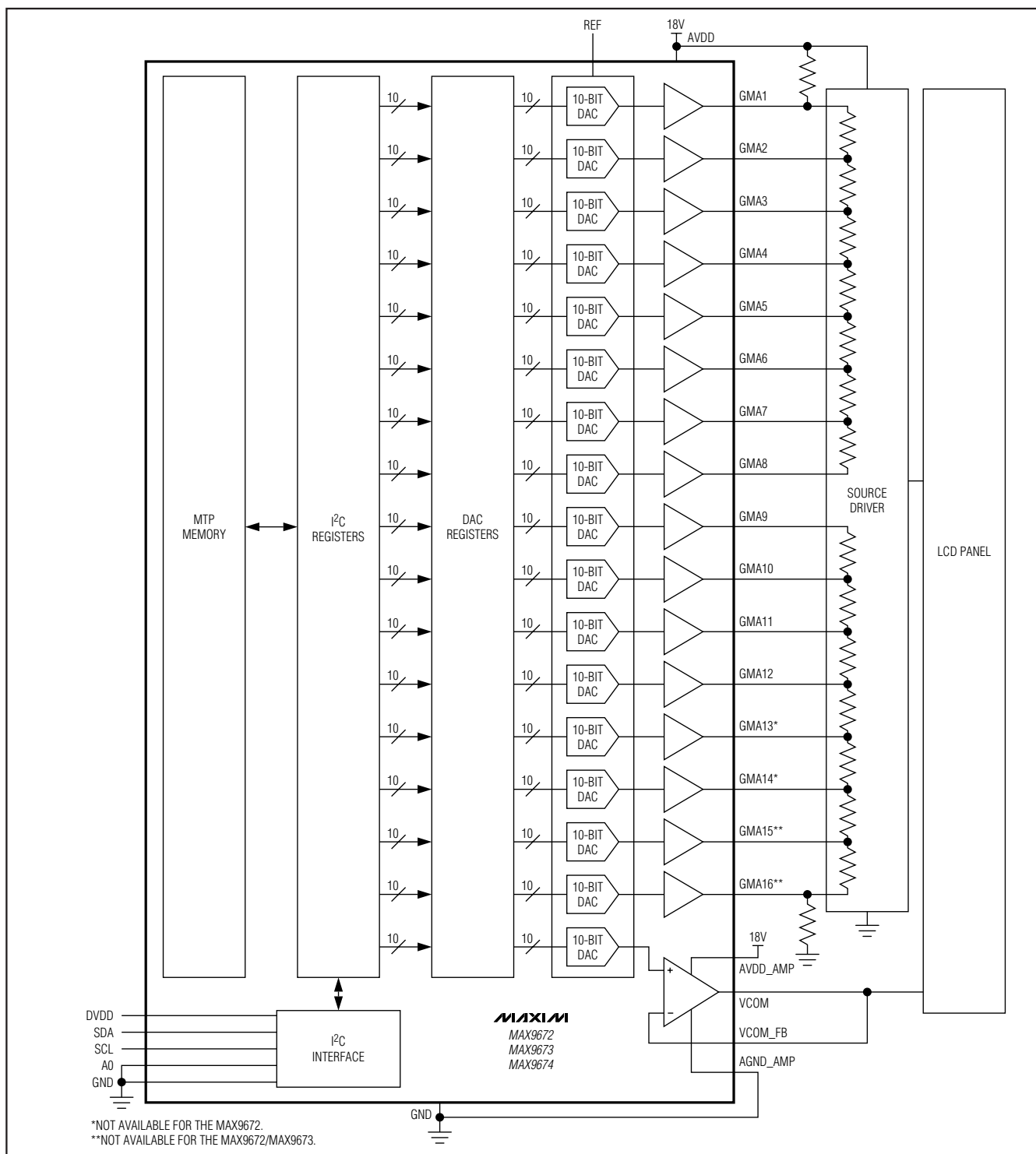


Figure 14. Typical Application Circuit with Additional Pullup and Pulldown Resistors on GMA1 and GMA16, Respectively

# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

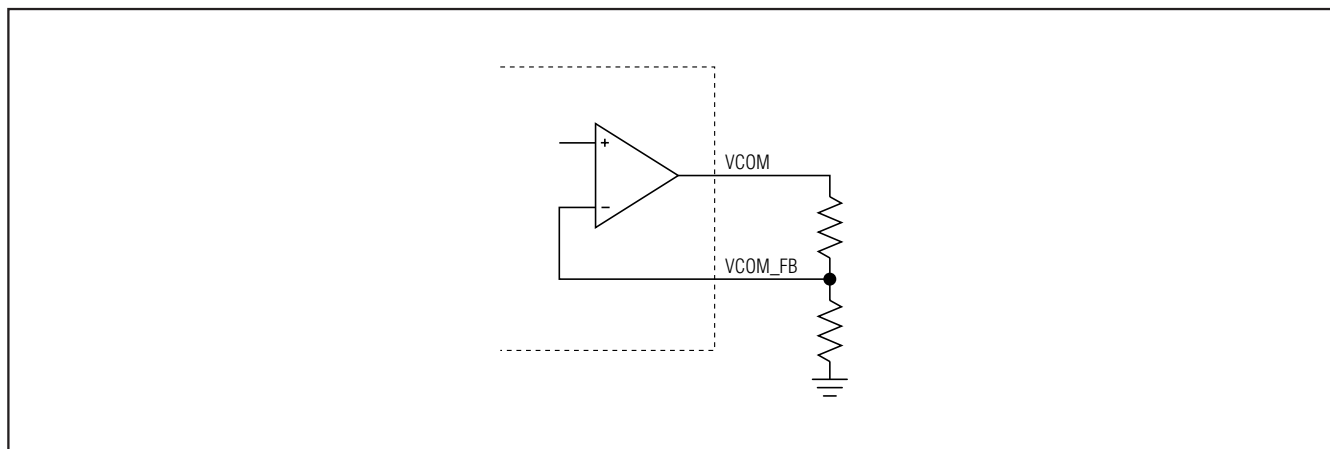


Figure 15. VCOM Operational Amplifier with Feedback Resistors

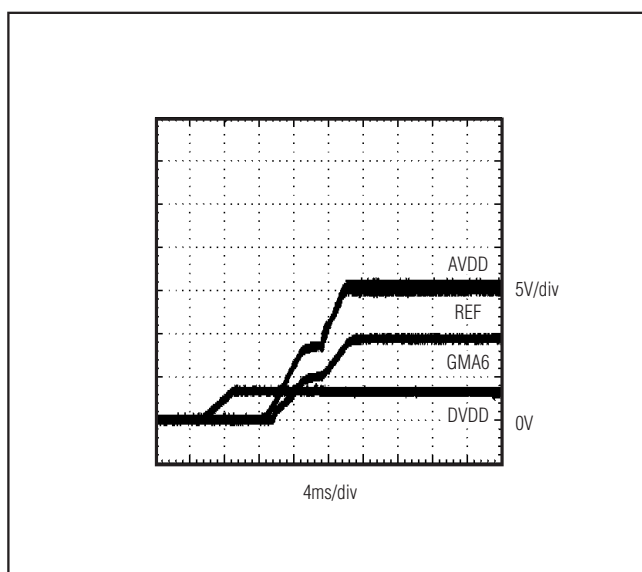


Figure 16. Recommended Power-Up Sequence

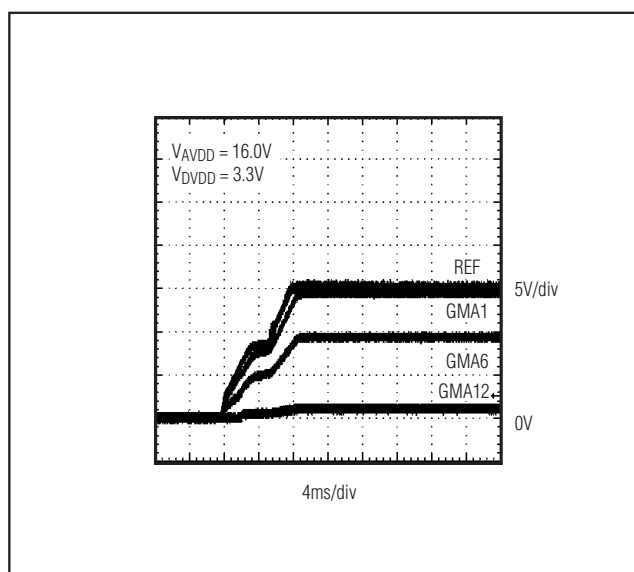


Figure 17. REF Powered Up After AVDD and DVDD

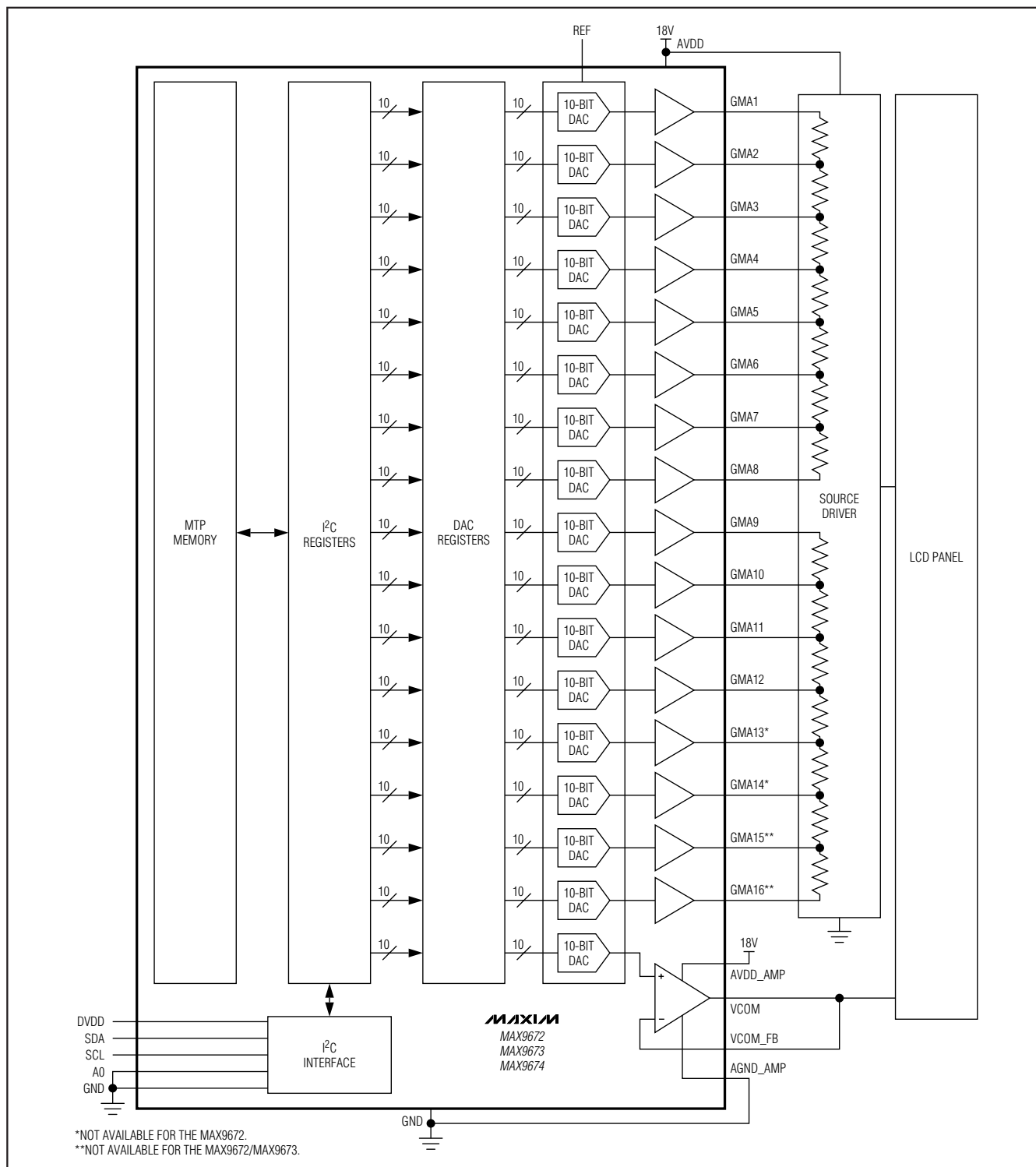
## Chip Information

PROCESS: BiCMOS

# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## Typical Operating Circuit

MAX9672/MAX9673/MAX9674

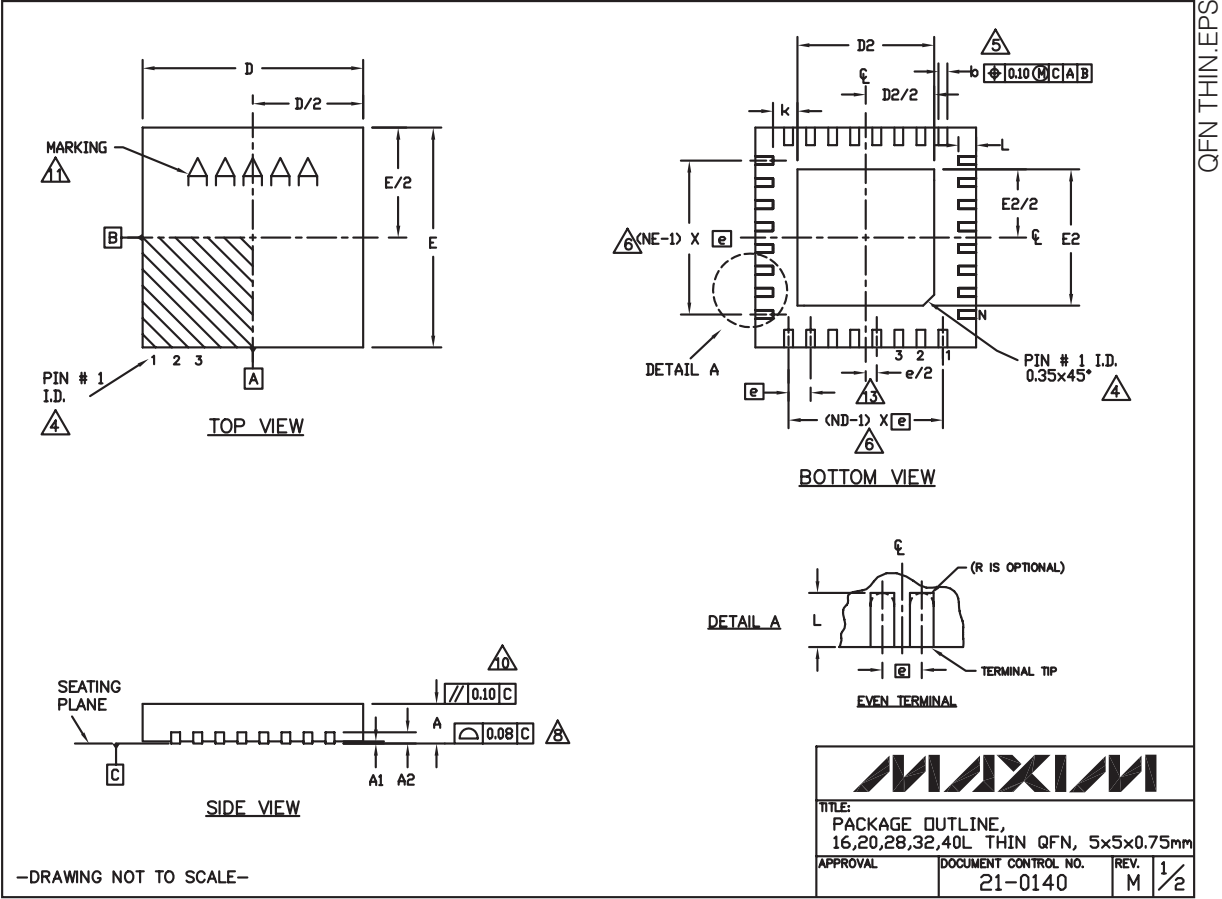


# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO.             | LAND PATTERN NO.        |
|--------------|--------------|-------------------------|-------------------------|
| 28 TQFN-EP   | T2855+8      | <a href="#">21-0140</a> | <a href="#">90-0028</a> |



# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## Package Information (continued)

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| COMMON DIMENSIONS |           |      |      |           |      |      |           |      |      |           |      |      |           |      |      |
|-------------------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|
| PKG.              | 16L 5x5   |      |      | 20L 5x5   |      |      | 28L 5x5   |      |      | 32L 5x5   |      |      | 40L 5x5   |      |      |
| SYMBOL            | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. |
| A                 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 |
| A1                | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 |
| A2                | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      |
| b                 | 0.25      | 0.30 | 0.35 | 0.25      | 0.30 | 0.35 | 0.20      | 0.25 | 0.30 | 0.20      | 0.25 | 0.30 | 0.15      | 0.20 | 0.25 |
| D                 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 |
| E                 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 |
| e                 | 0.80 BSC. |      |      | 0.65 BSC. |      |      | 0.50 BSC. |      |      | 0.50 BSC. |      |      | 0.40 BSC. |      |      |
| k                 | 0.25      | -    | -    | 0.25      | -    | -    | 0.25      | -    | -    | 0.25      | -    | -    | 0.25      | -    | -    |
| L                 | 0.30      | 0.40 | 0.50 | 0.45      | 0.55 | 0.65 | 0.45      | 0.55 | 0.65 | 0.30      | 0.40 | 0.50 | 0.30      | 0.40 | 0.50 |
| N                 | 16        |      |      | 20        |      |      | 28        |      |      | 32        |      |      | 40        |      |      |
| ND                | 4         |      |      | 5         |      |      | 7         |      |      | 8         |      |      | 10        |      |      |
| NE                | 4         |      |      | 5         |      |      | 7         |      |      | 8         |      |      | 10        |      |      |
| JEDEC             | VHHB      |      |      | VHHC      |      |      | VHHD-1    |      |      | VHHD-2    |      |      | -----     |      |      |

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3. N IS THE TOTAL NUMBER OF TERMINALS.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.

6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.

10. WARPAGE SHALL NOT EXCEED 0.10 mm.

11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

| EXPOSED PAD VARIATIONS |      |      |      |      |      |      |
|------------------------|------|------|------|------|------|------|
| PKG. CODES             | D2   |      |      | E2   |      |      |
|                        | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1655-2                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-3                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-4                | 2.19 | 2.29 | 2.39 | 2.19 | 2.29 | 2.39 |
| T165N-1                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-3                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-4                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-5                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2055MN-5              | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-3                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-4                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-5                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-6                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-7                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-8                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855N-1               | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T3255-3                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-4                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255N-4               | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-5                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255N-1               | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T4055-1                | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055-2                | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055N-1               | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055MN-1              | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |

MAXIM

TITLE:  
PACKAGE OUTLINE,  
16,20,28,32,40L THIN QFN, 5x5x0.75mm

APPROVAL

DOCUMENT CONTROL NO.  
21-0140

REV.  
M

2/2

MAX9672/MAX9673/MAX9674



# 10-Bit, Programmable Gamma Reference Systems with MTP for TFT LCDs

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION                                                               | PAGES CHANGED                 |
|-----------------|---------------|---------------------------------------------------------------------------|-------------------------------|
| 0               | 9/09          | Initial release                                                           | —                             |
| 1               | 10/09         | MTP factory initialization values changed per customer request in Table 3 | 12                            |
| 2               | 11/09         | Updated write operations and soldering temperature (reflow)               | 1, 2, 8, 16                   |
| 3               | 3/10          | Added lead temperature and made various corrections                       | 2, 3, 4, 6, 8, 11, 14, 19, 21 |
| 4               | 2/11          | Changed MTP factory initialization value of MAX9673 for GMA5              | 12                            |

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