MAX8752

TFT LCD Step-Up DC-DC Converter

General Description

The MAX8752 is a high-performance, step-up DC-DC converter that provides a regulated supply voltage for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs). The MAX8752 incorporates current-mode, fixed-frequency, pulse-width modulation (PWM) circuitry with a built-in n-channel power MOSFET to achieve high efficiency and fast transient response. The input supply voltage of the MAX8752 is from 1.8V to 5.5V.

The MAX8752 operates with a switching frequency of 1.2MHz, allowing the use of ultra-small inductors and low-ESR ceramic capacitors. The current-mode architecture provides fast transient response to the pulsed loads typical of LCD source-driver applications. A compensation pin (COMP) gives users flexibility in adjusting loop dynamics. The 14V internal MOSFET can generate output voltages up to 13V. The internal digital soft-start and current limit effectively control inrush and fault currents.

The MAX8752 is available in a 3mm x 3mm, 8-pin TDFN package with a maximum height of 8mm.

Applications

- Notebook Computer Displays
- LCD Monitor Panels

Features

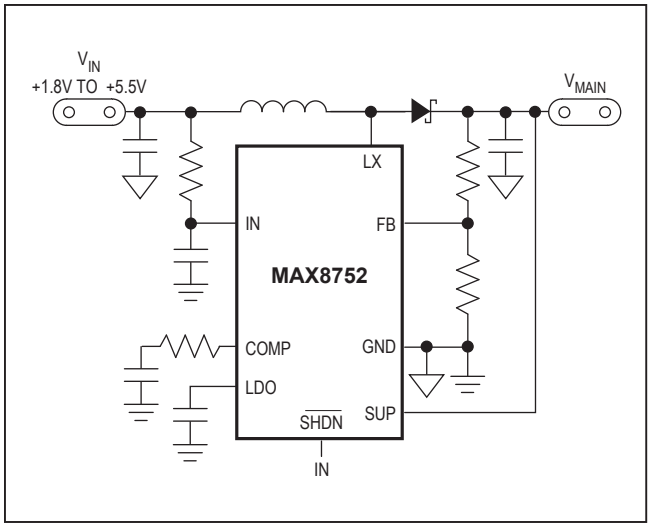
- 1.8V to 5.5V Input Supply Range
- Built-In 14V, 2.2A, 0.2Ω n-Channel MOSFET
- High Efficiency (> 85%)
- Fast Transient Response to Pulsed Load
- High-Accuracy Output Voltage (1.5%)
- Internal Digital Soft-Start
- Input Supply Undervoltage Lockout
- 1.2MHz Switching Frequency
- 0.1µA Shutdown Current
- Small 8-Pin TDFN Package

Ordering Information

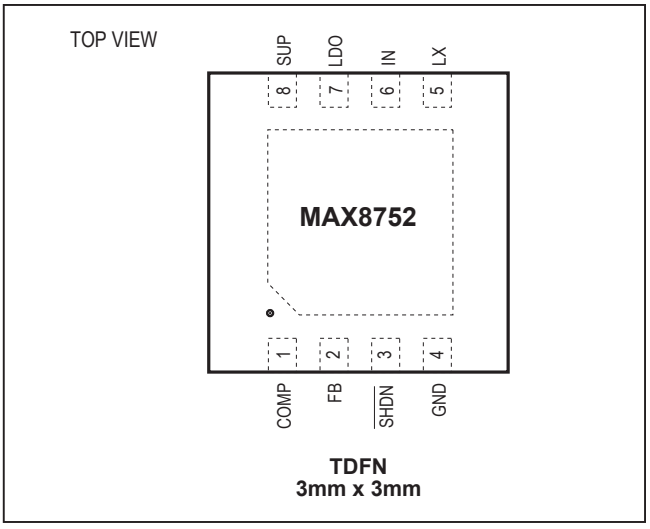
PART	TEMP RANGE	PIN-PACKAGE
MAX8752ETA	-40°C to +85°C	8 TDFN-EP*

**EP = Exposed pad.*

Typical Operating Circuit



Pin Configuration



maxim integrated™

Absolute Maximum Ratings

LX, SUP to GND .....-0.3V to +14V
IN, $\overline{SHDN}$, LDO to GND .....-0.3V to +6V
FB to GND .....-0.3V to (V_{IN} + 0.3V)
COMP to GND ..... -0.3V to (V_{LDO} + 0.3V)
LX Switch Maximum Continuous RMS Current 1.6A

Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 18.2mW/°C above +70°C).....1454mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = $V_{\overline{SHDN}}$ = 2.5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range		1.8		5.5	V
Output Voltage Range				13	V
IN Undervoltage Lockout Threshold	V_{IN} rising, typical hysteresis is 200mV	0.90	1.30	1.75	V
IN Quiescent Current	V_{FB} = 1.3V, not switching		0.18	0.35	mA
	V_{FB} = 1.0V, switching		2	5	
IN Shutdown Current	$\overline{SHDN}$ = GND		0.1	10.0	µA
LDO Output Voltage	6V ≤ V_{SUP} ≤ 13V, I_{LDO} = 12.5mA	4.6	5.0	5.4	V
LDO Undervoltage Lockout	V_{LDO} rising, typical hysteresis is 200mV	2.4	2.7	3.0	V
LDO Output Current		15			mA
SUP Supply Voltage Range		4.5		13.0	V
SUP Overvoltage-Lockout Threshold	V_{SUP} rising, typical hysteresis is 200mV (Note 1)	13.2	13.6	14.0	V
SUP Undervoltage-Lockout Threshold	V_{SUP} rising, typical hysteresis is 200mV (Note 2)			1.4	V
SUP Supply Current	LX not switching		1.5	2.0	mA
	LX switching		4	8	
ERROR AMPLIFIER					
FB Regulation Voltage	I_{LX} = 200mA, T = 0°C to +25°C	1.218	1.240	1.262	V
	I_{LX} = 200mA, T = +25°C to +85°C	1.223	1.240	1.257	
FB Input Bias Current	V_{FB} = 1.24V		0	40	nA
FB Line Regulation	V_{IN} = 1.8V to 5.5V		0.05	0.15	%/V
Transconductance		70	180	280	µS
Voltage Gain			700		V/V
OSCILLATOR					
Frequency		1000	1220	1500	kHz
Maximum Duty Cycle		88	92	96	%

Electrical Characteristics (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = 2.5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
n-CHANNEL MOSFET					
Current Limit	V_{FB} = 1V, 65% duty cycle	1.8	2.2	2.6	A
On-Resistance			0.2	0.4	Ω
Leakage Current	V_{LX} = 12V		0.1	10	µA
Current-Sense Transresistance		0.2	0.3	0.4	V/A
SOFT-START					
Soft-Start Period			13		ms
Soft-Start Step Size			0.275		A
CONTROL INPUTS					
$\overline{SHDN}$ Input Low Voltage	V_{IN} = 1.8V to 5.5V			0.6	V
$\overline{SHDN}$ Input High Voltage	V_{IN} = 1.8V to 5.5V	0.7 x V_{IN}			V
$\overline{SHDN}$ Input Current			0.001	1.000	µA

Electrical Characteristics

(V_{IN} = $V_{\overline{SHDN}}$ = 2.5V, **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range		1.8		5.5	V
Output Voltage Range				13	V
IN Undervoltage-Lockout Threshold	V_{IN} rising, typical hysteresis is 200mV	0.90		1.75	V
IN Quiescent Current	V_{FB} = 1.3V, not switching			0.35	mA
	V_{FB} = 1.0V, switching			5	
LDO Output Voltage	6V ≤ V_{SUP} ≤ 13V, I_{LDO} = 12.5mA	4.6		5.4	V
LDO Undervoltage Lockout	V_{LDO} rising, typical hysteresis is 200mV	2.4		3.0	V
LDO Output Current		15			mA
SUP Supply Voltage Range		4.5		13.0	V
SUP Overvoltage-Lockout Threshold	V_{SUP} rising, typical hysteresis is 200mV (Note 1)	13.2		14.0	V
SUP Undervoltage-Lockout Threshold	V_{SUP} rising, typical hysteresis is 200mV (Note 2)			1.4	V
SUP Supply Current	LX not switching			2.0	mA
	LX switching			8	
ERROR AMPLIFIER					
FB Regulation Voltage	I_{LX} = 200mA	1.210		1.270	V
OSCILLATOR					
Frequency		940		1560	kHz
n-CHANNEL MOSFET					
Current Limit	V_{FB} = 1V, 65% duty cycle	1.7		2.7	A
On-Resistance				0.4	Ω
Current-Sense Transresistance		0.2		0.4	V/A

Electrical Characteristics (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = 2.5V, **T_A = -40°C to +85°C**, unless otherwise noted.)

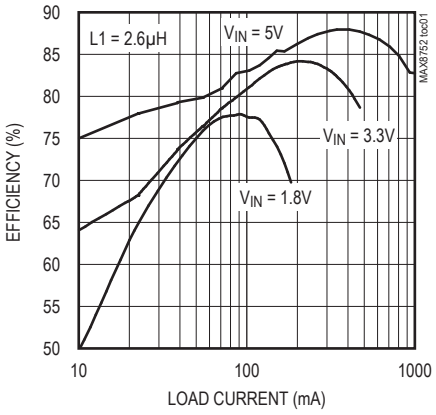
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS					
$\overline{SHDN}$ Input Low Voltage	V_{IN} = 1.8V to 5.5V			0.6	V
$\overline{SHDN}$ Input High Voltage	V_{IN} = 1.8V to 5.5V	0.7 x V_{IN}			V

Note 1: Step-up regulator inhibited when V_{SUP} exceeds this threshold.
Note 2: Step-up regulator inhibited until V_{SUP} exceeds this threshold.
Note 3: Specifications to -40°C are guaranteed by design, not production tested.

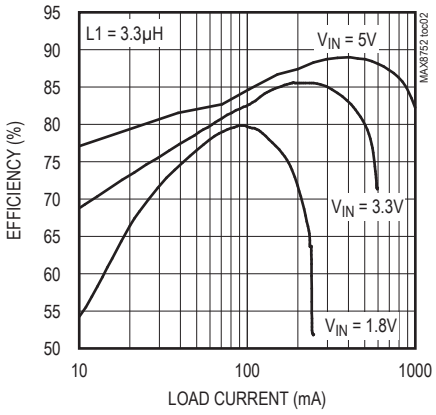
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 2.5V, V_{MAIN} = 10V, T_A = +25°C, unless otherwise noted.)

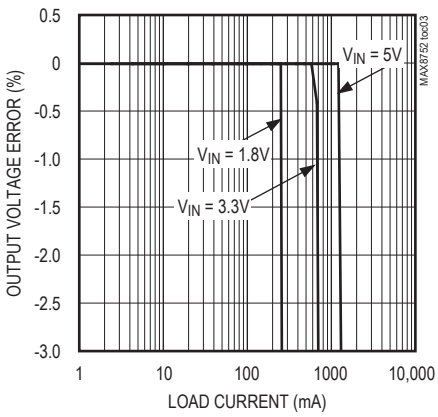
EFFICIENCY vs. LOAD CURRENT



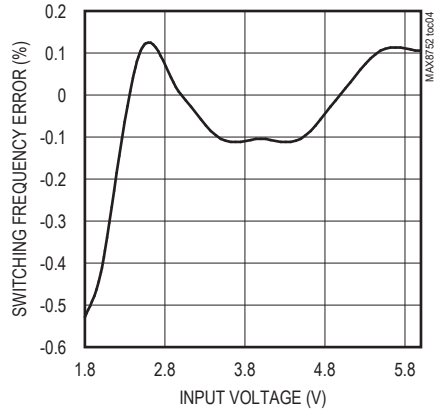
EFFICIENCY vs. LOAD CURRENT



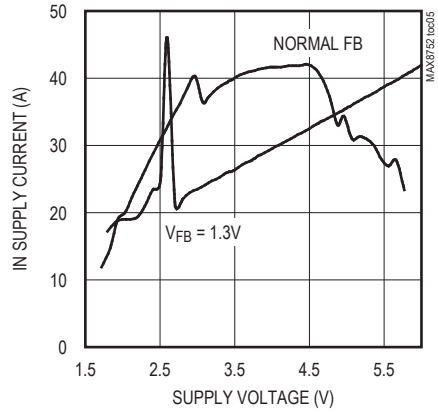
OUTPUT VOLTAGE ERROR vs. LOAD CURRENT



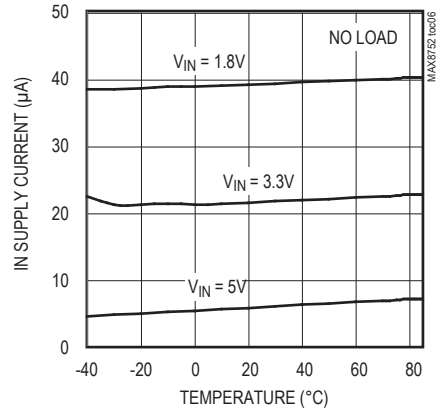
SWITCHING FREQUENCY ERROR vs. INPUT VOLTAGE



IN SUPPLY CURRENT vs. SUPPLY VOLTAGE



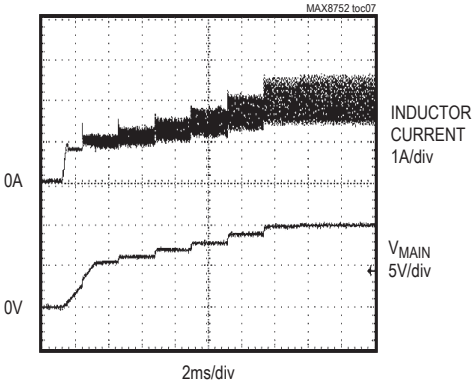
IN SUPPLY CURRENT vs. TEMPERATURE



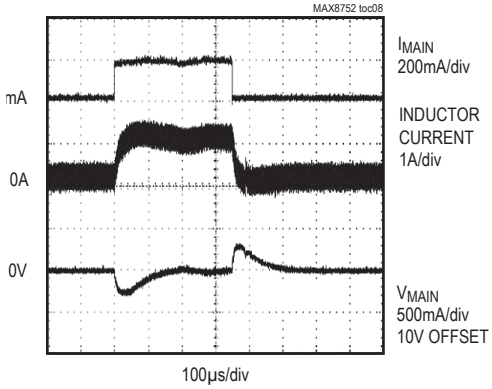
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 2.5V, V_{MAIN} = 10V, T_A = +25°C, unless otherwise noted.)

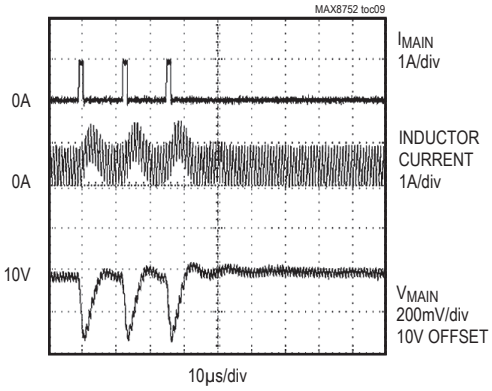
SOFT-START (HEAVY LOAD)



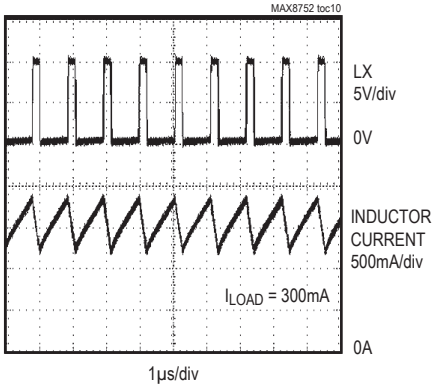
LOAD TRANSIENT RESPONSE



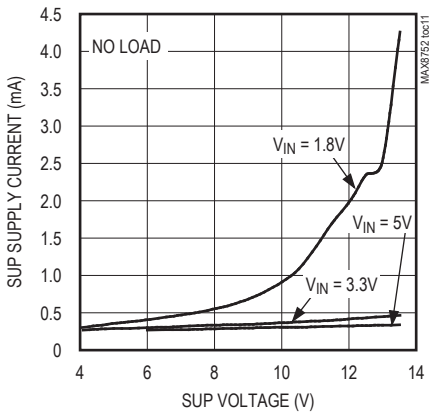
PULSED-LOAD TRANSIENT RESPONSE



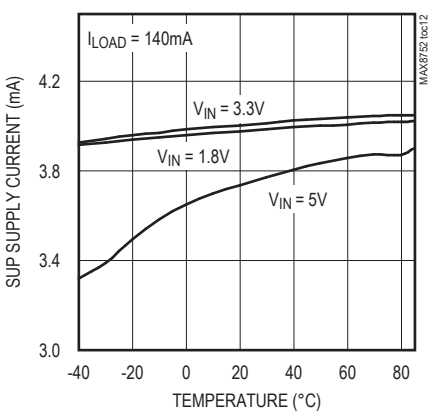
SWITCHING WAVEFORMS



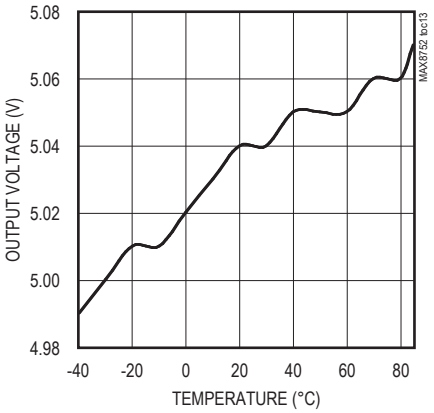
SUP SUPPLY CURRENT vs. SUP VOLTAGE



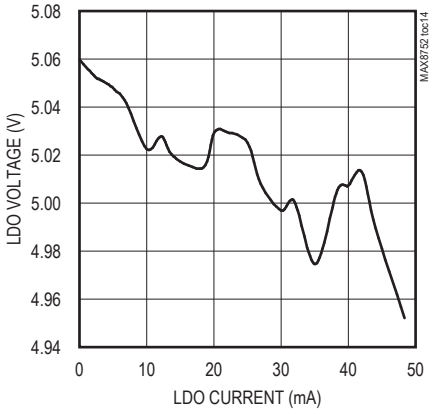
SUP SUPPLY CURRENT vs. TEMPERATURE



LDO OUTPUT VOLTAGE vs. TEMPERATURE



LDO OUTPUT VOLTAGE vs. LDO CURRENT



Pin Description

PIN	NAME	FUNCTION
1	COMP	Compensation Pin for Error Amplifier. Connect a series resistance and capacitor from COMP to GND. See the *Loop Compensation* section for component selection guidelines.
2	FB	Feedback Pin. The FB regulation voltage is 1.24V nominal. Connect an external resistive voltage-divider between the step-up regulator's output (V_{MAIN}) and GND, with the center tap connected to FB. Place the divider close to the IC and minimize the trace area to reduce noise coupling. Set V_{MAIN} according to the *Output Voltage Selection* section.
3	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to turn off the MAX8752.
4	GND	Ground
5	LX	Switching Node. LX is the drain of the internal MOSFET. Connect the inductor/rectifier diode junction to LX and minimize the trace area for lower EMI.
6	IN	Supply Pin. Connect IN to the input supply through a series 100Ω resistor and bypass it to GND with 0.1µF or greater ceramic capacitor.
7	LDO	Internal 5V Linear-Regulator Output. This regulator powers all internal circuitry. Bypass LDO to GND with a 0.22µF or greater ceramic capacitor.
8	SUP	Linear-Regulator Supply Input. SUP is the supply input of the internal 5V linear regulator. Connect SUP to the step-up regulator output and bypass SUP to GND with a 0.1µF capacitor.
—	EP	Exposed Paddle. Connect the exposed paddle to analog ground.

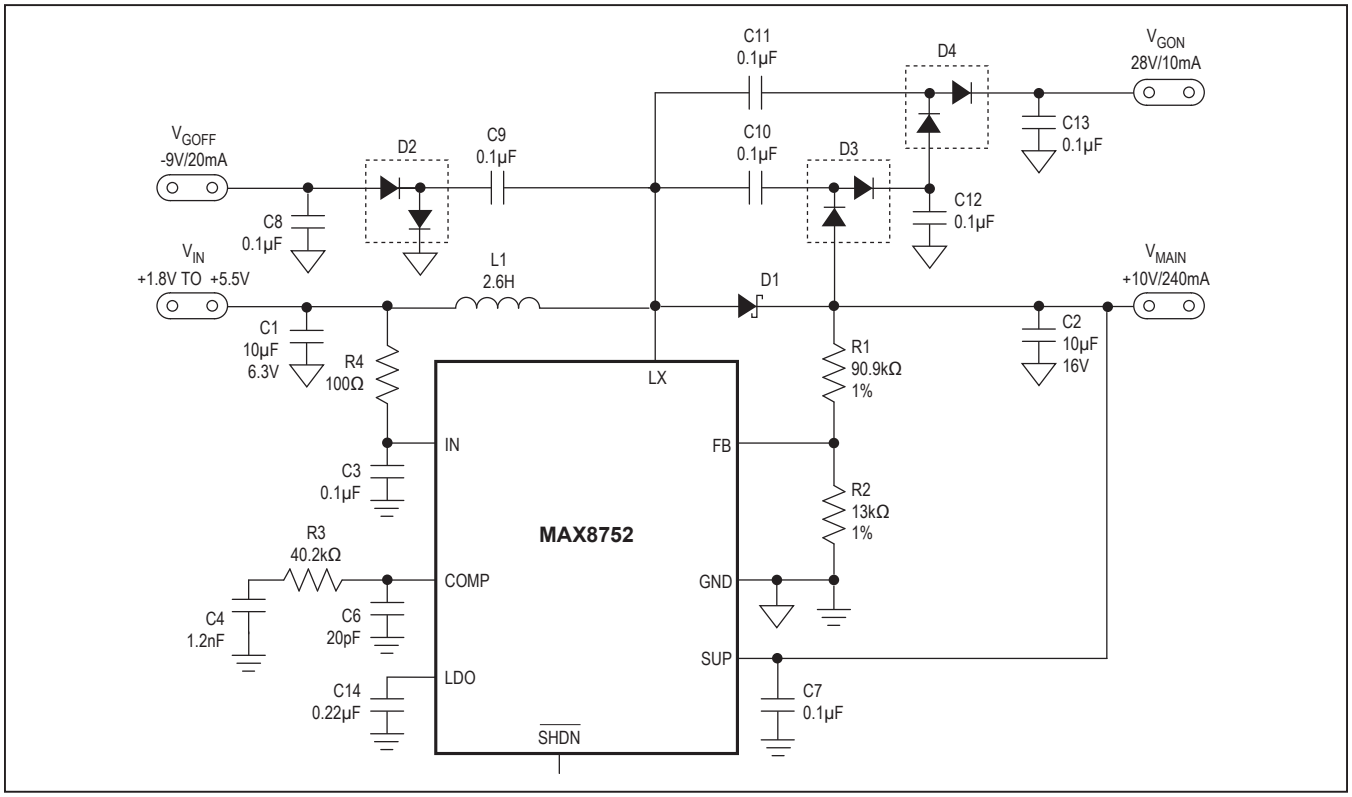


Figure 1. Typical Applications Circuit

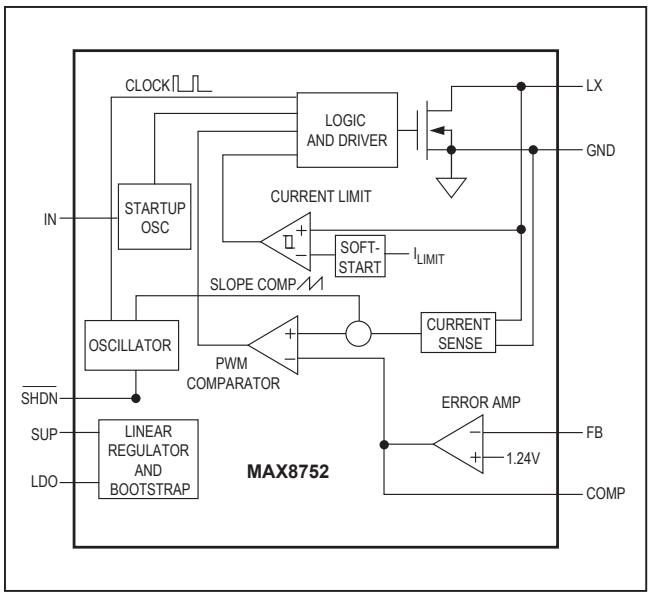


Figure 2. Functional Diagram

Detailed Description

The MAX8752 is a highly efficient, step-up power supply designed for TFT-LCD panels. The typical circuit shown in Figure 1 operates from an input voltage as low as 1.8V, and produces a MAIN output of 10V at 220mA from 2.5V input while supporting discrete diode-capacitor charge pumps that produce -9V at 20mA and +28V at 10mA. If the charge-pump outputs are not required, the diodes and capacitors associated with them may be eliminated and the main output increased to 270mA.

The MAX8752 employs a current-mode, fixed-frequency, pulse-width modulation (PWM) architecture for fast transient response and low-noise operation. The high switching frequency (1.2MHz) allows the use of lowprofile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and the IC's built-in digital soft-start function reduce the number of external components required. The output voltage can be set from V_{IN} to 13V with an external resistive voltage-divider.

The MAX8752 regulates the output voltage through a combination of an error amplifier, two comparators, and several signal generators (Figure 2). The error amplifier compares the signal at FB to 1.24V and varies the COMP output. The voltage at COMP determines the current trip point each time the internal MOSFET turns on. As the load changes, the error amplifier sources or sinks current to the COMP output to set the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flipflop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

At light loads, this architecture allows the MAX8752 to "skip" cycles to prevent overcharging the output capacitor voltage.

In this region of operation, the inductor ramps up to a peak value of approximately 250mA, discharges to the output, and waits until another pulse is needed.

Output-Current Capability

The output-current capability of the MAX8752 is a function of current limit, input voltage, operating frequency, and inductor value. Because of the slope compensation used to stabilize the feedback loop, the inductor current limit depends on the duty cycle. The current limit is determined by the following equation:

$$I_{LIM} = (1.162 - 0.361 \times D) \times I_{LIM_EC}$$

where I_{LIM_EC} is the current limit specified at 65% duty cycle (see the *Electrical Characteristics*) and D is the duty cycle.

The output current capability depends on the currentlimit value and is governed by the following equation:

$$I_{OUT(MAX)} = \left[I_{LIM} - \frac{0.5 \times D \times V_{IN}}{f_{OSC} \times L} \right] \times \frac{V_{IN}}{V_{OUT}} \times \eta$$

where I_{LIM} is the current limit calculated above, η is the regulator efficiency (85% nominal), and D is the duty cycle. The duty cycle when operating at the current limit is:

$$D = \frac{V_{OUT} - V_{IN} + V_{DIODE}}{V_{OUT} - I_{LIM} \times R_{ON} + V_{DIODE}}$$

where V_{DIODE} is the rectifier diode forward voltage and R_{ON} is the on-resistance of the internal MOSFET.

Bootstrapping and Soft-Start

The MAX8752 features bootstrapping operation. In normal operation, the internal linear regulator supplies power to the internal circuitry. The input of the linear regulator (SUP) should be directly connected to the output of the step-up regulator. After the input voltage at SUP is above 1.75V, the regulator starts open-loop switching to generate the supply voltage for the linear regulator. The internal reference block turns on when the LDO voltage exceeds 2.7V (typ).

When the reference voltage reaches regulation, the PWM controller and the current-limit circuit are enabled and the step-up regulator enters soft-start. During the soft-start, the main step-up regulator directly limits the peak inductor current, allowing from zero up to the full current limit in eight equal current steps. The maximum load current is available after the output voltage reaches regulation (which terminates soft-start), or after the soft-start timer expires (13ms typ). The soft-start routine minimizes the inrush current and voltage overshoot and ensures a well-defined startup behavior.

Shutdown

The MAX8752 shuts down to reduce the supply current to 0.1µA when $\overline{SHDN}$ is low. In this mode, the internal reference, error amplifier, comparators, and biasing circuitry turn off and the n-channel MOSFET is turned off. In shutdown, the step-up regulator's output is connected to IN through the external inductor and rectifier diode.

Table 1. Component List

DESIGNATION	DESCRIPTION
C1	10µF ±10%, 4V X5R ceramic capacitor (0603) TDK C1608X5R0G106K Murata GRM188R60G106M
C2	10µF ±10%, 16V X5R ceramic capacitor (1206) TDK C3216X5R1C106K Murata GRM319R61A106K
D1	3A, 30V Schottky diode (M-flat) Toshiba CRS02
L1	2.6µH, 2.1A power inductor 3.3µH, 1.7A power inductor Sumida CDRH6D12-3R3

Applications Information

Step-up regulators using the MAX8752 can be designed by performing simple calculations for a first iteration. All designs should be prototyped and tested prior to production. Table 1 provides a list of power components for the typical applications circuit. Table 2 lists component suppliers.

External component value choice is primarily dictated by the output voltage and the maximum load current, as well as maximum and minimum input voltages. Begin by selecting an inductor value. Once the inductor value and peak current are known, choose the diode and capacitors.

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output voltage ripple. Physical size and cost are also important factors to consider.

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Murata	770-436-1300	www.murata-northamerica.com
Sumida	847-545-6700	www.sumida.com
TDK	847-803-6100	www.component.tdk.com
Toshiba	949-623-2900	www.toshiba.com/taec

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant, LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

In Figure 1, the LCD's gate-on and gate-off voltages are generated from two unregulated charge pumps driven by the step-up regulator's LX node. The additional load on LX must therefore be considered in the inductance calculation. The effective maximum output current $I_{MAIN(EFF)}$ becomes the sum of the maximum load current on the step-up regulator's output plus the contributions from the positive and negative charge pumps:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + \eta_{NEG} \times I_{NEG} + (\eta_{POS} + 1) \times I_{POS}$$

where $I_{MAIN(MAX)}$ is the maximum main output current, n_{NEG} is the number of negative charge-pump stages, n_{POS} is the number of positive charge-pump stages, I_{NEG} is the negative charge-pump output current, and I_{POS} is the positive charge-pump output current, assuming the pump source for I_{POS} is V_{MAIN}.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(MAX)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(MAX)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times (V_{MAIN} - V_{IN(MIN)})}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX8752's LX current limit (I_{LIM}) should exceed IPEAK and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the Typical Applications Circuit (Figure 1), the maximum load current ($I_{MAIN(MAX)}$) is 180mA with a 10V output and a typical input voltage of 2.5V:

$$I_{MAIN(EFF)} = 180mA + 1 \times 20mA + 3 \times 10mA = 230mA$$

Choosing an LIR of 0.5 and estimating efficiency of 80% at this operating point:

$$L = \left(\frac{2.5V}{10V}\right)^2 \left(\frac{10V - 2.5V}{0.23A \times 1.2MHz}\right)\left(\frac{0.80}{0.50}\right) \approx 2.6\mu H$$

Using the circuit's minimum input voltage (2.2V) and estimating efficiency of 75% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.23A \times 10V}{2.2V \times 0.75} \approx 1.4A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{2.2V \times (10V - 2.2V)}{2.6\mu H \times 10V \times 1.2MHz} \approx 0.55A$$

$$I_{PEAK} = 1.4A + \frac{0.55A}{2} \approx 1.7A$$

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right), \text{and}$$

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10µF ceramic capacitor is used in the Typical Applications Circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in the Typical Applications Circuit. Ensure a low noise supply at IN by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter (see R3 and C3 in Figure 1).

Rectifier Diode Selection

The MAX8752's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. The diode should be rated to handle the output voltage and the peak switch current. Make sure that the diode's peak current rating is at least I_{PEAK} calculated in the *Inductor Selection* section and that its breakdown voltage exceeds the output voltage.

Output Voltage Selection

The MAX8752 operates with an adjustable output from V_{IN} to 13V. Connect a resistive voltage-divider from the output (V_{MAIN}) to GND with the center tap connected to FB (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{FB}} - 1\right)$$

where V_{FB}, the step-up regulator's feedback set point, is 1.24V (typ). Place R1 and R2 close to the IC.

Loop Compensation

The voltage-feedback loop needs proper compensation to prevent excessive output ripple and poor efficiency caused by instability. This is done by connecting a resistor (R_{COMP}) and capacitor (C_{COMP}) in series from COMP to GND, and another capacitor (C_{COMP2}) from COMP to GND. R_{COMP} is chosen to set the high-frequency integrator gain for fast transient response, while C_{COMP} is chosen to set the integrator zero to maintain loop stability. The second capacitor, C_{COMP2}, is chosen to cancel the zero introduced by output-capacitance ESR. For optimal performance, choose the components using the following equations:

$$R_{COMP} \approx \frac{264 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{MAIN(EFF)}}$$

$$C_{COMP} \approx \frac{V_{OUT} \times C_{OUT}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

$$C_{COMP2} \approx \frac{0.02 \times R_{ESR} \times L \times I_{MAIN(EFF)}}{V_{IN} \times V_{OUT}}$$

For the ceramic output capacitor, where ESR is small, C_{COMP2} is optional. The best gauge of correct loop compensation is by inspecting the transient response of the MAX8752. Adjust R_{COMP} and C_{COMP} as necessary to obtain optimal transient performance.

PC Board Layout and Grounding

Careful PC board layout is important for proper operation. Use the following guidelines for good PC board layout:

1) Minimize the area of high-current loops by placing the inductor, rectifier diode, and output capacitors near the input capacitors and near the LX and GND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out the IC's GND pin, and to the input capacitor's negative terminal. The highcurrent output loop is from the positive terminal of the input capacitor to the inductor, to the rectifier diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input-capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths, especially the ground paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2) Create a power ground island (PGND) consisting of the input and output capacitor grounds and GND. Connect all of these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the feedback divider's ground, the COMP capacitor's ground, and the IC's exposed backside pad near pin 1. Connect the AGND and PGND islands by connecting the GND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
3) Place the feedback voltage-divider resistors as close to FB as possible. The divider's center trace should be kept short. Placing the resistors far away causes the FB trace to become an antenna that can pick up switching noise. Avoid running the feedback trace near LX.
4) Place the SUP and LDO bypass capacitors and the IN bypass capacitors (C3 in Figure 1) if within 5mm of their respective pins. Connect their ground terminals to GND through the IC's exposed back paddle near GND (pin4).
5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and other sensitive nodes. Use DC traces as shield if necessary.

Refer to the MAX8752 evaluation kit for an example of proper board layout.

Chip Information

PROCESS: BiCMOS

Package Information

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PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T833-2	21-0137	90-0059

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/05	Initial release	—
1	10/14	Removed automotive reference from the *Applications*	1

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