BGA7204

400 MHz to 2750 MHz high linearity variable gain amplifier

Rev. 4 — 15 November 2016 Product data sheet

1. Product profile

1.1 General description

The BGA7204 MMIC is an extremely linear Variable Gain Amplifier (VGA), operating from 0.4 GHz to 2.75 GHz. At minimum attenuation it has a gain of 18.5 dB, an output IP3 of 38 dBm and a noise figure of 7 dB. The attenuation range is 31.5 dB with an attenuation step of 0.5 dB.

The gain control is offered through a digital parallel interface or a digital serial interface (SPI). The digital serial interface offers advanced features like reprogramming the attenuation curve and on-chip temperature monitoring. The interfaces can be combined to support response to fast fading. The serial interface can be used to pre-set the desired gain level, whereas the parallel interface can be used to select this gain setting in 0.15 μs.

It has been designed and qualified for the severe mission profile of cellular base stations, but its outstanding RF performance and interfacing flexibility makes it suitable for a wide variety of applications.

The BGA7204 is housed in a 32 pins 5 mm × 5 mm leadless HVQFN package.

1.2 Features and benefits

- High output IP3 of 38 dBm
- Attenuation range of 31.5 dB
- Output power at 1 dB compression of 21 dBm
- Noise figure of 7 dB at minimum attenuation
- Single 5 V supply
- Digital parallel and digital serial control (SPI)
- Programmable attenuation curve
- Temperature sensor
- ESD protection on all pins (HBM > 2 kV)
- Moisture sensitivity level 1
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- IF and RF applications
- WiMAX and cellular base stations
- Cable modem termination systems
- Temperature compensation circuits

1.4 Quick reference data

Table 1. Quick reference data

4.75 V ≤ V_{SUP} ≤ 5.25 V; f = 400 MHz to 2750 MHz; −40 °C ≤ T_{amb} ≤ +85 °C; input and output are terminated with 50 Ω, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{SUP}	supply voltage		[1]	4.75	5.0	5.25	V
$I_{CC(tot)}$	total supply current	PWRDN = 0		-	115	133	mA
		PWRDN = 1		-	15	-	mA
T_{amb}	ambient temperature			−40	+25	+85	°C
G_p	power gain	minimum attenuation					
		400 MHz ≤ f ≤ 1450 MHz		16	18.5	21	dB
		1450 MHz ≤ f ≤ 2100 MHz		15	17.5	20	dB
		2100 MHz ≤ f ≤ 2750 MHz		14	16.5	19	dB
α_{range}	attenuation range	400 MHz ≤ f ≤ 1450 MHz		29	31.5	34	dB
		1450 MHz ≤ f ≤ 2100 MHz		28	30.5	33	dB
		2100 MHz ≤ f ≤ 2750 MHz		27	30.0	33	dB
α_{step}	attenuation step			0	0.5	1	dB
NF	noise figure	minimum attenuation					
		400 MHz ≤ f ≤ 700 MHz		-	7	9.5	dB
		700 MHz ≤ f ≤ 2100 MHz		-	6.5	9	dB
		2100 MHz ≤ f ≤ 2750 MHz		-	7.0	10	dB
$IP3_O$	output third-order intercept point	minimum attenuation					
		400 MHz ≤ f ≤ 700 MHz	[2]	34	38	-	dBm
		700 MHz ≤ f ≤ 1450 MHz	[2]	33	37.5	-	dBm
		1450 MHz ≤ f ≤ 2100 MHz	[2]	31	36	-	dBm
		2100 MHz ≤ f ≤ 2750 MHz	[2]	28.5	34	-	dBm
$P_{L(1dB)}$	output power at 1 dB gain compression	minimum attenuation					
		400 MHz ≤ f ≤ 1450 MHz		19	21	-	dBm
		1450 MHz ≤ f ≤ 2100 MHz		18	20.5	-	dBm
		2100 MHz ≤ f ≤ 2750 MHz		17.5	20	-	dBm

[1] Absolute maximum DC voltage on pin RF_OUT and V_{DD}.

[2] Δf = 1 MHz; P_i = −12 dBm per tone.

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2. Pinning information

2.1 Pinning

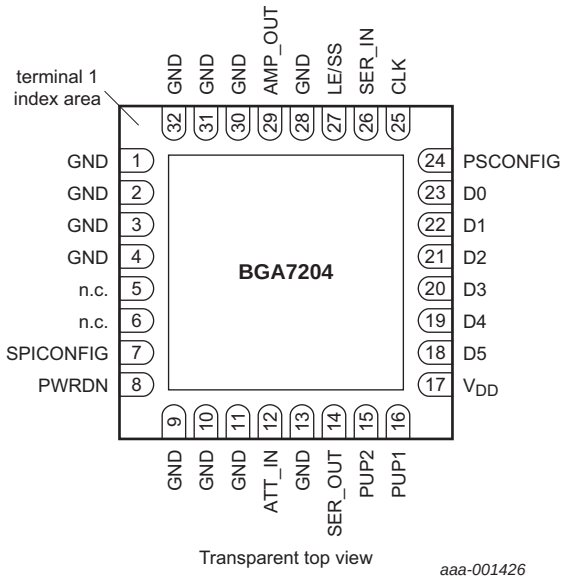

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	1, 2, 3, 4, 9, 10, 11, 13, 28, 30, 31, 32	Ground
n.c.	5, 6	not connected
SPICONFIG	7	set SPI mode [1]
PWRDN	8	power-down RF section [2]
ATT_IN	12	RF input to attenuator
SER_OUT	14	SPI data output
PUP2	15	power-up control 2
PUP1	16	power-up control 1
V_{DD}	17	supply voltage
D5	18	attenuation control word [3]
D4	19	attenuation control word [3]
D3	20	attenuation control word [3]
D2	21	attenuation control word [3]
D1	22	attenuation control word [3]
D0	23	attenuation control word [3]
PSCONFIG	24	set digital gain control mode [4]
CLK	25	SPI clock input

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Table 2. Pin description *...continued*

Symbol	Pin	Description
SER_IN	26	SPI data input
LE/SS	27	latch enable or slave select [5]
AMP_OUT	29	RF output of amplifier
GND	GND paddle	exposed die pad

[1] 0 = extended; 1 = basic; unconnected pulled up.

[2] 0 = enabled; 1 = disabled; unconnected pulled down.

[3] D5 = MSB; D0 = LSB; unconnected pulled down.

[4] 0 = parallel; 1 = SPI; unconnected pulled down.

[5] parallel = LE; SPI = SS (active LOW); unconnected pulled up.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BGA7204	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

4. Marking

Table 4. Marking

Type number	Marking code	Description
BGA7204	7204	
	*****	manufacturing code
	TSDyww	yww = The actual assembly date code.

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5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{SUP}	supply voltage		[1]	−0.6	+8	V
V_I	input voltage		[2]	−0.6	+8	V
V_O	output voltage		[3]	−0.6	+8	V
I_I	input current		[4]	−20	+20	mA
I_O	output current		[5]	−20	+20	mA
T_{stg}	storage temperature			−65	+150	°C
T_j	junction temperature			-	150	°C
$P_{i(RF)(ATT_IN)}$	RF input power on pin ATT_IN			-	30	dBm
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM); According JEDEC standard 22-A114E		-	4	kV
		Charged Device Model (CDM); According JEDEC standard 22-C101B		-	2	kV

[1] Absolute maximum DC voltage on pin RF_OUT and V_{DD}.

[2] Absolute maximum DC voltage on pin SPICONFIG, PWRDN, D5, D4, D3, D2, D1, D0, PSCONFIG, CLK, SER_IN and LE/SS.

[3] Absolute maximum DC voltage on pin SER_OUT.

[4] Absolute maximum DC current through pin SPICONFIG, PWRDN, D5, D4, D3, D2, D1, D0, PSCONFIG, CLK, SER_IN and LE/SS.

[5] Absolute maximum DC current through pin SER_OUT.

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	$T_{sp} \leq 85$ °C	[1]	10	K/W

[1] T_{sp} is the temperature at the solder point.

7. Static characteristics

Table 7. Static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{SUP}	supply voltage		[1]	4.75	5.0	5.25	V
$I_{CC(tot)}$	total supply current	PWRDN = 0		-	115	133	mA
		PWRDN = 1		-	15	-	mA
T_{amb}	ambient temperature			−40	+25	+85	°C
I_{DD}	supply current	on pin V_{DD}					
		PWRDN = 0		-	43	-	mA
		PWRDN = 1		-	15	-	mA
		on pin AMP_OUT					
		PWRDN = 0		-	72	-	mA
		PWRDN = 1		-	0.05	-	mA

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Table 7. Static characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage		[2]	−0.1	0	+0.8	V
V_{IH}	HIGH-level input voltage		[2]	2	3.3	V_{SUP} + 0.1	V
V_{OL}	LOW-level output voltage		[3]	−0.1	0	+0.8	V
V_{OH}	HIGH-level output voltage		[3]	2.5	3.3	3.4	V
I_{OL}	LOW-level output current		[3]	−4	-	-	mA
I_{OH}	HIGH-level output current		[3]	-	-	4	mA

[1] Supply voltage on pin RF_OUT and V_{DD}.

[2] Digital input pins are: SPICONFIG, PWRDN, PUP2, PUP1, D5, D4, D3, D2, D1, D0, PSCONFIG, CLK, SER_IN and LE/SS.

[3] Digital output pins are: SER_OUT.

8. Dynamic characteristics

Table 8. Dynamic characteristics

4.75 V ≤ V_{SUP} ≤ 5.25 V; f = 400 MHz to 2750 MHz; −40 °C ≤ T_{amb} ≤ +85 °C; input and output are terminated with 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_p	power gain	minimum attenuation					
		400 MHz ≤ f ≤ 1450 MHz		16	18.5	21	dB
		1450 MHz ≤ f ≤ 2100 MHz		15	17.5	20	dB
		2100 MHz ≤ f ≤ 2750 MHz		14	16.5	19	dB
α_{range}	attenuation range	400 MHz ≤ f ≤ 1450 MHz		29	31.5	34	dB
		1450 MHz ≤ f ≤ 2100 MHz		28	30.5	33	dB
		2100 MHz ≤ f ≤ 2750 MHz		27	30.0	33	dB
α_{step}	attenuation step			0	0.5	1	dB
ΔG_p	power gain variation		[1]	−2.0	-	+2.0	dB
$G_{p(flat)}$	power gain flatness	minimum attenuation; per 100 MHz		-	-	0.4	dB
RL_{in}	input return loss	400 MHz ≤ f ≤ 2750 MHz		10	-	-	dB
RL_{out}	output return loss	400 MHz ≤ f ≤ 2750 MHz		8	-	-	dB
NF	noise figure	minimum attenuation					
		400 MHz ≤ f ≤ 700 MHz		-	7	9.5	dB
		700 MHz ≤ f ≤ 2100 MHz		-	6.5	9	dB
		2100 MHz ≤ f ≤ 2750 MHz		-	7.0	10	dB
$IP3_O$	output third-order intercept point	minimum attenuation					
		400 MHz ≤ f ≤ 700 MHz	[2]	34	38	-	dBm
		700 MHz ≤ f ≤ 1450 MHz	[2]	33	37.5	-	dBm
		1450 MHz ≤ f ≤ 2100 MHz	[2]	31	36	-	dBm
		2100 MHz ≤ f ≤ 2750 MHz	[2]	28.5	34	-	dBm

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Table 8. Dynamic characteristics *...continued*

4.75 V ≤ V_{SUP} ≤ 5.25 V; f = 400 MHz to 2750 MHz; −40 °C ≤ T_{amb} ≤ +85 °C; input and output are terminated with 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(1dB)}$	output power at 1 dB gain compression	minimum attenuation				
		400 MHz ≤ f ≤ 1450 MHz	19	21	-	dBm
		1450 MHz ≤ f ≤ 2100 MHz	18	20.5	-	dBm
		2100 MHz ≤ f ≤ 2750 MHz	17.5	20	-	dBm

[1] Normalized to maximum gain and attenuation; see Figure 2.

[2] Δf = 1 MHz; P_i = −12 dBm per tone.

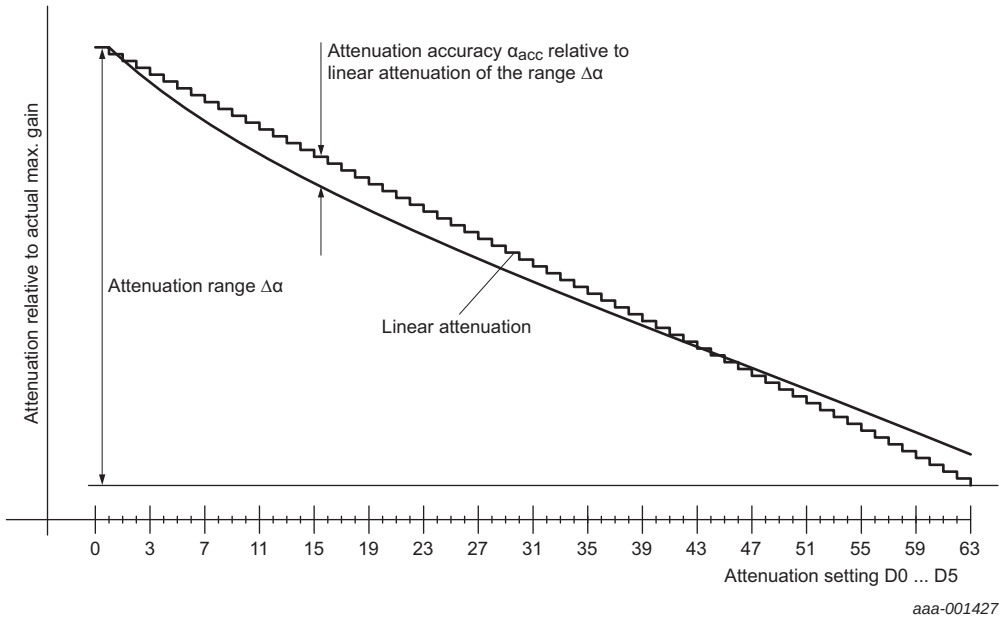

Fig 2. Attenuation accuracy definitions

9. Interface timing characteristics

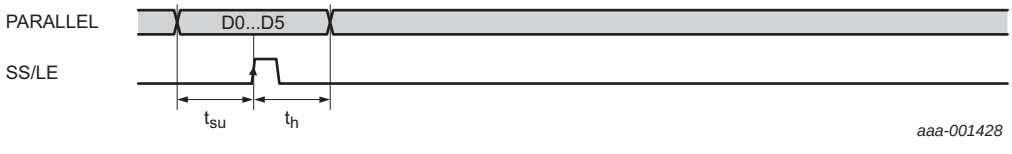

Fig 3. Timing diagram latched parallel mode

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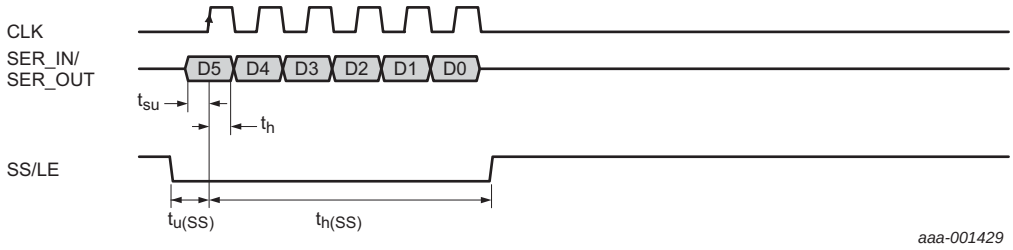

Fig 4. Timing basic SPI mode

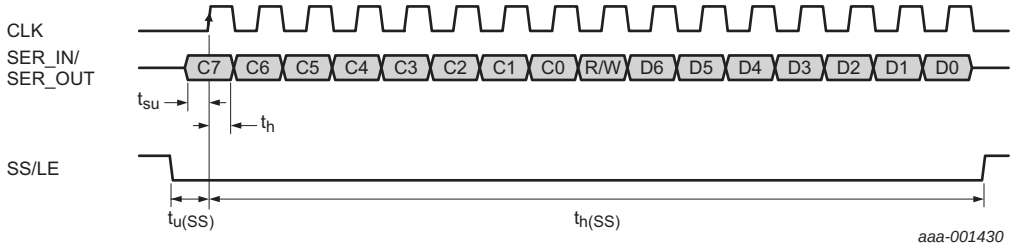

Fig 5. Timing extended SPI mode

Table 9. Interface timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SPI}	SPI frequency		-	-	10	MHz
$f_{intf(par)}$	parallel interface frequency		-	-	2	MHz
t_{su}	set-up time		-	10	-	ns
t_h	hold time		-	10	-	ns
$t_{su(SS)}$	set-up time on pin SS		-	10	-	ns
$t_{h(SS)}$	hold time on pin SS		-	0	-	ns

10. Control modes

10.1 Interface operating principles

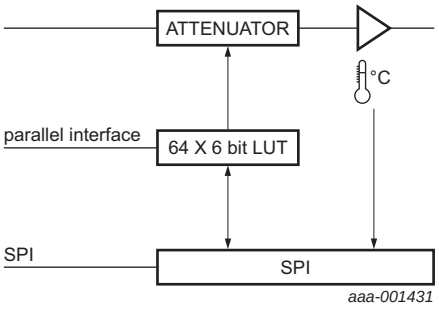

Fig 6. Interface operating principles

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Table 10. Control modes, control options and features

Control pin configuration	Parallel	Basic SPI	Extended SPI
PSCONFIG (pin 24)	0	1	1
SPICONFIG (pin 7)	don't care	1	0
Control features	**Parallel**	**Basic SPI**	**Extended SPI**
6 bits digital control	Yes	Yes	Yes
programmable attenuation curve	No [1]	No [1]	Yes
junction temperature read out	No	No	Yes
enable over-temperature protection	No	No	Yes
disable attenuator block	No	No	Yes
disable amplifier block	No	No	Yes
chip type read-out	No	No	Yes
chip version read-out	No	No	Yes
reset	No	No	Yes
daisy chaining multiple VGA's	No	Yes	No

[1] One could however switch to the SPI extended mode, reprogram the attenuation curve and switch back to the digital parallel or SPI basic control mode.

10.2 Attenuation truth table

Table 11. Attenuation control truth table

Factory setting of look-up table; major states only.

Attenuation control word						Typical attenuation at 700 MHz
D5	D4	D3	D2	D1	D0	
16 dB	8 dB	4 dB	2 dB	1 dB	0.5 dB	
1	1	1	1	1	1	0 dB
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB

10.3 Parallel control mode

The parallel input is connected internally to a latch. If LE/SS (pin 27) is logical HIGH the attenuation control word D5 to D0 is transferred to the attenuator register and the attenuator assumes the new attenuation setting. Upon a negative edge of LE/SS (pin 27) the actual attenuation control word will be hold: any changes in the control word at the parallel interface will be ignored. The timing is depicted in Figure 7.

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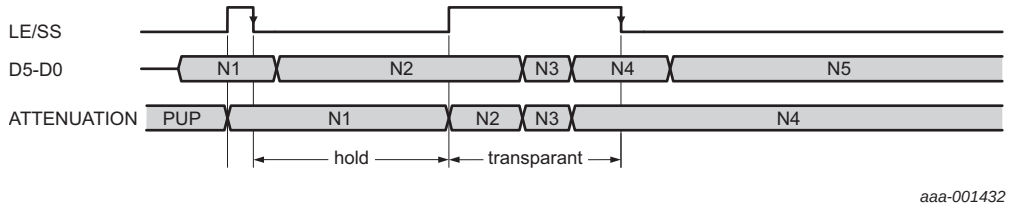

Fig 7. Timing diagram in parallel mode

LE/SS (pin 27) is provided with an internal pull-up resistor and can be left unconnected.

10.4 Basic SPI mode

In the Basic SPI mode the attenuator register is loaded via the SPI interface.

Table 12. SPI commands for basic mode: PSCONFIG (pin 24) = 1; SPICONFIG (pin 7) = 1

Control word [1]	D5	D4	D3	D2	D1	D0
Default attenuation	16 dB	8 dB	4 dB	2 dB	1 dB	0.5 dB

[1] D5 to D0 (bit 5 to 0) form the attenuation selecting word (address of the look-up table).

Figure 4 depicts the timing diagram of SPI data format in the basic SPI mode. The data is clocked into a 6-bit shift register. This mode also allows daisy chaining of multiple chips. Figure 8 shows a configuration of two VGAs in daisy chain. Data word D5 to D0 is stored in Attenuator 1, while data word E5 to E0 is stored in Attenuator 0. On the rising edge of LE/SS (pin 27), the data is captured and stored in the attenuator register. At the same moment the stored words become active on the attenuator outputs.

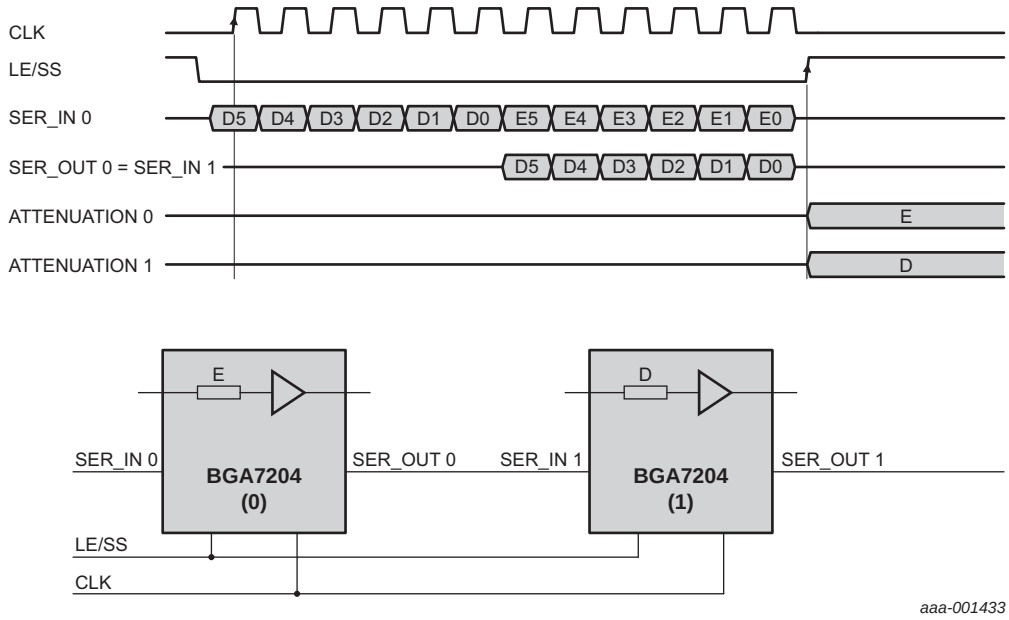

Fig 8. Timing diagram of SPI in basic mode

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10.5 Extended SPI mode

Table 13. SPI commands for extended mode: PSCONFIG (pin 24) = 1; SPICONFIG (pin 7) = 0

Bit 7 is used to indicate whether it is a read operation (bit 7 = 1) or a write operation (bit 7 = 0). In case of a read operation the logic state of bits 0 to 6 don't care for the data from the master to the slave. The bits are updated by the slave.

	Command									Data							Reset value
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Attenuation [1]	0	0	0	0	0	0	0	0	rw	0	D5	D4	D3	D2	D1	D0	0x00
Temperature status [2]	0	0	0	1	0	0	0	0	1	0	0	0	D3	D2	D1	D0	0x8-
Temperature configuration [3]	0	0	0	1	0	0	0	1	rw	RF	PG	MG	D3	D2	D1	D0	0x00
Enable [4]	0	1	0	1	0	0	0	0	rw	0	0	0	0	AT	AM	TS	0x3F
Program LUT / attenuation curve [5]	1	0	C5	C4	C3	C2	C1	C0	rw	0	D5	D4	D3	D2	D1	D0	N/A
Chip type [6]	1	1	1	1	0	0	0	0	1	0	0	0	0	1	0	0	0x84

[1] D0 to D5 (bit 5 to 0) forms the attenuation selecting word (address of the look-up table).

[2] D3 to D0 (bit 3 to 0) forms the temperature read out word.

[3] D3 to D0 (bit 3 to 0) forms the temperature threshold for the temperature protection. Next to the temperature, RF, PG or MG is selected (mutual exclusive). In case RF is selected the RF part of the chip will switch off if the threshold is exceeded. If PG is selected the attenuator will switch to the attenuation gain that is configured with the PUPn pins if the threshold is exceeded. If MG is selected the attenuation gain will drop to a minimum value if the threshold is exceeded.

[4] TS (bit 0) enables the temperature sensor, AM (bit 1) enables the amplifier and AT (bit 2) enables the attenuator.

[5] D5 to D0 (bit 5 to 0) forms the attenuation control word to be programmed at address C5 to C0 (bit 13 to 8). After reset the curve is linear: D5 to D0 = C5 to C0 for all attenuation states.

[6] Returns 04: 4 bits for third digit (0000 = 0) and 4 bits for the last digit (0010 = 2) of the chip type.

Figure 9 depicts the timing diagram of SPI data write format in extended mode. The first 8 bits indicate the command. The first data bit indicates if it is a read or write action. In case of a read action, the data bits on pin SER_OUT (pin 14) are replaced with the read value.

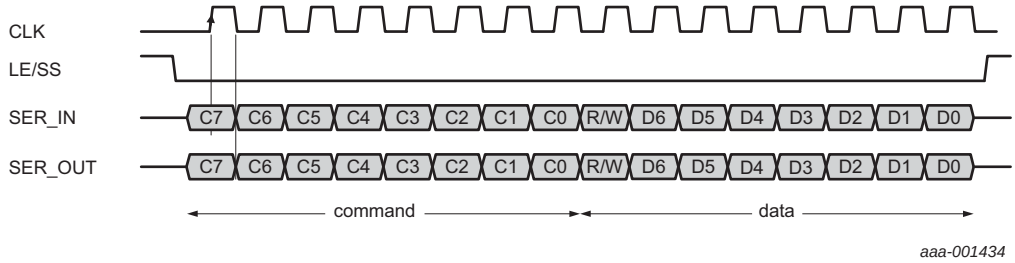

Fig 9. Timing diagram of SPI in extended mode

10.6 Temperature sensor

In the extended SPI mode the temperature sensor can be read out. The temperature sensor is located close to the amplifier junctions. The temperature coding is listed in Table 14.

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Table 14. Temperature ranges

The overlap between ranges reflects the inaccuracy of the temperature sensor.

T_j (°C)	D3	D2	D1	D0
< −15	0	0	0	0
−35 to +5	0	0	0	1
−15 to +35	0	0	1	0
15 to 80	0	0	1	1
60 to 110	0	1	0	0
90 to 130	0	1	0	1
110 to 140	0	1	1	0
120 to 150	0	1	1	1
130 to 160	1	0	0	0
> 140	1	0	0	1

10.7 Power-up states

The VGA is provided with power-up program pins. These pins configure the attenuation after start-up (see Table 15) depending on how LE/SS (pin 27) and PSCONFIG (pin 24) are configured at start-up (see Table 16).

Table 15. Power-up configuration

PUP2 (pin 15)	PUP1 (pin 16)	Attenuator gain at 700 MHz
0	0	−31.5 dB
0	1	−24 dB
1	0	−16 dB
1	1	0 dB

Table 16. Power-up states

LE/SS (pin 27)	PSCONFIG (pin 24)	Power up state defined by
0	don't care	power-up program pins (PUP2 and PUP1) [1]
1	0	D5 to D0 (bit 5 to 0)
1	1	power-up program pins (PUP2 and PUP1) [1]

[1] See Table 15.

The attenuation gain remains valid until it is updated with the parallel interface or SPI interface.

10.8 Power-on sequence

Digital inputs (SPICONFIG, PWRDN, PUP2, PUP1, D5, D4, D3, D2, D1, D0, PSCONFIG and LE/SS) should be powered simultaneously or after V_{DD} and GND are powered (see also Table 5). This prevents damage to the ESD protection diodes of the digital input. If the digital inputs need to be powered before V_{DD} is powered measures should be taken to limit the current to 20 mA, e.g. by means of an external resistor.

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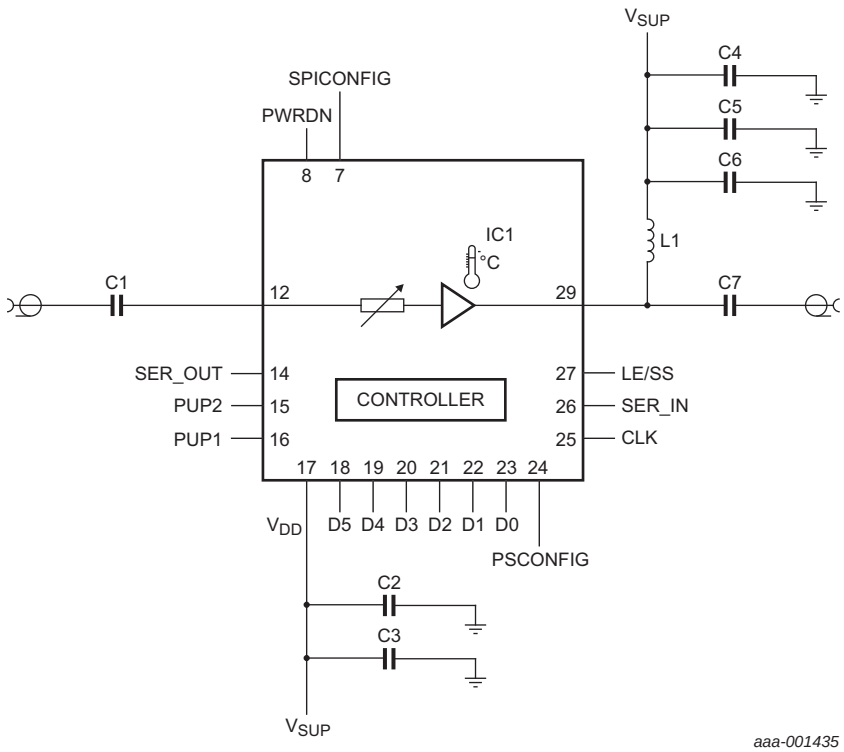
11. Application information

11.1 Application board

A customer application board is available from NXP upon request. It includes USB interface circuitry and customer software to facilitate evaluation of the BGA7204.

The final application shall be decoupled as depicted in Figure 10. The ground leads and exposed paddle should be connected directly to the ground plane. Enough via holes should be provided to connect the top and bottom ground planes in the final application board. Sufficient cooling should be provided that the temperature of the exposed die pad does not exceed 85 °C.



See Table 17 for list of components.

Fig 10. Customer evaluation board

Table 17. List of components

See Figure 10 for schematics.

Component	Description	Value	Supplier
C1	capacitor	100 pF	various
C2	capacitor	330 nF	various
C3	capacitor	100 pF	various
C4	capacitor	100 nF	various
C5	capacitor	100 pF	various
C6	capacitor	4.7 μF	various

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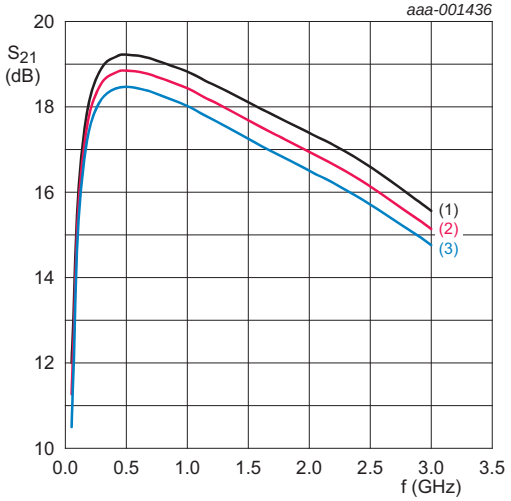
Table 17. List of components *…continued*

See Figure 10 for schematics.

Component	Description	Value	Supplier
C7	capacitor	100 pF	various
IC1	BGA7204		NXP
L1	choke	47 nH	

11.2 Characteristics



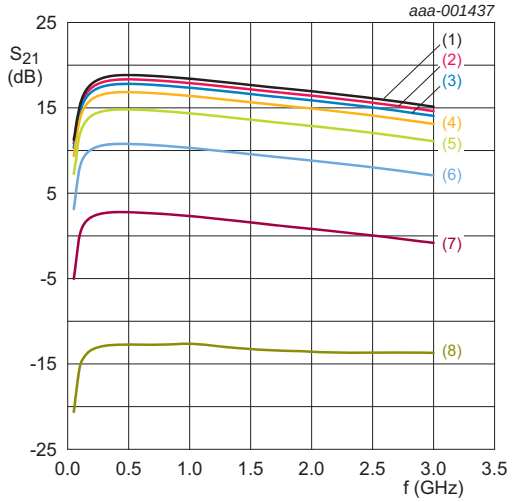
V_{SUP} = 5 V.

(1) T_{amb} = −40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 11. Maximum power gain as a function of frequency; typical values



V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) attenuation = 63 (0x3F, minimum)

(2) attenuation = 62 (0x3E)

(3) attenuation = 61 (0x3D)

(4) attenuation = 59 (0x3B)

(5) attenuation = 55 (0x37)

(6) attenuation = 47 (0x2F)

(7) attenuation = 31 (0x1F)

(8) attenuation = 00 (0x00, maximum)

Fig 12. Power gain as a function of frequency; typical values

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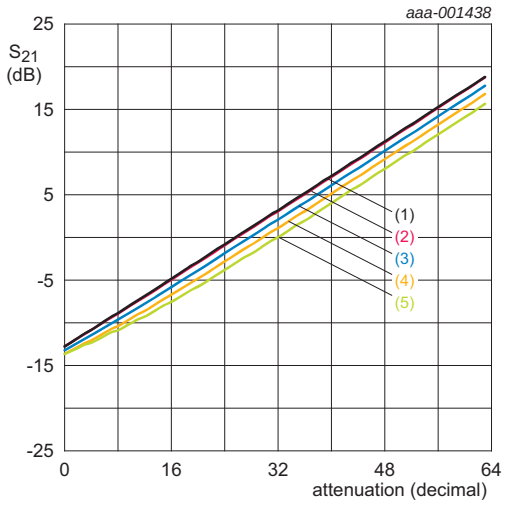


V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) f = 0.4 GHz

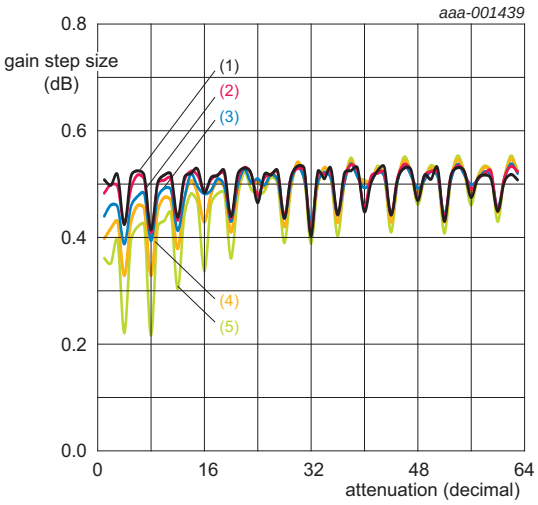
(2) f = 0.7 GHz

(3) f = 1.45 GHz

(4) f = 2.10 GHz

(5) f = 2.75 GHz

Fig 13. Power gain as a function of attenuation state (63 = minimum attenuation); typical values



V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) f = 0.4 GHz

(2) f = 0.7 GHz

(3) f = 1.45 GHz

(4) f = 2.10 GHz

(5) f = 2.75 GHz

Fig 14. Gain step size as a function of attenuation state (63 = minimum attenuation); typical values

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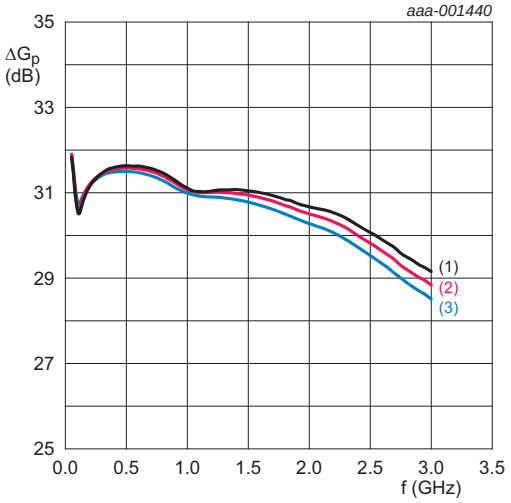


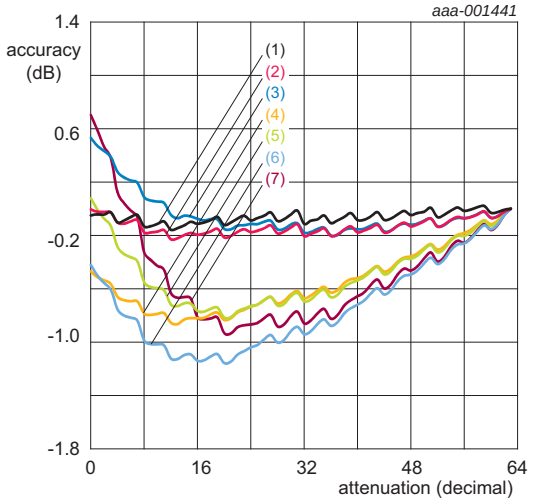
V_{SUP} = 5 V.

(1) T_{amb} = −40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 15. Power gain range as a function of frequency; typical values



V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) f = 0.4 GHz; α_{range} = 31.5 dB

(2) f = 0.7 GHz; α_{range} = 31.5 dB

(3) f = 1.45 GHz; α_{range} = 31.5 dB

(4) f = 1.45 GHz; α_{range} = 30.5 dB

(5) f = 2.10 GHz; α_{range} = 30.5 dB

(6) f = 2.10 GHz; α_{range} = 30.0 dB

(7) f = 2.75 GHz; α_{range} = 30.5 dB

Fig 16. Relative power gain accuracy as a function of attenuation state (63 = minimum attenuation); typical values

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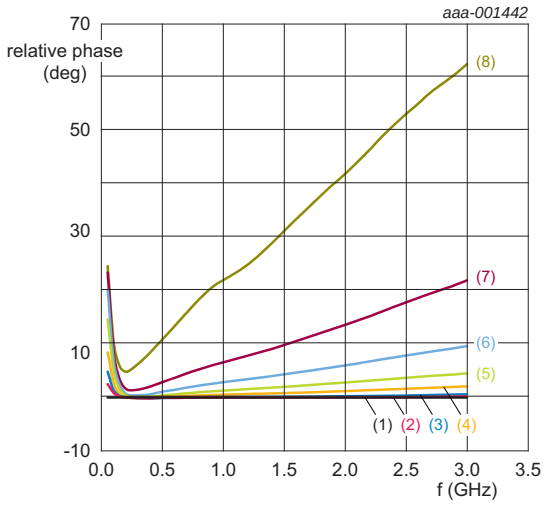
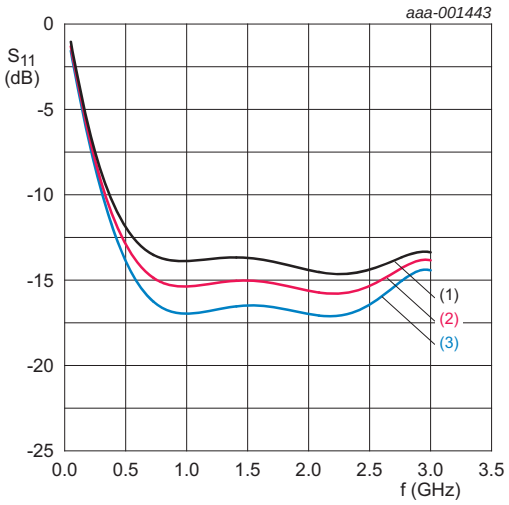


V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) attenuation = 63 (0x3F, minimum)
(2) attenuation = 62 (0x3E)
(3) attenuation = 61 (0x3D)
(4) attenuation = 59 (0x3B)
(5) attenuation = 55 (0x37)
(6) attenuation = 47 (0x2F)
(7) attenuation = 31 (0x1F)
(8) attenuation = 00 (0x00, maximum)

Fig 17. Relative phase as a function of frequency; typical values



V_{SUP} = 5 V; minimum attenuation.

(1) T_{amb} = −40 °C
(2) T_{amb} = +25 °C
(3) T_{amb} = +85 °C

Fig 18. Input return loss as a function of frequency; typical values

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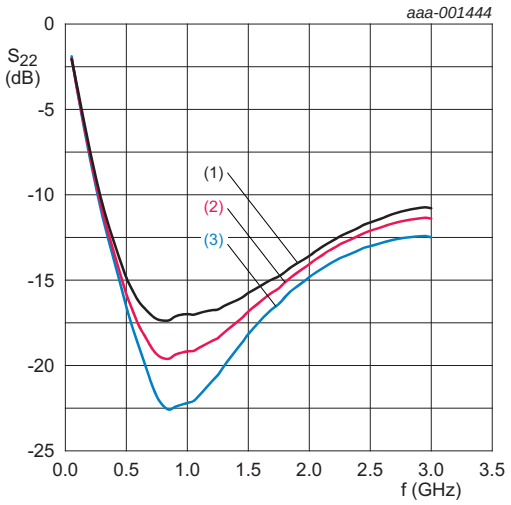


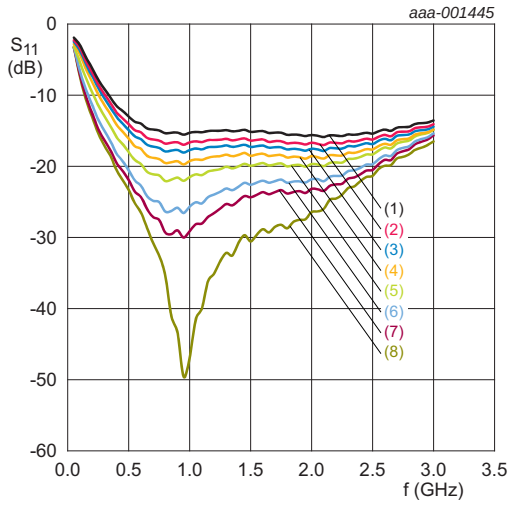
V_{SUP} = 5 V; minimum attenuation.

(1) T_{amb} = −40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 19. Output return loss as a function of frequency; typical values



V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) attenuation = 63 (0x3F, minimum)

(2) attenuation = 62 (0x3E)

(3) attenuation = 61 (0x3D)

(4) attenuation = 59 (0x3B)

(5) attenuation = 55 (0x37)

(6) attenuation = 47 (0x2F)

(7) attenuation = 31 (0x1F)

(8) attenuation = 00 (0x00, maximum)

Fig 20. Input return loss as a function of frequency; typical values

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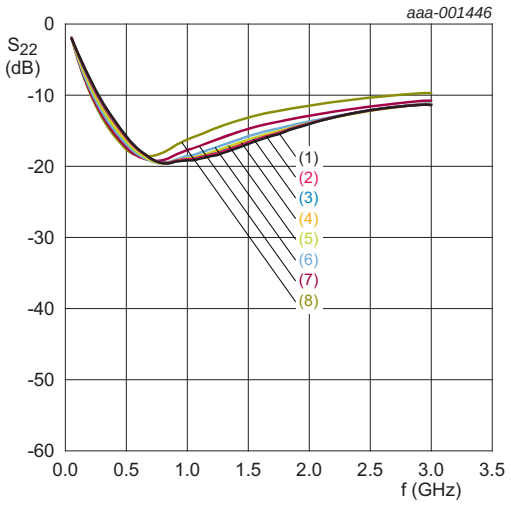
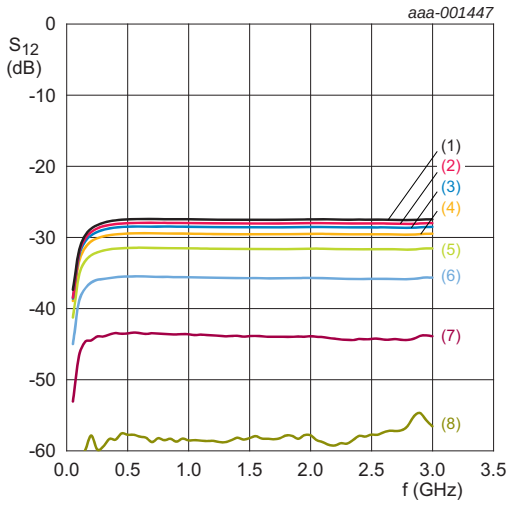


V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) attenuation = 63 (0x3F, minimum)
(2) attenuation = 62 (0x3E)
(3) attenuation = 61 (0x3D)
(4) attenuation = 59 (0x3B)
(5) attenuation = 55 (0x37)
(6) attenuation = 47 (0x2F)
(7) attenuation = 31 (0x1F)
(8) attenuation = 00 (0x00, maximum)

Fig 21. Output return loss as a function of frequency; typical values



V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) attenuation = 63 (0x3F, minimum)
(2) attenuation = 62 (0x3E)
(3) attenuation = 61 (0x3D)
(4) attenuation = 59 (0x3B)
(5) attenuation = 55 (0x37)
(6) attenuation = 47 (0x2F)
(7) attenuation = 31 (0x1F)
(8) attenuation = 00 (0x00, maximum)

Fig 22. Isolation as a function of frequency; typical values

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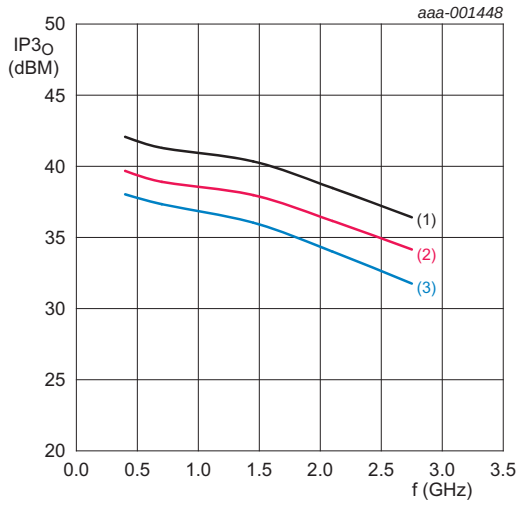


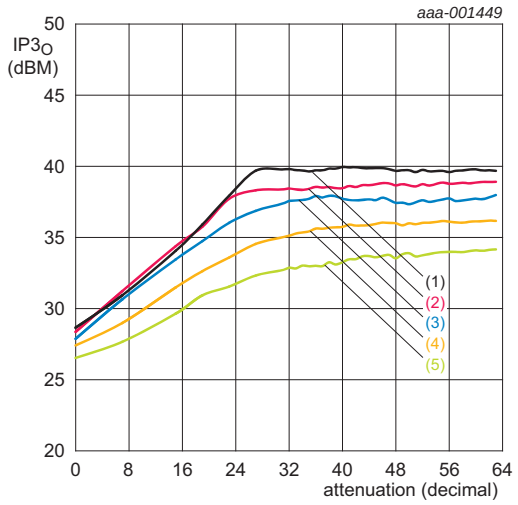
V_{SUP} = 5 V; minimum attenuation.

(1) T_{amb} = −40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 23. Output third-order intercept point as a function of frequency; typical values



V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) f = 0.4 GHz

(2) f = 0.7 GHz

(3) f = 1.45 GHz

(4) f = 2.10 GHz

(5) f = 2.75 GHz

Fig 24. Output third-order intercept point as a function of attenuation state (63 = minimum attenuation); typical values

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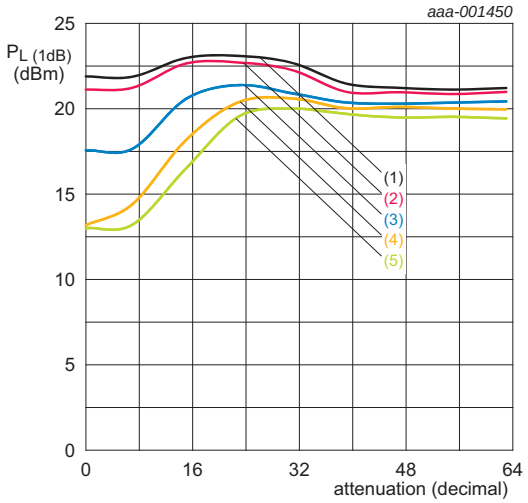

V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) f = 0.4 GHz

(2) f = 0.7 GHz

(3) f = 1.45 GHz

(4) f = 2.10 GHz

(5) f = 2.75 GHz

Fig 25. Output power at 1 dB gain compression as a function of attenuation state (63 = minimum attenuation); typical values

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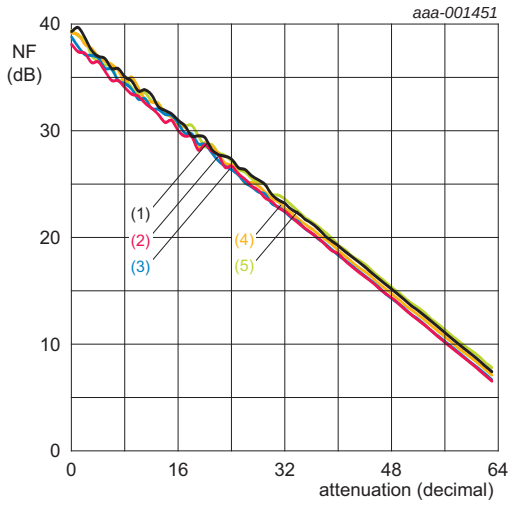


V_{SUP} = 5 V; T_{amb} = 25 °C.

(1) f = 0.4 GHz

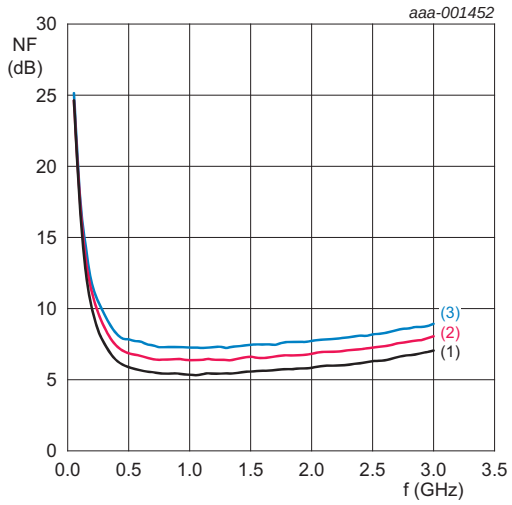
(2) f = 0.7 GHz

(3) f = 1.45 GHz

(4) f = 2.10 GHz

(5) f = 2.75 GHz

Fig 26. Noise figure as a function of attenuation state (63 = minimum attenuation); typical values



V_{SUP} = 5 V; minimum attenuation.

(1) T_{amb} = −40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 27. Noise figure as a function of frequency; typical values

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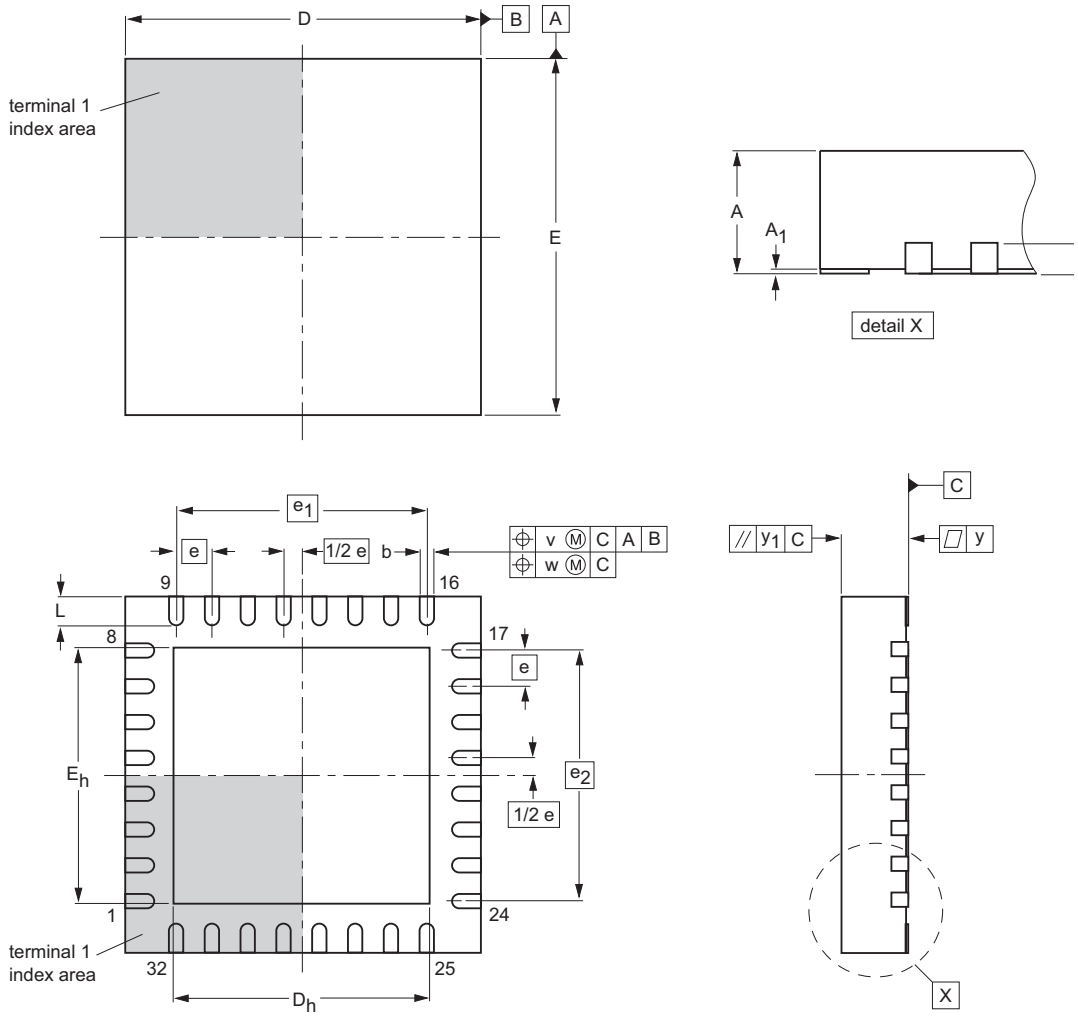
12. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



Dimensions

Unit(1)		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	max		0.05	0.30		5.1	3.75	5.1	3.75				0.5				
	nom	0.85			0.2					0.5	3.5	3.5		0.1	0.05	0.05	0.1
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-3		MO-220				~~11-06-14~~ 11-06-21

Fig 28. Package outline SOT617-3 (HVQFN32)

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13. Packing information

The BGA7204 will be delivered in reel pack SMD 7”, 1500 pieces per reel.

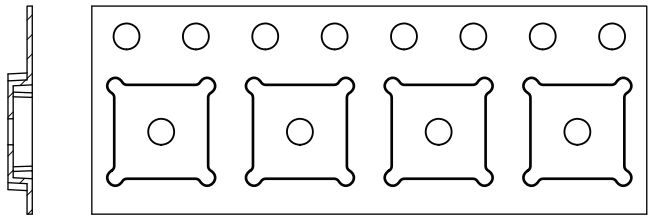

Fig 29. Carrier tape

14. Abbreviations

Table 18. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
IF	Intermediate Frequency
LSB	Least Significant Bit
LUT	Look-Up Table
MMIC	Monolithic Microwave Integrated Circuit
MSB	Most Significant Bit
RF	Radio Frequency
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
WiMAX	Worldwide Interoperability for Microwave Access

15. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGA7204 v.4	20161115	Product data sheet		BGA7204 v.3
Modifications:	• Table 4 on page 4: Marking code has been changed from TSS to TSD.			
BGA7204 v.3	20130128	Product data sheet	-	BGA7204 v.2
Modifications:	• Section 1.2 on page 1: moisture sensitivity level 2 has been changed to 1.			
BGA7204 v.2	20120118	Product data sheet	-	BGA7204 v.1
BGA7204 v.1	20120105	Product data sheet	-	-

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16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 15 November 2016
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