



ON Semiconductor®

FDS4685

40V P-Channel PowerTrench® MOSFET

Features

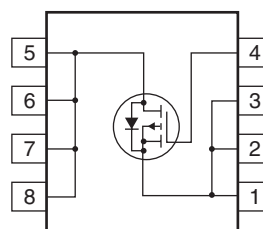
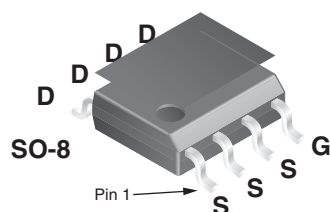
- -8.2 A , -40 V $R_{DS(ON)} = 0.027\ \Omega$ @ $V_{GS} = -10\text{ V}$
 $R_{DS(ON)} = 0.035\ \Omega$ @ $V_{GS} = -4.5\text{ V}$
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

Applications

- Power management
- Load switch
- Battery protection

General Description

This P-Channel MOSFET is a rugged gate version of ON Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings ($4.5\text{ V} - 20\text{ V}$).



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		−40	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Drain Current - Continuous			

Package Marking and Ordering Information

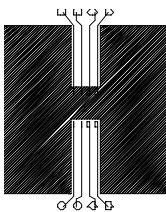
Device Marking	Device	Reel Size	Tape width	Quantity
FDS4685	FDS4685	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

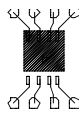
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = −250 μA	−40			V
ΔBV _{DSS} ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = −250 μA, Referenced to 25°C		−32		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = −32 V, V _{GS} = 0 V			−1	μA
I _{GSS}	Gate–Body Leakage	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = −250 μA	−1	−1.6	−3	V
ΔV _{GS(th)} ΔT _J	Gate Threshold Voltage Temperature Coefficient	I _D = −250 μA, Referenced to 25°C		4.7		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = −10 V, I _D = −8.2 A V _{GS} = −4.5 V, I _D = −7 A V _{GS} = −10 V, I _D = −8.2 A, T _J = 125°C		22 29 31	27 35 42	mΩ
g _{FS}	Forward Transconductance	V _{DS} = −5 V, I _D = −8.2 A		22		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = −20 V, V _{GS} = 0 V, f = 1.0 MHz		1872		pF
C _{oss}	Output Capacitance			256		pF
C _{rss}	Reverse Transfer Capacitance			134		pF
R _G	Gate Resistance	V _{GS} = 15 mV, f = 1MHz		4		Ω
Switching Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	V _{DD} = −20 V, I _D = −1 A, V _{GS} = −10 V, R _{GEN} = 6 Ω		14	25	ns
t _r	Turn–On Rise Time			11	20	ns
t _{d(off)}	Turn–Off Delay Time			50	80	ns
t _f	Turn–Off Fall Time			18	32	ns
Q _g	Total Gate Charge	V _{DS} = −20 V, I _D = −8.2 A, V _{GS} = −5 V		19	27	nC
Q _{gs}	Gate–Source Charge			5.6		nC
Q _{gd}	Gate–Drain Charge			6.1		nC
Drain–Source Diode Characteristics						
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = −2.1 A (Note 2)		−0.7	−1.2	V
t _{rr}	Diode Reverse Recovery Time	I _F = −8.2 A,		26		nS
Q _{rr}	Diode Reverse Recovery Charge	dI _F /d _t = 100 A/μs		15		nC

Notes:

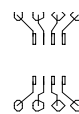
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $50^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $105^\circ\text{C}/\text{W}$ when mounted on a $.04\text{ in}^2$ pad of 2 oz copper



c) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics:

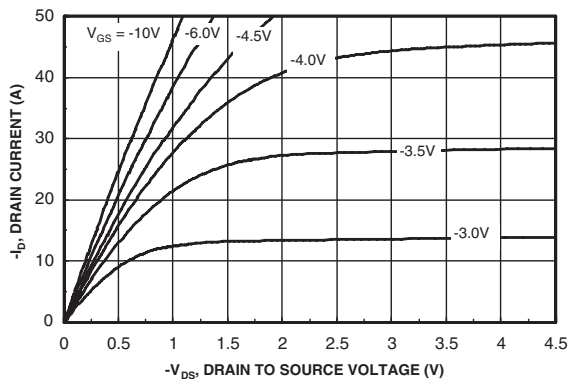


Figure 1. On-Region Characteristics.

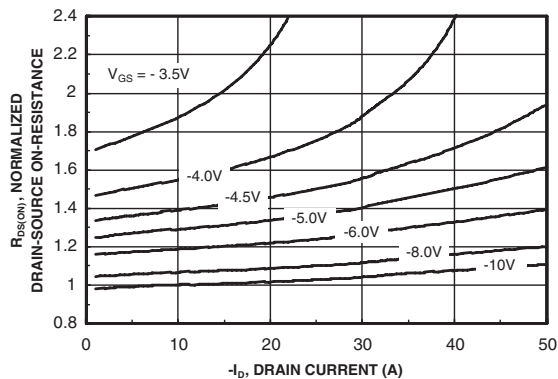


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

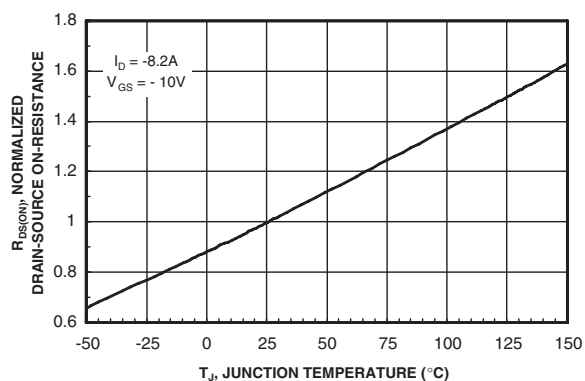


Figure 3. On-Resistance Variation with Temperature.

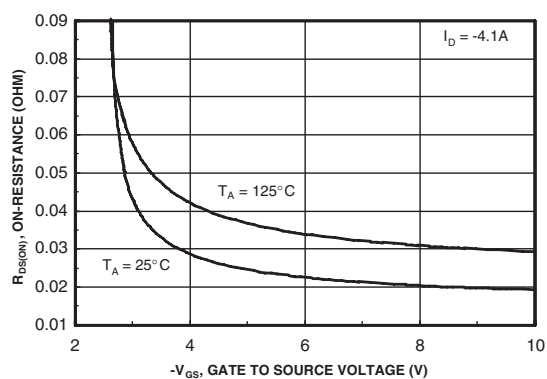


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

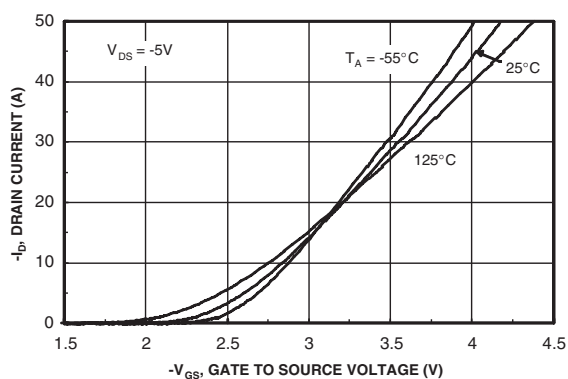


Figure 5. Transfer Characteristics.

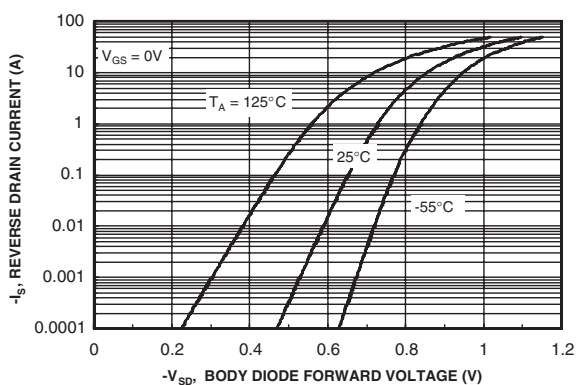


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics:

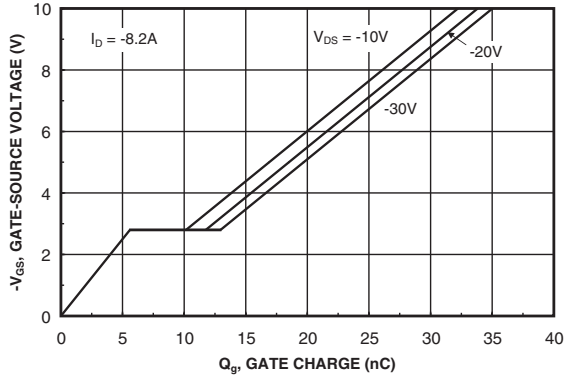


Figure 7. Gate Charge Characteristics.

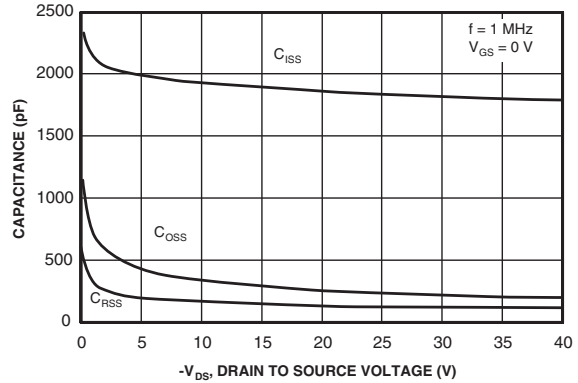


Figure 8. Capacitance Characteristics.

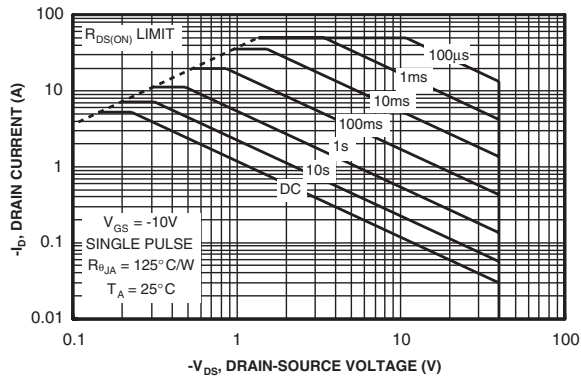


Figure 9. Maximum Safe Operating Area.

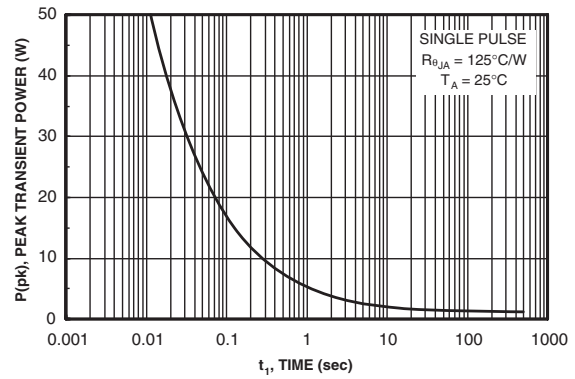


Figure 10. Single Pulse Maximum Power Dissipation.

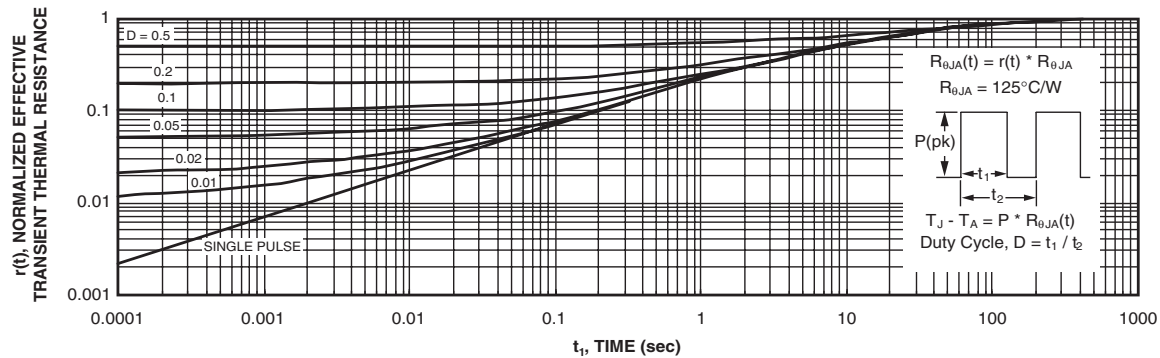


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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