# Single Supply, 24-Bit, Sigma-Delta ADC with ±10 V and 0 mA to 20 mA Inputs

Data Sheet **AD4112**

## FEATURES

- Tested for robustness per: IEC61000-4-2, IEC61000-4-3, IEC61000-4-4, IEC61000-4-5, IEC61000-4-6, CISPR 11
- 24-bit ADC with integrated analog front end
  - Fast and flexible output rate: 1.25 SPS to 31.25 kSPS
  - Channel scan data rate of 6.21 kSPS per channel (161 µs settling)
  - 16 noise free bits at 1 kSPS per channel
  - 85 dB rejection of 50 Hz and 60 Hz at 20 SPS per channel
- ±10 V inputs, 4 differential or 8 single-ended
  - Pin absolute maximum rating ±50 V
  - Overrange up to ±20 V
  - ≥1 MΩ impedance
  - ±0.06% accuracy at 25°C
- 0 mA to 20 mA inputs, 4 single-ended
  - Pin absolute maximum rating ±50 mA
  - Overrange from −0.5 mA to +24 mA
  - 60 Ω impedance
  - ±0.08% accuracy at 25°C
- On-chip 2.5 V reference
  - ±0.12% accuracy at 25°C, ±5 ppm/°C (typical) drift
- Internal or external clock
- Power supplies
  - AVDD = 3.0 V to 5.5 V
  - IOVDD = 2 V to 5.5 V
  - Total IDD = 3.9 mA
- Temperature range: −40°C to +105°C
- 3-wire or 4-wire serial digital interface (Schmitt trigger on SCLK)
  - SPI, QSPI, MICROWIRE, and DSP compatible

## APPLICATIONS

- Process control
  - PLC and DCS modules
  - Instrumentation and measurement

## GENERAL DESCRIPTION

The AD4112 is a low power, low noise, 24-bit, sigma-delta (Σ-Δ) analog-to-digital converter (ADC) that integrates an analog front end (AFE) for fully differential or single-ended, high impedance (≥1 MΩ) bipolar, ±10 V voltage inputs, and 0 mA to 20 mA current inputs.

The AD4112 also integrates key analog and digital signal conditioning blocks to configure eight individual setups for each analog input channel in use. The AD4112 features a maximum channel scan rate of 6.21 kSPS (161 µs) for fully settled data.

The embedded 2.5 V, low drift (5 ppm/°C), band gap internal reference (with output reference buffer) reduces the external component count.

The digital filter allows flexible settings, including simultaneous 50 Hz and 60 Hz rejection at a 27.27 SPS output data rate. The user can select between the different filter settings depending on the demands of each channel in the application. The automatic channel sequencer enables the ADC to switch through each enabled channel.

The precision performance of the AD4112 is achieved by integrating the proprietary *i*Passives™ technology from Analog Devices, Inc. The AD4112 is factory calibrated to achieve a high degree of specified accuracy.

The AD4112 operates with a single power supply, making it easy to use in galvanically isolated applications. The specified operating temperature range is −40°C to +105°C. The AD4112 is housed in a 40-lead, 6 mm × 6 mm LFCSP package.

Rev. A


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**8/2018—Revision 0: Initial Version**

# FUNCTIONAL BLOCK DIAGRAM

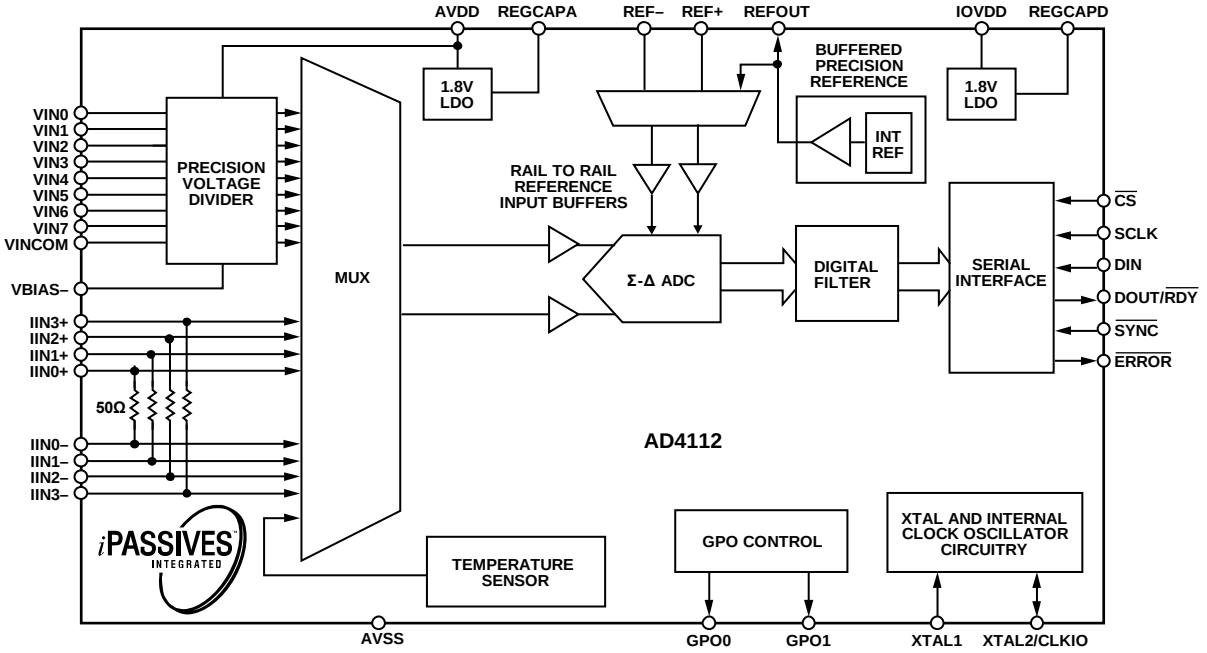



*Figure 1.*

# SPECIFICATIONS

AVDD = 3.0 V to 5.5 V, IOVDD = 2 V to 5.5 V, AVSS = 0 V, DGND = 0 V, VBIAS− = 0 V, REF+ = 2.5 V, REF− = AVSS, internal master clock (MCLK) = 2 MHz, $T_A = T_{MIN}$ to $T_{MAX}$ (−40°C to +105°C), unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VOLTAGE INPUTS | | | | | |
| Differential Input Voltage Range[1] | Specified performance | −10 | | +10 | V |
| | Functional | $-V_{REF} \times 10$ | | $+V_{REF} \times 10$ | V |
| Absolute (Pin) Input Voltage | AVDD ≥ 4.75 V | −20 | | +20 | V |
| | AVDD = 3.0 V | −12 | | +12 | V |
| Input Impedance | | 1 | | | MΩ |
| Offset Error[2] | 25°C | | ±1.5 | | mV |
| Offset Drift | | | ±7 | | µV/°C |
| Gain Error | Internal full-scale calibration[3], 25°C | | ±0.05 | | % of FS |
| Gain Drift | | | ±1 | | ppm/°C |
| Integral Nonlinearity (INL) | | | ±0.01 | | % of FSR |
| Total Unadjusted Error (TUE)[4] | Internal full-scale calibration | | | | |
| | 25°C, internal $V_{REF}$ | | | ±0.06 | % of FSR |
| | −40°C to +105°C, internal $V_{REF}$ | | | ±0.1 | % of FSR |
| | 25°C, external $V_{REF}$ | | | ±0.06 | % of FSR |
| | −40°C to +105°C, external $V_{REF}$ | | | ±0.08 | % of FSR |
| Power Supply Rejection | AVDD for $V_{IN}$ = 1 V | | 70 | | dB |
| Common-Mode Rejection | $V_{IN}$ = 1 V | | | | |
| At DC | | | 85 | | dB |
| At 50 Hz, 60 Hz | 20 Hz output data rate (postfilter), 50 Hz ± 1 Hz and 60 Hz ± 1 Hz | | 120 | | dB |
| Normal Mode Rejection[4] | 50 Hz ± 1 Hz and 60 Hz ± 1 Hz | | | | |
| | Internal clock, 20 SPS ODR (postfilter) | 71 | 90 | | dB |
| | External clock, 20 SPS ODR (postfilter) | 85 | 90 | | dB |
| Resolution | See Table 6 and Table 8 | | | | |
| Noise | See Table 6 and Table 8 | | | | |
| CURRENT INPUTS | | | | | |
| Input Current Range | | −0.5 | | +24 | mA |
| Absolute (Pin) Input Voltage | | AVSS −0.05 | | AVDD +0.05[5] | V |
| Input Impedance[6] | | 54 | 60 | 75 | Ω |
| Offset Error[2] | | | ±2 | | µA |
| Offset Drift | | | ±3 | | nA/°C |
| Gain Error | Factory calibrated gain, 25°C | | ±0.02 | | % of FS |
| Gain Drift | | | ±10 | | ppm/°C |
| INL | | | ±0.01 | | % of FSR |
| TUE[4] | 25°C, internal $V_{REF}$ | | | ±0.08 | % of FSR |
| | −40°C to +105°C, internal $V_{REF}$ | | | ±0.2 | % of FSR |
| | 25°C, external $V_{REF}$ | | | ±0.08 | % of FSR |
| | −40°C to +105°C, external $V_{REF}$ | | | ±0.2 | % of FSR |
| Power Supply Rejection | AVDD for $I_{IN}$ = 10 mA | | 0.5 | | µA/V |
| Normal Mode Rejection[4] | 50 Hz ± 1 Hz and 60 Hz ± 1 Hz | | | | |
| | Internal clock, 20 SPS ODR (postfilter) | 71 | 90 | | dB |
| | External clock, 20 SPS ODR (postfilter) | 85 | 90 | | dB |
| Resolution | See Table 7 and Table 9 | | | | |
| Noise | See Table 7 and Table 9 | | | | |
| ADC SPEED AND PERFORMANCE | | | | | |
| ADC Output Data Rate (ODR) | One channel, see Table 6 | 1.25 | | 31,250 | SPS |
| No Missing Codes[4] | Excluding sinc3 filter ≥ 15 kHz notch | 24 | | | Bits |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| INTERNAL REFERENCE | 100 nF external capacitor to AVSS | | | | |
| Output Voltage | REFOUT with respect to AVSS | | 2.5 | | V |
| Initial Accuracy[4, 7] | REFOUT, $T_A$ = 25°C | −0.12 | | +0.12 | % of V |
| Temperature Coefficient | | | ±5 | +12 | ppm/°C |
| Reference Load Current, $I_{LOAD}$ | | −10 | | +10 | mA |
| Power Supply Rejection | AVDD (line regulation) | | 95 | | dB |
| Load Regulation | $\Delta V_{OUT}/\Delta I_{LOAD}$ | | 32 | | ppm/mA |
| Voltage Noise | $e_N$, 0.1 Hz to 10 Hz, 2.5 V reference | | 4.5 | | µV rms |
| Voltage Noise Density | $e_N$, 1 kHz, 2.5 V reference | | 215 | | nV/√Hz |
| Turn On Settling Time | 100 nF REFOUT capacitor | | 200 | | µs |
| Short-Circuit Current, $I_{SC}$ | | | 25 | | mA |
| EXTERNAL REFERENCE INPUTS | | | | | |
| Differential Input Range | $V_{REF}$ = (REF+) − (REF−) | 1 | 2.5 | AVDD | V |
| Absolute Voltage Limits | | | | | |
| Buffers Disabled | | AVSS −0.05 | | AVDD +0.05 | V |
| Buffers Enabled | | AVSS | | AVDD | V |
| REF± Input Current | | | | | |
| Buffers Disabled | | | | | |
| Input Current | | | ±9 | | µA/V |
| Input Current Drift | External clock | | ±0.75 | | nA/V/°C |
| | Internal clock | | ±2 | | nA/V/°C |
| Buffers Enabled | | | | | |
| Input Current | | | ±100 | | nA |
| Input Current Drift | | | 0.25 | | nA/°C |
| Normal Mode Rejection | See the rejection parameter | | | | |
| Common-Mode Rejection | | | 95 | | dB |
| TEMPERATURE SENSOR | | | | | |
| Accuracy | After user calibration at 25°C | | ±2 | | °C |
| Sensitivity | | | 477 | | µV/K |
| GENERAL-PURPOSE OUTPUTS (GPO0, GPO1) | With respect to AVSS | | | | |
| Floating State Output Capacitance | | | 5 | | pF |
| Output Voltage[4] | | | | | |
| High, $V_{OH}$ | Source current ($I_{SOURCE}$) = 200 µA | AVDD − 1 | | | V |
| Low, $V_{OL}$ | Sink current ($I_{SINK}$) = 800 µA | | | AVSS + 0.4 | V |
| CLOCK | | | | | |
| Internal Clock | | | | | |
| Frequency | | | 2 | | MHz |
| Accuracy | | −2.5% | | +2.5% | % |
| Duty Cycle | | | 50 | | % |
| Output Voltage | | | | | |
| Low, $V_{OL}$ | | | | 0.4 | V |
| High, $V_{OH}$ | | 0.8 × IOVDD | | | V |
| Crystal | | | | | |
| Frequency | | 14 | 16 | 16.384 | MHz |
| Start-Up Time | | | 10 | | µs |
| External Clock (CLKIO) | | | 2 | 2.048 | MHz |
| Duty Cycle | | 30 | 50 | 70 | % |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
| Input Voltage[4] | | | | | |
| High, $V_{INH}$ | 2 V ≤ IOVDD < 2.3 V | 0.65 × IOVDD | | | V |
| | 2.3 V ≤ IOVDD ≤ 5.5 V | 0.7 × IOVDD | | | V |
| Low, $V_{INL}$ | 2 V ≤ IOVDD < 2.3 V | | | 0.35 × IOVDD | V |
| | 2.3 V ≤ IOVDD ≤ 5.5 V | | | 0.7 | V |
| Hysteresis | IOVDD ≥ 2.7 V | 0.08 | | 0.25 | V |
| | IOVDD < 2.7 V | 0.04 | | 0.2 | V |
| Leakage Current | | −10 | | +10 | µA |
| LOGIC OUTPUT (DOUT/$\overline{RDY}$) | | | | | |
| Output Voltage[4] | | | | | |
| High, $V_{OH}$ | IOVDD ≥ 4.5 V, $I_{SOURCE}$ = 1 mA | 0.8 × IOVDD | | | V |
| | 2.7 V ≤ IOVDD < 4.5 V, $I_{SOURCE}$ = 500 µA | 0.8 × IOVDD | | | V |
| | IOVDD < 2.7 V, $I_{SOURCE}$ = 200 µA | 0.8 × IOVDD | | | V |
| Low, $V_{OL}$ | IOVDD ≥ 4.5 V, $I_{SINK}$ = 2 mA | | | 0.4 | V |
| | 2.7 V ≤ IOVDD < 4.5 V, $I_{SINK}$ = 1 mA | | | 0.4 | V |
| | IOVDD < 2.7 V, $I_{SINK}$ = 400 µA | | | 0.4 | V |
| Leakage Current[4] | Floating state | −10 | | +10 | µA |
| Output Capacitance | Floating state | | 10 | | pF |
| POWER REQUIREMENTS | | | | | |
| Power Supply Voltage | | | | | |
| AVDD to AVSS | | 3.0 | | 5.5 | V |
| AVSS to DGND | | −2.75 | | 0 | V |
| IOVDD to DGND | | 2 | | 5.5 | V |
| IOVDD to AVSS | For AVSS < DGND | | | 6.35 | V |
| POWER SUPPLY CURRENTS[8] | All outputs unloaded, digital inputs connected to IOVDD or DGND | | | | |
| Full Operating Mode | | | | | |
| AVDD Current | Including internal reference | | 3.3 | 3.7 | mA |
| IOVDD Current | Internal clock | | 0.6 | 0.8 | mA |
| Standby Mode | All $V_{IN}$ = 0 V | | 120 | | µA |
| Power-Down Mode | All $V_{IN}$ = 0 V | | 90 | | µA |
| POWER DISSIPATION | | | | | |
| Full Operating Mode | | | 19.5 | | mW |
| Standby Mode | | | 600 | | µW |
| Power-Down Mode | | | 450 | | µW |

[1] The full specification is guaranteed for a differential input signal of ±10 V. The device is functional up to a differential input signal of ±$V_{REF}$ × 10. However, the specified absolute (pin) voltage must not be exceeded for the proper function.
[2] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected.
[3] The gain calibration register is overwritten by performing an internal full-scale calibration. Alternatively, a system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate for the channel that is calibrated.
[4] Specification is not production tested but is supported by characterization data at the initial product release.
[5] This maximum specification is only possible if IINx− is biased so that the current through the resistor is less than 24 mA. It is not possible with IINx− connected to 0 V.
[6] This specification shows the impedance seen between current input pins. The current is measured across a 50 Ω sense resistor.
[7] This specification includes moisture sensitivity level (MSL) preconditioning effects.
[8] This specification is with no load on the REFOUT pin and the digital output pins.

## TIMING CHARACTERISTICS

IOVDD = 2 V to 5.5 V, DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOVDD, capacitive load ($C_{LOAD}$) = 20 pF, unless otherwise noted.

**Table 2.**

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Description[1, 2] |
|---|---|---|---|
| SCLK | | | |
| $t_3$ | 25 | ns min | SCLK high pulse width |
| $t_4$ | 25 | ns min | SCLK low pulse width |
| READ OPERATION | | | |
| $t_1$ | 0 | ns min | $\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time |
| | 15 | ns max | IOVDD = 4.75 V to 5.5 V |
| | 40 | ns max | IOVDD = 2 V to 3.6 V |
| $t_2$[3] | 0 | ns min | SCLK active edge to data valid delay[4] |
| | 12.5 | ns max | IOVDD = 4.75 V to 5.5 V |
| | 25 | ns max | IOVDD = 2 V to 3.6 V |
| $t_5$[5] | 2.5 | ns min | Bus relinquish time after $\overline{CS}$ inactive edge |
| | 20 | ns max | |
| $t_6$ | 0 | ns min | SCLK inactive edge to $\overline{CS}$ inactive edge |
| $t_7$ | 10 | ns min | SCLK inactive edge to DOUT/$\overline{RDY}$ high/low |
| WRITE OPERATION | | | |
| $t_8$ | 0 | ns min | $\overline{CS}$ falling edge to SCLK active edge setup time[4] |
| $t_9$ | 8 | ns min | Data valid to SCLK edge setup time |
| $t_{10}$ | 8 | ns min | Data valid to SCLK edge hold time |
| $t_{11}$ | 5 | ns min | $\overline{CS}$ rising edge to SCLK edge hold time |

[1] Sample tested during initial release to ensure compliance.
[2] See Figure 2 and Figure 3.
[3] This parameter is defined as the time required for the output to cross the $V_{OL}$ or $V_{OH}$ limits.
[4] The SCLK active edge is the falling edge of SCLK.
[5] DOUT/$\overline{RDY}$ returns high after a read of the data register. In single-conversion mode and continuous conversion mode, the same data can be read again, if required, while DOUT/$\overline{RDY}$ is high. However, care must be taken to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

### *Timing Diagrams*

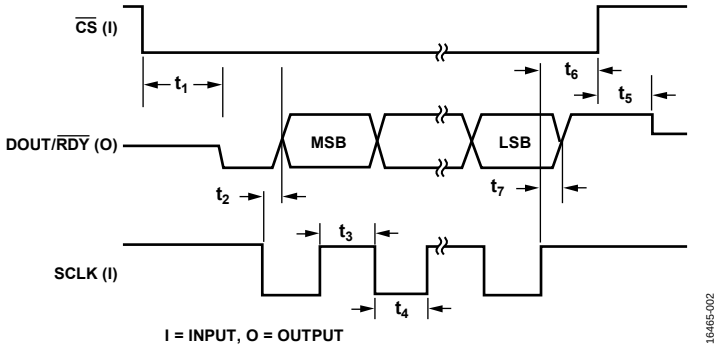



*Figure 2. Read Cycle Timing Diagram*

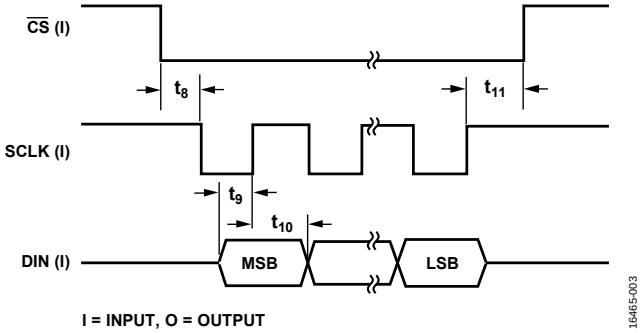



*Figure 3. Write Cycle Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| AVDD to AVSS | −0.3 V to +6.5 V |
| AVDD to DGND | −0.3 V to +6.5 V |
| IOVDD to DGND | −0.3 V to +6.5 V |
| IOVDD to AVSS | −0.3 V to +7.5 V |
| AVSS to DGND | −3.25 V to +0.3 V |
| VINx to AVSS | −50 V to +50 V |
| IINx+ to AVSS | −0.3 V to AVDD + 0.3 V |
| IINx− to AVSS | −0.3 V to AVDD + 0.3 V |
| Current Input Current[1] | −50 mA to +50 mA |
| Reference Input Voltage to AVSS | −0.3 V to AVDD + 0.3 V |
| Digital Input Voltage to DGND | −0.3 V to IOVDD + 0.3 V |
| Digital Output Voltage to DGND | −0.3 V to IOVDD + 0.3 V |
| Digital Input Current | 10 mA |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| Lead Soldering, Reflow Temperature | 260°C |

[1] The absolute maximum current input current, current input voltage, and IINx− voltage must all be within the specified limits.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$ is specified for a device soldered on a JEDEC test board for surface-mount packages.

**Table 4. Thermal Resistance**

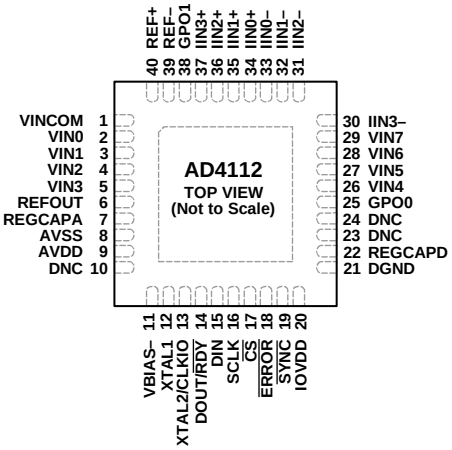
| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| CP-40-15[1] | | |
| 4-Layer JEDEC Board | 34 | °C/W |

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 16 thermal vias. See JEDEC JESD51.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS




NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT ANYTHING TO THIS PIN. PIN 24 IS INTERNALLY CONNECTED TO AVSS.
2. SOLDER THE EXPOSED PAD TO A SIMILAR PAD ON THE PCB UNDER THE EXPOSED PAD TO CONFER MECHANICAL STRENGTH AND FOR HEAT DISSIPATION. THE EXPOSED PAD MUST BE CONNECTED TO AVSS THROUGH THIS PAD ON THE PCB.

16465-004

*Figure 4. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic[1] | Type[2] | Description |
|---|---|---|---|
| 1 | VINCOM | AI | Voltage Input Common. Voltage inputs are referenced to this pin when configured as single-ended. Connect this pin to analog ground. |
| 2 | VIN0 | AI | Voltage Input 0. Input referenced to VINCOM in single ended configuration, or a positive input of an input pair with VIN1 in differential configuration. |
| 3 | VIN1 | AI | Voltage Input 1. Input referenced to VINCOM in single ended configuration, or a negative input of an input pair with VIN0 in differential configuration. |
| 4 | VIN2 | AI | Voltage Input 2. Input referenced to VINCOM in single ended configuration, or a positive input of an input pair with VIN3 in differential configuration. |
| 5 | VIN3 | AI | Voltage Input 3. Input referenced to VINCOM in single ended configuration, or a negative input of an input pair with VIN2 in differential configuration. |
| 6 | REFOUT | AO | Buffered Output of Internal Reference. The output is 2.5 V with respect to AVSS. Decouple this pin to AVSS using a 0.1 µF capacitor. |
| 7 | REGCAPA | AO | Analog Low Dropout (LDO) Regulator Output. Decouple this pin to AVSS using a 1 µF capacitor and a 0.1 µF capacitor. |
| 8 | AVSS | P | Negative Analog Supply. This supply ranges from −2.75 V to 0 V and is nominally set to 0 V. |
| 9 | AVDD | P | Analog Supply Voltage. This voltage ranges from 3.0 V to 5.5 V with respect to AVSS. |
| 10 | DNC | N/A | Do Not Connect. Do not connect anything to this pin. |
| 11 | VBIAS– | AI | Voltage Bias Negative. The pin is setting bias voltage for the voltage input analog front-end. Connect this pin to AVSS. |
| 12 | XTAL1 | AI | Input 1 for Crystal. |
| 13 | XTAL2/CLKIO | AI/DI | Input 2 for Crystal/Clock Input or Output. See the CLOCKSEL bit settings in the ADCMODE register for more information. |
| 14 | DOUT/$\overline{\text{RDY}}$ | DO | Serial Data Output/Data Ready Output. This pin serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. The data-word/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated. When $\overline{\text{CS}}$ is low, and a register is not being read, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. |
| 15 | DIN | DI | Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register address (RA) bits of the communications register identifying the appropriate register. Data is clocked in on the rising edge of SCLK. |

| Pin No. | Mnemonic[1] | Type[2] | Description |
|---|---|---|---|
| 16 | SCLK | DI | Serial Clock Input. This serial clock input is for data transfers to and from the ADC. SCLK has a Schmitt triggered input. |
| 17 | $\overline{CS}$ | DI | Chip Select Input. This pin is an active low logic input used to select the ADC. Use $\overline{CS}$ to select the ADC in systems with more than one device on the serial bus. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT/$\overline{RDY}$ used to interface with the device. When $\overline{CS}$ is high, the DOUT/$\overline{RDY}$ output is tristated. |
| 18 | $\overline{ERROR}$ | DI/O | Error Input/Output or General-Purpose Output. This pin can be used in one of the following three modes:<br>Active low error input mode. This mode sets the ADC_ERROR bit in the status register.<br>Active low, open-drain error output mode. The status register error bits are mapped to the $\overline{ERROR}$ pin. The $\overline{ERROR}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed.<br>General-purpose output mode. The status of the pin is controlled by the ERR_DAT bit in the GPIOCON register. The pin is referenced between IOVDD and DGND. |
| 19 | $\overline{SYNC}$ | DI | Synchronization Input. Allows synchronization of the digital filters and analog modulators when using multiple AD4112 devices. |
| 20 | IOVDD | P | Digital I/O Supply Voltage. The IOVDD voltage ranges from 2 V to 5.5 V (nominal). IOVDD is independent of AVDD. For example, IOVDD can be operated at 3.3 V when AVDD equals 5 V, or vice versa. If AVSS is set to −2.5 V, the voltage on IOVDD must not exceed 3.6 V. |
| 21 | DGND | P | Digital Ground. |
| 22 | REGCAPD | AO | Digital LDO Regulator Output. This pin is for decoupling purposes only. Decouple this pin to DGND using a 1 µF capacitor. |
| 23 | DNC | N/A | Do Not Connect. Do not connect anything to this pin. |
| 24 | DNC | N/A | Do Not Connect. Do not connect anything to this pin. This pin is internally connected to AVSS. |
| 25 | GPO0 | DO | General-Purpose Output. Logic output on this this pin is referred to the AVDD and AVSS supplies. |
| 26 | VIN4 | AI | Voltage Input 4. Input referenced to VINCOM in single ended configuration, or a positive input of an input pair with VIN5 in differential configuration. |
| 27 | VIN5 | AI | Voltage Input 5. Input referenced to VINCOM in single ended configuration, or a negative input of an input pair with VIN4 in differential configuration. |
| 28 | VIN6 | AI | Voltage Input 6. Input referenced to VINCOM in single ended configuration, or a positive input of an input pair with VIN7 in differential configuration. |
| 29 | VIN7 | AI | Voltage Input 7. Input referenced to VINCOM in single ended configuration, or a negative input of an input pair with VIN6 in differential configuration. |
| 30 | IIN3− | AI | Current Input Return 3. Connect this pin to analog ground. |
| 31 | IIN2− | AI | Current Input Return 2. Connect this pin to analog ground. |
| 32 | IIN1− | AI | Current Input Return 1. Connect this pin to analog ground. |
| 33 | IIN0− | AI | Current Input Return 0. Connect this pin to analog ground. |
| 34 | IIN0+ | AI | Current Input 0. |
| 35 | IIN1+ | AI | Current Input 1. |
| 36 | IIN2+ | AI | Current Input 2. |
| 37 | IIN3+ | AI | Current Input 3. |
| 38 | GPO1 | DO | General-Purpose Output. Logic output on this pin is referred to the AVDD and AVSS supplies. |
| 39 | REF− | AI | Reference Input Negative Terminal. REF− can span from AVSS to AVDD − 1 V. Reference can be selected through the REF_SELx bits in the setup configuration registers. |
| 40 | REF+ | AI | Reference Input Positive Terminal. An external reference can be applied between REF+ and REF−. REF+ can span from AVDD to AVSS + 1 V. Reference can be selected through the REF_SELx bits in the setup configuration registers. |
| | EP | P | Exposed Pad. Solder the exposed pad to a similar pad on the PCB under the exposed pad to confer mechanical strength to the package and for heat dissipation. The exposed pad must be connected to AVSS through this pad on the PCB. |

[1] Note that, throughout this data sheet, the dual function pin mnemonics are referenced by the relevant function only.
[2] AI means analog input, AO means analog output, P means power supply, N/A means not applicable, DI means digital input, DO means digital output, and DI/O means bidirectional digital input/output.

# TYPICAL PERFORMANCE CHARACTERISTICS

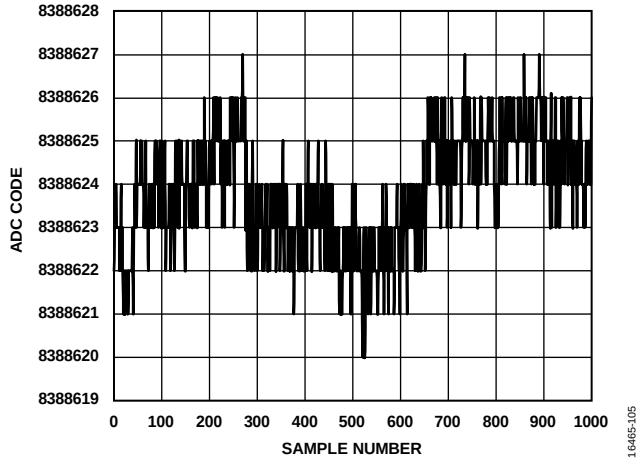



Figure 5. Noise (Voltage Input, Output Data Rate = 1.25 SPS)

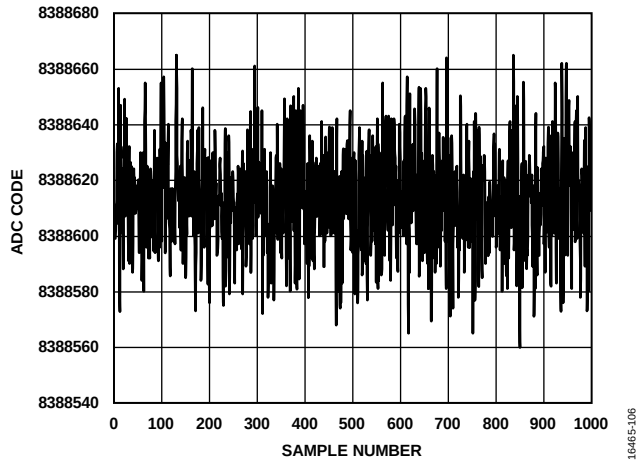



Figure 6. Noise (Voltage Input, Output Data Rate = 2.5 kSPS)

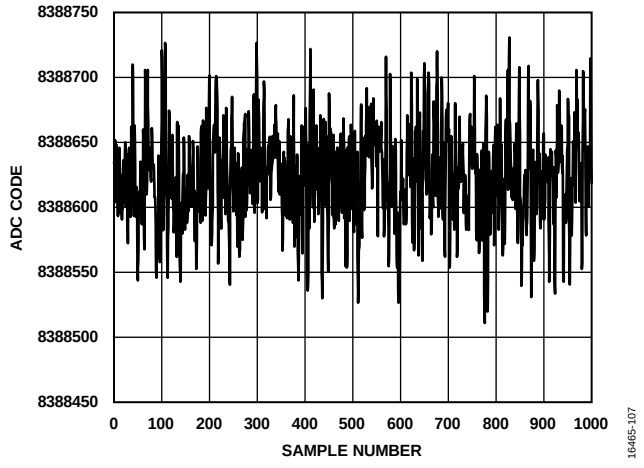



Figure 7. Noise (Voltage Input, Output Data Rate = 31.25 kSPS)

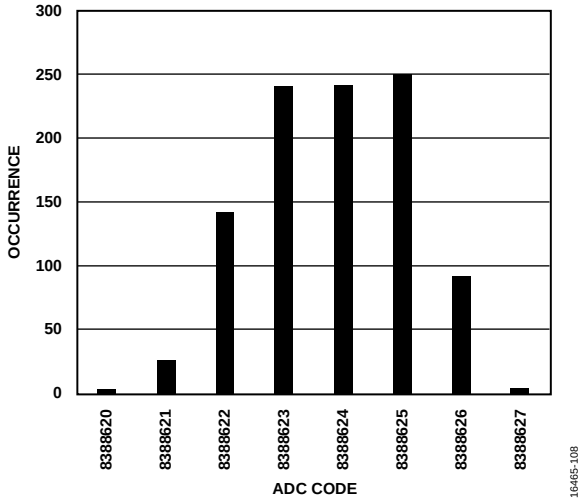



Figure 8. Histogram (Voltage Input, Output Data Rate = 1.25 SPS)

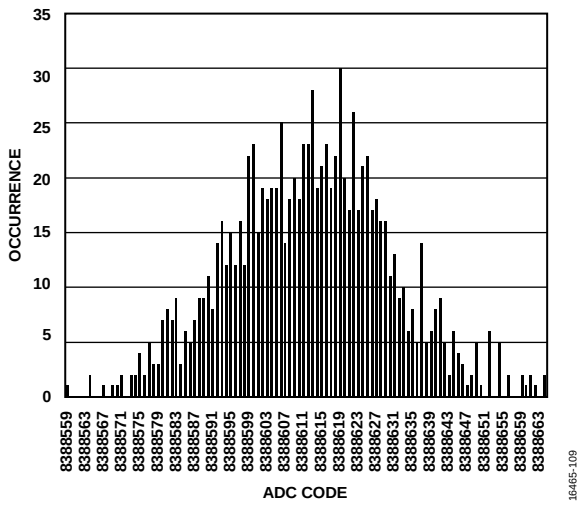



Figure 9. Histogram (Voltage Input, Output Data Rate = 2.5 kSPS)

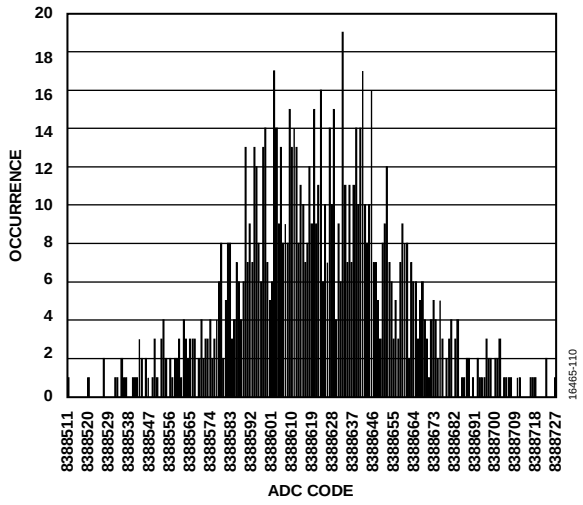



Figure 10. Histogram (Voltage Input, Output Data Rate = 31.25 kSPS)

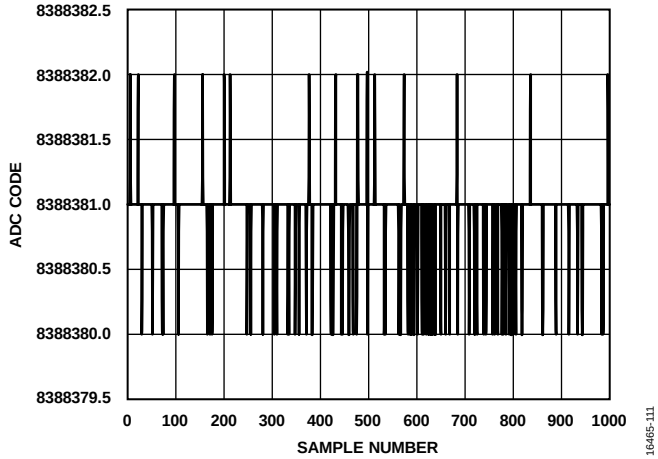



Figure 11. Noise (Current Input, Output Data Rate = 1.25 SPS)

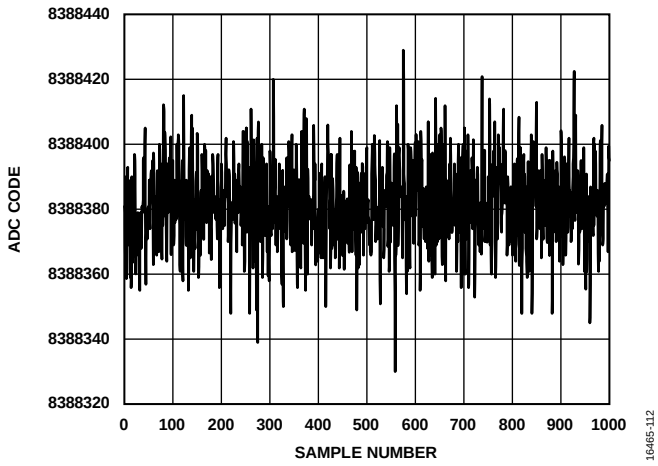



Figure 12. Noise (Current Input, Output Data Rate = 2.5 kSPS)

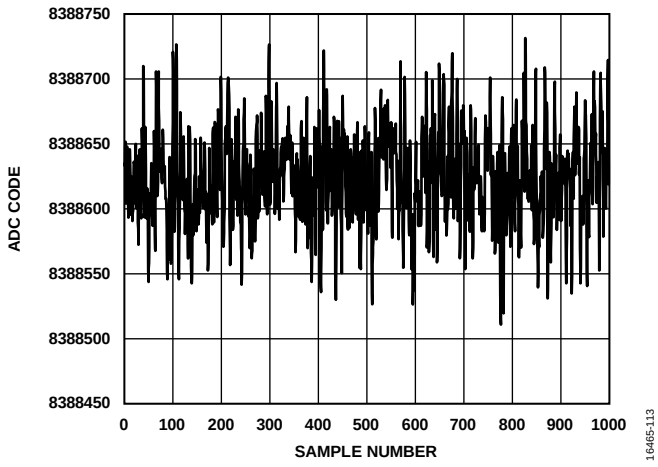



Figure 13. Noise (Current Input, Output Data Rate = 31.25 kSPS)

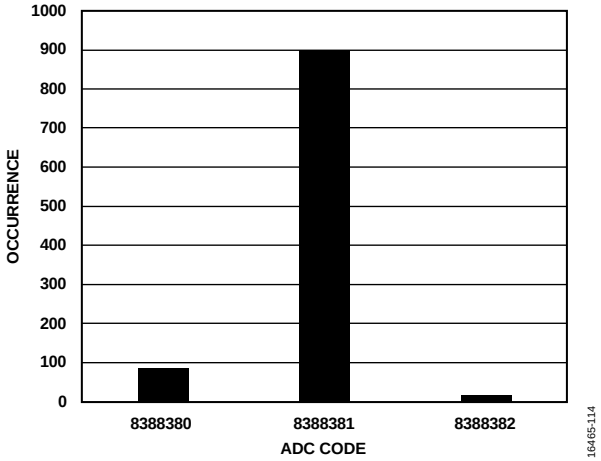



Figure 14. Histogram (Current Input, Output Data Rate = 1.25 SPS)

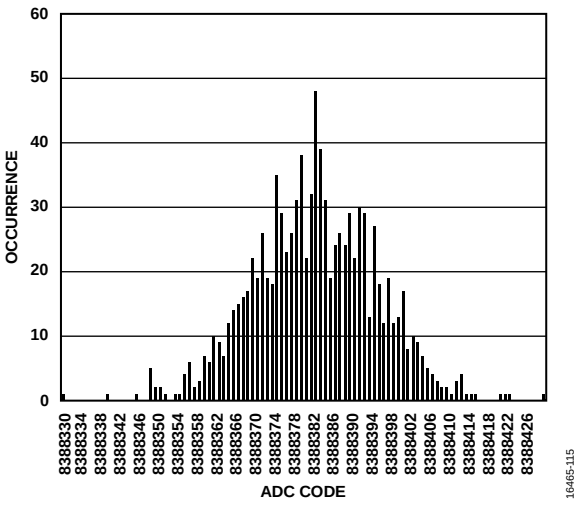



Figure 15. Histogram (Current Input, Output Data Rate = 31.25 SPS)

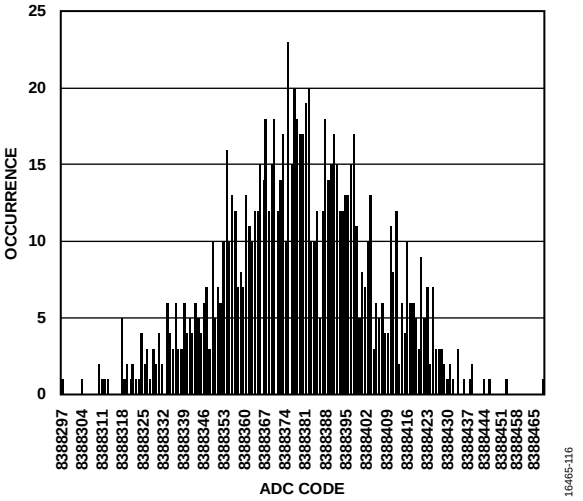



Figure 16. Histogram (Current Input, Output Data Rate = 31.25 kSPS)

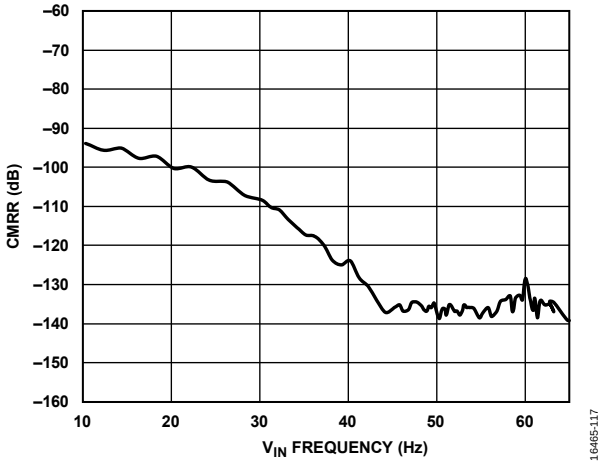



Figure 17. Common-Mode Rejection Ratio (CMRR) vs. $V_{IN}$ Frequency ($V_{IN}$ = 0.1 V, 10 Hz to 70 Hz, Output)

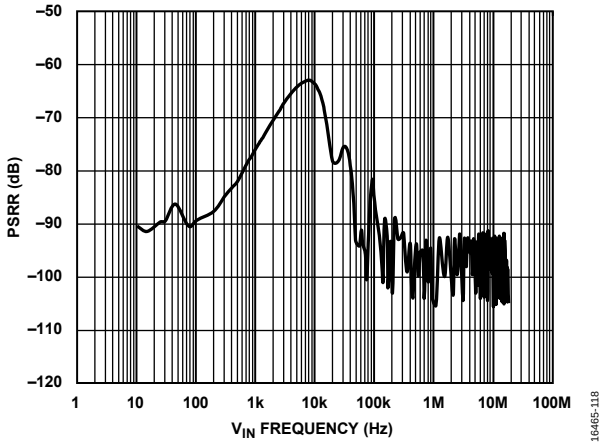



Figure 18. Power Supply Rejection Ratio (PSRR) vs. $V_{IN}$ Frequency

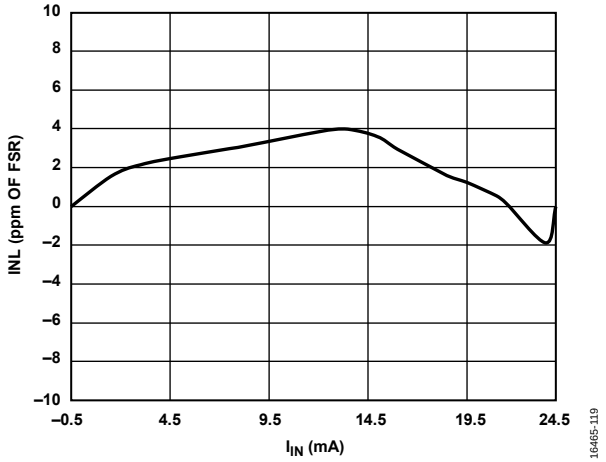



Figure 19. Integral Nonlinearity (INL) vs. Input (Current Input)

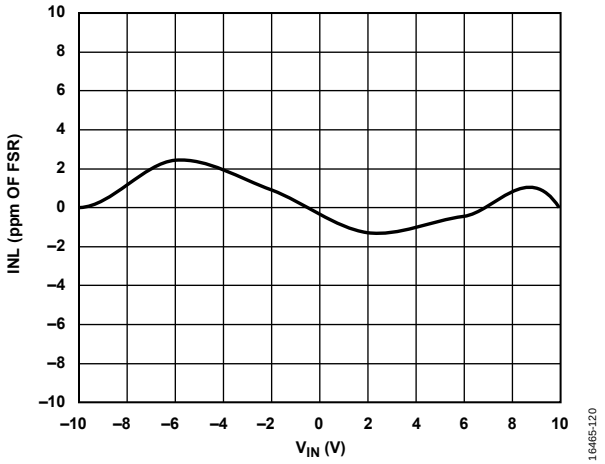



Figure 20. Integral Nonlinearity (INL) vs. Input Range (Voltage Input)

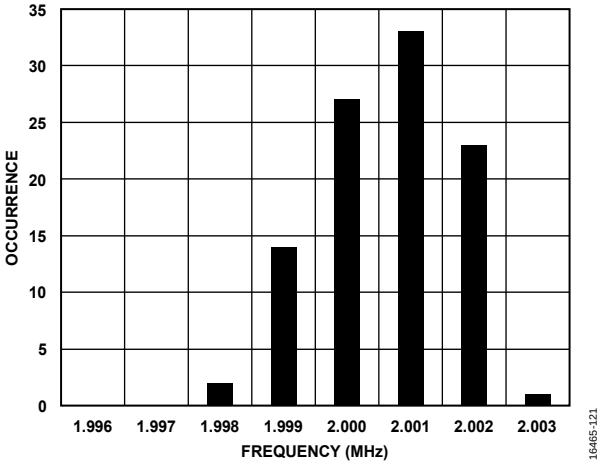



Figure 21. Internal Oscillator Frequency/Accuracy Distribution Histogram

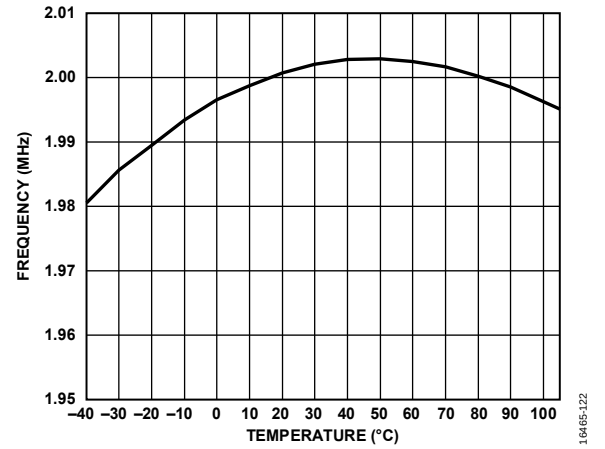



Figure 22. Internal Oscillator Frequency vs. Temperature

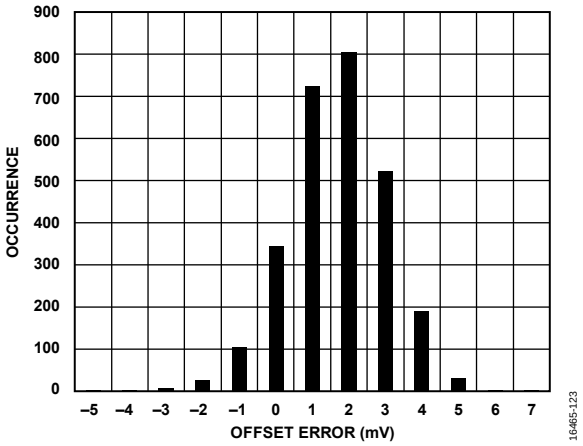



Figure 23. Offset Error Distribution Histogram (Voltage Input)

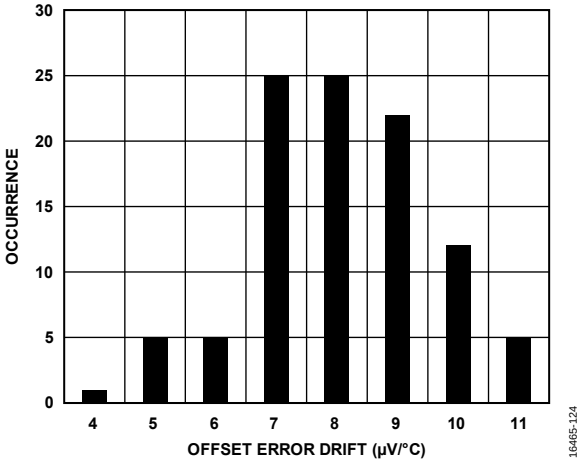



Figure 24. Offset Error Drift Distribution Histogram (Voltage Input)

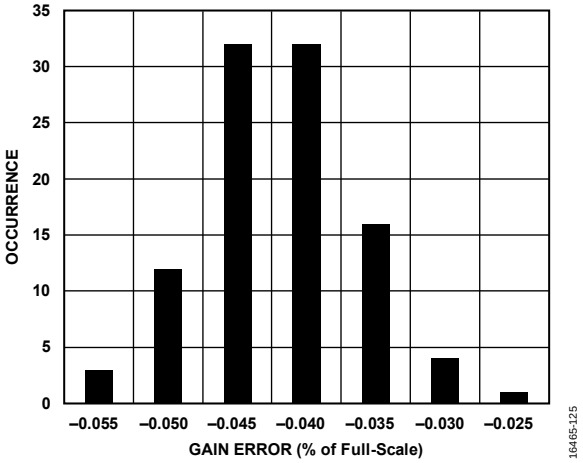



Figure 25. Gain Error Distribution Histogram (Voltage Input)

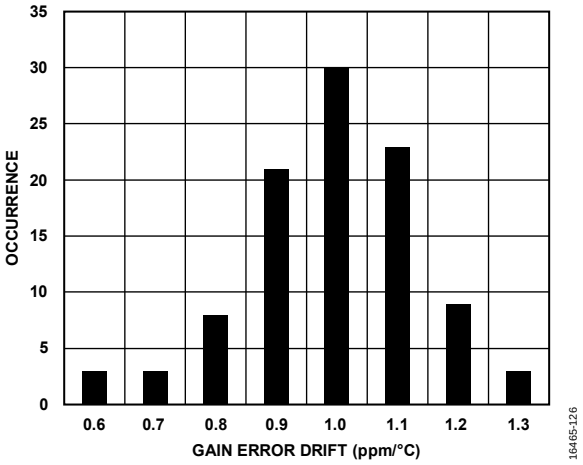



Figure 26. Gain Error Drift Distribution Histogram (Voltage Input)

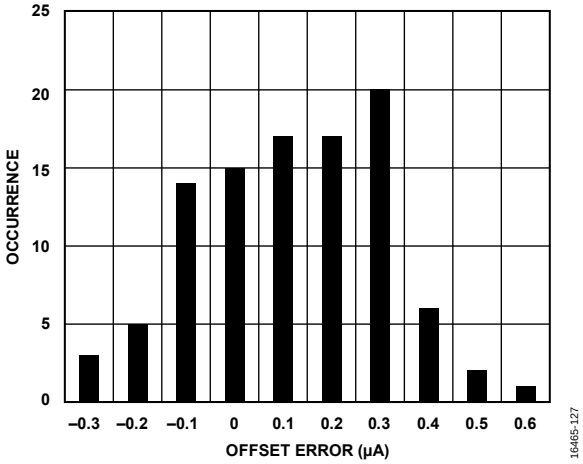



Figure 27. Offset Error Distribution Histogram (Current Input)

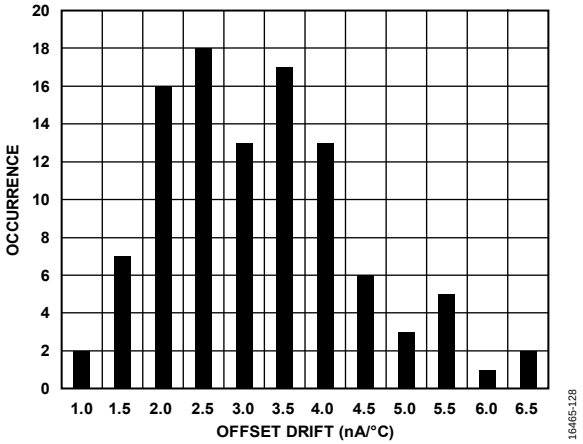



Figure 28. Offset Error Drift Distribution Histogram (Current Input)

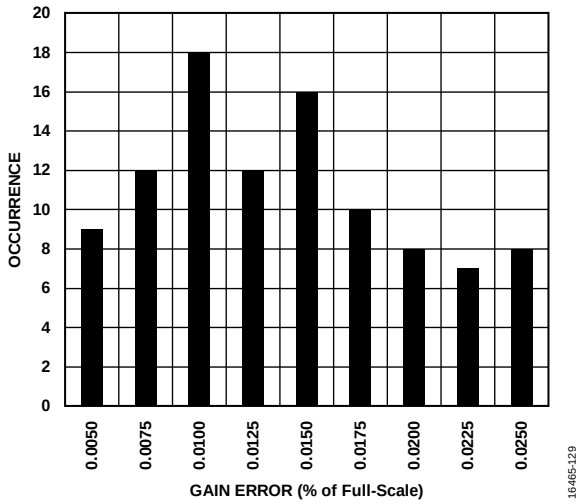



Figure 29. Gain Error Distribution Histogram (Current Input)

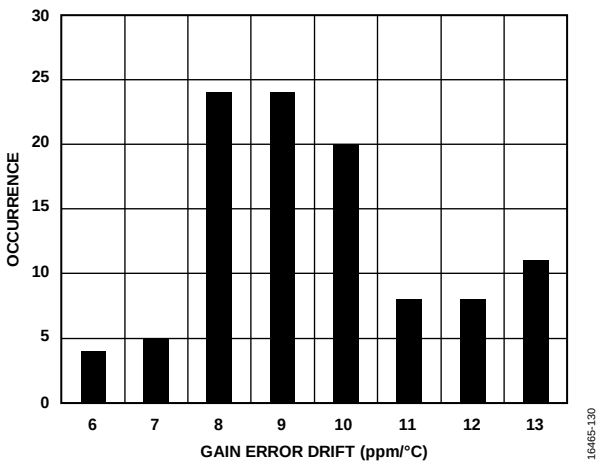



Figure 30. Gain Error Drift Distribution Histogram (Current Input)

# NOISE PERFORMANCE AND RESOLUTION

Table 6 to Table 9 show the rms noise, peak-to-peak noise, effective resolution, and the noise free (peak-to-peak) resolution of the AD4112 for various ODRs. These values are typical and are measured with an external 2.5 V reference and with the ADC continuously converting on multiple channels. The values in Table 6 and Table 8 are generated for the ±10 V voltage input range, with a differential input voltage of 0 V. The values in Table 7 and Table 9 are generated for the 0 mA to 20 mA input range, with an input current of 0 mA. It is important to note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker.

**Table 6. ±10 V Voltage Input RMS Noise Resolution vs. ODR Using a Sinc5 + Sinc1 Filter**

| Default Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled | Output Data Rate (SPS per Channel); SING_CYC = 1 or Multiple Channels Enabled | Settling Time[1] | Notch Frequency (Hz) | Noise (µV rms)[2] | Effective Resolution (Bits) | Noise (µV p-p) | Peak-to-Peak Resolution (Bits) |
|---|---|---|---|---|---|---|---|
| 31,250 | 6211 | 161 µs | 31,250 | 106 | 17.5 | 750 | 14.7 |
| 15,625 | 5181 | 193 µs | 15,625 | 94 | 17.7 | 580 | 15.1 |
| 10,417 | 4444 | 225 µs | 10,417 | 82 | 17.9 | 512 | 15.3 |
| 5208 | 3115 | 321 µs | 5208 | 62 | 18.3 | 372 | 15.7 |
| 2597 | 2597 | 385 µs | 3906 | 47 | 18.7 | 312 | 16.0 |
| 1007 | 1007 | 993 µs | 1157 | 27 | 19.5 | 190 | 16.7 |
| 504 | 504 | 1.99 ms | 539 | 21 | 19.9 | 140 | 17.1 |
| 381 | 381 | 2.63 ms | 401 | 17 | 20.2 | 92 | 17.7 |
| 200.3 | 200.3 | 4.99 ms | 206 | 13 | 20.6 | 62 | 18.3 |
| 100.2 | 100.2 | 9.99 ms | 102 | 8 | 21.3 | 45 | 18.8 |
| 59.52 | 59.52 | 16.8 ms | 59.98 | 7 | 21.4 | 33 | 19.2 |
| 49.68 | 49.68 | 20.13 ms | 50 | 7 | 21.4 | 33 | 19.2 |
| 20 | 20.01 | 49.98 ms | 20 | 4 | 22.3 | 22 | 19.8 |
| 16.67 | 16.63 | 60.13 ms | 16.67 | 4 | 22.3 | 21 | 19.9 |
| 10 | 10 | 100 ms | 10 | 3.7 | 22.4 | 18 | 20.1 |
| 5 | 5 | 200 ms | 5 | 3.4 | 22.5 | 17 | 20.2 |
| 2.5 | 2.5 | 400 ms | 2.5 | 2.4 | 23 | 12 | 20.7 |
| 1.25 | 1.25 | 800 ms | 1.25 | 2.3 | 23.1 | 11 | 20.8 |

[1] The settling time is rounded to the nearest microsecond, which is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] Based on 1000 samples for data rates ≥ 381 SPS per channel, based on 100 samples for data rates ≤ 200.3 SPS per channel.

**Table 7. 0 mA to 20 mA Current Input Noise and Resolution vs. Output Data Rate Using a Sinc5 + Sinc1 Filter**

| Default Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled | Output Data Rate (SPS per Channel); SING_CYC = 1 or Multiple Channels Enabled | Settling Time[1] | Notch Frequency (Hz) | Noise (nA rms)[2] | Effective Resolution (Bits) | Noise (nA p-p) | Peak-to-Peak Resolution (Bits) |
|---|---|---|---|---|---|---|---|
| 31,250 | 6211 | 161 µs | 31,250 | 155 | 17.0 | 1100 | 14.2 |
| 15,625 | 5181 | 193 µs | 15,625 | 136 | 17.2 | 920 | 14.4 |
| 10,417 | 4444 | 225 µs | 10,417 | 113 | 17.4 | 720 | 14.8 |
| 5208 | 3115 | 321 µs | 5208 | 84 | 17.9 | 580 | 15.1 |
| 2597 | 2597 | 385 µs | 3906 | 75 | 18.0 | 480 | 15.3 |
| 1007 | 1007 | 993 µs | 1157 | 43 | 18.8 | 220 | 16.5 |
| 504 | 503.8 | 1.99 ms | 539 | 29 | 19.4 | 150 | 17.0 |
| 381 | 381 | 2.63 ms | 401 | 21 | 19.9 | 125 | 17.3 |
| 200.3 | 200.3 | 4.99 ms | 206 | 18 | 20.1 | 95 | 17.7 |
| 100.2 | 100.2 | 9.99 ms | 102 | 13 | 20.6 | 71 | 18.1 |
| 59.52 | 59.52 | 16.8 ms | 59.98 | 10 | 20.9 | 48 | 18.7 |
| 49.68 | 49.68 | 20.13 ms | 50 | 9 | 21.1 | 41 | 18.9 |
| 20 | 20.01 | 49.98 ms | 20 | 6 | 21.7 | 30 | 19.3 |
| 16.67 | 16.63 | 60.13 ms | 16.67 | 5.3 | 21.8 | 23 | 19.7 |
| 10 | 10 | 100 ms | 10 | 4.6 | 22.1 | 18 | 20.1 |
| 5 | 5 | 200 ms | 5 | 3 | 22.7 | 12 | 20.7 |
| 2.5 | 2.5 | 400 ms | 2.5 | 2.8 | 22.8 | 12 | 20.7 |
| 1.25 | 1.25 | 800 ms | 1.25 | 2.7 | 22.8 | 6 | 21.7 |

[1] The settling time is rounded to the nearest microsecond, which is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] Based on 1000 samples for data rates ≥ 381 SPS per channel, based on 100 samples for data rates ≤ 200.3 SPS per channel.

Table 8. ±10 V Voltage Input RMS Noise Resolution vs. ODR Using a Sinc3 Filter

| Default Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled | Output Data Rate (SPS per Channel); SING_CYC = 1 or Multiple Channels Enabled | Settling Time[1] | Notch Frequency (Hz) | Noise (μV rms)[2] | Effective Resolution (Bits) | Noise (μV p-p) | Peak-to-Peak Resolution (Bits) |
|---|---|---|---|---|---|---|---|
| 31,250 | 6211 | 96 μs | 31,250 | 1035 | 14.2 | 6037 | 11.7 |
| 15,625 | 5181 | 192 μs | 15,625 | 158 | 16.9 | 954 | 14.4 |
| 10,417 | 4444 | 288 μs | 10,417 | 77 | 18 | 536 | 15.2 |
| 5208 | 3115 | 576 μs | 5208 | 50 | 18.6 | 334 | 15.9 |
| 3906 | 2597 | 1.15 ms | 3906 | 34 | 19.2 | 205 | 16.6 |
| 1157 | 1007 | 2.98 ms | 1157 | 22 | 19.8 | 137 | 17.2 |
| 539 | 504 | 5.95 ms | 539 | 15 | 20.3 | 15 | 17.5 |
| 401 | 381 | 7.49 ms | 401 | 13 | 20.5 | 13 | 17.9 |
| 206 | 200.3 | 14.99 ms | 206 | 10 | 20.9 | 10 | 18.2 |
| 102 | 100.2 | 29.85 ms | 102 | 7.3 | 21.4 | 39 | 18.9 |
| 59.98 | 59.52 | 50.02 ms | 59.98 | 6.2 | 21.6 | 35 | 19.1 |
| 50 | 49.68 | 60 ms | 50 | 5.3 | 21.8 | 36 | 19.1 |
| 20 | 20.01 | 149.93 ms | 20 | 4.9 | 22 | 33 | 19.2 |
| 16.67 | 16.63 | 179.96 ms | 16.67 | 4.2 | 22.1 | 29.8 | 19.35 |
| 10 | 10 | 300 ms | 10 | 3.7 | 22.4 | 20.9 | 19.9 |
| 5 | 5 | 600 ms | 5 | 3.5 | 22.4 | 17.8 | 20.1 |
| 2.5 | 2.5 | 1.2 sec | 2.5 | 3 | 22.7 | 17.8 | 20.1 |
| 1.25 | 1.25 | 2.4 sec | 1.25 | 2.9 | 22.7 | 14.9 | 20.4 |

[1] The settling time is rounded to the nearest microsecond, which is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] Based on 1000 samples for data rates ≥ 381 SPS per channel, based on 100 samples for data rates ≤ 200.3 SPS per channel.

Table 9. 0 mA to 20 mA Current Input Noise and Resolution vs. Output Data Rate Using a Sinc3 Filter

| Default Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled | Output Data Rate (SPS per Channel); SING_CYC = 1 or Multiple Channels Enabled | Settling Time[1] | Notch Frequency (Hz) | Noise (nA rms)[2] | Effective Resolution (Bits) | Noise (nA p-p) | Peak-to-Peak Resolution (Bits) |
|---|---|---|---|---|---|---|---|
| 31,250 | 6211 | 96 μs | 31,250 | 2177 | 15.5 | 13315 | 12.9 |
| 15,625 | 5181 | 192 μs | 15,625 | 309 | 18.3 | 1830 | 15.8 |
| 10,417 | 4444 | 288 μs | 10,417 | 121 | 19.7 | 781 | 17 |
| 5208 | 3115 | 576 μs | 5208 | 72 | 20.4 | 452 | 17.8 |
| 3906 | 2597 | 1.15 ms | 3906 | 49 | 20.9 | 339 | 18.2 |
| 1157 | 1007 | 2.98 ms | 1157 | 30 | 21.6 | 214 | 18.8 |
| 539 | 503.8 | 5.95 ms | 539 | 22 | 22.1 | 149 | 19.4 |
| 401 | 381 | 7.49 ms | 401 | 19 | 2.3 | 125 | 19.6 |
| 206 | 200.3 | 14.99 ms | 206 | 14 | 22.8 | 77 | 20.3 |
| 102 | 100.2 | 29.85 ms | 102 | 10 | 23.2 | 71 | 20.4 |
| 59.98 | 59.52 | 50.02 ms | 59.98 | 7.6 | 23.6 | 53 | 20.8 |
| 50 | 49.68 | 60 ms | 50 | 7.2 | 23.7 | 41 | 21.2 |
| 20 | 20.01 | 149.93 ms | 20 | 4.8 | 24 | 29.8 | 21.7 |
| 16.67 | 16.63 | 179.96 ms | 16.67 | 4.4 | 24 | 29.8 | 21.7 |
| 10 | 10 | 300 ms | 10 | 3.8 | 24 | 23.8 | 22 |
| 5 | 5 | 600 ms | 5 | 3.1 | 24 | 17.9 | 22.4 |
| 2.5 | 2.5 | 1.2 sec | 2.5 | 2.6 | 24 | 11.9 | 23 |
| 1.25 | 1.25 | 2.4 sec | 1.25 | 2.4 | 24 | 11.9 | 23 |

[1] The settling time is rounded to the nearest microsecond, which is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] Based on 1000 samples for data rates ≥ 381 SPS per channel, based on 100 samples for data rates ≤ 200.3 SPS per channel.

# THEORY OF OPERATION

The AD4112 offers the user a fast settling, high resolution, multiplexed ADC with high levels of configurability, including the following features:

- Four fully differential or eight single-ended voltage inputs.
- High impedance voltage divider with integrated precision matched resistors
- Four current inputs with integrated current sense resistors.
- Embedded proprietary *i*Passives™ technology within a very small device footprint.
- Per channel configurability—up to eight different setups can be defined. A separate setup can be mapped to each of the channels. Each setup allows the user to configure whether the buffers are enabled or disabled, gain and offset correction, filter type, ODR, and reference source selection.

The AD4112 includes a precision, 2.5 V, low drift (5 ppm/°C), band gap internal reference. This reference can be selected for use in ADC conversions, reducing the external component count. When enabled, the internal reference is output to the REFOUT pin. It can be used as a low noise biasing voltage for the external circuitry and must be connected to a 0.1 µF decoupling capacitor.

The AD4112 includes two separate linear regulator blocks for both the analog and digital circuitry. The analog LDO regulator regulates the AVDD supply to 1.8 V.

The linear regulator for the digital IOVDD supply performs a similar function, regulating the input voltage applied at the IOVDD pin to 1.8 V. The serial interface signals always operate from the IOVDD supply seen at the pin; meaning that, if 3.3 V is applied to the IOVDD pin, the interface logic inputs and outputs operate at this level.

The AD4112 is designed for a multitude of factory automation and process control applications, such as programmable logic controller (PLC) and distributed control system (DCS) modules. The AD4112 reduces overall system cost and design burden while maintaining a very high level of accuracy. The AD4112 offers the following system benefits:

- A single 5 V or 3.3 V power supply.
- Guaranteed minimum 1 MΩ input impedance.
- Overrange voltage greater than ±10 V.
- Integrated sense resistors for direct current input measurement.
- Reduced calibration costs.

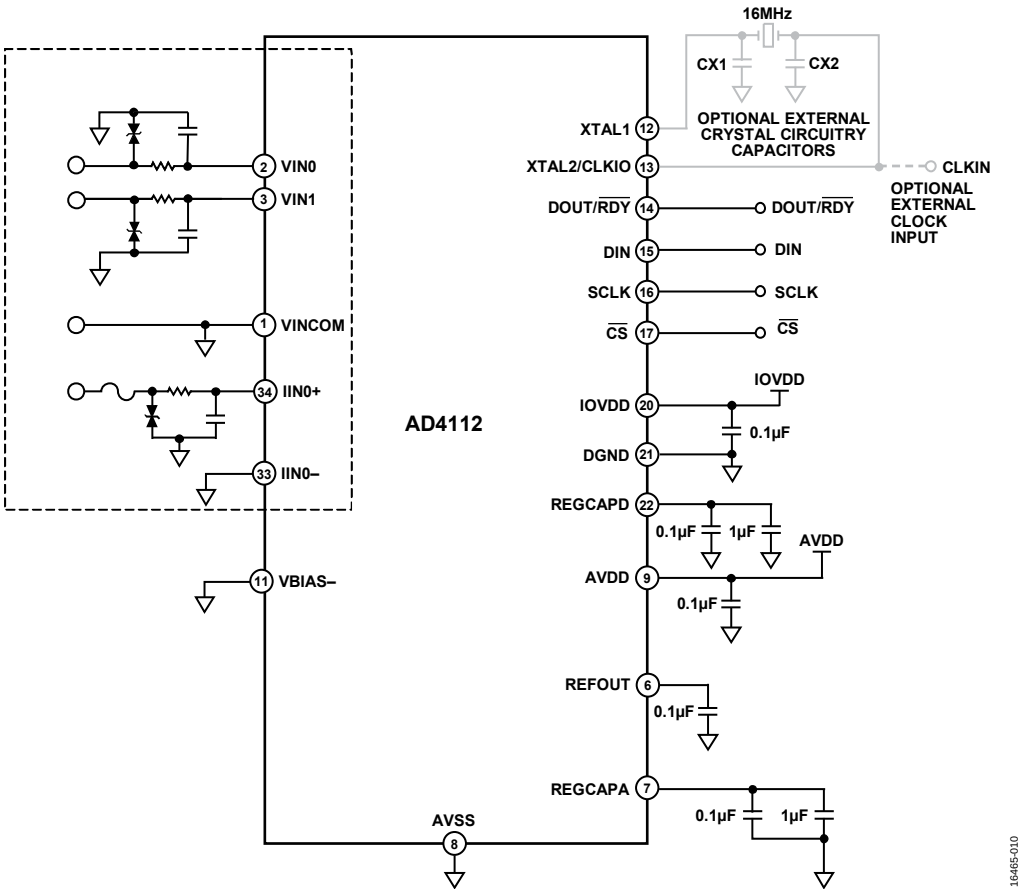



*Figure 31. Typical Connection Diagram*

## POWER SUPPLIES

The AD4112 has two independent power supply pins: AVDD, and IOVDD. The AD4112 has no specific requirements for a power supply sequence. However, when all power supplies are stable, a device reset is required. See the AD4112 Reset section for details on how to reset the device.

AVDD powers the internal 1.8 V analog LDO regulator, which powers the ADC core. AVDD also powers the crosspoint multiplexer and integrated input buffers. AVDD is referenced to AVSS, and AVDD – AVSS = 3.3 V or 5 V. AVDD and AVSS can be a single 3.3 V or 5 V supply, or a ±1.65 V or ±2.5 V split supply. When using split supplies, consider the absolute maximum ratings (see the Absolute Maximum Ratings section).

IOVDD powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC IOVDD sets the voltage levels for the serial peripheral interface (SPI) of the ADC. IOVDD is referenced to DGND, and IOVDD to DGND can vary from 2 V (minimum) to 5.5 V (maximum).

### *Single-Supply Operation (AVSS = DGND)*

When the AD4112 is powered from a single supply connected to AVDD, the supply can be either 3.3 V or 5 V. In this configuration, AVSS and DGND can be shorted together on one single ground plane.

IOVDD can range from 2 V to 5.5 V in this unipolar input configuration.

## DIGITAL COMMUNICATION

The AD4112 has a 3-wire or 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ tied low. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. Data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

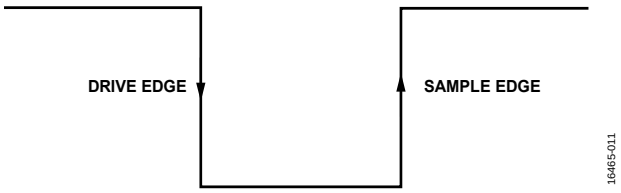



*Figure 32. SPI Mode 3 SCLK Edges*

### *Accessing the ADC Register Map*

The communications register controls access to the full register map of the ADC. This register is an 8-bit write only register. On power-up or after a reset, the digital interface defaults to a state where it is expecting a write to the communications register. Therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is being accessed and if the next operation is a read or write. The RA bits (Bits[5:0] in Register 0x00) determine the specific register to which the read or write operation applies.

When the read or write operation to the selected register is complete, the interface returns to its default state, where it expects a write operation to the communications register.

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to its default state by resetting the entire device, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high resets the digital interface to its default state and aborts any current operation.

Figure 33 and Figure 34 show writing to and reading from a register by first writing the 8-bit command to the communications register followed by the data for the addressed register.

Reading the ID register is the recommended method for verifying correct communication with the device. The ID register is a read only register and contains the value 0x30DX for the AD4112 The communication register and ID register details are described in Table 10 and Table 11.

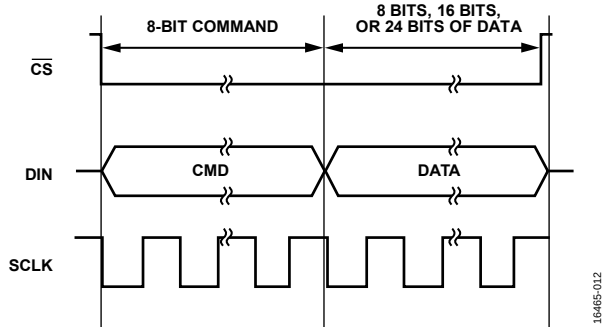



*Figure 33. Writing to a Register (8-Bit Command with Register Address Followed by Data of 8 Bits, 16 Bits, or 24 Bits; Data Length Is Dependent on the Register Selected)*

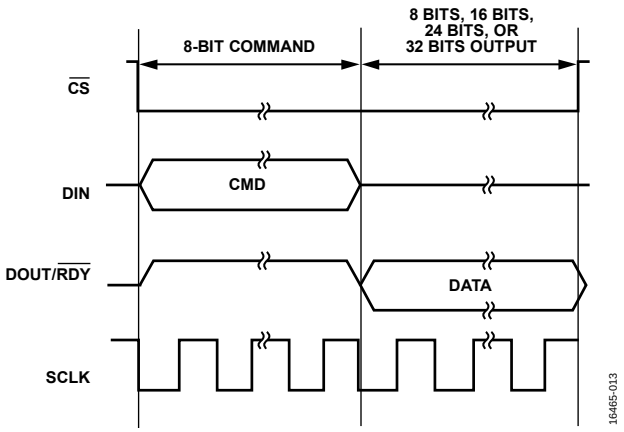



*Figure 34. Reading from a Register (8-Bit Command with Register Address Followed by Data of 8 Bits, 16 Bits, 24, or 32 Bits; Data Length on DOUT Is Dependent on the Register Selected)*

## AD4112 RESET

After a power-up cycle and when the power supplies are stable, a device reset is required. In situations where interface synchronization is lost, a device reset is also required. A write operation of at least 64 serial clock cycles with DIN high returns the ADC to the default state by resetting the entire device, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high sets the digital interface to the default state and halts any serial interface operation.

**Table 10. Communications Register Bit Map**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | COMMS | [7:0] | $\overline{WEN}$ | R/$\overline{W}$ | RA | | | | | | 0x00 | W |

**Table 11. ID Register Bit Map**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x07 | ID | [15:8] | ID[15:8] | | | | | | | | 0x30DX[1] | R |
| | | [7:0] | ID[7:0] | | | | | | | | | |

[1] X means don't care.

## CONFIGURATION OVERVIEW

After power-on or reset, the AD4112 default configuration is as follows:

- Channel configuration: Channel 0 is enabled, the VIN0 and VIN1 pair is selected as the input. Setup 0 is selected.
- Setup configuration: the analog input buffers are disabled and the reference input buffers are also disabled. The REF± pins are selected as the reference source. Note that for this setup, the default channel does not operate correctly because the input buffers need to be enabled for a VIN input.
- Filter configuration: the sinc5 + sinc1 filter is selected and the maximum output data rate of 31.25 kSPS is selected.
- ADC mode: continuous conversion mode and the internal oscillator are enabled. The internal reference is disabled.
- Interface mode: CRC and the data and status output are disabled.

Note that only a few of the register setting options are shown. This list is only an example. For full register information, see the Register Details section.

Figure 35 shows an overview of the suggested flow for changing the ADC configuration, divided into the following three blocks:

- Channel configuration (see Box A in Figure 35)
- Setup configuration (see Box B in Figure 35)
- ADC mode and interface mode configuration (see Box C in Figure 35)

### *Channel Configuration*

The AD4112 has 16 independent channels and 8 independent setups. The user can select any of the input pairs on any channel, as well as any of the eight setups for any channel, giving the user full flexibility in the channel configuration. This flexibility also allows per channel configuration when using differential inputs and single-ended inputs because each channel can have its own dedicated setup.

#### Channel Registers

The channel registers select which of the voltage or current inputs is used for that channel. This register also contains a channel enable/disable bit and the setup selection bits, which are used to select which of the eight available setups to use for this channel.

When the AD4112 is operating with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order, from Channel 0 to Channel 15. If a channel is disabled, it is skipped by the sequencer. Details of the channel register for Channel 0 are shown in Table 12.

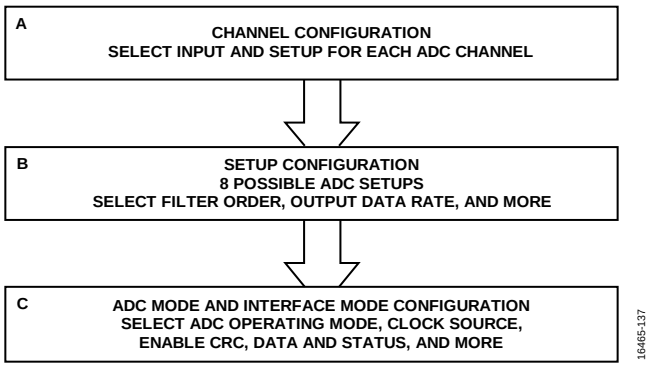



*Figure 35. Suggested ADC Configuration Flow*

**Table 12. Channel Register 0**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x10 | CH0 | [15:8] | CH_EN0 | SETUP_SEL0 | | | Reserved | | INPUT[9:8] | | 0x8001 | RW |
| | | [7:0] | INPUT[7:0] | | | | | | | | | |

### *ADC Setups*

The AD4112 has eight independent setups. Each setup consists of the following four registers:

- Setup configuration register
- Filter configuration register
- Gain register
- Offset register

For example, Setup 0 consists of Setup Configuration Register 0, Filter Configuration Register 0, Gain Register 0, and Offset Register 0. Figure 36 shows the grouping of these registers The setup is selectable from the channel registers (see the Channel Configuration section), which allows each channel to be assigned to one of eight separate setups. Table 13 through Table 16 show the four registers that are associated with Setup 0. This structure is repeated for Setup 1 to Setup 7.

#### Setup Configuration Registers

The setup configuration registers allow the user to select the output coding of the ADC by selecting between bipolar mode and unipolar mode. The user can select the reference source using these registers. Three options are available: a reference connected between the REF+ and REF− pins, the internal reference, or using AVDD − AVSS. The input and reference buffers can also be enabled or disabled using these registers.

#### Filter Configuration Registers

The filter configuration registers select which digital filter is used at the output of the ADC modulator. The order of the filter and the output data rate are selected by setting the bits in these registers. For more information, see the Digital Filter section.

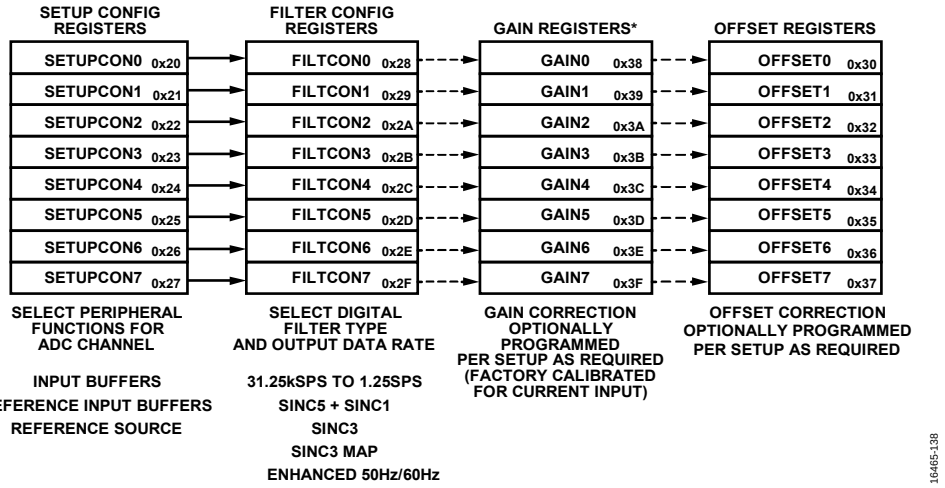



*Figure 36. ADC Setup Register Grouping*

**Table 13. Setup Configuration Register 0**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x20 | SETUPCON0 | [15:8] | Reserved | | | BI_UNIPOLAR0 | REFBUF0+ | REFBUF0− | INBUF0 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL0 | | Reserved | | | | | |

**Table 14. Filter Configuration Register 0**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x28 | FILTCON0 | [15:8] | SINC3_MAP0 | Reserved | | | ENHFILTEN0 | ENHFILT0 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER0 | | ODR0 | | | | | | |

**Table 15. Gain Register 0**

| Reg. | Name | Bits | Bits[23:0] | Reset | RW |
|---|---|---|---|---|---|
| 0x38 | GAIN0 | [23:0] | GAIN0[23:0] | 0x5XXXX0 | RW |

**Table 16. Offset Register 0**

| Reg. | Name | Bits | Bits[23:0] | Reset | RW |
|---|---|---|---|---|---|
| 0x30 | OFFSET0 | [23:0] | OFFSET0[23:0] | 0x800000 | RW |

### Gain Registers

The gain registers are 24-bit registers that hold the gain calibration coefficient for the ADC. The gain registers are read/write registers. At power-on, these registers are configured for current inputs with factory calibrated coefficients. Therefore, every device has different default coefficients. When enabling a voltage input on a channel register (see the Channel Registers section), the user must also update the gain register for the corresponding setup. For more information, see the Adjusting Voltage Input Gain section.

### Offset Registers

The offset registers hold the offset calibration coefficient for the ADC. The power-on reset value of the offset registers is 0x800000. The offset registers are 24-bit read and write registers.

## *ADC Mode and Interface Mode Configuration*

The ADC mode register and the interface mode register configure the core peripherals for use by the AD4112 and the mode for the digital interface.

### ADC Mode Register

The ADC mode register primarily sets the conversion mode of the ADC to either continuous or single conversion. The user can also select the standby and power-down modes, as well as any of the calibration modes. In addition, this register contains the clock source select bits and internal reference enable bit. The reference select bits are contained in the setup configuration registers (see the ADC Setups section for more information). The details of this register are shown in Table 17.

### Interface Mode Register

The interface mode register configures the digital interface operation. This register allows the user to control data-word length, CRC enable, data plus status read, and continuous read mode. The details of this register are shown in Table 18. For more information, see the Digital Interface section.

**Table 17. ADC Mode Register**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x01 | ADCMODE | [15:8] | REF_EN | Reserved | SING_CYC | Reserved | | Delay | | | 0x2000 | RW |
| | | [7:0] | Reserved | Mode | | | CLOCKSEL | | Reserved | | | |

**Table 18. Interface Mode Register**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x02 | IFMODE | [15:8] | Reserved | | | ALT_SYNC | IOSTRENGTH | Reserved | | DOUT_RESET | 0x0000 | RW |
| | | [7:0] | CONTREAD | DATA_STAT | REG_CHECK | Reserved | CRC_EN | | Reserved | WL16 | | |

# CIRCUIT DESCRIPTION

## MULTIPLEXER

There are nine voltage pins and eight current inputs: VIN0− to VIN7, VINCOM, IIN0+ to IIN3+, and IIN0− to IIN3−. Each of these pins connects to the internal multiplexer. The multiplexer enables these inputs to be configured as input pairs (see the Voltage Inputs section and the Current Inputs section for more information on how to set up these inputs). The AD4112 can have up to 16 active channels. When more than one channel is enabled, the channels are automatically sequenced in order from the lowest enabled channel number to the highest enabled channel number. The output of the multiplexer is connected to the input of the integrated true rail-to-rail buffers. These buffers can be bypassed and the multiplexer output can be directly connected to the switched capacitor input of the ADC. The simplified input circuits are shown in Figure 37 and Figure 38.

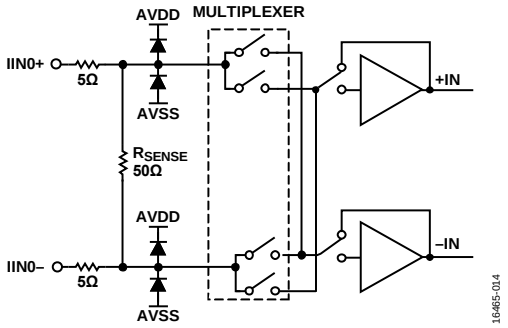



*Figure 37. Simplified Current Input Circuit*

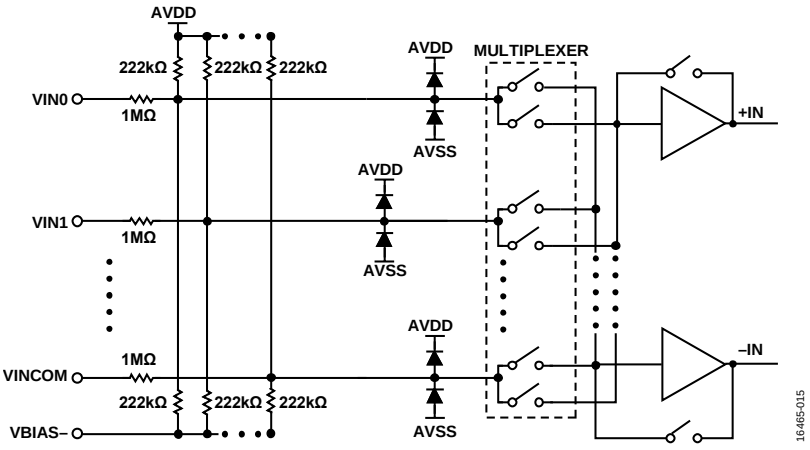



*Figure 38. Simplified Voltage Input Circuit*

## CURRENT INPUTS

There are four current input pins (IIN0+ to IIN3+) and four current return pins (IIN0− to IIN3−). Connect these pins in numbered pairs (for example, IIN0+ and IIN0−).

Disable the input buffers for the current inputs.

To achieve specified accuracy, the current channels are factory calibrated. This calibration value is stored in on-chip nonvolatile memory and is copied to all gain registers after a power-up or reset.

## VOLTAGE INPUTS

The AD4112 can be set up to have eight single-ended inputs or four fully differential inputs. The voltage divider on the analog front end has a division ratio of 10 and consists of precision matched resistors that enable an input range of ±20 V from a single 5 V power supply.

Enable the input buffers in the setup register for voltage input channels.

### *Fully Differential Inputs*

Due to the matching resistors on the analog front end, the differential inputs must be paired together in the following pairs: VIN0 and VIN1, VIN2 and VIN3, VIN4 and VIN5, and VIN6 and VIN7. If any two voltage inputs are paired in a configuration other than what is described in this data sheet, the accuracy of the device cannot be guaranteed.

### *Single-Ended Inputs*

The user can also choose to measure up to eight different single-ended voltage inputs. In this case, each of the voltage inputs must be paired with VINCOM. Connect VINCOM externally to AVSS.

### *Adjusting Voltage Input Gain*

After a power up or reset, all gain registers are loaded with factory calibration coefficients for current inputs. When using a voltage input, the corresponding gain register must be modified after powering up or resetting the device. Perform this modification by running an internal full-scale calibration (see the Calibration section for more information). Alternatively, the gain register can be overwritten with a nominal value of 0x55567C. However, a calibration is recommended because the ideal value varies from device to device.

Alternatively, the gain can be calibrated by connecting a precision voltage source to the voltage input and performing a full-scale system calibration.

## DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00 … 00, a midscale voltage resulting in a code of 100 … 000, and a full-scale input voltage resulting in a code of 111 … 111. The output code for any input voltage is represented as

$$Code = (2^N \times V_{IN} \times 0.1)/V_{REF}$$

The output code for any input current is represented as

$$Code = (2^N \times I_{IN} \times 50\ \Omega)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000 … 000, a zero differential input voltage resulting in a code of 100 … 000, and a positive full-scale input voltage resulting in a code of 111 … 111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times ((V_{IN} \times 0.1/V_{REF}) + 1)$$

The output code for any input current is represented as

$$Code = 2^{N-1} \times ((I_{IN} \times 50\ \Omega/V_{REF}) + 1)$$

where:
$N$ = 24.
$V_{IN}$ is the input voltage.
$V_{REF}$ is the reference voltage.
$I_{IN}$ is the input current.

## AD4112 REFERENCE

The AD4112 offers the user the option of either supplying an external reference to the REF+ and REF− pins of the device, using AVDD − AVSS, or by allowing the use of the internal 2.5 V, low noise, low drift reference. Select the reference source to be used by the analog input by setting the REF_SELx bits, Bits[5:4], in the setup configuration registers appropriately. The structure of the Setup Configuration 0 register is shown in Table 19. By default, the AD4112 uses an external reference on power-up.

### *Internal Reference*

The AD4112 includes a low noise, low drift voltage reference. The internal reference has a 2.5 V output. The internal reference is output on the REFOUT pin after the REF_EN bit in the ADC mode register is set and is decoupled to AVSS with a 0.1 µF capacitor. The AD4112 internal reference is disabled by default on power-up.

### External Reference

The AD4112 has a fully differential reference input applied through the REF+ and REF− pins. Standard low noise, low drift voltage references, such as the ADR4525, are recommended for use. Apply the external reference to the AD4112 reference pins as shown in Figure 39. Decouple the output of any external reference to AVSS. As shown in Figure 39, the ADR4525 output is decoupled with a 0.1 µF capacitor at the output for stability purposes. The output is then connected to a 4.7 µF capacitor, which acts as a reservoir for any dynamic charge required by the ADC, and is followed by a 0.1 µF decoupling capacitor at the REF+ input. This capacitor is placed as close as possible to the REF+ and REF− pins.

The REF− pin is connected directly to the AVSS potential. When an external reference is used instead of the internal reference to supply the AD4112, attention must be paid to the output of the REFOUT pin. The internal reference is controlled by the REF_EN bit (Bit 15) in the ADC mode register, which is shown in Table 20. If the internal reference is not being used elsewhere in the application, ensure that the REF_EN bit is disabled.

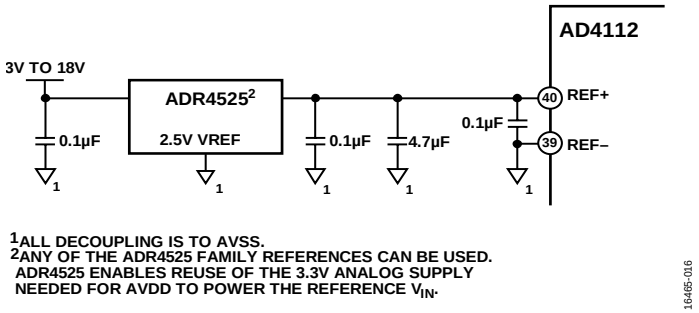



*Figure 39. ADR4525 Connected to AD4112 REF± Pins*

**Table 19. Setup Configuration 0 Register**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x20 | SETUPCON0 | [15:8] | Reserved | | | BI_UNIPOLAR0 | REFBUF0+ | REFBUF0− | INBUF0 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL0 | | Reserved | | | | | |

**Table 20. ADC Mode Register**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x01 | ADCMODE | [15:8] | REF_EN | Reserved | SING_CYC | Reserved | | Delay | | | 0x2000 | RW |
| | | [7:0] | Reserved | Mode | | | CLOCKSEL | Reserved | | | | |

## BUFFERED REFERENCE INPUT

The AD4112 has true rail-to-rail, integrated, precision unity gain buffers on both ADC reference inputs. The buffers provide the benefit of providing high input impedance and allowing high impedance external sources to be directly connected to the reference inputs. The integrated reference buffers can fully drive the internal reference switch capacitor sampling network, simplifying the reference circuit requirements. Each reference input buffer amplifier is fully chopped, meaning that it minimizes the offset error drift and 1/f noise of the buffer. When using a reference, such as the ADR4525, these buffers are not required because these references, with proper decoupling, can drive the reference inputs directly.

## CLOCK SOURCE

The AD4112 uses a nominal master clock of 2 MHz. The AD4112 can source its sampling clock from one of three sources:

- An internal oscillator.
- An external crystal (use a 16 MHz crystal automatically divided internally to set the 2 MHz clock).
- An external clock source.

All output data rates listed in the data sheet relate to a master clock rate of 2 MHz. Using a lower clock frequency from, for instance, an external source scales any listed data rate proportionally. To achieve the specified data rates, particularly rates for rejection of 50 Hz and 60 Hz, use a 2 MHz clock. The source of the master clock is selected by setting the CLOCKSEL bits (Bits[3:2]) in the ADC mode register, as shown in Table 20. The default operation on power-up and reset of the AD4112 is to operate with the internal oscillator. It is possible to fine tune the output data rate and filter notch at low output data rates using the SINC3_MAPx bits.

### *Internal Oscillator*

The internal oscillator runs at 16 MHz and is internally divided down to 2 MHz for the modulator and can be used as the ADC master clock. The internal oscillator is the default clock source for the AD4112 and is specified with an accuracy of −2.5% to +2.5%.

There is an option to allow the internal clock oscillator to be output on the XTAL2/CLKIO pin. The clock output is driven to the IOVDD logic level. This option can affect the dc performance of the AD4112 due to the disturbance introduced by the output driver. The extent to which the performance is affected depends on the IOVDD voltage supply. Higher IOVDD voltages create a wider logic output swing from the driver and affect performance to a greater extent. This effect is further exaggerated if the IOSTRENGTH bit is set at higher IOVDD levels (see Table 27 for more information).

### *External Crystal*

If higher precision, lower jitter clock sources are required, the AD4112 can use an external crystal to generate the master clock. The crystal is connected to the XTAL1 and XTAL2/CLKIO pins. A recommended crystal for use is the FA-20H, a 16 MHz, 10 ppm, 9 pF crystal from Epson-Toyocom that is available in a surface-mount package. As shown in Figure 40, insert two capacitors (CX1 and CX2) from the traces connecting the crystal to the XTAL1 and XTAL2/CLKIO pins. These capacitors allow circuit tuning. Connect these capacitors to the DGND pin. The value for these capacitors depends on the length and capacitance of the trace connections between the crystal and the XTAL1 and XTAL2/CLKIO pins. Therefore, the values of these capacitors differ depending on the PCB layout and the crystal used.

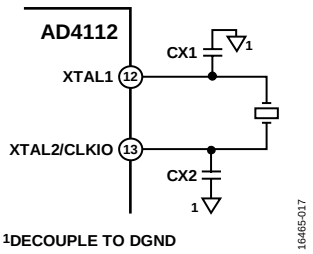



*Figure 40. External Crystal Connections*

The external crystal circuitry can be sensitive to the SCLK edges, depending on the SCLK frequency, IOVDD voltage, crystal circuitry layout, and the crystal used. During crystal startup, any disturbances caused by the SLCK edges may cause double edges on the crystal input, resulting in invalid conversions until the crystal voltage has reached a high enough level such that any interference from the SCLK edges is insufficient to cause double clocking. This double clocking can be avoided by ensuring that the crystal circuitry has reached a sufficient voltage level after startup before applying any SCLK.

Because of the nature of the crystal circuitry, it is recommended that empirical testing of the circuit be performed under the required conditions, with the final PCB layout and crystal, to ensure correct operation.

### *External Clock*

The AD4112 can also use an externally supplied clock. In systems where an externally supplied clock is used, the external clock is routed to the XTAL2/CLKIO pin. In this configuration, the XTAL2/ CLKIO pin accepts the externally sourced clock and routes it to the modulator. The logic level of this clock input is defined by the voltage applied to the IOVDD pin.

# DIGITAL FILTER

The AD4112 has three flexible filter options to allow optimization of noise, settling time, and rejection:

- The sinc5 + sinc1 filter.
- The sinc3 filter.
- Enhanced 50 Hz and 60 Hz rejection filters.

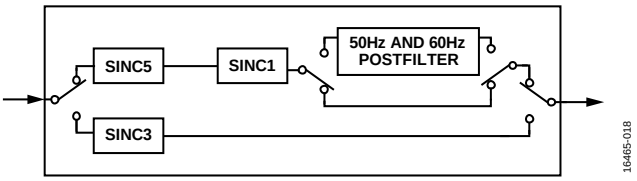



*Figure 41. Digital Filter Block Diagram*

The filter and output data rate are configured by setting the appropriate bits in the filter configuration register for the selected setup. Each channel can use a different setup and therefore, a different filter and output data rate. See the Register Details section for more information.

## SINC5 + SINC1 FILTER

The sinc5 + sinc1 filter is targeted at multiplexed applications and achieves single cycle settling at output data rates of 2.6 kSPS and less. The sinc5 block output is fixed at the maximum rate of 31.25 kSPS, and the sinc1 block output data rate can be varied to control the final ADC output data rate. Figure 42 shows the frequency domain response of the sinc5 + sinc1 filter at a 50 SPS output data rate. The sinc5 + sinc1 filter has a slow roll-off over frequency and narrow notches.

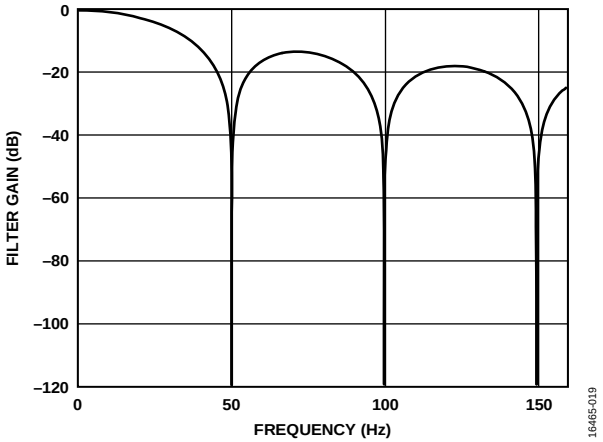



*Figure 42. Sinc5 + Sinc1 Filter Response at 50 SPS ODR*

The output data rates with the accompanying settling time and rms noise for the sinc5 + sinc1 filter are shown in in Table 6 and Table 7.

## SINC3 FILTER

The sinc3 filter achieves the best single-channel noise performance at lower rates and is, therefore, most suitable for single-channel applications. The sinc3 filter always has a settling time equal to

$$t_{SETTLE} = 3/Output\ Data\ Rate$$

Figure 43 shows the frequency domain filter response for the sinc3 filter. The sinc3 filter has good roll-off over frequency and has wide notches for good notch frequency rejection.

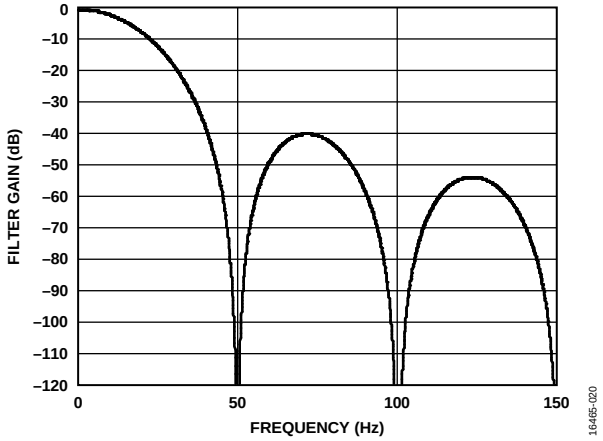



*Figure 43. Sinc3 Filter Response*

The output data rates with the accompanying settling time and rms noise for the sinc3 filter are shown in Table 8 and Table 9. It is possible to fine tune the output data rate for the sinc3 filter by setting the SINC3_MAPx bit in the filter configuration registers. If this bit is set, the mapping of the filter register changes to directly program the decimation rate of the sinc3 filter. All other options are eliminated. The data rate when on a single channel can be calculated using the following equation:

$$Output\ Data\ Rate = f_{MOD}/(32 \times FILTCONx[14:0])$$

where:

$f_{MOD}$ is the modulator rate (MCLK/2) and is equal to 1 MHz.
*FILTCONx[14:0]* are the contents on the filter configuration registers, excluding the MSB.

For example, an output data rate of 50 SPS can be achieved with SINC3_MAPx enabled by setting the FILTCONx[14:0] bits to a value of 625.

## SINGLE CYCLE SETTLING

The AD4112 can be configured by setting the SING_CYC bit in the ADC mode register so that only fully settled data is output, thus effectively putting the ADC into a single cycle settling mode. This mode achieves single cycle settling by reducing the output data rate to be equal to the settling time of the ADC for the selected output data rate. This bit has no effect with the sinc5 + sinc1 filter at output data rates of 2.6 kSPS and less or when multiple channels are enabled.

Figure 44 shows a step on the analog input with single cycle settling mode disabled and the sinc3 filter selected. The analog input requires at least three cycles after the step change for the output to reach the final settled value.

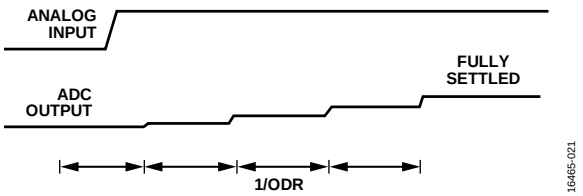



*Figure 44. Step Input Without Single Cycle Settling*

Figure 45 shows the same step on the analog input but with single cycle settling enabled. The analog input requires at least a single cycle for the output to be fully settled. The output data rate, as indicated by the $\overline{RDY}$ signal, is now reduced to equal the settling time of the filter at the selected output data rate.


*Figure 45. Step Input with Single Cycle Settling*

## ENHANCED 50 Hz AND 60 Hz REJECTION FILTERS

The enhanced filters provide rejection of 50 Hz and 60 Hz simultaneously and allow the user to trade off settling time and rejection. These filters can operate at up to 27.27 SPS or can reject up to 90 dB of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz interference. These filters are operated by postfiltering the output of the sinc5 + sinc1 filter. For this reason, the sinc5 + sinc1 filter must be selected when using the enhanced filters to achieve the specified settling time and noise performance. Table 21 and Table 22 show the output data rates with the accompanying settling time, rejection, and rms noise. Figure 46 to Figure 53 show the frequency domain plots of the responses from the enhanced filters.

**Table 21. Enhanced Filters Output Data Rate, Voltage Input Noise, Settling Time, and Rejection Using the Enhanced Filters**

| Output Data Rate (SPS) | Settling Time (ms) | Simultaneous Rejection of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz(dB)[1] | Noise (μV rms) | Peak-to-Peak Resolution (Bits) | Comments |
|---|---|---|---|---|---|
| 27.27 | 36.67 | 47 | 6.44 | 19.1 | See Figure 46 and Figure 49 |
| 25 | 40.0 | 62 | 6.09 | 19.2 | See Figure 47 and Figure 50 |
| 20 | 50.0 | 85 | 5.54 | 19.35 | See Figure 48 and Figure 51 |
| 16.667 | 60.0 | 90 | 5.38 | 19.51 | See Figure 52 and Figure 53 |

[1] Master clock = 2.00 MHz.

**Table 22. Enhanced Filters Output Data Rate, Current Input Noise, Settling Time, and Rejection Using the Enhanced Filters**

| Output Data Rate (SPS) | Settling Time (ms) | Simultaneous Rejection of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz(dB)[1] | Noise (nA rms) | Peak-to-Peak Resolution (Bits) | Comments |
|---|---|---|---|---|---|
| 27.27 | 36.67 | 47 | 7.69 | 21.4 | See Figure 46 and Figure 49 |
| 25 | 40.0 | 62 | 7.68 | 21.2 | See Figure 47 and Figure 50 |
| 20 | 50.0 | 85 | 7.26 | 21.7 | See Figure 48 and Figure 51 |
| 16.667 | 60.0 | 90 | 7.25 | 21.7 | See Figure 52 and Figure 53 |

[1] Master clock = 2.00 MHz.

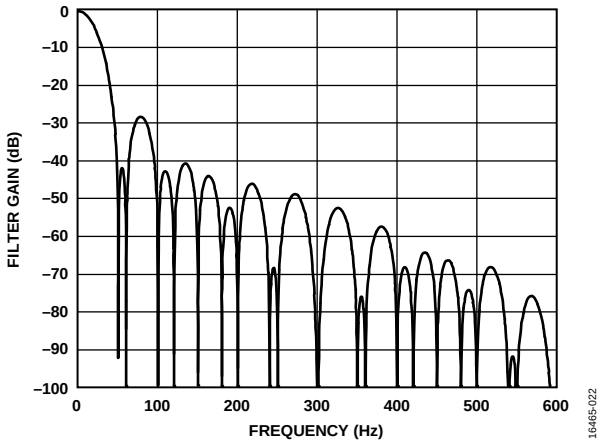



Figure 46. 27.27 SPS ODR, 36.67 ms Settling Time

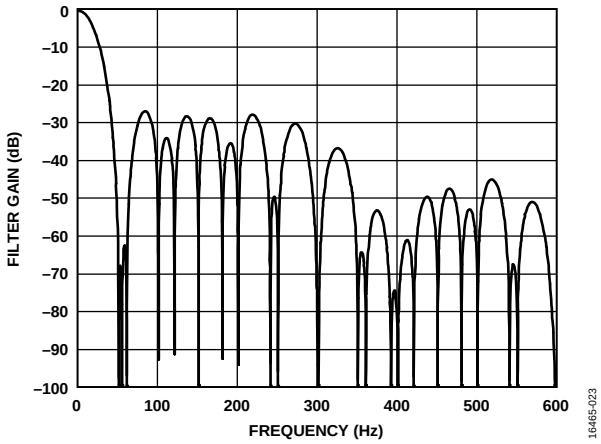



Figure 47. 25 SPS ODR, 40 ms Settling Time

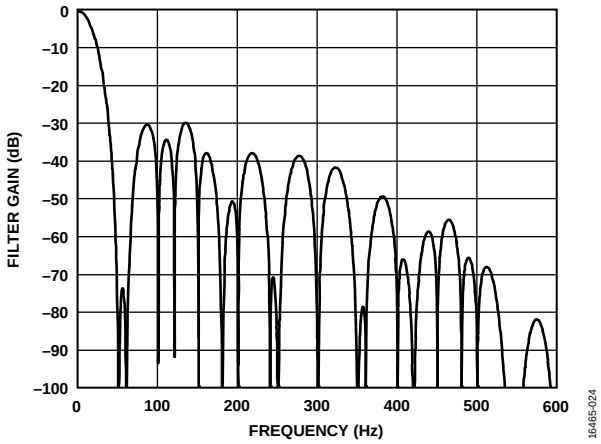



Figure 48. 20 SPS ODR, 50 ms Settling Time

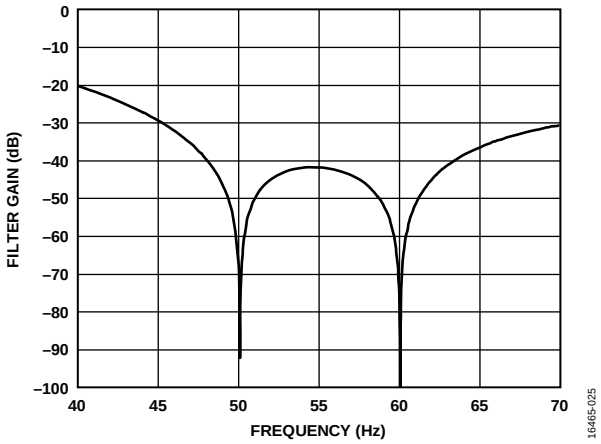



Figure 49. 27.27 SPS ODR, 36.67 ms Settling Time (40 Hz to 70 Hz)

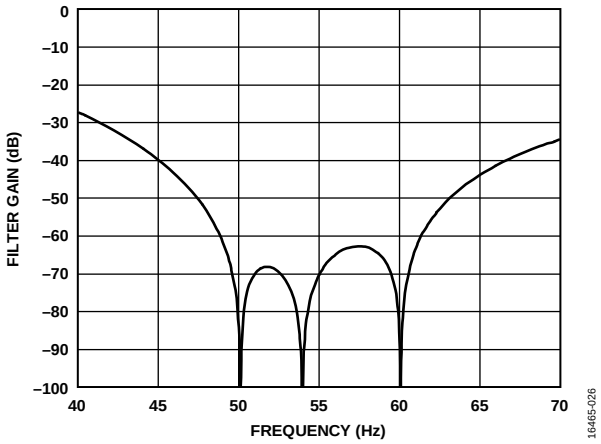



Figure 50. 25 SPS ODR, 40 ms Settling Time (40 Hz to 70 Hz)

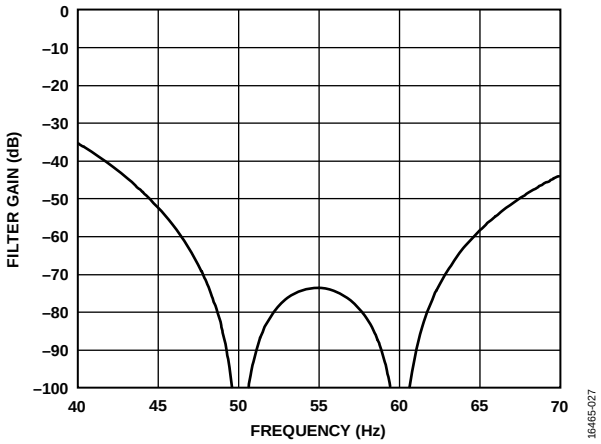



Figure 51. 20 SPS ODR, 50 ms Settling Time (40 Hz to 70 Hz)

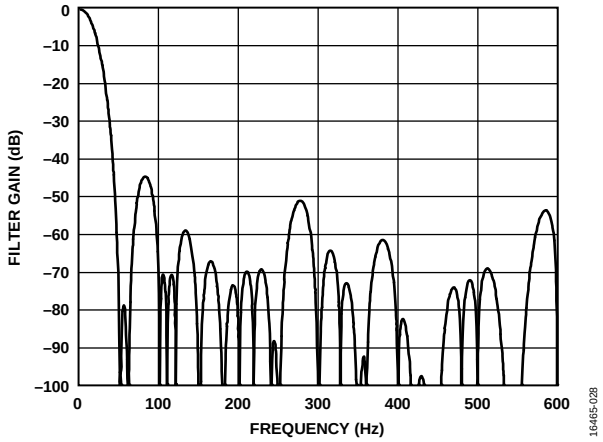



Figure 52. 16.667 SPS ODR, 60 ms Settling Time

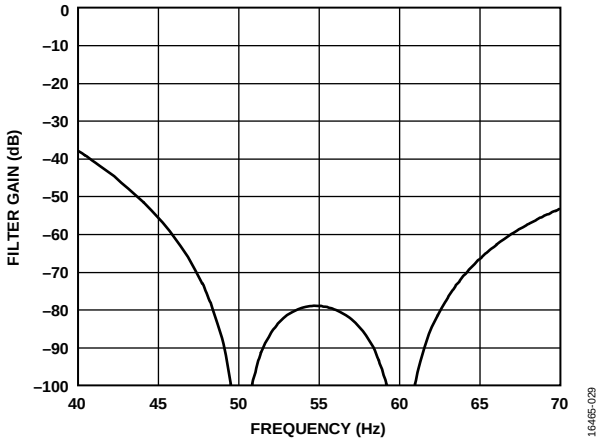



Figure 53. 16.667 SPS ODR, 60 ms Settling Time (40 Hz to 70 Hz)

# OPERATING MODES

The AD4112 has a number of operating modes that can be set from the ADC mode register and interface mode register (see Table 26 and Table 27). These modes are as follows:

- Continuous conversion mode
- Continuous read mode
- Single conversion mode
- Standby mode
- Power-down mode
- Calibration modes (four)

## CONTINUOUS CONVERSION MODE

Continuous conversion mode is the default power-up mode. The AD4112 converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the $\overline{RDY}$ output also goes low when a conversion is complete. To read a conversion, write to the communications register to indicate that the next operation is a read of the data register. When the data-word has been read from the data register, the DOUT/$\overline{RDY}$ pin goes high. The user can read this register additional times, if required. However, ensure that the data register is not being accessed at the completion of the next conversion. Otherwise, the new conversion word is lost.

When several channels are enabled, the ADC automatically sequences through the enabled channels, performing one conversion on each channel. When all the channels are converted, the sequence starts again with the first channel. The channels are converted in order from the lowest enabled channel to the highest enabled channel. The data register is updated as soon as each conversion is available. The $\overline{RDY}$ output pulses low each time a conversion is available. The user can then read the conversion while the ADC converts the next enabled channel.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion data, are output each time the data register is read. The four LSBs of the status register indicates the channel to which the conversion corresponds.

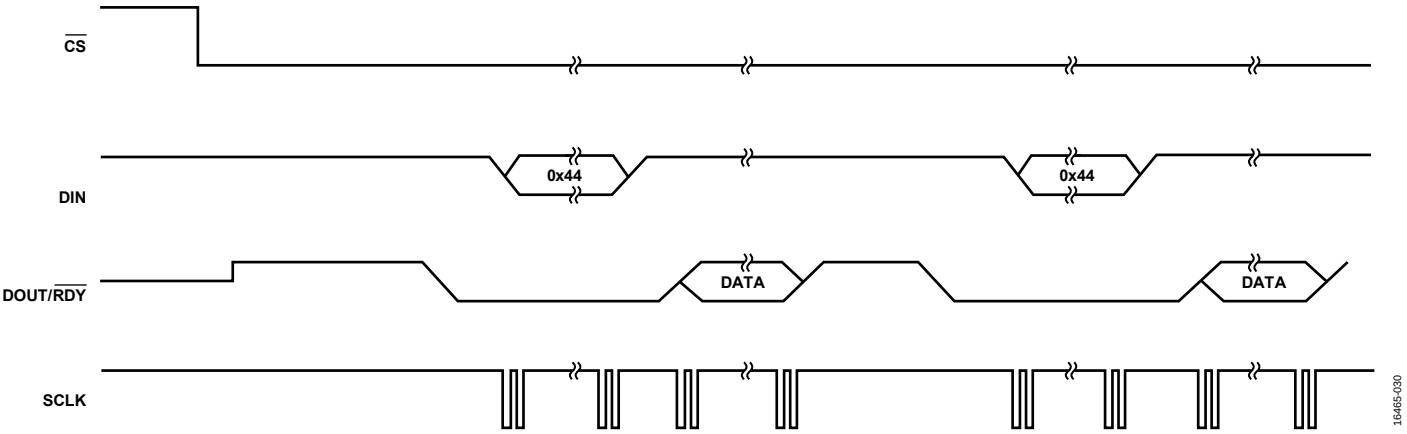



*Figure 54. Continuous Conversion Mode*

## CONTINUOUS READ MODE

In continuous read mode, it is not required to write to the communications register before reading ADC data. Apply only the required number of SCLKs after the $\overline{RDY}$ output goes low to indicate the end of a conversion. When the conversion is read, the $\overline{RDY}$ output returns high until the next conversion is available. In this mode, the data can be read only once. Ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion or if insufficient serial clocks are applied to the AD4112 to read the data-word, the serial output register is reset shortly before the next conversion is complete, and the new conversion is placed in the output serial register. The ADC must be configured for continuous conversion mode to use continuous read mode. To enable continuous read mode, set the CONTREAD bit in the interface mode register. When this bit is set, the only serial interface operations possible are reads from the data register. To exit continuous read mode, issue a dummy read of the ADC data register command (0x44) while the $\overline{RDY}$ output is low. Alternatively, apply a software reset (that is, 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1) to reset the ADC and all register contents. The dummy read and the software reset are the only commands that the interface recognizes after it is placed in continuous read mode. Hold DIN low in continuous read mode until an instruction is to be written to the device.

If multiple ADC channels are enabled, each channel is output in turn, with the status bits being appended to the data if the DATA_STAT bit is set in the interface mode register. The four LSBs of the status register indicates the channel to which the conversion corresponds.

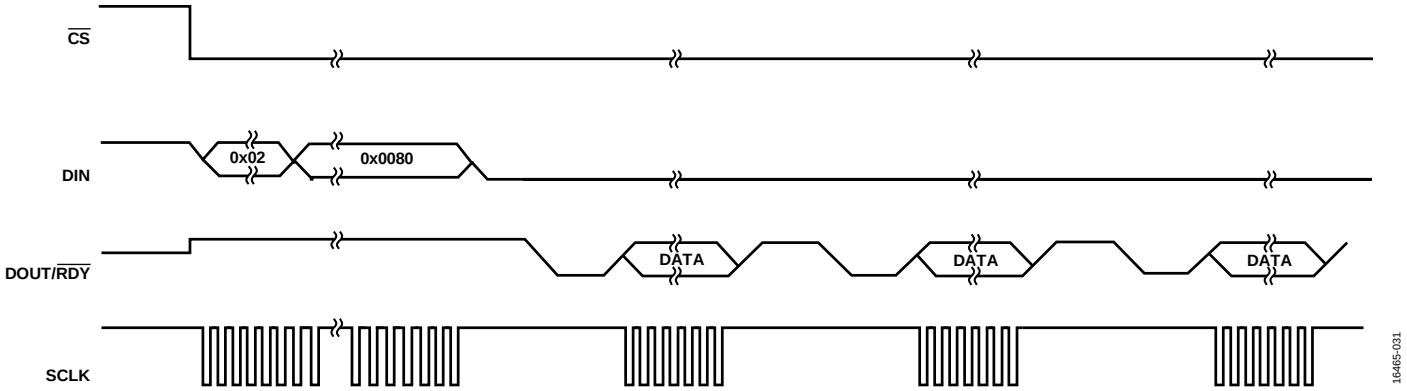



*Figure 55. Continuous Read Mode*

## SINGLE CONVERSION MODE

In single conversion mode, the AD4112 performs a single conversion and is placed in standby mode after the conversion is complete. The $\overline{RDY}$ output goes low to indicate the completion of a conversion. When the data-word has been read from the data register, the $\overline{RDY}$ output goes high. The data register can be read several times, if required, even when the $\overline{RDY}$ output goes high.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When the first conversion is started, the $\overline{RDY}$ output goes high and remains high until a valid conversion is available and $\overline{CS}$ is low. When the conversion is available, the $\overline{RDY}$ output goes low. The ADC then selects the next channel and begins a conversion. The user can read the present conversion while the next conversion is being performed. When the next conversion is complete, the data register is updated; therefore, the user has a limited period in which to read the conversion. When the ADC has performed a single conversion on each of the selected channels, it returns to standby mode.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion, are output each time the data register is read. The four LSBs of the status register indicate the channel to which the conversion corresponds.

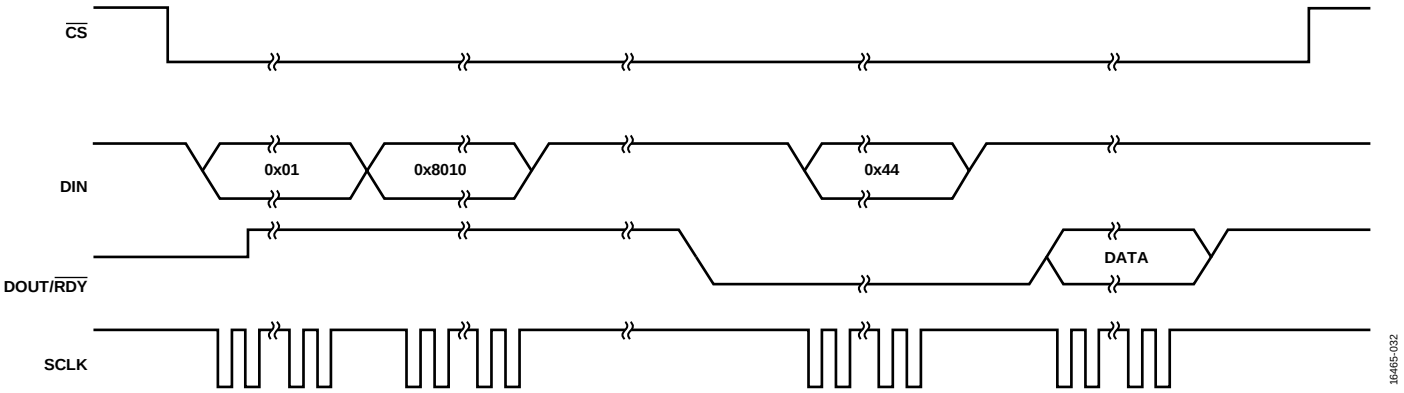



*Figure 56. Single Conversion Mode*

## STANDBY AND POWER-DOWN MODES

In standby mode, most blocks are powered down. The LDO regulators remain active so that the registers maintain their contents. The crystal oscillator remains active if selected. To power down the clock in standby mode, set the CLOCKSEL bits in the ADC mode register to 00 (internal oscillator mode).

In power-down mode, all blocks are powered down, including the LDO regulators. All registers lose their contents, and the GPIO outputs are placed in three-state. To prevent accidental entry to power-down mode, the ADC must first be placed in standby mode. Exiting power-down mode requires 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1, that is, a serial interface reset. A delay of 500 µs is recommended before issuing a subsequent serial interface command to allow the LDO regulator to power up.

## CALIBRATION

The AD4112 allows a two-point calibration to be performed to eliminate any offset and gain errors. Four calibration modes are used to eliminate these offset and gain errors on a per setup basis:

- Internal zero-scale calibration mode
- Internal full-scale calibration mode
- System zero-scale calibration mode
- System full-scale calibration mode

Only one channel can be active during calibration. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register.

The default value of the offset register is 0x800000, and the nominal value of the gain register is factory calibrated for the current channels; therefore, this value can vary from 0x500000 to 0x5FFFFF. When enabling a voltage channel, run an internal full-scale calibration. The following equations show the calculations that are used. In unipolar mode, the ideal relationship (that is, not taking into account the ADC gain error and offset error) is as follows:

$$Data = ((0.075 \times V_{IN}/V_{REF}) \times 2^{23} - (Offset - 0x800000)) \times (Gain/0x400000) \times 2$$

For a current input, the ideal relationship is as follows:

$$Data = ((0.75 \times (I_{IN} \times 50)/V_{REF}) \times 2^{123} - (Offset - 0x800000)) \times (Gain/0x400000) \times 2$$

In bipolar mode, the ideal relationship (that is, not taking into account the ADC gain error and offset error) is as follows:

$$Data = ((0.075 \times V_{IN}/V_{REF}) \times 2^{23} - (Offset - 0x800000)) \times (Gain/0x400000) + 0x800000$$

For a current input, the ideal relationship is as follows:

$$Data = ((0.75 \times (I_{IN} \times 50)/V_{REF}) \times 2^{23} - (Offset - 0x800000)) \times (Gain/0x400000) + 0x800000$$

To start a calibration, write the relevant value to the mode bits in the ADC mode register. The DOUT/$\overline{RDY}$ pin and the $\overline{RDY}$ bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding offset or gain register are updated, the $\overline{RDY}$ bit in the status register is reset and the $\overline{RDY}$ output pin returns low (if $\overline{CS}$ is low), and the AD4112 reverts to standby mode.

During an internal offset calibration both modulator inputs are connected internally to the selected negative analog input pin. Therefore, it is necessary to ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference. To perform an internal full-scale calibration, a full-scale input voltage is automatically connected to the ADC input for this calibration. Internal full-scale calibrations must only be performed on voltage inputs. Do not perform internal full-scale calibrations on the current inputs.

However, for system calibrations, the system zero-scale (offset) and system full-scale (gain) voltages must be applied to the input pins before initiating the calibration modes. As a result, errors external to the AD4112 are removed. The calibration range of the ADC gain for a system full-scale calibration on a voltage input is from 3.75 × $V_{REF}$ to 10.5 × $V_{REF}$. However, if 10.5 × $V_{REF}$ is greater than the absolute input voltage specification for the applied AVDD, use the specification as the upper limit instead of 10.5 × $V_{REF}$ (see the Specifications section).

Current inputs are factory calibrated. Therefore, it is not necessary to perform a system calibration. However if a system calibration is required, apply a full-scale value of 24 mA for a $V_{REF}$ = 2.5 V.

An internal zero-scale calibration only removes the offset error of the ADC core. It does not remove error from the resistive front end. A system zero-scale calibration reduces the offset error to the order of the noise on that channel.

From an operational point of view, treat a calibration like another ADC conversion. An offset calibration, if required, must always be performed before a full-scale calibration. Set the system software to monitor the $\overline{RDY}$ bit in the status register or the $\overline{RDY}$ output to determine the end of a calibration via a polling sequence or an interrupt driven routine. All calibrations require a time equal to the settling time of the selected filter and output data rate to be completed.

Any calibration can be performed at any output data rate. Using lower output data rates results in better calibration accuracy and is accurate for all output data rates. A new offset calibration is required for a given channel if the reference source for that channel is changed.

The AD4112 provides the user with access to the on-chip calibration registers, allowing the microprocessor to read the calibration coefficients of the device and to write its own calibration coefficients. A read or write of the offset and gain registers can be performed at any time except during an internal or self calibration.

# DIGITAL INTERFACE

The programmable functions of the AD4112 are accessible via the SPI serial interface. The serial interface of the AD4112 consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line transfers data into the on-chip registers. The DOUT output accesses data from the on-chip registers. SCLK is the serial clock input for the device. All data transfers (either on DIN or on DOUT) occur with respect to the SCLK signal.

The DOUT/$\overline{RDY}$ pin also functions as a data ready signal, with the line going low if $\overline{CS}$ is low when a new data-word is available in the data register. The pin is reset high when a read operation from the data register is complete. The $\overline{RDY}$ output also goes high before updating the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. Take care to avoid reading from the data register when $\overline{RDY}$ is about to go low. The best method to ensure that no data read occurs is to always monitor the $\overline{RDY}$ output. Start reading the data register as soon as $\overline{RDY}$ goes low, and ensure a sufficient SCLK rate, such that the read is completed before the next conversion result. $\overline{CS}$ is used to select a device. $\overline{CS}$ can be used to decode the AD4112 in systems where several components are connected to the serial bus.

Figure 2 and Figure 3 show timing diagrams for interfacing to the AD4112 using $\overline{CS}$ to decode the device. Figure 2 shows the timing for a read operation from the AD4112, and Figure 3 shows the timing for a write operation to the AD4112. It is possible to read from the data register several times, even though the $\overline{RDY}$ output returns high after the first read operation. However, take care to ensure that the read operations are completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD4112. The end of the conversion can also be monitored using the $\overline{RDY}$ bit in the status register.

The serial interface can be reset by writing 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1. A reset returns the interface to the state in which it expects a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, allow a period of 500 µs before addressing the serial interface.

## CHECKSUM PROTECTION

The AD4112 has a checksum mode that can be used to improve interface robustness. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERROR bit is set in the status register. However, to ensure that the register write was completed. It is important to read back the register and verify the checksum.

For CRC checksum calculations during a write operation, the following polynomial is always used:

$$x^8 + x^2 + x + 1$$

During read operations, the user can select between this polynomial and a similar exclusive OR (XOR) function. The XOR function requires less time to process on the host microcontroller than the polynomial-based checksum. The CRC_EN bits in the interface mode register enable and disable the checksum and allow the user to select between the polynomial check and the simple XOR check.

The checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8-bit to 24-bit data. For a read transaction, the checksum is calculated using the command word and the 8-bit to 32-bit data output. Figure 57 and Figure 58 show SPI write and read transactions, respectively.

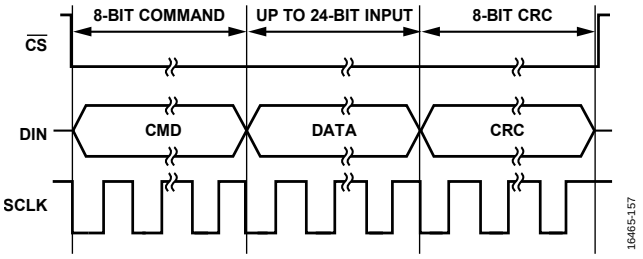



*Figure 57. SPI Write Transaction with CRC*

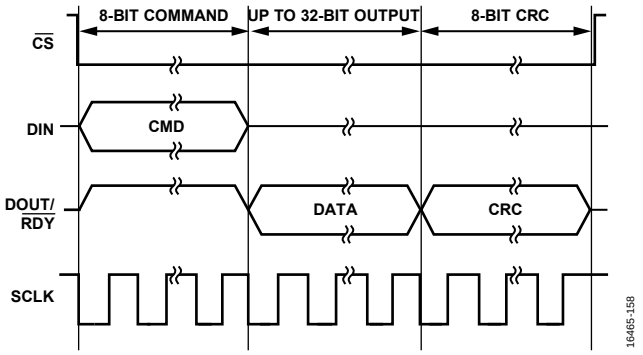



*Figure 58. SPI Read Transaction with CRC*

If checksum protection is enabled when continuous read mode is active, there is an implied read data command of 0x44 before every data transmission that must be accounted for when calculating the checksum value. The checksum protection ensures a nonzero checksum value even if the ADC data equals 0x000000.

## CRC CALCULATION

### *Polynomial*

The checksum, which is eight bits wide, is generated using the following polynomial:

$$x^8 + x^2 + x + 1$$

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This value is the 8-bit checksum.

**Example of a Polynomial CRC Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)**

An example of generating the 8-bit checksum using the polynomial based checksum is as follows.

```
Initial value       011001010100001100100001
                    011001010100001100100001000000000       left shifted eight bits
x8 + x2 + x + 1 =   100000111                                polynomial
   100100100000110010000100000000                           XOR result
   100000111                                                 polynomial
      100011000110010000100000000                            XOR result
      100000111                                              polynomial
         111111100100001000000000                            XOR result
         100000111                                           polynomial value
            111110111000010000000                            XOR result
            100000111                                        polynomial value
               111100000000100000000                         XOR result
               100000111                                     polynomial value
                  111001110000100000000                      XOR result
                  100000111                                  polynomial value
                     110010010010000000                      XOR result
                     100000111                               polynomial value
                        100101010100000000                   XOR result
                        100000111                            polynomial value
                           101101100000000                   XOR result
                           100000111                         polynomial value
                              1101011000000                  XOR result
                              100000111                      polynomial value
                                 101010110000                XOR result
                                 100000111                   polynomial value
                                    1010001000               XOR result
                                    100000111                polynomial value
                                       10000110              checksum = 0x86.
```

### *XOR Calculation*

The checksum, which is eight bits wide, is generated by splitting the data into bytes and then performing an XOR of the bytes.

**Example of an XOR Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)**

Using the example shown in the Polynomial section, divide the checksum into three bytes: 0x65, 0x43, and 0x21.

The XOR calculation is then as follows:

```
01100101    0x65
01000011    0x43
00100110    XOR result
00100001    0x21
00000111    CRC
```

# INTEGRATED FUNCTIONS

The AD4112 has a number of integrated functions.

## GENERAL-PURPOSE OUPUTS

The AD4112 has two general-purpose digital output pins (GPO0, GPO1). The GPO pins are enabled using the OP_EN0_1 bit in the GPIOCON register.

The GP_DATA0 and GP_DATA1 bits determines the logic level output at the pin, respectively. The logic levels for these pins are referenced to AVDD and AVSS. Therefore, outputs have an amplitude of either 5 V or 3.3 V depending on the AVDD − AVSS voltage.

The $\overline{\text{ERROR}}$ pin can also be used as a general-purpose output if the ERR_EN bits in the GPIOCON register are set to 11. In this configuration, the ERR_DAT bit in the GPIOCON register determines the logic level output at the $\overline{\text{ERROR}}$ pin. The logic level for the pin is referenced to IOVDD and DGND, and the $\overline{\text{ERROR}}$ pin has an active pull-up resistor.

## DELAY

It is possible to insert a programmable delay before the AD4112 begins to take samples. This delay allows an external amplifier or multiplexer to settle and can also alleviate the specification requirements for the external amplifier or multiplexer. Eight programmable settings, ranging from 0 µs to 8 ms, can be set using the delay bits in the ADC mode register (Register 0x01, Bits[10:8]).

## 16-BIT/24-BIT CONVERSIONS

By default, the AD4112 generates 24-bit conversions. However, the width of the conversions can be reduced to 16 bits. Setting Bit WL16 in the interface mode register to 1 rounds all data conversions to 16 bits. Clearing this bit sets the width of the data conversions to 24 bits.

## DOUT_RESET

The serial interface uses a shared DOUT/$\overline{\text{RDY}}$ pin. By default, this pin outputs the $\overline{\text{RDY}}$ signal. During a data read, this pin outputs the data from the register being read. After the read is complete, the pin reverts to outputting the $\overline{\text{RDY}}$ signal after a short fixed period of time ($t_7$). However, this time may be too short for some microcontrollers and can be extended until the $\overline{\text{CS}}$ pin is brought high by setting the DOUT_RESET bit in the interface mode register to 1. This setting means that $\overline{\text{CS}}$ must frame each read operation and complete the serial interface transaction.

## SYNCHRONIZATION

### *Normal Synchronization*

When the SYNC_EN bit in the GPIOCON register is set to 1, the $\overline{\text{SYNC}}$ pin functions as a synchronization pin. The $\overline{\text{SYNC}}$ input allows the user to reset the modulator and the digital filter without affecting any of the setup conditions on the device. This reset allows the user to start gathering samples of the analog input from a known point in time, that is, the rising edge of $\overline{\text{SYNC}}$. This pin must be low for at least one master clock cycle to ensure that synchronization occurs. If multiple channels are enabled, the sequencer is reset to the first enabled channel.

If multiple AD4112 devices are operated from a common master clock, they can be synchronized so that their data registers are updated simultaneously. Synchronization is normally done after each AD4112 has performed its own calibration or has calibration coefficients loaded into its calibration registers. A falling edge on the $\overline{\text{SYNC}}$ pin resets the digital filter and the analog modulator and places the AD4112 into a consistent known state. While the $\overline{\text{SYNC}}$ pin is low, the AD4112 is maintained in this state. On the $\overline{\text{SYNC}}$ rising edge, the modulator and filter are taken out of this reset state, and on the next master clock edge, the device starts to gather input samples again.

The device is taken out of reset on the master clock falling edge following the $\overline{\text{SYNC}}$ low-to-high transition. Therefore, when multiple devices are being synchronized, take the $\overline{\text{SYNC}}$ pin high on the master clock rising edge to ensure that all devices begin sampling on the master clock falling edge. If the $\overline{\text{SYNC}}$ pin is not taken high in sufficient time, it is possible to have a difference of one master clock cycle between the devices, that is, the instant at which conversions are available differs from device to device by a maximum of one master clock cycle.

The $\overline{\text{SYNC}}$ input can also be used as a start conversion command for a single channel when in normal synchronization mode. In this mode, the rising edge of the $\overline{\text{SYNC}}$ input starts a conversion, and the falling edge of the $\overline{\text{RDY}}$ output indicates when the conversion is complete. The settling time of the filter is required for each data register update. After the conversion is complete, bring the $\overline{\text{SYNC}}$ input low in preparation for the next conversion start signal.

### *Alternate Synchronization*

In alternate synchronization mode, the $\overline{\text{SYNC}}$ input operates as a start conversion command when several channels of the AD4112 are enabled. Setting the ALT_SYNC bit in the interface mode register to 1 enables an alternate synchronization scheme. When the $\overline{\text{SYNC}}$ input is taken low, the ADC completes the conversion on the enabled channel, selects the next channel in the sequence, and then waits until the $\overline{\text{SYNC}}$ input is taken high to start the conversion. The $\overline{\text{RDY}}$ output goes low when the conversion is complete on the current channel, and the data register is updated with the corresponding conversion. Therefore, the $\overline{\text{SYNC}}$ input does not interfere with the sampling on the currently selected channel but allows the user to control the instant at which the conversion begins on the next channel in the sequence.

Alternate synchronization mode can be used only when several channels are enabled. It is not recommended to use this mode when a single channel is enabled.

## ERROR FLAGS

The status register contains three error bits (ADC_ERROR, CRC_ERROR, and REG_ERROR) that flag errors with the ADC conversion, errors with the CRC check, and errors caused by changes in the registers, respectively. In addition, the $\overline{\text{ERROR}}$ output can indicate that an error has occurred.

### *ADC_ERROR*

The ADC_ERROR bit in the status register flags any errors that occur during the conversion process. The flag is set when an overrange or underrange result is output from the ADC. The ADC also outputs all 0s or all 1s when an undervoltage or overvoltage occurs. This flag is reset only when the overvoltage or undervoltage is removed. This flag is not reset by a read of the data register.

### *CRC_ERROR*

If the CRC value that accompanies a write operation does not correspond with the information sent, the CRC_ERROR flag is set. The flag is reset as soon as the status register is explicitly read.

### *REG_ERROR*

The REG_ERROR flag is used in conjunction with the REG_CHECK bit in the interface mode register. When the REG_CHECK bit is set, the AD4112 monitors the values in the on-chip registers. If a bit changes, the REG_ERROR bit is set to 1. Therefore, for writes to the on-chip registers, set the REG_CHECK bit to 0. When the registers have been updated, the REG_CHECK bit can be set to 1. The AD4112 calculates a checksum of the on-chip registers. If one of the register values has changed, the REG_ERROR bit is set to 1. If an error is flagged, the REG_CHECK bit must be set to 0 to clear the REG_ERROR bit in the status register. The register check function does not monitor the data register, status register, or interface mode register.

### *$\overline{\text{ERROR}}$ Input/Output*

The $\overline{\text{ERROR}}$ pin functions as an error input/output pin or as a general-purpose output pin. The ERR_EN bits in the GPIOCON register determine the function of the pin.

When ERR_EN is set to 10, the $\overline{\text{ERROR}}$ pin functions as an open-drain error output. The three error bits in the status register (ADC_ERROR, CRC_ERROR, and REG_ERROR) are ORed, inverted, and mapped to the $\overline{\text{ERROR}}$ output. Therefore, the $\overline{\text{ERROR}}$ output indicates that an error has occurred. The status register must be read to identify the error source.

When ERR_EN is set to 01, the $\overline{\text{ERROR}}$ pin functions as an error input. The error output of another component can be connected to the AD4112 $\overline{\text{ERROR}}$ input so that the AD4112 indicates when an error occurs on either itself or the external component. The value on the $\overline{\text{ERROR}}$ input is inverted and ORed with the errors from the ADC conversion, and the result is indicated via the ADC_ERROR bit in the status register. The value of the $\overline{\text{ERROR}}$ input is reflected in the ERR_DAT bit in the GPIO configuration register.

The $\overline{\text{ERROR}}$ input/output is disabled when ERR_EN is set to 00. When the ERR_EN bits are set to 11, the $\overline{\text{ERROR}}$ pin operates as a general-purpose output where the ERR_DAT bit is used to determine the logic level of the pin.

## DATA_STAT

The contents of the status register can be appended to each conversion on the AD4112 using the DATA_STAT bit in the IFMODE register. This function is useful if several channels are enabled. Each time a conversion is output, the contents of the status register are appended. The four LSBs of the status register indicate to which channel the conversion corresponds. In addition, the user can determine if any errors are being flagged by the error bits.

## IOSTRENGTH

The serial interface can operate with a power supply as low as 2 V. However, at this low voltage, the DOUT/$\overline{\text{RDY}}$ pin may not have sufficient drive strength if there is moderate parasitic capacitance on the board or if the SCLK frequency is high. The IOSTRENGTH bit in the interface mode register increases the drive strength of the DOUT/$\overline{\text{RDY}}$ pin.

## INTERNAL TEMPERATURE SENSOR

The AD4112 has an integrated temperature sensor. The temperature sensor can be used as a guide for the ambient temperature at which the device is operating. The ambient temperature can be used for diagnostic purposes or as an indicator of when the application circuit must rerun a calibration routine to take into account a shift in operating temperature. The temperature sensor is selected using the multiplexer and is selected in the same way as an input channel.

The temperature sensor requires that the input buffers be enabled on both inputs and the internal reference be enabled.

To use the temperature sensor, the first step is to calibrate the device in a known temperature (25°C) and take a conversion as a reference point. The temperature sensor has a nominal sensitivity of 477 µV/K. The difference in this ideal slope and the slope measured can calibrate the temperature sensor. The temperature sensor is specified with a ±2°C typical accuracy after calibration at 25°C. Calculate the temperature as follows:

$$\textit{Temperature}\ (°C) = (\textit{Conversion Result} \div 477\ \mu V) - 273.15$$

# APPLICATIONS INFORMATION

## IEC61000-4-x AND CISPR 11 ROBUSTNESS

PLC and DCS modules often operate in harsh industrial environments and must survive electromagnetic interference (EMI) conditions. To aid the design of electromagnetic compatibility (EMC) capable solutions, the AN-1572 Application Note is available. AN-1572 details all the necessary information on the test procedures used, as well as the layout and board design schematics necessary to design an EMC proven input module for the AD4111. The board ensures that the circuit performance is not permanently affected by radiated radio frequency (RF) or conducted RF disturbances and has sufficient immunity against electrostatic discharge (ESD), electrical fast transients (EFT), and surge as per the IEC61000-4-x standards. The AD4111 was also evaluated for CISPR 11, where the radiated emissions for the board are less than the Class A limits.

## GROUNDING AND LAYOUT

The inputs and reference inputs are differential and, therefore, most of the voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the device removes common-mode noise on these inputs. The analog and digital supplies to the AD4112 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the master clock frequency.

The digital filter also removes noise from the analog inputs and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD4112 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD4112 is high and the noise levels from the converter are so low, take care with regard to grounding and layout.

The PCB that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it results in the best shielding.

In any layout, the user must keep in mind the flow of currents in the system, ensuring that the paths for all return currents are as close as possible to the paths the currents took to reach their destinations.

Avoid running digital lines under the device because this couples noise onto the die and allows the analog ground plane to run under the AD4112 to prevent noise coupling. The power supply lines to the AD4112 must use as wide a trace as possible to provide low impedance paths and reduce glitches on the power supply line. Shield fast switching signals like clocks with digital ground to prevent radiating noise to other sections of the board and never run clock signals near the inputs. Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This layout reduces the effects of feedthrough on the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, whereas signals are placed on the solder side.

Proper decoupling is important when using high resolution ADCs. The AD4112 has two power supply pins: AVDD and IOVDD. The AVDD pin is referenced to AVSS, and the IOVDD pin is referenced to DGND. Decouple AVDD with a 10 µF tantalum capacitor in parallel with a 0.1 µF capacitor to AVSS on each pin. Place the 0.1 µF capacitor as near as possible to the device on each supply, ideally right up against the device. Decouple IOVDD with a 10 µF tantalum capacitor, in parallel with a 0.1 µF capacitor to DGND. Decouple all inputs to AVSS. If an external reference is used, decouple the REF+ and REF− pins to AVSS.

The AD4112 also has two on-board LDO regulators: one that regulates the AVDD supply, and one that regulates the IOVDD supply. For the REGCAPA pin, it is recommended that 1 µF and 0.1 µF capacitors to AVSS be used. Similarly, for the REGCAPD pin, it is recommended that 1 µF and 0.1 µF capacitors to DGND be used.

# REGISTER SUMMARY

**Table 23. Register Summary**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | COMMS | [7:0] | $\overline{WEN}$ | R/$\overline{W}$ | RA | | | | | | 0x00 | W |
| 0x00 | Status | [7:0] | $\overline{RDY}$ | ADC_ERROR | CRC_ERROR | REG_ERROR | Channel | | | | 0x80 | R |
| 0x01 | ADCMODE | [15:8] | REF_EN | Reserved | SING_CYC | Reserved | | Delay | | | 0x2000 | RW |
| | | [7:0] | Reserved | Mode | | | CLOCKSEL | | Reserved | | | |
| 0x02 | IFMODE | [15:8] | Reserved | | | ALT_SYNC | IOSTRENGTH | Reserved | | DOUT_RESET | 0x0000 | RW |
| | | [7:0] | CONTREAD | DATA_STAT | REG_CHECK | Reserved | CRC_EN | | Reserved | WL16 | | |
| 0x03 | REGCHECK | [23:16] | REGISTER_CHECK[23:16] | | | | | | | | 0x000000 | R |
| | | [15:8] | REGISTER_CHECK[15:8] | | | | | | | | | |
| | | [7:0] | REGISTER_CHECK[7:0] | | | | | | | | | |
| 0x04 | Data | [23:16] | Data [23:16] | | | | | | | | 0x000000 | R |
| | | [15:8] | Data [15:8] | | | | | | | | | |
| | | [7:0] | Data [7:0] | | | | | | | | | |
| 0x06 | GPIOCON | [15:8] | Reserved | Reserved | OP_EN0_1 | Reserved | SYNC_EN | ERR_EN | | ERR_DAT | 0x0800 | RW |
| | | [7:0] | GP_DATA1 | GP_DATA0 | Reserved | | | | | | | |
| 0x07 | ID | [15:8] | ID[15:8] | | | | | | | | 0x30Dx | R |
| | | [7:0] | ID[7:0] | | | | | | | | | |
| 0x10 | CH0 | [15:8] | CH_EN0 | SETUP_SEL0 | | | Reserved | | INPUT0[9:8] | | 0x8001 | RW |
| | | [7:0] | INPUT0 [7:0] | | | | | | | | | |
| 0x11 | CH1 | [15:8] | CH_EN1 | SETUP_SEL1 | | | Reserved | | INPUT1[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT1[7:0] | | | | | | | | | |
| 0x12 | CH2 | [15:8] | CH_EN2 | SETUP_SEL2 | | | Reserved | | INPUT2[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT2[7:0] | | | | | | | | | |
| 0x13 | CH3 | [15:8] | CH_EN3 | SETUP_SEL3 | | | Reserved | | INPUT3[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT3[7:0] | | | | | | | | | |
| 0x14 | CH4 | [15:8] | CH_EN4 | SETUP_SEL4 | | | Reserved | | INPUT4[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT4[7:0] | | | | | | | | | |
| 0x15 | CH5 | [15:8] | CH_EN5 | SETUP_SEL5 | | | Reserved | | INPUT5[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT5[7:0] | | | | | | | | | |
| 0x16 | CH6 | [15:8] | CH_EN6 | SETUP_SEL6 | | | Reserved | | INPUT6[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT6[7:0] | | | | | | | | | |
| 0x17 | CH7 | [15:8] | CH_EN7 | SETUP_SEL7 | | | Reserved | | INPUT7[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT7[7:0] | | | | | | | | | |
| 0x18 | CH8 | [15:8] | CH_EN8 | SETUP_SEL8 | | | Reserved | | INPUT8[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT8[7:0] | | | | | | | | | |
| 0x19 | CH9 | [15:8] | CH_EN9 | SETUP_SEL9 | | | Reserved | | INPUT9[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT9[7:0] | | | | | | | | | |
| 0x1A | CH10 | [15:8] | CH_EN10 | SETUP_SEL10 | | | Reserved | | INPUT10[9:8] | | 0x0001 | RW |
| | | [7:0] | Input10[7:0] | | | | | | | | | |
| 0x1B | CH11 | [15:8] | CH_EN11 | SETUP_SEL11 | | | Reserved | | INPUT11[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT11[7:0] | | | | | | | | | |
| 0x1C | CH12 | [15:8] | CH_EN12 | SETUP_SEL12 | | | Reserved | | INPUT12[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT12[7:0] | | | | | | | | | |
| 0x1D | CH13 | [15:8] | CH_EN13 | SETUP_SEL13 | | | Reserved | | INPUT13[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT13[7:0] | | | | | | | | | |
| 0x1E | CH14 | [15:8] | CH_EN14 | SETUP_SEL14 | | | Reserved | | INPUT14[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT14[7:0] | | | | | | | | | |
| 0x1F | CH15 | [15:8] | CH_EN15 | SETUP_SEL15 | | | Reserved | | INPUT15[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT15[7:0] | | | | | | | | | |
| 0x20 | SETUPCON0 | [15:8] | Reserved | | | BI_UNIPOLAR0 | REFBUF0+ | REFBUF0− | INBUF0 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL0 | | Reserved | | | | | |
| 0x21 | SETUPCON1 | [15:8] | Reserved | | | BI_UNIPOLAR1 | REFBUF1+ | REFBUF1− | INBUF1 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL1 | | Reserved | | | | | |

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x22 | SETUPCON2 | [15:8] | Reserved | | | BI_UNIPOLAR2 | REFBUF2+ | REFBUF2− | INBUF2 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL2 | | Reserved | | | | | |
| 0x23 | SETUPCON3 | [15:8] | Reserved | | | BI_UNIPOLAR3 | REFBUF3+ | REFBUF3− | INBUF3 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL3 | | Reserved | | | | | |
| 0x24 | SETUPCON4 | [15:8] | Reserved | | | BI_UNIPOLAR4 | REFBUF4+ | REFBUF4− | INBUF4 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL4 | | Reserved | | | | | |
| 0x25 | SETUPCON5 | [15:8] | Reserved | | | BI_UNIPOLAR5 | REFBUF5+ | REFBUF5− | INBUF5 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL5 | | Reserved | | | | | |
| 0x26 | SETUPCON6 | [15:8] | Reserved | | | BI_UNIPOLAR6 | REFBUF6+ | REFBUF6− | INBUF6 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL6 | | Reserved | | | | | |
| 0x27 | SETUPCON7 | [15:8] | Reserved | | | BI_UNIPOLAR7 | REFBUF7+ | REFBUF7− | INBUF7 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | REF_SEL7 | | Reserved | | | | | |
| 0x28 | FILTCON0 | [15:8] | SINC3_MAP0 | Reserved | | | ENHFILTEN0 | ENHFILT0 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER0 | | ODR0 | | | | | | |
| 0x29 | FILTCON1 | [15:8] | SINC3_MAP1 | Reserved | | | ENHFILTEN1 | ENHFILT1 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER1 | | ODR1 | | | | | | |
| 0x2A | FILTCON2 | [15:8] | SINC3_MAP2 | Reserved | | | ENHFILTEN2 | ENHFILT2 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER2 | | ODR2 | | | | | | |
| 0x2B | FILTCON3 | [15:8] | SINC3_MAP3 | Reserved | | | ENHFILTEN3 | ENHFILT3 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER3 | | ODR3 | | | | | | |
| 0x2C | FILTCON4 | [15:8] | SINC3_MAP4 | Reserved | | | ENHFILTEN4 | ENHFILT4 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER4 | | ODR4 | | | | | | |
| 0x2D | FILTCON5 | [15:8] | SINC3_MAP5 | Reserved | | | ENHFILTEN5 | ENHFILT5 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER5 | | ODR5 | | | | | | |
| 0x2E | FILTCON6 | [15:8] | SINC3_MAP6 | Reserved | | | ENHFILTEN6 | ENHFILT6 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER6 | | ODR6 | | | | | | |
| 0x2F | FILTCON7 | [15:8] | SINC3_MAP7 | Reserved | | | ENHFILTEN7 | ENHFILT7 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER7 | | ODR7 | | | | | | |
| 0x30 | OFFSET0 | [23:0] | OFFSET0[23:0] | | | | | | | | 0x800000 | RW |
| 0x31 | OFFSET1 | [23:0] | OFFSET1[23:0] | | | | | | | | 0x800000 | RW |
| 0x32 | OFFSET2 | [23:0] | OFFSET2[23:0] | | | | | | | | 0x800000 | RW |
| 0x33 | OFFSET3 | [23:0] | OFFSET3[23:0] | | | | | | | | 0x800000 | RW |
| 0x34 | OFFSET4 | [23:0] | OFFSET4[23:0] | | | | | | | | 0x800000 | RW |
| 0x35 | OFFSET5 | [23:0] | OFFSET5[23:0] | | | | | | | | 0x800000 | RW |
| 0x36 | OFFSET6 | [23:0] | OFFSET6[23:0] | | | | | | | | 0x800000 | RW |
| 0x37 | OFFSET7 | [23:0] | OFFSET7[23:0] | | | | | | | | 0x800000 | RW |
| 0x38 | GAIN0 | [23:0] | GAIN0[23:0] | | | | | | | | 0x5XXXX0 | RW |
| 0x39 | GAIN1 | [23:0] | GAIN1[23:0] | | | | | | | | 0x5XXXX0 | RW |
| 0x3A | GAIN2 | [23:0] | GAIN2[23:0] | | | | | | | | 0x5XXXX0 | RW |
| 0x3B | GAIN3 | [23:0] | GAIN3[23:0] | | | | | | | | 0x5XXXX0 | RW |
| 0x3C | GAIN4 | [23:0] | GAIN4[23:0] | | | | | | | | 0x5XXXX0 | RW |
| 0x3D | GAIN5 | [23:0] | GAIN5[23:0] | | | | | | | | 0x5XXXX0 | RW |
| 0x3E | GAIN6 | [23:0] | GAIN6[23:0] | | | | | | | | 0x5XXXX0 | RW |
| 0x3F | GAIN7 | [23:0] | GAIN7[23:0] | | | | | | | | 0x5XXXX0 | RW |

# REGISTER DETAILS

## COMMUNICATIONS REGISTER

**Address: 0x00, Reset: 0x00, Name: COMMS**

All access to the on-chip registers must start with a write to the communications register. This write determines which register is accessed next and whether that operation is a write or a read.

**Table 24. Bit Descriptions for COMMS**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | $\overline{WEN}$ | | This bit must be low to begin communications with the ADC | 0x0 | W |
| 6 | R/$\overline{W}$ | | This bit determines if the command is a read or write operation | 0x0 | W |
| | | 0 | Write command | | |
| | | 1 | Read command | | |
| [5:0] | RA | | The register address bits determine the register to be read from or written to as part of the current communication | 0x00 | W |
| | | 000000 | Status register | | |
| | | 000001 | ADC mode register | | |
| | | 000010 | Interface mode register | | |
| | | 000011 | Register checksum register | | |
| | | 000100 | Data register | | |
| | | 000110 | GPIO configuration register | | |
| | | 000111 | ID register | | |
| | | 010000 | Channel 0 register | | |
| | | 010001 | Channel 1 register | | |
| | | 010010 | Channel 2 register | | |
| | | 010011 | Channel 3 register | | |
| | | 010100 | Channel 4 register | | |
| | | 010101 | Channel 5 register | | |
| | | 010110 | Channel 6 register | | |
| | | 010111 | Channel 7 register | | |
| | | 011000 | Channel 8 register | | |
| | | 011001 | Channel 9 register | | |
| | | 011010 | Channel 10 register | | |
| | | 011011 | Channel 11 register | | |
| | | 011100 | Channel 12 register | | |
| | | 011101 | Channel 13 register | | |
| | | 011110 | Channel 14 register | | |
| | | 011111 | Channel 15 register | | |
| | | 100000 | Setup Configuration 0 register | | |
| | | 100001 | Setup Configuration 1 register | | |
| | | 100010 | Setup Configuration 2 register | | |
| | | 100011 | Setup Configuration 3 register | | |
| | | 100100 | Setup Configuration 4 register | | |
| | | 100101 | Setup Configuration 5 register | | |
| | | 100110 | Setup Configuration 6 register | | |
| | | 100111 | Setup Configuration 7 register | | |
| | | 101000 | Filter Configuration 0 register | | |
| | | 101001 | Filter Configuration 1 register | | |
| | | 101010 | Filter Configuration 2 register | | |
| | | 101011 | Filter Configuration 3 register | | |
| | | 101100 | Filter Configuration 4 register | | |
| | | 101101 | Filter Configuration 5 register | | |
| | | 101110 | Filter Configuration 6 register | | |
| | | 101111 | Filter Configuration 7 register | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| | | 110000 | Offset 0 register | | |
| | | 110001 | Offset 1 register | | |
| | | 110010 | Offset 2 register | | |
| | | 110011 | Offset 3 register | | |
| | | 110100 | Offset 4 register | | |
| | | 110101 | Offset 5 register | | |
| | | 110110 | Offset 6 register | | |
| | | 110111 | Offset 7 register | | |
| | | 111000 | Gain 0 register | | |
| | | 111001 | Gain 1 register | | |
| | | 111010 | Gain 2 register | | |
| | | 111011 | Gain 3 register | | |
| | | 111100 | Gain 4 register | | |
| | | 111101 | Gain 5 register | | |
| | | 111110 | Gain 6 register | | |
| | | 111111 | Gain 7 register | | |

## STATUS REGISTER

**Address: 0x00, Reset: 0x80, Name: Status**

The status register is an 8-bit register that contains ADC and serial interface status information. The register can optionally be appended to the data register by setting the DATA_STAT bit in the interface mode register.

**Table 25. Bit Descriptions for STATUS**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | $\overline{RDY}$ | | The status of $\overline{RDY}$ is output to the DOUT/$\overline{RDY}$ pin when $\overline{CS}$ is low and a register is not being read. This bit goes low when the ADC writes a new result to the data register. In ADC calibration modes, this bit goes low when the ADC writes the calibration result. $\overline{RDY}$ is brought high automatically by a read of the data register. | 0x1 | R |
| | | 0 | New data result available. | | |
| | | 1 | Awaiting new data result. | | |
| 6 | ADC_ERROR | | By default, this bit indicates if an ADC overrange or underrange occurred. The ADC result is clamped to 0xFFFFFF for overrange errors and 0x000000 for underrange errors. This bit is updated when the ADC result is written and is cleared at the next update after removing the overrange or underrange condition. | 0x0 | R |
| | | 0 | No error. | | |
| | | 1 | Error. | | |
| 5 | CRC_ERROR | | This bit indicates if a CRC error occurred during a register write. For register reads, the host microcontroller determines if a CRC error occurred. This bit is cleared by a read of this register. | 0x0 | R |
| | | 0 | No error. | | |
| | | 1 | CRC error. | | |
| 4 | REG_ERROR | | This bit indicates if the content of one of the internal registers changes from the value calculated when the register integrity check is activated. The check is activated by setting the REG_CHECK bit in the interface mode register. This bit is cleared by clearing the REG_CHECK bit. | 0x0 | R |
| | | 0 | No error. | | |
| | | 1 | Error. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [3:0] | Channel | | These bits indicate which channel was active for the ADC conversion whose result is currently in the data register. This may be different from the channel currently being converted. The mapping is a direct map from the channel register; therefore, Channel 0 results in 0x0 and Channel 15 results in 0xF. | 0x0 | R |
| | | 0000 | Channel 0. | | |
| | | 0001 | Channel 1. | | |
| | | 0010 | Channel 2. | | |
| | | 0011 | Channel 3. | | |
| | | 0100 | Channel 4. | | |
| | | 0101 | Channel 5. | | |
| | | 0110 | Channel 6. | | |
| | | 0111 | Channel 7. | | |
| | | 1000 | Channel 8. | | |
| | | 1001 | Channel 9. | | |
| | | 1010 | Channel 10. | | |
| | | 1011 | Channel 11. | | |
| | | 1100 | Channel 12. | | |
| | | 1101 | Channel 13. | | |
| | | 1110 | Channel 14. | | |
| | | 1111 | Channel 15. | | |

## ADC MODE REGISTER

**Address: 0x01, Reset: 0x2000, Name: ADCMODE**

The ADC mode register controls the operating mode of the ADC and the master clock selection. A write to the ADC mode register resets the filter and the $\overline{\text{RDY}}$ bits and starts a new conversion or calibration.

**Table 26. Bit Descriptions for ADCMODE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 15 | REF_EN | | Enables internal reference and outputs a buffered 2.5 V to the REFOUT pin. | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 14 | Reserved | | This bit is reserved. Set this bit to 0. | 0x0 | RW |
| 13 | SING_CYC | | This bit can be used when only a single channel is active to set the ADC to only output at the settled filter data rate. | 0x1 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| [12:11] | Reserved | | These bits are reserved; set these bits to 0. | 0x0 | R |
| [10:8] | Delay | | These bits allow a programmable delay to be added after a channel switch to allow the settling of external circuitry before the ADC starts processing its input. | 0x0 | RW |
| | | 000 | 0 µs. | | |
| | | 001 | 32 µs. | | |
| | | 010 | 128 µs. | | |
| | | 011 | 320 µs. | | |
| | | 100 | 800 µs. | | |
| | | 101 | 1.6 ms. | | |
| | | 110 | 4 ms. | | |
| | | 111 | 8 ms. | | |
| 7 | Reserved | | This bit is reserved. Set this bit to 0. | 0x0 | R |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [6:4] | Mode | | These bits control the operating mode of the ADC. See the Operating Modes section for more information. | 0x0 | RW |
| | | 000 | Continuous conversion mode. | | |
| | | 001 | Single conversion mode. | | |
| | | 010 | Standby mode. | | |
| | | 011 | Power-down mode. | | |
| | | 100 | Internal offset calibration. | | |
| | | 101 | Internal gain calibration | | |
| | | 110 | System offset calibration. | | |
| | | 111 | System gain calibration. | | |
| [3:2] | CLOCKSEL | | These bits select the ADC clock source. Selecting the internal oscillator also enables the internal oscillator. | 0x0 | RW |
| | | 00 | Internal oscillator. | | |
| | | 01 | Internal oscillator output on the XTAL2/CLKIO pin. | | |
| | | 10 | External clock input on the XTAL2/CLKIO pin. | | |
| | | 11 | External crystal on the XTAL1 pin and the XTAL2/CLKIO pin. | | |
| [1:0] | Reserved | | These bits are reserved; set these bits to 0. | 0x0 | R |

## INTERFACE MODE REGISTER

**Address: 0x02, Reset: 0x0000, Name: IFMODE**

The interface mode register configures various serial interface options.

**Table 27. Bit Descriptions for IFMODE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:13] | Reserved | | These bits are reserved; set these bits to 0. | 0x0 | R |
| 12 | ALT_SYNC | | This bit enables a different behavior of the $\overline{\text{SYNC}}$ pin to allow the use of $\overline{\text{SYNC}}$ as a control for conversions when cycling channels | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 11 | IOSTRENGTH | | This bit controls the drive strength of the DOUT/$\overline{\text{RDY}}$ pin. Set this bit when reading from the serial interface at high speed with a low IOVDD supply and moderate capacitance. | 0x0 | RW |
| | | 0 | Disabled (default). | | |
| | | 1 | Enabled. | | |
| [10:9] | Reserved | | These bits are reserved; set these bits to 0. | 0x0 | R |
| 8 | DOUT_RESET | | See the DOUT_RESET section | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 7 | CONTREAD | | This bit enables the continuous read mode of the ADC data register. The ADC must be configured in continuous conversion mode to use continuous read mode. For more details, see the Operating Modes section. | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 6 | DATA_STAT | | This bit enables the status register to be appended to the data register when read so that channel and status information are transmitted with the data. This is the only way to be sure that the channel bits read from the status register correspond to the data in the data register. | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 5 | REG_CHECK | | This bit enables a register integrity checker, which can be used to monitor any change in the value of the user registers. To use this feature, configure all other registers as desired with this bit cleared. Then, write to this register to set the REG_CHECK bit to 1. If the contents of any of the registers change, the REG_ERROR bit is set in the status register. To clear the error, set the REG_CHECK bit to 0. Neither the interface mode register nor the ADC data or status registers are included in the registers that are checked. If a register must have a new value written, this bit must first be cleared; otherwise, an error is flagged when the new register contents are written. | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 4 | Reserved | | This bit is reserved. Set this bit to 0. | 0x0 | R |
| [3:2] | CRC_EN | | These bits enable CRC protection of register reads/writes. CRC increases the number of bytes in a serial interface transfer by one. | 0x00 | RW |
| | | 00 | Disabled | | |
| | | 01 | XOR checksum enabled for register read transactions; register writes still use CRC with these bits set. | | |
| | | 10 | CRC checksum enabled for read and write transactions. | | |
| 1 | Reserved | | This bit is reserved. Set this bit to 0. | 0x0 | R |
| 0 | WL16 | | This bit changes the ADC data register to 16 bits. The ADC is not reset by a write to the interface mode register; therefore, the ADC result is not rounded to the correct word length immediately after writing to these bits. The first new ADC result is correct. | 0x0 | RW |
| | | 0 | 24-bit data. | | |
| | | 1 | 16-bit data. | | |

## REGISTER CHECK

**Address: 0x03, Reset: 0x000000, Name: REGCHECK**

The register check register is a 24-bit checksum calculated by exclusively OR'ing the contents of the user registers. The REG_CHECK bit in the interface mode register must be set for this checksum to operate; otherwise, the register reads 0.

**Table 28. Bit Descriptions for REGCHECK**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [23:0] | REGISTER_CHECK | | This register contains the 24-bit checksum of user registers when the REG_CHECK bit is set in the interface mode register. | 0x000000 | R |

## DATA REGISTER

**Address: 0x04, Reset: 0x000000, Name: Data**

The data register contains the ADC conversion result. The encoding is offset binary, or it can be changed to unipolar by the BI_UNIPOLARx bits in the setup configuration registers. Reading the data register brings the $\overline{\text{RDY}}$ bit and the $\overline{\text{RDY}}$ output high if it is low. The ADC result can be read multiple times. However, because the $\overline{\text{RDY}}$ output is brought high, it is not possible to determine if another ADC result is imminent. After the command to read the ADC register is received, the ADC does not write a new result into the data register.

**Table 29. Bit Descriptions for Data**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [23:0] | Data | | This register contains the ADC conversion result. If DATA_STAT is set in the interface mode register, the status register is appended to this register when read, making this a 32-bit register. If WL16 is set in the interface mode register, this register is reduced to 16 bits. | 0x000000 | R |

## GPIO CONFIGURATION REGISTER

**Address: 0x06, Reset: 0x0800, Name: GPIOCON**

The GPIO configuration register controls the general-purpose I/O pins of the ADC.

**Table 30. Bit Descriptions for GPIOCON**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:14] | Reserved | | Reserved. | 0x0 | R |
| 13 | OP_EN0_1 | | GPO0/GPO1 output enable. This bit enables the GPO0 and GPO1 pins. The outputs are referenced between AVDD and AVSS. | 0x0 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 12 | Reserved | | Reserved | 0x0 | R |
| 11 | SYNC_EN | | $\overline{\text{SYNC}}$ input enable. This bit enables the $\overline{\text{SYNC}}$ pin as a sync input. When set low, the $\overline{\text{SYNC}}$ pin holds the ADC and filter in reset until $\overline{\text{SYNC}}$ goes high. An alternative operation of the $\overline{\text{SYNC}}$ pin is available when the ALT_SYNC bit in the interface mode register is set. This mode works only when multiple channels are enabled. In such cases, a low on the $\overline{\text{SYNC}}$ pin does not immediately reset the filter/modulator. Instead, if the $\overline{\text{SYNC}}$ pin is low when the channel is due to be switched, the modulator and filter are prevented from starting a new conversion. Bringing $\overline{\text{SYNC}}$ high begins the next conversion. This alternative sync mode allows $\overline{\text{SYNC}}$ to be used while cycling through channels. | 0x1 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| [10:9] | ERR_EN | | Error pin mode. These bits enable the $\overline{\text{ERROR}}$ pin as an error input/output. | 0x0 | R/W |
| | | 00 | Disabled. | | |
| | | 01 | Enable error input (active low). $\overline{\text{ERROR}}$ is an error input. The (inverted) readback state is OR'ed with other error sources and is available in the ADC_ERROR bit in the status register. The ERROR pin state can also be read from the ERR_DAT bit in this register. | | |
| | | 10 | Enable open-drain error output (active low). $\overline{\text{ERROR}}$ is an open-drain error output. The status register error bits are OR'ed, inverted, and mapped to the $\overline{\text{ERROR}}$ pin. $\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed. | | |
| | | 11 | General-purpose output (active low). $\overline{\text{ERROR}}$ is a general-purpose output. The status of the pin is controlled by the ERR_DAT bit in this register. This output is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the GPIOx pins. The output has an active pull-up resistor in this case. | | |
| 8 | ERR_DAT | | Error pin data. This bit determines the logic level at the $\overline{\text{ERROR}}$ pin if the pin is enabled as a general-purpose output. This bit reflects the readback status of the pin if the pin is enabled as an input. | 0x0 | R/W |
| | | 0 | Logic 0. | | |
| | | 1 | Logic 1. | | |
| 7 | GP_DATA1 | | GPO1 data. This bit is the write data for GPO1. | 0x0 | R/W |
| | | 0 | GPO1 = 0. | | |
| | | 1 | GPO1 = 1. | | |
| 6 | GP_DATA0 | | GPO0 data. This bit is the write data for GPO0. | 0x0 | R/W |
| | | 0 | GPO0 = 0. | | |
| | | 1 | GPO0 = 1. | | |
| [5:0] | Reserved | | Reserved. | 0x0 | R |

## ID REGISTER

**Address: 0x07, Reset: 0x30DX, Name: ID**

The ID register returns a 16-bit ID. For the AD4112, this value is 0x30DX.

**Table 31. Bit Descriptions for ID**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:0] | ID | | Product ID. The ID register returns a 16-bit ID code that is specific to the ADC. | 0x30DX | R |

## CHANNEL REGISTER 0

**Address: 0x10, Reset: 0x8001, Name: CH0**

The channel registers are 16-bit registers that select the currently active channels, the selected inputs for each channel, and the setup to be used to configure the ADC for that channel.

**Table 32. Bit Descriptions for CH0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 15 | CH_EN0 | | This bit enables Channel 0. If more than one channel is enabled, the ADC automatically sequences between them. | 0x1 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| [14:12] | SETUP_SEL0 | | These bits identify which of the eight setups is used to configure the ADC for this channel. A setup comprises a set of four registers: a setup configuration register, a filter configuration register, an offset register, and a gain register. All channels can use the same setup, in which case the same 3-bit value must be written to these bits on all active channels, or up to eight channels can be configured differently. | 0x0 | R/W |
| | | 000 | Setup 0. | | |
| | | 001 | Setup 1. | | |
| | | 010 | Setup 2. | | |
| | | 011 | Setup 3. | | |
| | | 100 | Setup 4. | | |
| | | 101 | Setup 5. | | |
| | | 110 | Setup 6. | | |
| | | 111 | Setup 7. | | |
| [11:10] | Reserved | | Reserved. | 0x0 | R |
| [9:0] | INPUT0 | | These bits select which input pair is connected to the input of the ADC for this channel. | 0x1 | R/W |
| | | 0000000001 | VIN0, VIN1. | | |
| | | 0000010000 | VIN0, VINCOM. | | |
| | | 0000100000 | VIN1, VIN0. | | |
| | | 0000110000 | VIN1, VINCOM. | | |
| | | 0001000011 | VIN2, VIN3. | | |
| | | 0001010000 | VIN2, VINCOM. | | |
| | | 0001100010 | VIN3, VIN2. | | |
| | | 0001110000 | VIN3, VINCOM. | | |
| | | 0010000101 | VIN4, VIN5. | | |
| | | 0010010000 | VIN4, VINCOM. | | |
| | | 0010100100 | VIN5, VIN4. | | |
| | | 0010110000 | VIN5, VINCOM. | | |
| | | 0011000111 | VIN6, VIN7. | | |
| | | 0011010000 | VIN6, VINCOM. | | |
| | | 0011100110 | VIN7, VIN6. | | |
| | | 0011110000 | IN7, VINCOM. | | |
| | | 0110001011 | IIN3+, IIN3−. | | |
| | | 0110101010 | IIN2+, IIN2−. | | |
| | | 0111001001 | IIN1+, IIN1−. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| | | 0111101000 | IIN0+, IIN0−. | | |
| | | 1000110010 | Temperature sensor. | | |
| | | 1010110110 | Reference. | | |

## CHANNEL REGISTER 1 TO CHANNEL REGISTER 15

**Address: 0x11 to Address 0x1F, Reset: 0x0001, Name: CH1 to CH7**

The remaining 15 channel registers share the same layout as Channel Register 0.

**Table 33. CH1 to CH15 Register Map**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x11 | CH1 | [15:8] | CH_EN1 | SETUP_SEL1 | | | Reserved | | INPUT1[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT1[7:0] | | | | | | | | | |
| 0x12 | CH2 | [15:8] | CH_EN2 | SETUP_SEL2 | | | Reserved | | INPUT2[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT2[7:0] | | | | | | | | | |
| 0x13 | CH3 | [15:8] | CH_EN3 | SETUP_SEL3 | | | Reserved | | INPUT3[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT3[7:0] | | | | | | | | | |
| 0x14 | CH4 | [15:8] | CH_EN4 | SETUP_SEL4 | | | Reserved | | INPUT4[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT4[7:0] | | | | | | | | | |
| 0x15 | CH5 | [15:8] | CH_EN5 | SETUP_SEL5 | | | Reserved | | INPUT5[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT5[7:0] | | | | | | | | | |
| 0x16 | CH6 | [15:8] | CH_EN6 | SETUP_SEL6 | | | Reserved | | INPUT6[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT6[7:0] | | | | | | | | | |
| 0x17 | CH7 | [15:8] | CH_EN7 | SETUP_SEL7 | | | Reserved | | INPUT7[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT7[7:0] | | | | | | | | | |
| 0x18 | CH8 | [15:8] | CH_EN8 | SETUP_SEL8 | | | Reserved | | INPUT8[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT8[7:0] | | | | | | | | | |
| 0x19 | CH9 | [15:8] | CH_EN9 | SETUP_SEL9 | | | Reserved | | INPUT9[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT9[7:0] | | | | | | | | | |
| 0x1A | CH10 | [15:8] | CH_EN10 | SETUP_SEL10 | | | Reserved | | INPUT10[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT10[7:0] | | | | | | | | | |
| 0x1B | CH11 | [15:8] | CH_EN11 | SETUP_SEL11 | | | Reserved | | INPUT11[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT11[7:0] | | | | | | | | | |
| 0x1C | CH12 | [15:8] | CH_EN12 | SETUP_SEL12 | | | Reserved | | INPUT12[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT12[7:0] | | | | | | | | | |
| 0x1D | CH13 | [15:8] | CH_EN13 | SETUP_SEL13 | | | Reserved | | INPUT13[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT13[7:0] | | | | | | | | | |
| 0x1E | CH14 | [15:8] | CH_EN14 | SETUP_SEL14 | | | Reserved | | INPUT14[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT14[7:0] | | | | | | | | | |
| 0x1F | CH15 | [15:8] | CH_EN15 | SETUP_SEL15 | | | Reserved | | INPUT15[9:8] | | 0x0001 | RW |
| | | [7:0] | INPUT15[7:0] | | | | | | | | | |

## SETUP CONFIGURATION REGISTER 0

**Address: 0x20, Reset: 0x1000 Name: SETUPCON0**

The setup configuration registers are 16-bit registers that configure the reference selection, input buffers, and output coding of the ADC.

**Table 34. Bit Descriptions for SETUPCON0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:13] | Reserved | | These bits are reserved; set these bits to 0. | 0x0 | R |
| 12 | BI_UNIPOLAR0 | | Bipolar/unipolar. This bit sets the output coding of the ADC for Setup 0. | 0x1 | R/W |
| | | 0 | Unipolar coded output. | | |
| | | 1 | Bipolar coded output. | | |
| 11 | REFBUF0+ | | REF+ buffer. This bit enables or disables the REF+ input buffer. | 0x0 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 10 | REFBUF0− | | REF− buffer. This bit enables or disables the REF− input buffer. | 0x0 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| [9:8] | INBUF0 | | Input buffer. This bit enables or disables input buffers. | 0x0 | R/W |
| | | 00 | Disabled. | | |
| | | 01 | Reserved. | | |
| | | 10 | Reserved. | | |
| | | 11 | Enabled. | | |
| 7 | Reserved | | This bit is reserved. Set this bit to 0. | 0x0 | R |
| 6 | Reserved | | This bit is reserved. Set this bit to 0. | 0x0 | R |
| [5:4] | REF_SEL0 | | These bits allow the user to select the reference source for ADC conversion on Setup 0. | 0x0 | R/W |
| | | 00 | External reference − REF±. | | |
| | | 10 | Internal 2.5 V reference, must be enabled via ADCMODE (see Table 26). | | |
| | | 11 | AVDD − AVSS. | | |
| [3:0] | Reserved | | These bits are reserved; set these bits to 0. | 0x0 | R |

## SETUP CONFIGURATION REGISTER 1 TO SETUP CONFIGURATION REGISTER 7

**Address: 0x21 to Address 0x27, Reset: 0x1000, Name: SETUPCON1 to SETUPCON7**

The remaining seven setup configuration registers share the same layout as Setup Configuration Register 0.

**Table 35. SETUPCON1 to SETUPCON7 Register Map**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x21 | SETUPCON1 | [15:8] | Reserved | | | BI_UNIPOLAR1 | REFBUF1+ | REFBUF1− | INBUF1 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | | REF_SEL1 | Reserved | | | | | |
| 0x22 | SETUPCON2 | [15:8] | Reserved | | | BI_UNIPOLAR2 | REFBUF2+ | REFBUF2− | INBUF2 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | | REF_SEL2 | Reserved | | | | | |
| 0x23 | SETUPCON3 | [15:8] | Reserved | | | BI_UNIPOLAR3 | REFBUF3+ | REFBUF3− | INBUF3 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | | REF_SEL3 | Reserved | | | | | |
| 0x24 | SETUPCON4 | [15:8] | Reserved | | | BI_UNIPOLAR4 | REFBUF4+ | REFBUF4− | INBUF4 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | | REF_SEL4 | Reserved | | | | | |
| 0x25 | SETUPCON5 | [15:8] | Reserved | | | BI_UNIPOLAR5 | REFBUF5+ | REFBUF5− | INBUF5 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | | REF_SEL5 | Reserved | | | | | |
| 0x26 | SETUPCON6 | [15:8] | Reserved | | | BI_UNIPOLAR6 | REFBUF6+ | REFBUF6− | INBUF6 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | | REF_SEL6 | Reserved | | | | | |
| 0x27 | SETUPCON7 | [15:8] | Reserved | | | BI_UNIPOLAR7 | REFBUF7+ | REFBUF7− | INBUF7 | | 0x1000 | RW |
| | | [7:0] | Reserved | Reserved | | REF_SEL7 | Reserved | | | | | |

## FILTER CONFIGURATION REGISTER 0

**Address: 0x28, Reset: 0x0500, Name: FILTCON0**

The filter configuration registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

**Table 36. Bit Descriptions for FILTCON0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 15 | SINC3_MAP0 | | If this bit is set, the mapping of the filter register changes to directly program the decimation rate of the sinc3 filter for Setup 0. All other options are eliminated. This bit allows fine tuning of the output data rate and filter notch for rejection of specific frequencies. The data rate when on a single channel equals $f_{MOD}/(32 \times FILTCON0[14:0])$. | 0x0 | RW |
| [14:12] | Reserved | | These bits are reserved; set these bits to 0. | 0x0 | R |
| 11 | ENHFILTEN0 | | This bit enables various postfilters for enhanced 50 Hz/60 Hz rejection for Setup 0. The ORDER0 bits must be set to 00 to select the sinc5 + sinc1 filter for this function to work. | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| [10:8] | ENHFILT0 | | These bits select between various postfilters for enhanced 50 Hz/60 Hz rejection for Setup 0. | 0x5 | RW |
| | | 010 | 27 SPS, 47 dB rejection, 36.7 ms settling | | |
| | | 011 | 25 SPS, 62 dB rejection, 40 ms settling | | |
| | | 101 | 20 SPS, 86 dB rejection, 50 ms settling | | |
| | | 110 | 16.67 SPS, 92 dB rejection, 60 ms settling | | |
| 7 | Reserved | | This bit is reserved. Set this bit to 0. | 0x0 | R |
| [6:5] | ORDER0 | | These bits control the order of the digital filter that processes the modulator data for Setup 0. | 0x0 | RW |
| | | 00 | Sinc5 + sinc1 (default). | | |
| | | 11 | Sinc3. | | |
| [4:0] | ODR0 | | These bits control the output data rate of the ADC and, therefore, the settling time and noise for Setup 0. Rates shown are for-single channel enabled sinc5 + sinc 1 filter. See Table 6 to Table 9 for multiple channels enabled. | 0x0 | RW |
| | | 00000 | 31,250 SPS. | | |
| | | 00001 | 31,250 SPS. | | |
| | | 00010 | 31,250 SPS. | | |
| | | 00011 | 31,250 SPS. | | |
| | | 00100 | 31,250 SPS. | | |
| | | 00101 | 31,250 SPS. | | |
| | | 00110 | 15,625 SPS. | | |
| | | 00111 | 10,417 SPS. | | |
| | | 01000 | 5208 SPS. | | |
| | | 01001 | 2597 SPS (3906 SPS for sinc3). | | |
| | | 01010 | 1007 SPS (1157 SPS for sinc3). | | |
| | | 01011 | 503.8 SPS (539 SPS for sinc3). | | |
| | | 01100 | 381 SPS (401 SPS for sinc3). | | |
| | | 01101 | 200.3 SPS (206 SPS for sinc3). | | |
| | | 01110 | 100.2 SPS (102 SPS for sinc3). | | |
| | | 01111 | 59.52 SPS (59.98 SPS for sinc3). | | |
| | | 10000 | 49.68 SPS (50 SPS for sinc3). | | |
| | | 10001 | 20.01 SPS. | | |
| | | 10010 | 16.63 SPS (16.67 SPS for sinc3). | | |
| | | 10011 | 10 SPS. | | |
| | | 10100 | 5 SPS. | | |
| | | 10101 | 2.5 SPS. | | |
| | | 10110 | 1.25 SPS. | | |

## FILTER CONFIGURATION REGISTER 1 TO FILTER CONFIGURATION REGISTER 7

**Address: 0x29 to Address 0x2F, Reset: 0x0500, Name: FILTCON1 to FILTCON7**

The remaining seven filter configuration registers share the same layout as Filter Configuration Register 0.

**Table 37. FILTCON1 to FILTCON7 Register Map**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x29 | FILTCON1 | [15:8] | SINC3_MAP1 | Reserved | | | ENHFILTEN1 | ENHFILT1 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER1 | | ODR1 | | | | | | |
| 0x2A | FILTCON2 | [15:8] | SINC3_MAP2 | Reserved | | | ENHFILTEN2 | ENHFILT2 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER2 | | ODR2 | | | | | | |
| 0x2B | FILTCON3 | [15:8] | SINC3_MAP3 | Reserved | | | ENHFILTEN3 | ENHFILT3 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER3 | | ODR3 | | | | | | |
| 0x2C | FILTCON4 | [15:8] | SINC3_MAP4 | Reserved | | | ENHFILTEN4 | ENHFILT4 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER4 | | ODR4 | | | | | | |
| 0x2D | FILTCON5 | [15:8] | SINC3_MAP5 | Reserved | | | ENHFILTEN5 | ENHFILT5 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER5 | | ODR5 | | | | | | |
| 0x2E | FILTCON6 | [15:8] | SINC3_MAP6 | Reserved | | | ENHFILTEN6 | ENHFILT6 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER6 | | ODR6 | | | | | | |
| 0x2F | FILTCON7 | [15:8] | SINC3_MAP7 | Reserved | | | ENHFILTEN7 | ENHFILT7 | | | 0x0500 | RW |
| | | [7:0] | Reserved | ORDER7 | | ODR7 | | | | | | |

## OFFSET REGISTER 0

**Address: 0x30, Reset: 0x800000, Name: OFFSET0**

The offset (zero-scale) registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system.

**Table 38. Bit Descriptions for OFFSET0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [23:0] | OFFSET0 | | Offset calibration coefficient for Setup 0. | 0x800000 | RW |

## OFFSET REGISTER 1 TO OFFSET REGISTER 7

**Address: 0x31 to Address 0x37, Reset: 0x800000, Name: OFFSET1 to OFFSET7**

The remaining seven offset registers share the same layout as Offset Register 0.

**Table 39. OFFSET1 to OFFSET7 Register Map**

| Reg. | Name | Bits | Bits[23:0] | Reset | RW |
|---|---|---|---|---|---|
| 0x31 | OFFSET1 | [23:0] | OFFSET1[23:0] | 0x800000 | RW |
| 0x32 | OFFSET2 | [23:0] | OFFSET2[23:0] | 0x800000 | RW |
| 0x33 | OFFSET3 | [23:0] | OFFSET3[23:0] | 0x800000 | RW |
| 0x34 | OFFSET4 | [23:0] | OFFSET4[23:0] | 0x800000 | RW |
| 0x35 | OFFSET5 | [23:0] | OFFSET5[23:0] | 0x800000 | RW |
| 0x36 | OFFSET6 | [23:0] | OFFSET6[23:0] | 0x800000 | RW |
| 0x37 | OFFSET7 | [23:0] | OFFSET7[23:0] | 0x800000 | RW |

## GAIN REGISTER 0

**Address: 0x38, Reset: 0x5XXXX0, Name: GAIN0**

The gain (full-scale) registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system.

**Table 40. Bit Descriptions for GAIN0**

| Bits | Bit Name | Settings | Description | Reset[1] | Access |
|---|---|---|---|---|---|
| [23:0] | GAIN0 | | Gain calibration coefficient for Setup 0. | 0x5XXXX0 | RW |

[1] X means don't care.

## GAIN REGISTER 1 TO GAIN REGISTER 7

**Address: 0x39 to 0x3F, Reset: 0x5XXXX0, Name: GAIN1 to GAIN7**

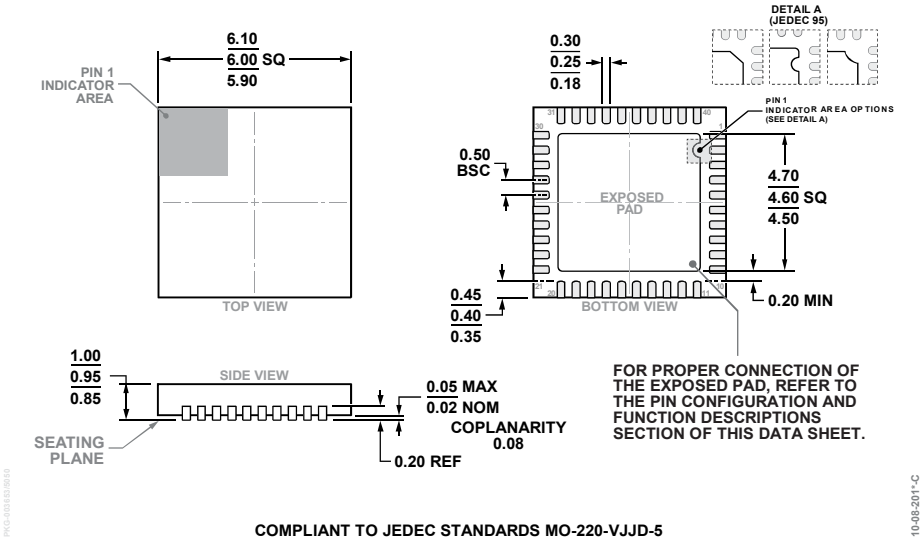
The remaining seven gain registers share the same layout as Gain Register 0.

**Table 41. GAIN1 to GAIN7 Register Map**

| Reg. | Name | Bits | Bits[23:0] | Reset[1] | RW |
|---|---|---|---|---|---|
| 0x39 | GAIN1 | [23:0] | GAIN1[23:0] | 0x5XXXX0 | RW |
| 0x3A | GAIN2 | [23:0] | GAIN2[23:0] | 0x5XXXX0 | RW |
| 0x3B | GAIN3 | [23:0] | GAIN3[23:0] | 0x5XXXX0 | RW |
| 0x3C | GAIN4 | [23:0] | GAIN4[23:0] | 0x5XXXX0 | RW |
| 0x3D | GAIN5 | [23:0] | GAIN5[23:0] | 0x5XXXX0 | RW |
| 0x3E | GAIN6 | [23:0] | GAIN6[23:0] | 0x5XXXX0 | RW |
| 0x3F | GAIN7 | [23:0] | GAIN7[23:0] | 0x5XXXX0 | RW |

[1] X means don't care.

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5

*Figure 59. 40-Lead Lead Frame Chip Scale Package [LFCSP]*
*6 mm × 6 mm Body and 0.95 mm Package Height*
*(CP-40-15)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD4112BCPZ | −40°C to +105°C | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-15 |
| AD4112BCPZ-RL7 | −40°C to +105°C | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-15 |
| EVAL-AD4112SDZ | | Evaluation Board | |
| EVAL-SDP-CB1Z | | Evaluation Controller Board | |

[1] Z = RoHS Compliant Part.