

NTR5105P

MOSFET – Power, Single, P-Channel, SOT-23 -60 V, -211 mA

Features

- Trench Technology
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Small Signal Load Switch
- Analog Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-60	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	-196	mA
		$T_A = 85^{\circ}\text{C}$		-141	
	$t \leq 5\text{ s}$	$T_A = 25^{\circ}\text{C}$		-211	
		$T_A = 85^{\circ}\text{C}$		-152	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	P_D	347	mW
	$t \leq 5\text{ s}$	403			
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$		I_{DM}	-784	mA
Operating Junction and Storage Temperature			T_J, T_{stg}	-55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode) (Note 2)			I_S	-347	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	360	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5$ s (Note 1)	$R_{\theta JA}$	310	$^\circ\text{C/W}$

1. Surface-mounted on FR4 board using 1 in. sq. pad size (Cu area – 1.127 in. sq. [2 oz.] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu pad.

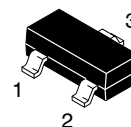
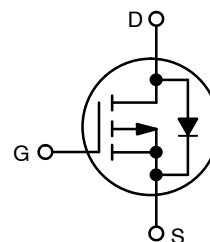


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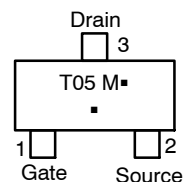
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
-60 V	5 Ω @ -10 V	-211 mA
	6 Ω @ -4.5 V	

P-Channel



SOT-23
CASE 318
STYLE 21

MARKING DIAGRAM/ PIN ASSIGNMENT



T05 = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTR5105PT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTR5105P

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	Reference to 25°C , $I_D = -250\text{ }\mu\text{A}$		6.5		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -60\text{ V}$	$T_J = 25^\circ\text{C}$		-1.0	μA
			$T_J = 125^\circ\text{C}$		-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-1.0		-3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.2		$\text{mV}/^\circ\text{C}$
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -100\text{ mA}$		1.6	5.0	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -100\text{ mA}$		2.2	6.0	
Forward Transconductance	g_{FS}	$V_{DS} = -5.0\text{ V}, I_D = -100\text{ mA}$		227		mS

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -25\text{ V}$		30.3		pF
Output Capacitance	C_{oss}			4.7		
Reverse Transfer Capacitance	C_{rss}			3.2		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5\text{ V}, V_{DS} = -25\text{ V}, I_D = -100\text{ mA}$		1.0		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.2		
Gate-to-Source Charge	Q_{GS}			0.4		
Gate-to-Drain Charge	Q_{GD}			0.3		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -5\text{ V}, V_{DD} = -48\text{ V}, I_D = -100\text{ mA}, R_G = 1\text{ }\Omega$		5.8		ns
Rise Time	t_r			4.0		
Turn-Off Delay Time	$t_{d(off)}$			8.8		
Fall Time	t_f			12.8		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -100\text{ mA}$	$T_J = 25^\circ\text{C}$		0.78	1.0	V
			$T_J = 125^\circ\text{C}$		0.59		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

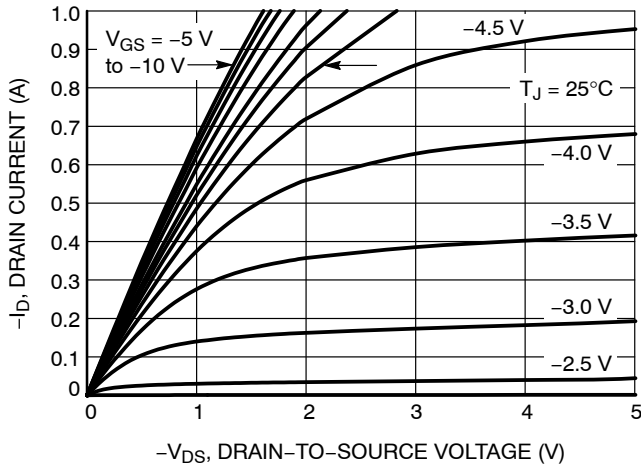


Figure 1. On-Region Characteristics

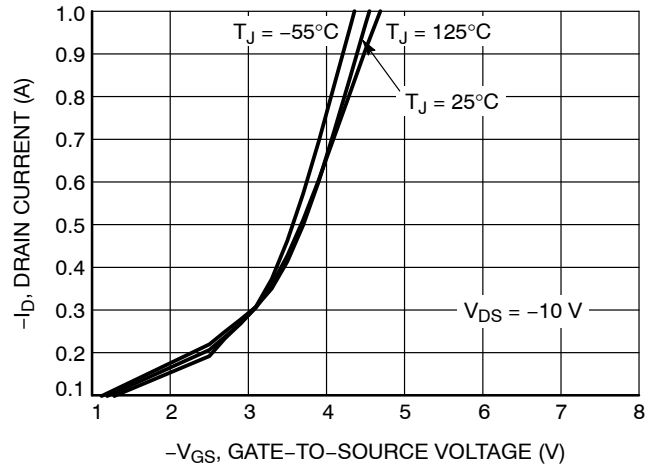


Figure 2. Transfer Characteristics

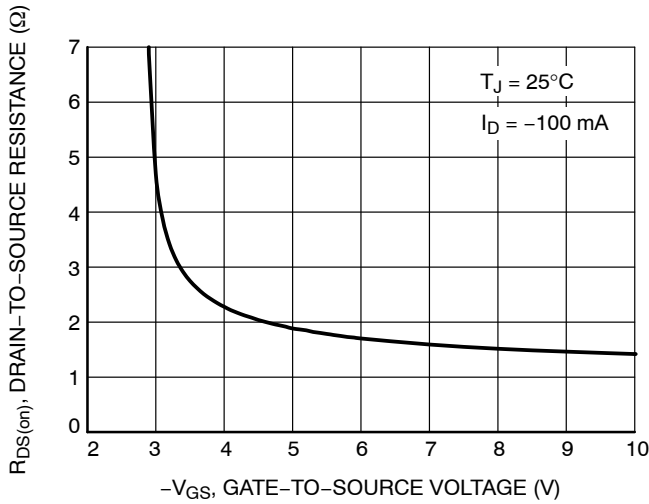


Figure 3. On-Resistance vs. Gate-to-Source Voltage

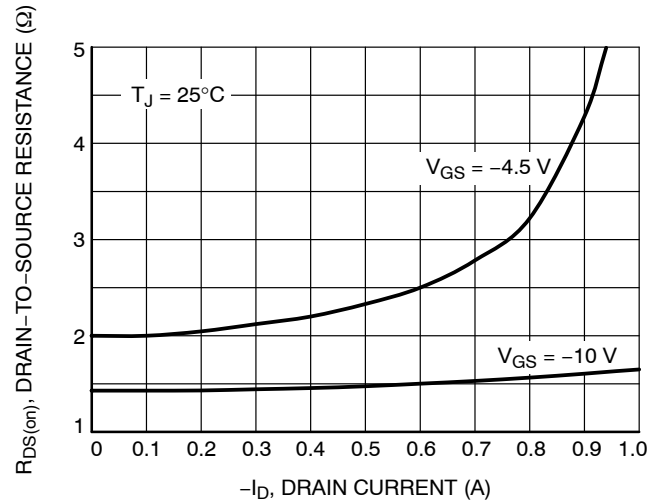


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

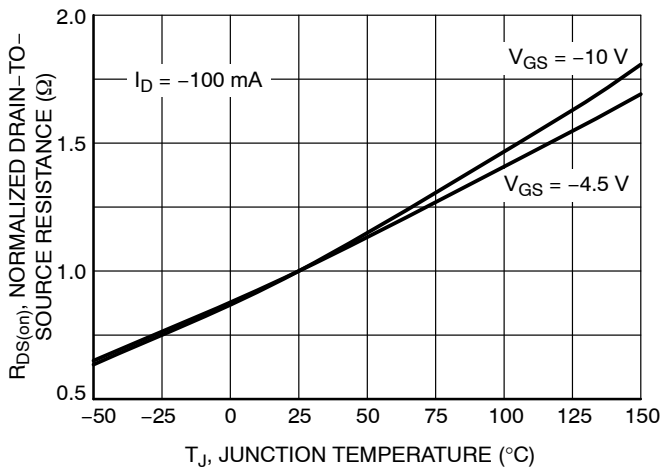


Figure 5. On-Resistance Variation with Temperature

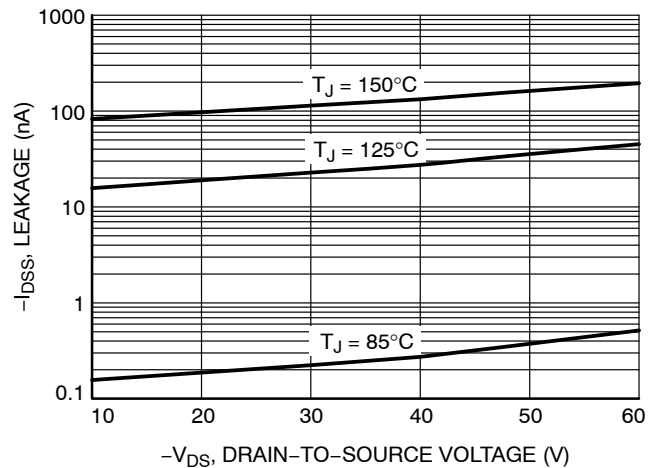


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

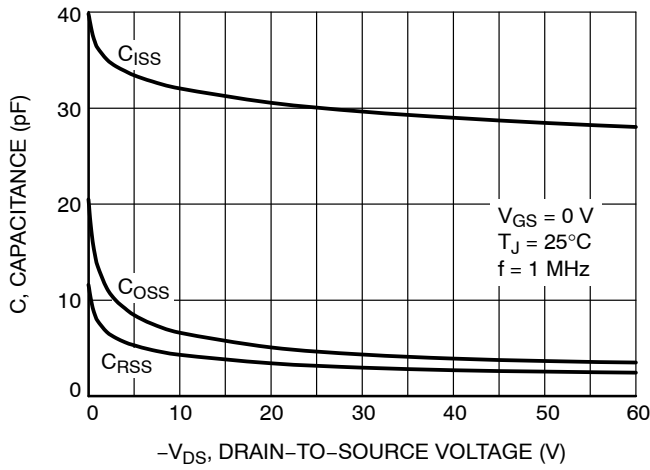


Figure 7. Capacitance Variation

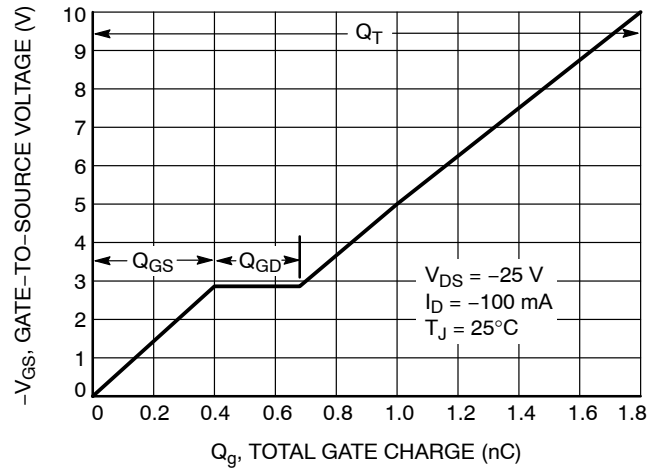


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

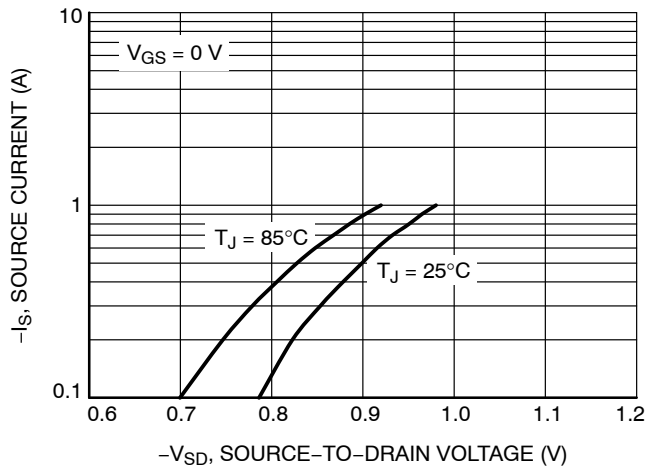


Figure 9. Diode Forward Voltage vs. Current

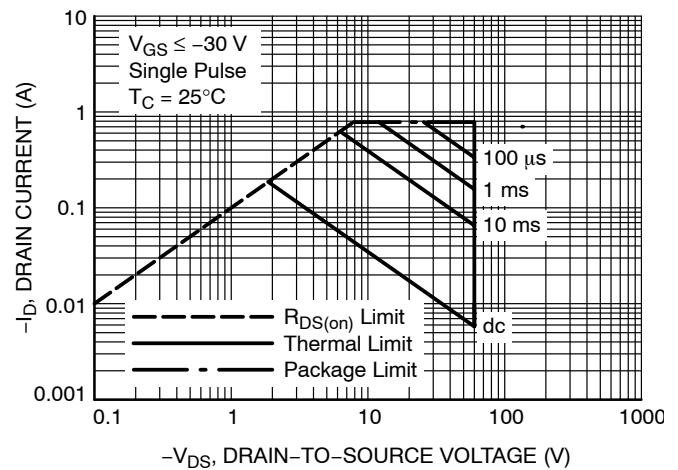


Figure 10. Maximum Rated Forward Biased Safe Operating Area

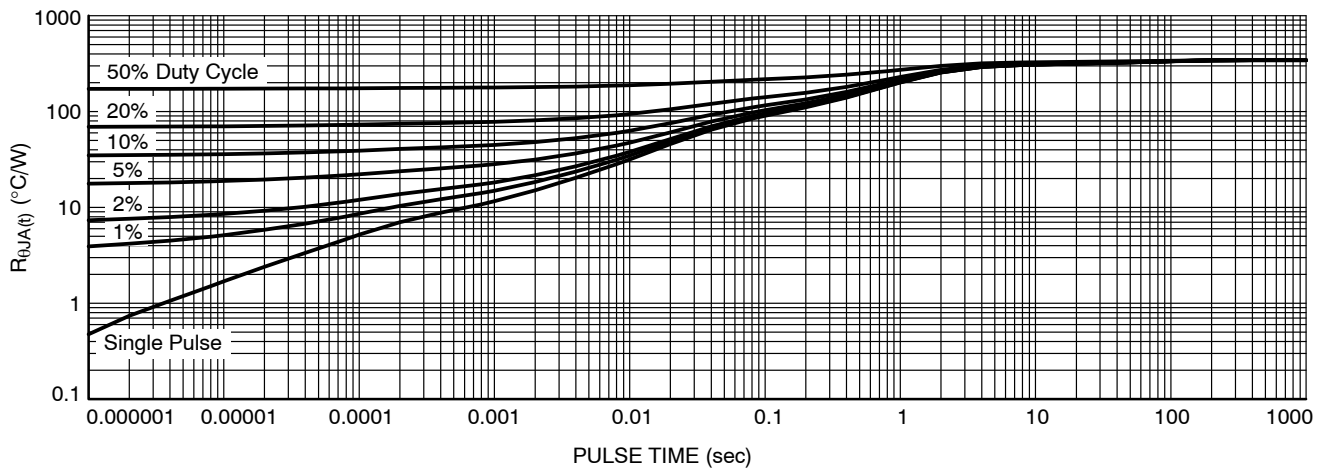
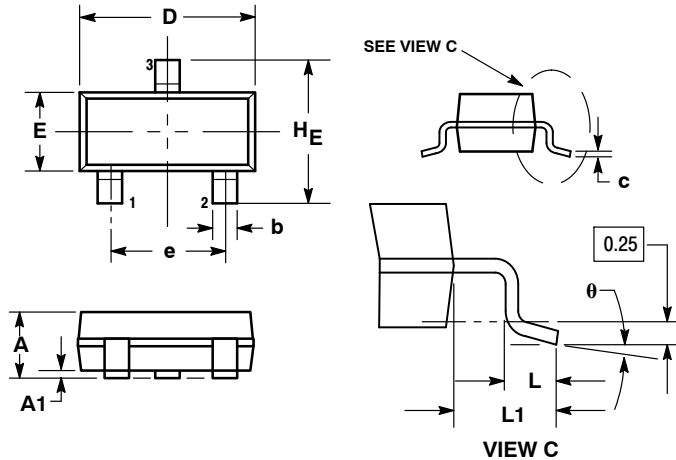


Figure 11. Thermal Response

NTR5105P

PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 ISSUE AP

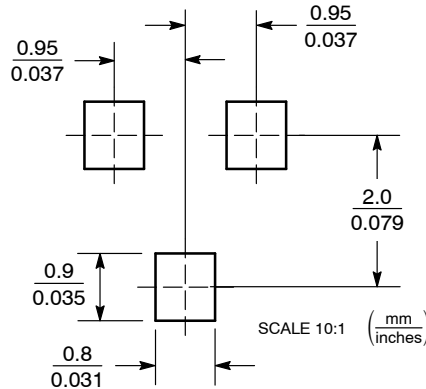


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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