CSPEMI306A

6-Channel EMI Filter Array with ESD Protection

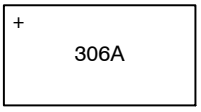
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WLCSP15
CASE 567BS

MARKING DIAGRAM



306A = CSPEMI306A

ORDERING INFORMATION

Device	Package	Shipping†
CSPEMI306A	CSP−15 (Pb−Free)	3500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Product Description

The CSPEMI306A is a six channel low − pass filter array that reduces EMI/RFI emissions while at the same time providing ESD protection. It is used on data ports on mobile devices. To reduce EMI/RFI emissions, the CSPEMI306A integrates a pi − style filter (C − R − C) for each of the 6 channels. Each high quality filter provides greater than 30 dB attenuation in the 800 − 2700 MHz range. These pi − style filters also support bidirectional filtering, controlling EMI both to and from a data port connector.

In addition, the CSPEMI306A provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). The input pins safely dissipate ESD strikes of ±15 kV, exceeding the maximum requirement of the IEC 61000 − 4 − 2 international standard. Using the MIL − STD − 883 (Method 3015) specification for Human Body Model (HBM) ESD, the device provides protection for contact discharges to greater than ±30 kV.

The CSPEMI306A is particularly well suited for portable electronics (e.g. cellular telephones, PDAs, notebook computers) because of its small package footprint and low weight. The CSPEMI306A is available in a space − saving, low − profile Chip Scale Package with optional lead − free finishing.

Features

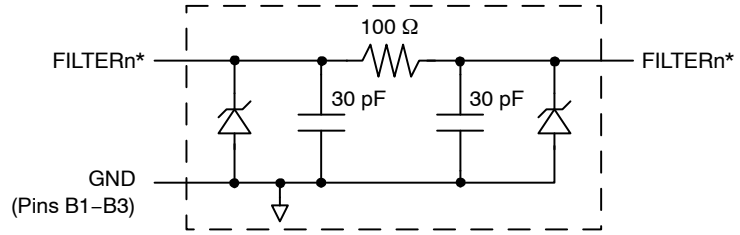
- Six Channels of EMI Filtering for Data Ports
- Pi − Style EMI Filters in a Capacitor − Resistor − Capacitor (C − R − C) Network
- Greater than 32 dB Attenuation at 1 GHz
- ±15 kV ESD Protection on each Channel (IEC 61000−4−2 Level 4, Contact Discharge)
- ±30 kV ESD Protection on each Channel (HBM)
- Chip Scale Package Features Extremely Low Lead Inductance for Optimum Filter and ESD Performance
- 15−Bump, 2.960 mm x 1.330 mm Footprint Chip Scale Package (CSP)
- These Devices are Pb−Free and are RoHS Compliant

Applications

- EMI Filtering and ESD Protection for both Data and I/O Ports
- Wireless Handsets
- Handheld PCs / PDAs
- MP3 Players
- Notebooks
- Desktop PCs

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ELECTRICAL SCHEMATIC



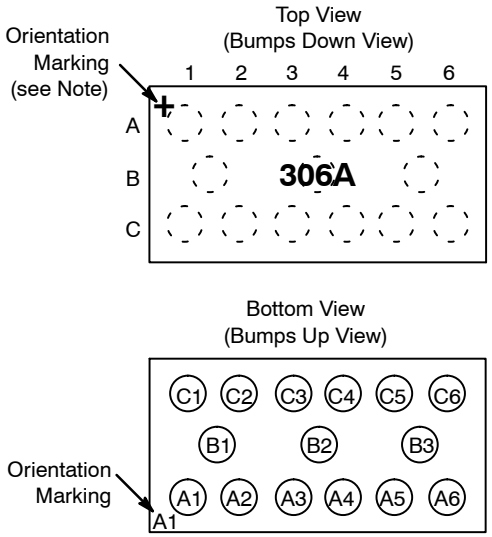
1 of 6 EMI/RFI + ESD Channels

*See Package/Pinout Diagrams for expanded pin information.

Table 1. PIN DESCRIPTIONS

Pin(s)	Name	Description
A1	FILTER1	Filter Channel 1
A2	FILTER2	Filter Channel 2
A3	FILTER3	Filter Channel 3
A4	FILTER4	Filter Channel 4
A5	FILTER5	Filter Channel 5
A6	FILTER6	Filter Channel 6
B1−B3	GND	Device Ground
C1	FILTER1	Filter Channel 1
C2	FILTER2	Filter Channel 2
C3	FILTER3	Filter Channel 3
C4	FILTER4	Filter Channel 4
C5	FILTER5	Filter Channel 5
C6	FILTER6	Filter Channel 6

PACKAGE / PINOUT DIAGRAMS



CSPEMI306A
CSP Package

Note: Lead−free devices are specified by using a “+” character for the top side orientation mark.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature Range	−65 to +150	°C
DC Power per Resistor	100	mW
DC Package Power Rating	600	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R	Resistance		80	100	120	Ω
C	Capacitance	At 2.5 V DC	24	30	36	pF
TCR	Temperature Coefficient of Resistance			1200		ppm/°C
TCC	Temperature Coefficient of Capacitance	At 2.5 V DC		−300		ppm/°C
V_{DIODE}	Diode Voltage (reverse bias)	I_{DIODE} = 10 μA	5.5			V
I_{LEAK}	Diode Leakage Current (reverse bias)	V_{DIODE} = 3.3 V			100	nA
V_{SIG}	Signal Voltage Positive Clamp Negative Clamp	I_{LOAD} = 10 mA	 5.6 −0.4	 6.8 −0.8	 9.0 −1.5	V
V_{ESD}	In−system ESD Withstand Voltage a) Human Body Model, MIL−STD−883, Method 3015 b) Contact Discharge per IEC 61000−4−2 Level 4	(Notes 2 and 4)	 ±30 ±15			kV
V_{CL}	Clamping Voltage during ESD Discharge MIL−STD−883 (Method 3015), 8 kV Positive Transients Negative Transients	(Notes 2, 3 and 4)		 +10 −5		V
f_C	Cut−off frequency Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω	R = 100 Ω, C = 30 pF		58		MHz

1. T_A = 25°C unless otherwise specified.
2. ESD applied to input and output pins with respect to GND, one at a time.
3. Clamping voltage is measured at the opposite side of the EMI filter to the ESD pin. For example, if ESD is applied to Pin A1, then clamping voltage is measured at Pin C1.
4. Unused pins are left open.

PERFORMANCE INFORMATION

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

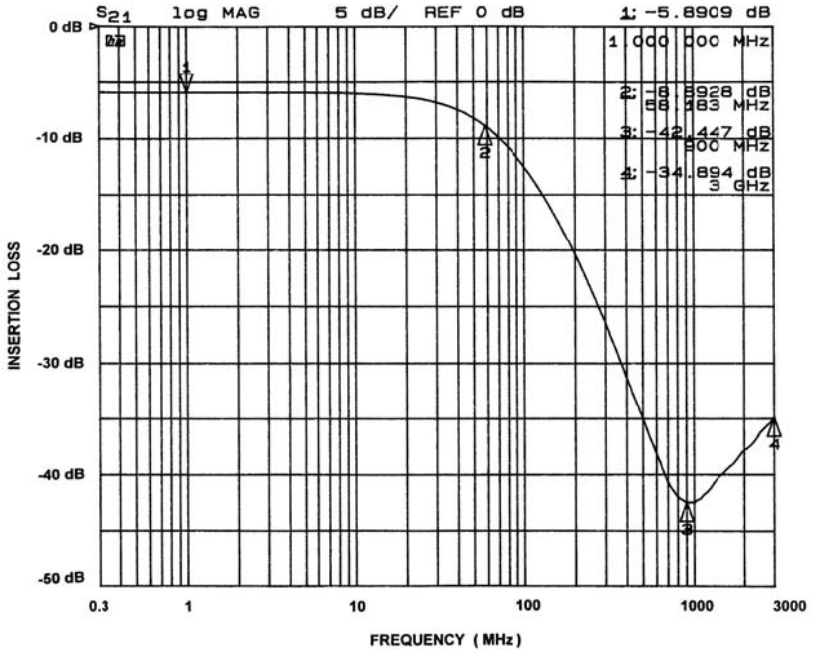


Figure 1. Insertion Loss vs. Frequency (A1−C1 to GND B2)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

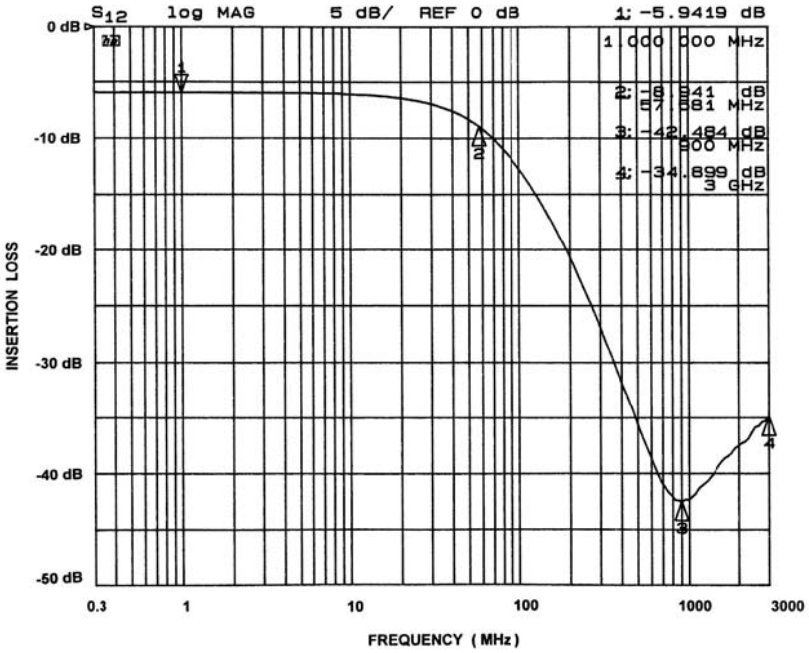


Figure 2. Insertion Loss vs. Frequency (A2−C2 to GND B2)

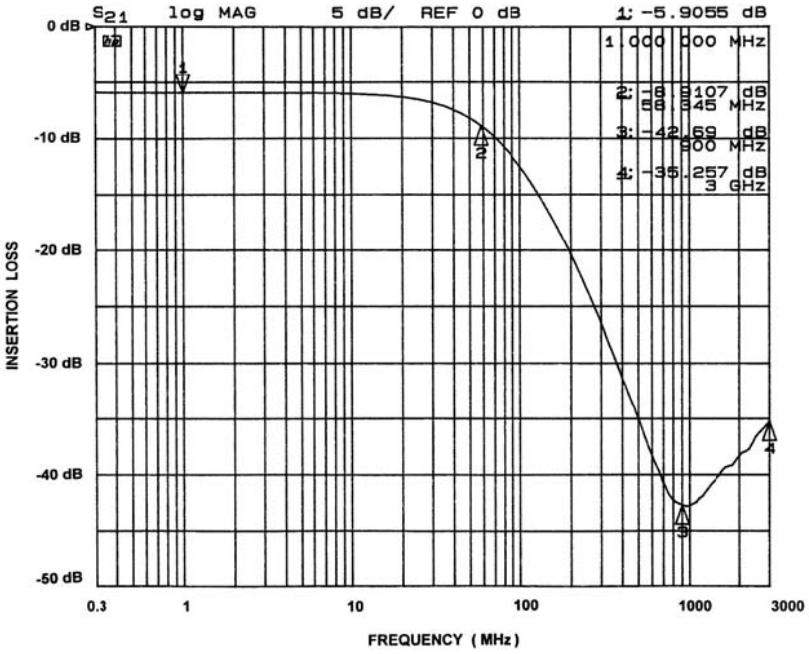


Figure 3. Insertion Loss vs. Frequency (A3−C3 to GND B2)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

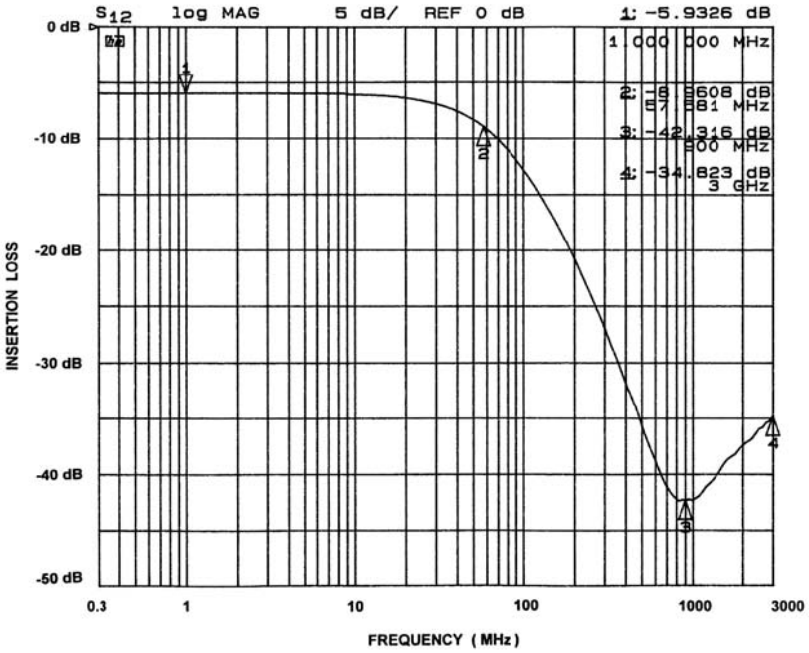


Figure 4. Insertion Loss vs. Frequency (A4−C4 to GND B2)

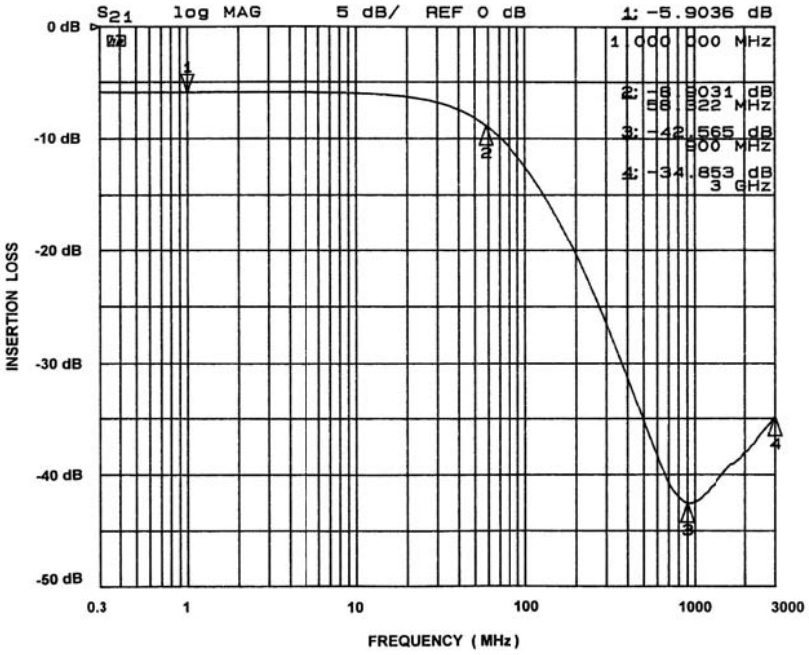


Figure 5. Insertion Loss vs. Frequency (A5−C5 to GND B2)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

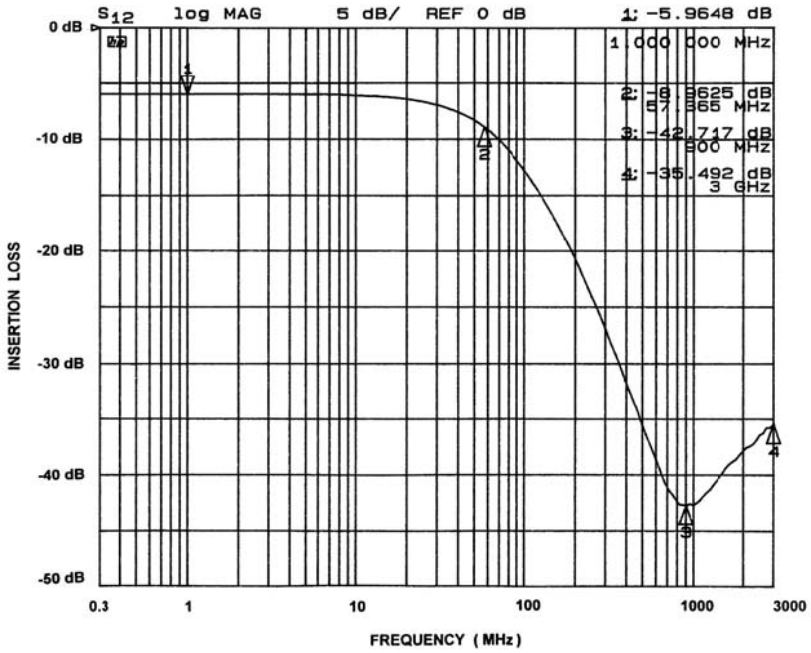


Figure 6. Insertion Loss vs. Frequency (A6−C6 to GND B2)

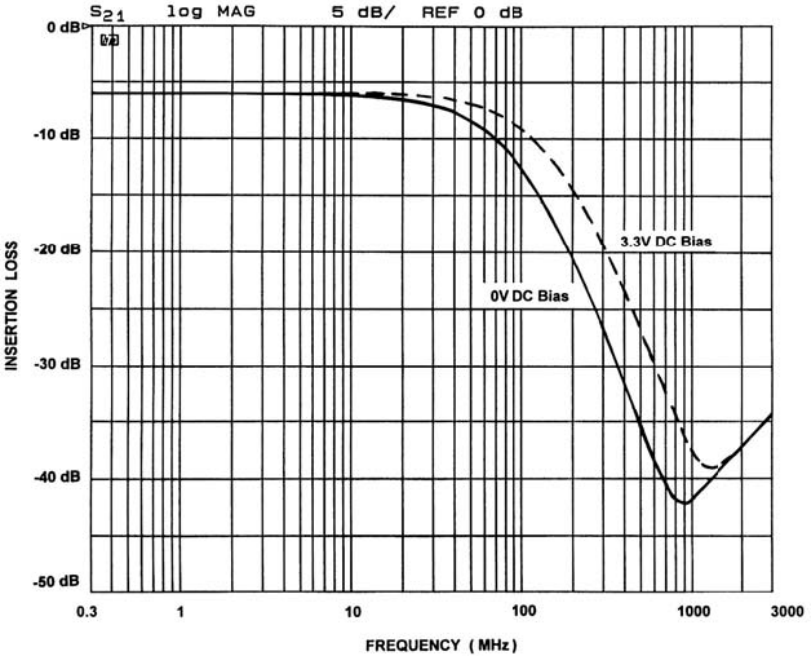


Figure 7. Comparison of Filter Response Curves for CSPEMI306A vs. DC Bias

PERFORMANCE INFORMATION (Cont'd)

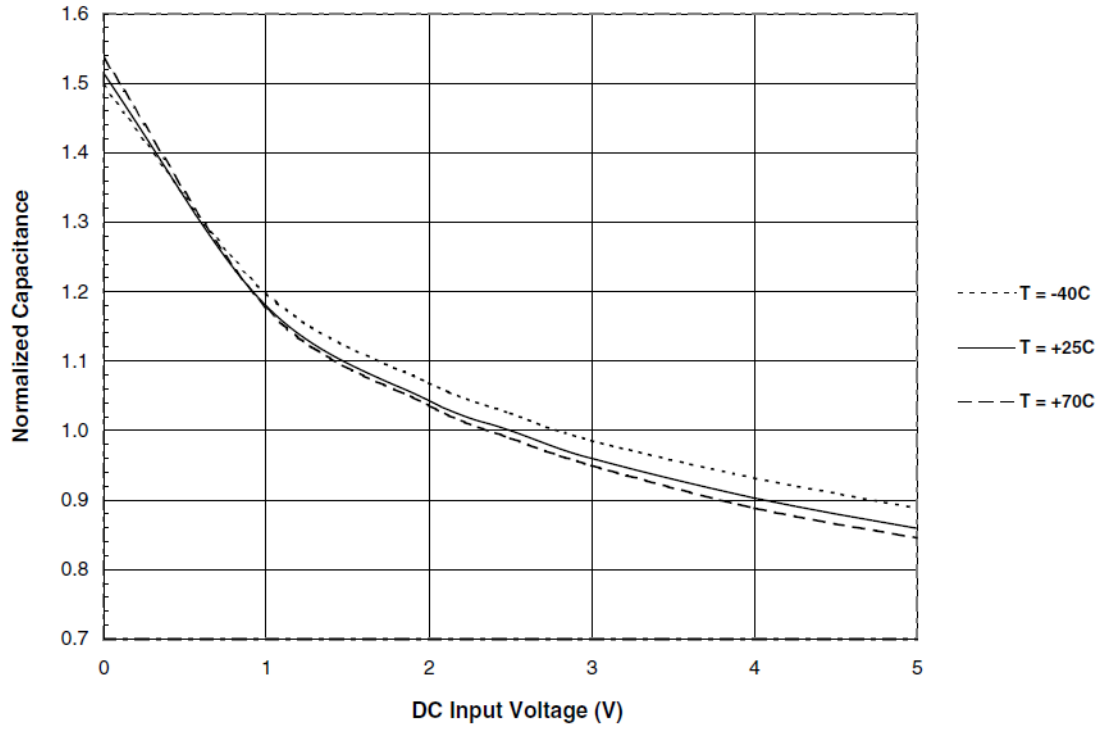


Figure 8. Filter Capacitance vs. Input Voltage over Temperature (normalized to capacitance at 2.5 VDC and 25°C)

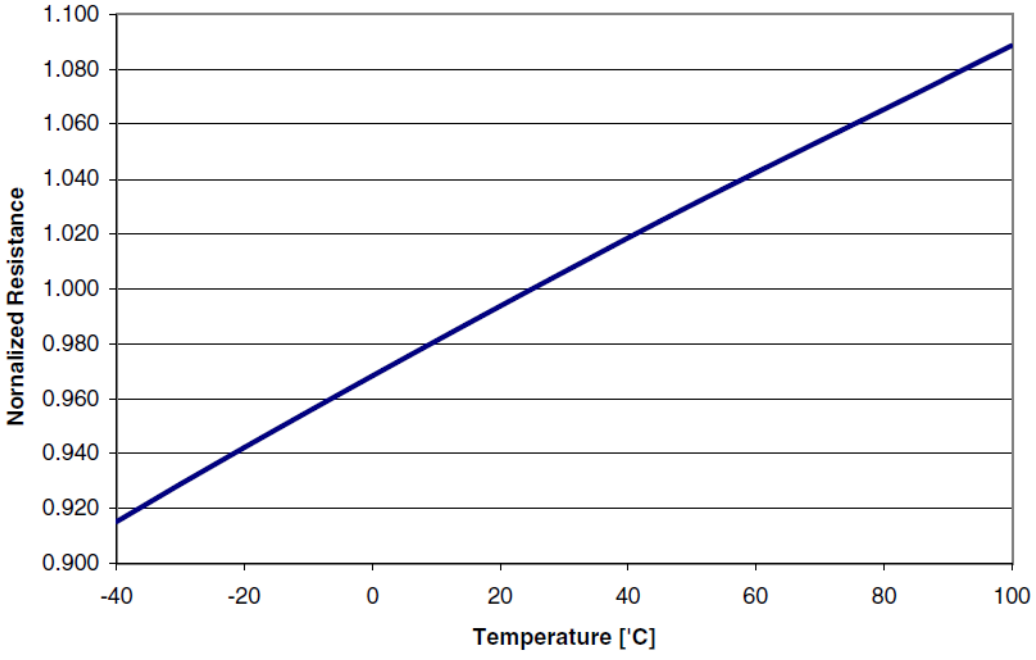


Figure 9. Resistance vs. Temperature (normalized to resistance at 25°C)

APPLICATION INFORMATION

Parameter	Value
Pad Size on PCB	0.240 mm
Pad Shape	Round
Pad Definition	Non−Solder Mask defined pads
Solder Mask Opening	0.290 mm Round
Solder Stencil Thickness	0.125 mm − 0.150 mm
Solder Stencil Aperture Opening (laser cut, 5% tapered walls)	0.300 mm Round
Solder Flux Ratio	50/50 by volume
Solder Paste Type	No Clean
Pad Protective Finish	OSP (Entek Cu Plus 106A)
Tolerance − Edge To Corner Ball	±50 μm
Solder Ball Side Coplanarity	±20 μm
Maximum Dwell Time Above Liquidous	60 seconds
Maximum Soldering Temperature for Lead−free Devices using a Lead−free Solder Paste	260°C

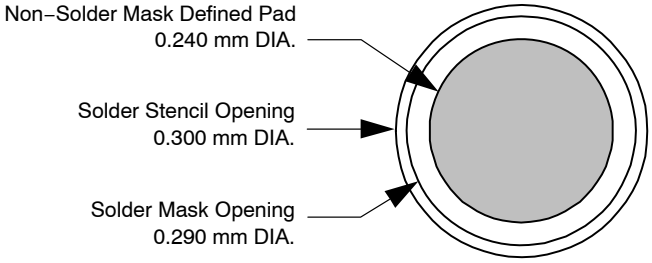


Figure 10. Recommended Non−Solder Mask Defined Pad Illustration

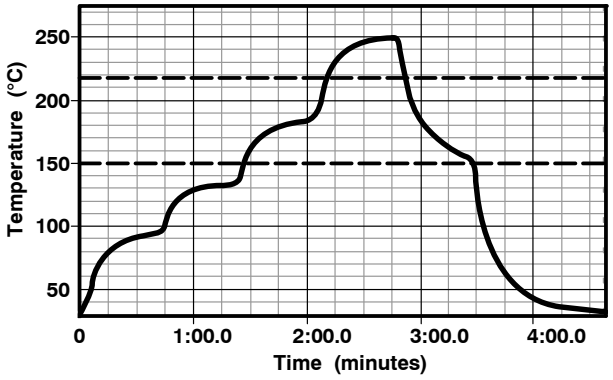
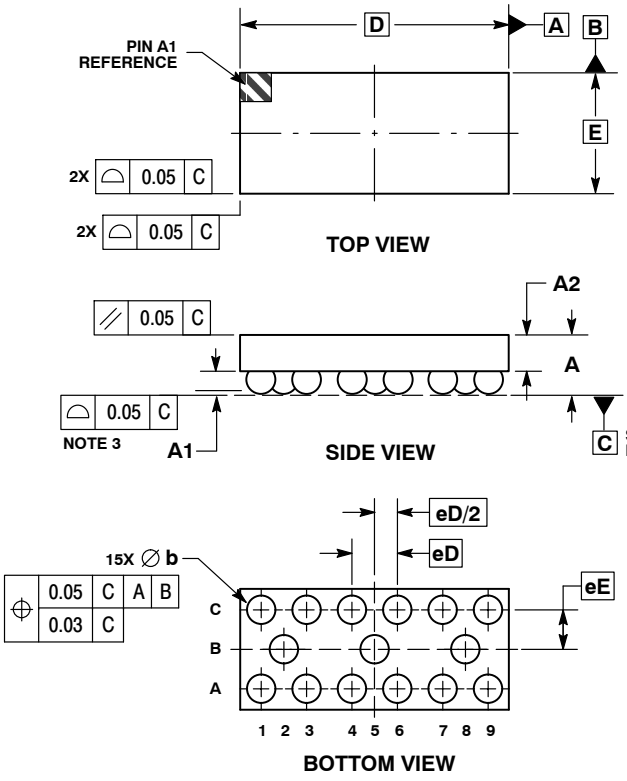


Figure 11. Lead−free (SnAgCu) Solder Ball Reflow Profile

CSPEMI306A

PACKAGE DIMENSIONS

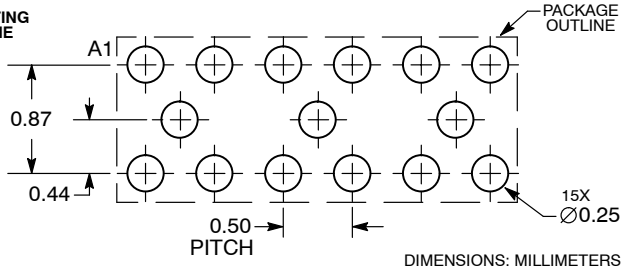
WLCSP15, 2.96x1.33
CASE 567BS−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.56	0.65
A1	0.21	0.27
A2	0.40 REF	
b	0.29	0.35
D	2.96 BSC	
E	1.33 BSC	
eD	0.50 BSC	
eE	0.435 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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