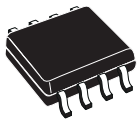
STS1NK60Z

N-CHANNEL 600V - 13Ω - 0.25A - SO-8
Zener-Protected SuperMESH™ Power MOSFET

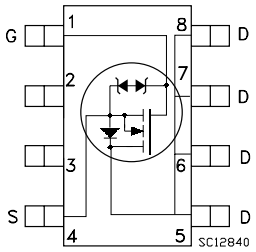
TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STS1NK60Z	600 V	< 15 Ω	0.25 A	2 W

- TYPICAL $R_{DS}(on)$ = 13Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED



SO-8

INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- AC ADAPTORS AND BATTERY CHARGERS
- SWITH MODE POWER SUPPLIES (SMPS)

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS1NK60Z	S1NK60Z	SO-8	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25°C	0.25	A
I_D	Drain Current (continuous) at T_C = 100°C	0.16	A
I_{DM} (•)	Drain Current (pulsed)	1	A
P_{TOT}	Total Dissipation at T_C = 25°C	2	W
	Derating Factor	0.016	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	800	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150	°C °C

(•) Pulse width limited by safe operating area
(1) I_{SD} ≤0.3A, di/dt ≤200A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.

THERMAL DATA

Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 0.4 A		13	15	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = V, I_D = 0.4 A		0.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		94 17.6 2.8		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 480V		11		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 300V, I_D = 0.4 A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		5.5 5		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 480V, I_D = 0.8 A, V_{GS} = 10V		4.9 1 2.7	6.9	nC nC nC

SWITCHING OFF

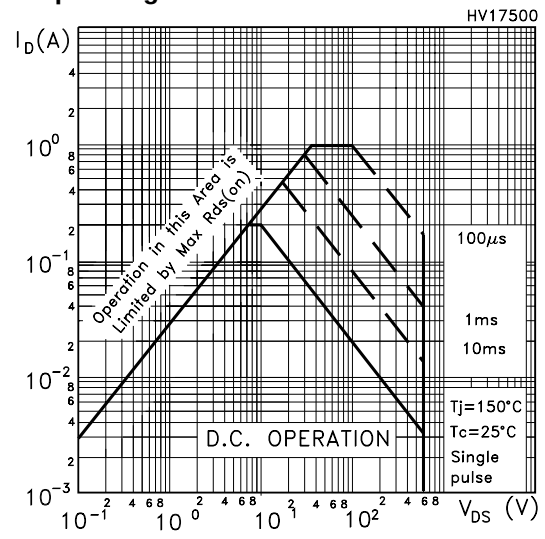
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 300V, I_D = 0.4A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		13 28		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} =480V, I_D = 0.8A, R_G = 4.7Ω, V_{GS} = 10V (Inductive Load see, Figure 5)		28 12.5 48		ns ns ns

SOURCE DRAIN DIODE

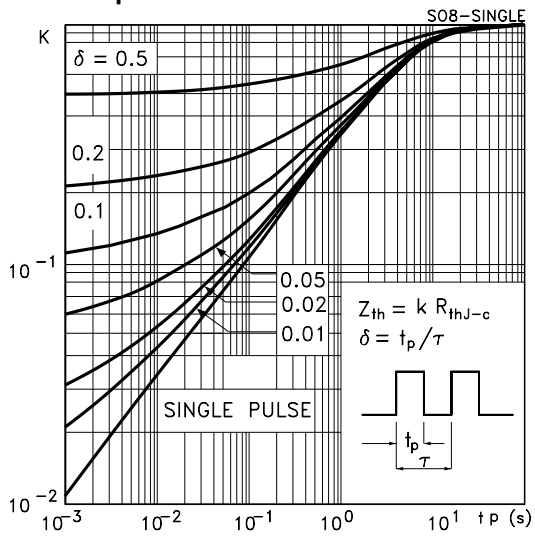
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				0.25 1	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 0.25A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 0.8 A, di/dt = 100A/µs V_{DD} = 20V, T_j = 150°C (see test circuit, Figure 5)		140 224 3.2		ns nC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

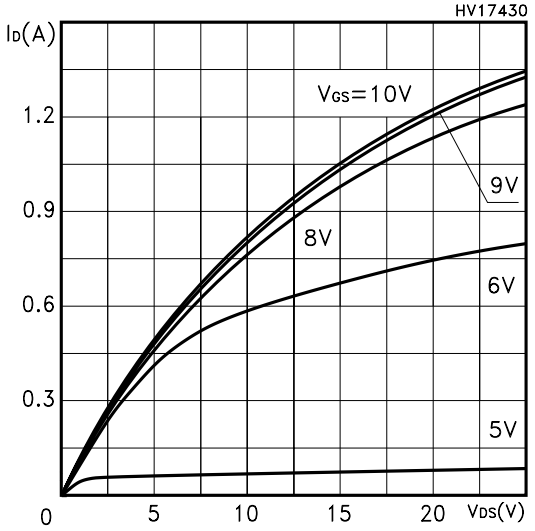
Safe Operating Area



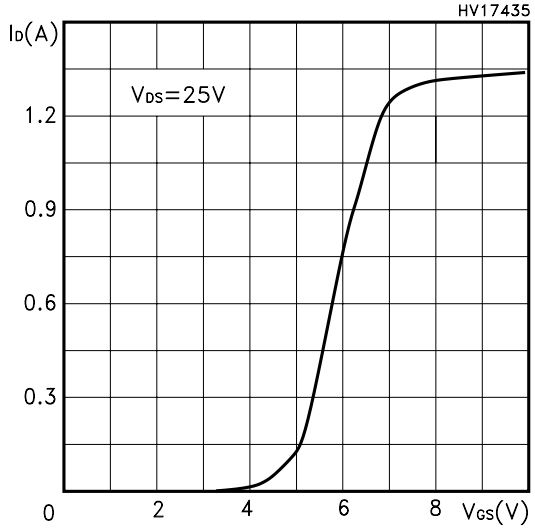
Thermal Impedance



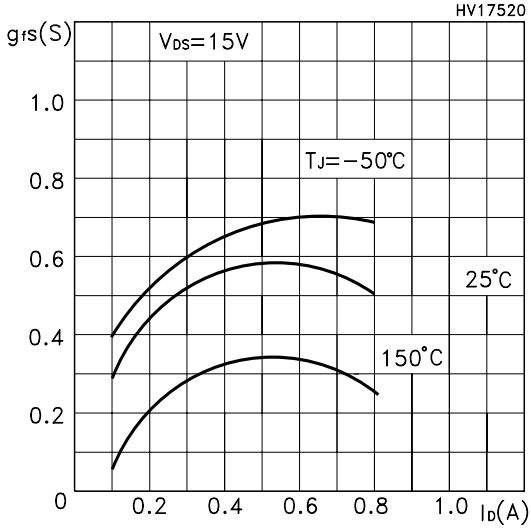
Output Characteristics



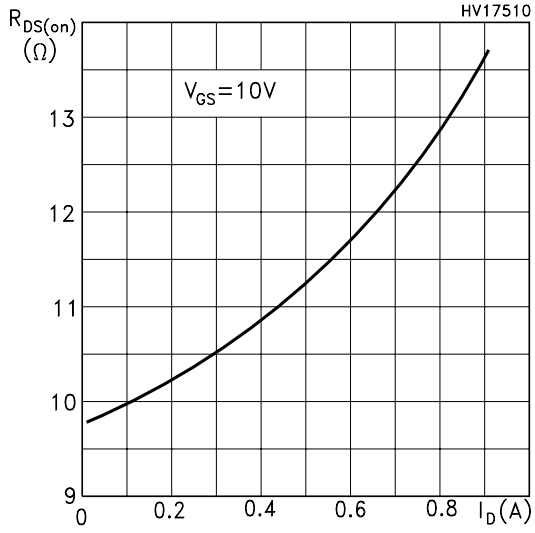
Transfer Characteristics



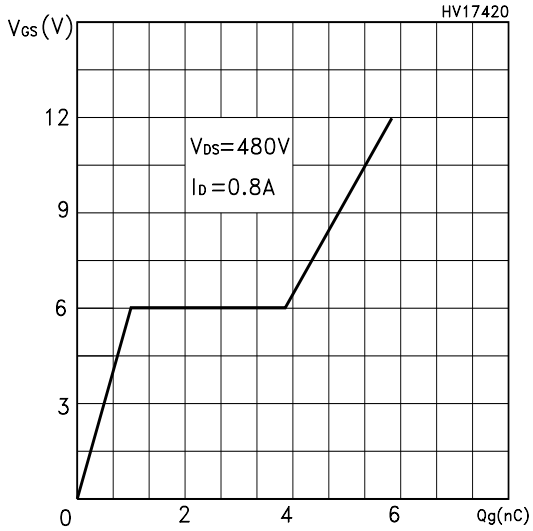
Transconductance



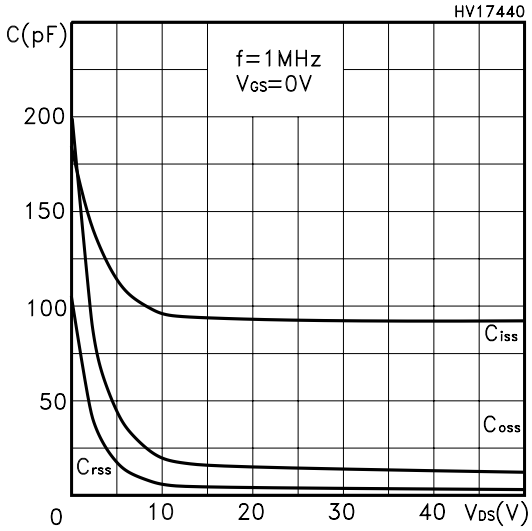
Static Drain-source On Resistance



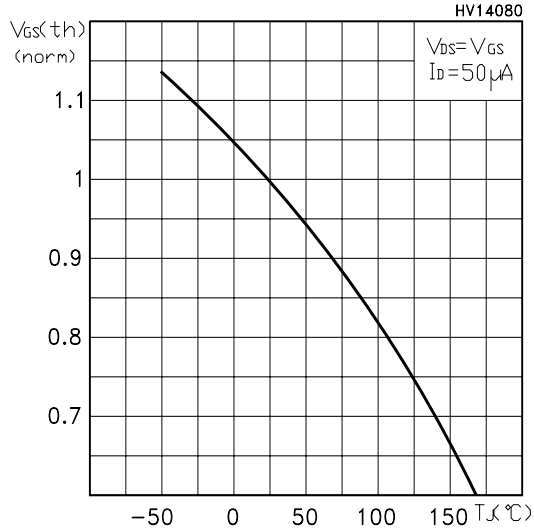
Gate Charge vs Gate-source Voltage



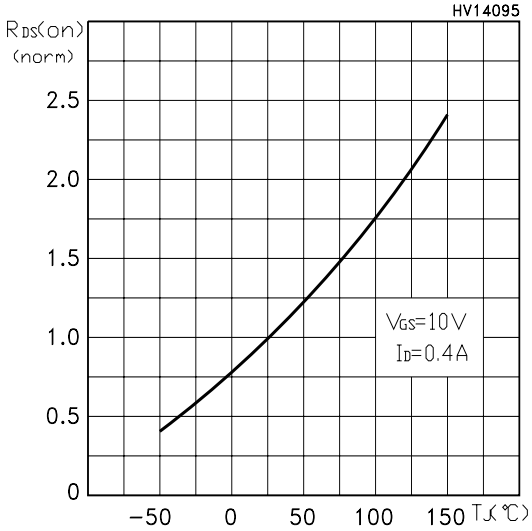
Capacitance Variations



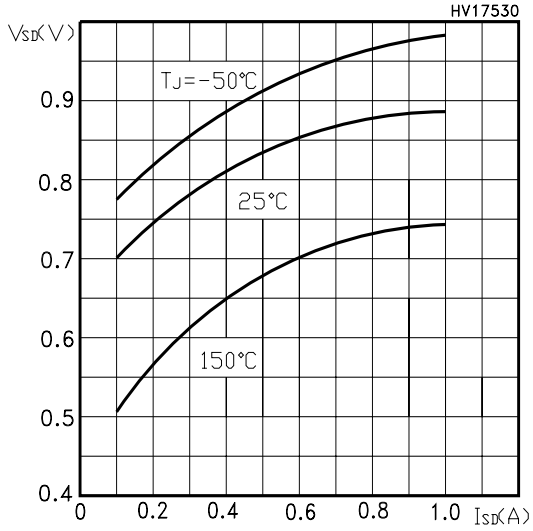
Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature

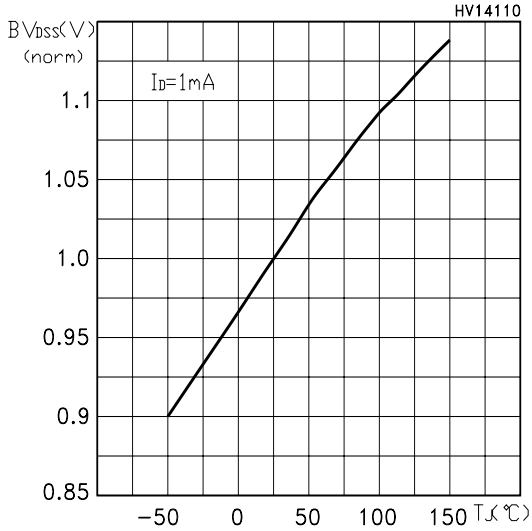


Fig. 1: Unclamped Inductive Load Test Circuit

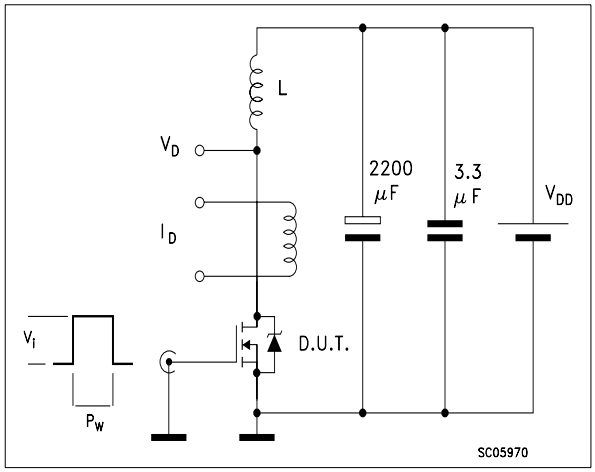


Fig. 2: Unclamped Inductive Waveform

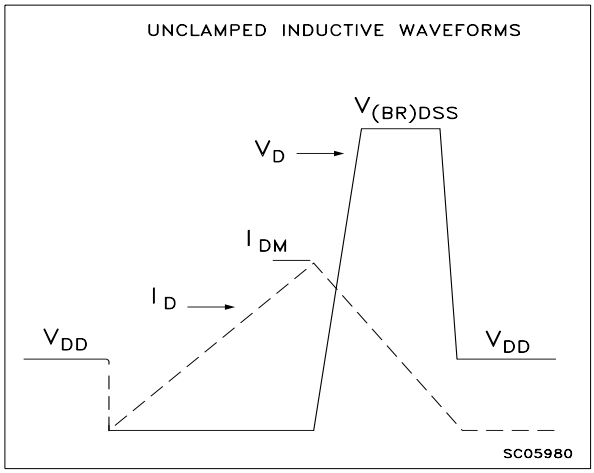


Fig. 3: Switching Times Test Circuit For Resistive Load

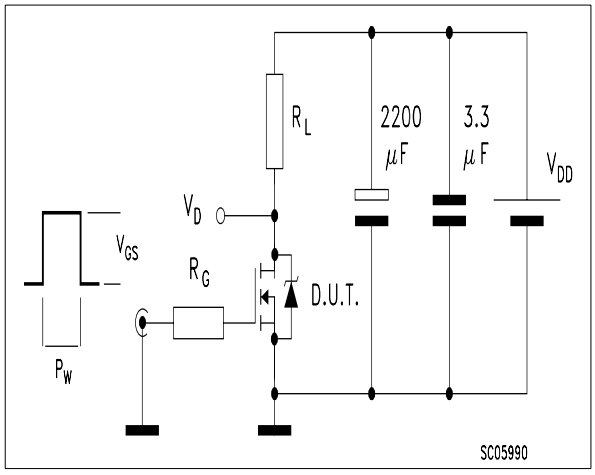


Fig. 4: Gate Charge test Circuit

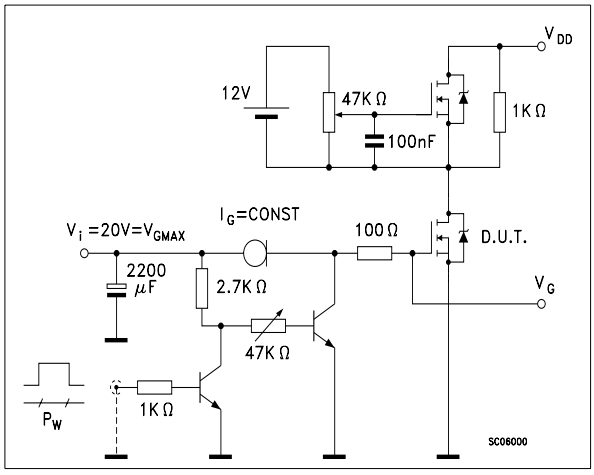
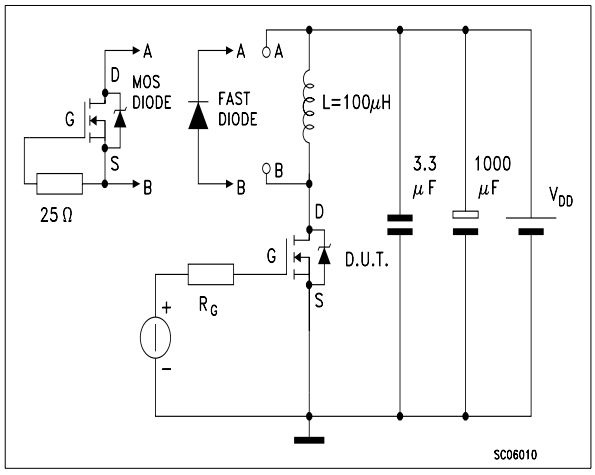
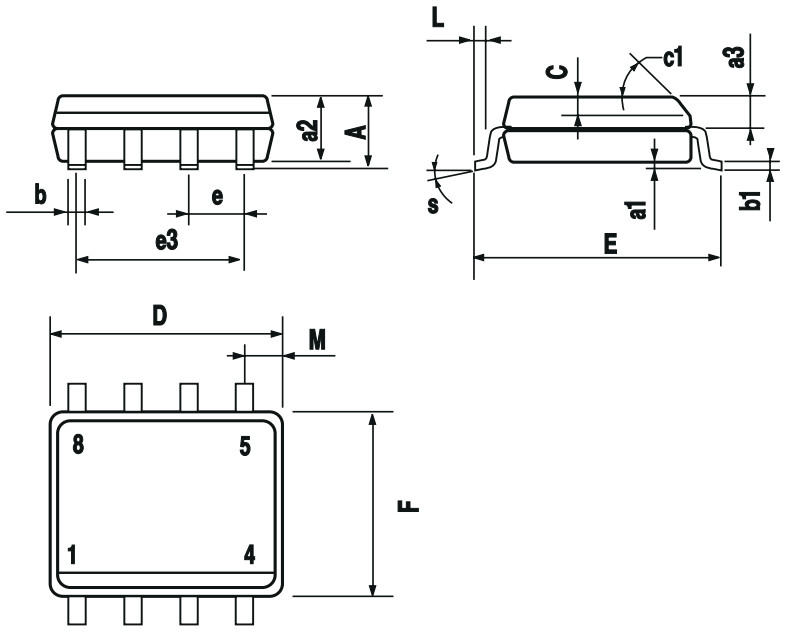


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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