

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max  $t_{pd}$  of 4.8 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- B-Port Outputs Have Equivalent 26- $\Omega$  Series Resistors, So No External Resistors Are Required
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## DESCRIPTION/ORDERING INFORMATION

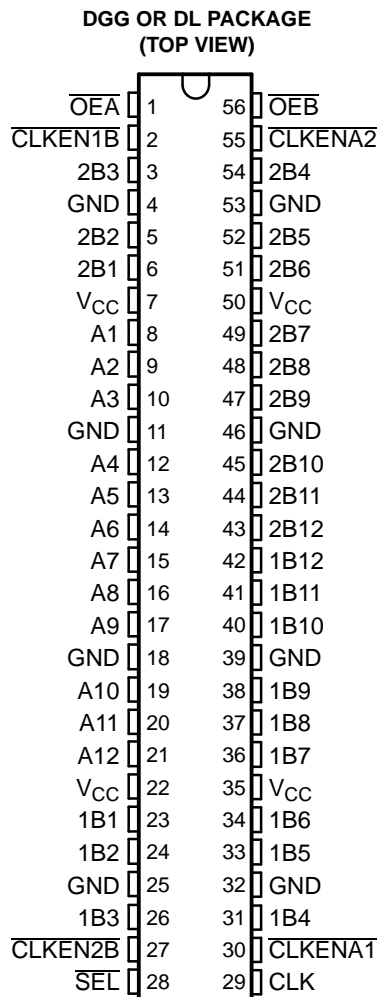
This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH162268 is used for applications in which data must be transferred from a narrow high-speed bus to a wide, lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKEN) inputs are low. The select ( $\overline{SEL}$ ) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables ( $\overline{OEA}$ ,  $\overline{OEB}$ ). These control terminals are registered, so bus direction changes are synchronous with CLK.

The B outputs, which are designed to sink up to 12 mA, include equivalent 26- $\Omega$  resistors to reduce overshoot and undershoot.



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCH162268DL	ALVCH162268
		Tape and reel	SN74ALVCH162268DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH162268GR	ALVCH162268
	VFBGA - GQL	Tape and reel	SN74ALVCH162268KR	VH2268
VFBGA - ZQL (Pb-free)	74ALVCH162268ZQLR			

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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Widebus is a trademark of Texas Instruments.

**SN74ALVCH162268**  
**12-BIT TO 24-BIT REGISTERED BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

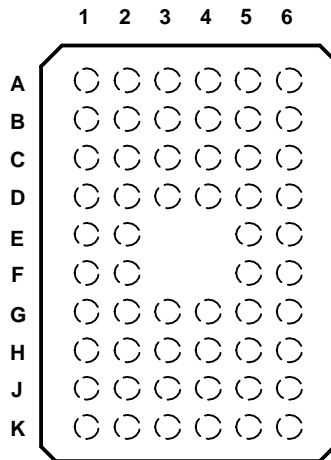
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**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible, and  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to  $\overline{OE}$  being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**GQL OR ZQL PACKAGE**  
**(TOP VIEW)**



**TERMINAL ASSIGNMENTS**

	1	2	3	4	5	6
A	2B3	$\overline{CLKEN1B}$	$\overline{OE\bar{A}}$	$\overline{OE\bar{B}}$	$\overline{CLKENA2}$	2B4
B	2B1	2B2	GND	GND	2B5	2B6
C	A2	A1	$V_{CC}$	$V_{CC}$	2B7	2B8
D	A4	A3	GND	GND	2B9	2B10
E	A6	A5			2B11	2B12
F	A7	A8			1B11	1B12
G	A9	A10	GND	GND	1B9	1B10
H	A11	A12	$V_{CC}$	$V_{CC}$	1B7	1B8
J	1B1	1B2	GND	GND	1B5	1B6
K	1B3	$\overline{CLKEN2B}$	$\overline{SEL}$	CLK	$\overline{CLKENA1}$	1B4

## FUNCTION TABLES

### OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OE\bar{A}}$	$\overline{OE\bar{B}}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

### A-TO-B STORAGE ( $\overline{OE\bar{B}} = L$ )

INPUTS				OUTPUTS	
$\overline{CLKEN\bar{A}1}$	$\overline{CLKEN\bar{A}2}$	CLK	A	1B	2B
H	H	X	X	1B <sub>0</sub> <sup>(1)</sup>	2B <sub>0</sub> <sup>(1)</sup>
L	L	↑	L	L <sup>(2)</sup>	X
L	L	↑	H	H <sup>(2)</sup>	X
X	L	↑	L	X	L
X	L	↑	H	X	H

- (1) Output level before the indicated steady-state input conditions were established
- (2) Two CLK edges are needed to propagate data.

### B-TO-A STORAGE ( $\overline{OE\bar{A}} = L$ )

INPUTS						OUTPUT
$\overline{CLKEN\bar{1}B}$	$\overline{CLKEN\bar{2}B}$	CLK	$\overline{SEL}$	1B	2B	A
H	X	X	H	X	X	A <sub>0</sub> <sup>(1)</sup>
X	H	X	L	X	X	A <sub>0</sub> <sup>(1)</sup>
L	L	↑	H	L	X	L
L	L	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

- (1) Output level before the indicated steady-state input conditions were established



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range	Except I/O ports <sup>(2)</sup>		V
		-0.5	V <sub>CC</sub> + 0.5	
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50 mA
I <sub>O</sub>	Continuous output current			±50 mA
	Continuous current through each V <sub>CC</sub> or GND			±100 mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package		64 °C/W
		DL package		56
		GQL/ZQL package		42
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V, maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**SN74ALVCH162268**  
**12-BIT TO 24-BIT REGISTERED BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

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**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.65	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current (A port)	$V_{CC} = 1.65\text{ V}$	-4	mA
		$V_{CC} = 2.3\text{ V}$	-12	
		$V_{CC} = 2.7\text{ V}$	-12	
		$V_{CC} = 3\text{ V}$	-24	
	High-level output current (B port)	$V_{CC} = 1.65\text{ V}$	-2	
		$V_{CC} = 2.3\text{ V}$	-6	
		$V_{CC} = 2.7\text{ V}$	-8	
		$V_{CC} = 3\text{ V}$	-12	
$I_{OL}$	Low-level output current (A port)	$V_{CC} = 1.65\text{ V}$	4	mA
		$V_{CC} = 2.3\text{ V}$	12	
		$V_{CC} = 2.7\text{ V}$	12	
		$V_{CC} = 3\text{ V}$	24	
	Low-level output current (B port)	$V_{CC} = 1.65\text{ V}$	2	
		$V_{CC} = 2.3\text{ V}$	6	
		$V_{CC} = 2.7\text{ V}$	8	
		$V_{CC} = 3\text{ V}$	12	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	A port	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V
		I <sub>OH</sub> = -4 mA	1.65 V	1.2			
		I <sub>OH</sub> = -6 mA	2.3 V	2			
		I <sub>OH</sub> = -12 mA	2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
	I <sub>OH</sub> = -24 mA	3 V	2				
	B port	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			
		I <sub>OH</sub> = -2 mA	1.65 V	1.2			
		I <sub>OH</sub> = -4 mA	2.3 V	1.9			
		I <sub>OH</sub> = -6 mA	2.3 V	1.7			
			3 V	2.4			
		I <sub>OH</sub> = -8 mA	2.7 V	2			
	I <sub>OH</sub> = -12 mA	3 V	2				
V <sub>OL</sub>	A port	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		I <sub>OL</sub> = 6 mA	2.3 V			0.4	
		I <sub>OL</sub> = 12 mA	2.3 V			0.7	
			2.7 V			0.4	
		I <sub>OL</sub> = 24 mA	3 V			0.55	
	B port	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	
		I <sub>OL</sub> = 2 mA	1.65 V			0.45	
		I <sub>OL</sub> = 4 mA	2.3 V			0.4	
		I <sub>OL</sub> = 6 mA	2.3 V			0.55	
			3 V			0.55	
		I <sub>OL</sub> = 8 mA	2.7 V			0.6	
	I <sub>OL</sub> = 12 mA	3 V			0.8		
	I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V	25		μA		
	V <sub>I</sub> = 1.07 V		-25				
	V <sub>I</sub> = 0.7 V	2.3 V	45				
	V <sub>I</sub> = 1.7 V		-45				
	V <sub>I</sub> = 0.8 V	3 V	75				
	V <sub>I</sub> = 2 V		-75				
	V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V	±500				
I <sub>OZ</sub> <sup>(3)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	μA	
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3.5		pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	9		pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**SN74ALVCH162268**  
**12-BIT TO 24-BIT REGISTERED BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

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**TIMING REQUIREMENTS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
$f_{\text{clock}}$	Clock frequency	120		125		150		MHz	
$t_w$	Pulse duration, CLK high or low	3.3		3.3		3.3		ns	
$t_{\text{su}}$	Setup time	A data before CLK $\uparrow$		4.5		4		3.4	
		B data before CLK $\uparrow$		0.8		1.2		1	
		$\overline{\text{SEL}}$ before CLK $\uparrow$		1.4		1.6		1.3	
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ before CLK $\uparrow$		3.6		3.4		2.8	
		$\overline{\text{CLKEN1B}}$ or $\overline{\text{CLKEN2B}}$ before CLK $\uparrow$		3.2		3		2.5	
		$\overline{\text{OE}}$ before CLK $\uparrow$		4.2		3.9		3.2	
$t_h$	Hold time	A data after CLK $\uparrow$		0		0		0.2	
		B data after CLK $\uparrow$		1.3		1.2		1.3	
		$\overline{\text{SEL}}$ after CLK $\uparrow$		1		1		1	
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ after CLK $\uparrow$		0.1		0.1		0.4	
		$\overline{\text{CLKEN1B}}$ or $\overline{\text{CLKEN2B}}$ after CLK $\uparrow$		0.1		0		0.5	
		$\overline{\text{OE}}$ after CLK $\uparrow$		0		0		0.2	

**SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

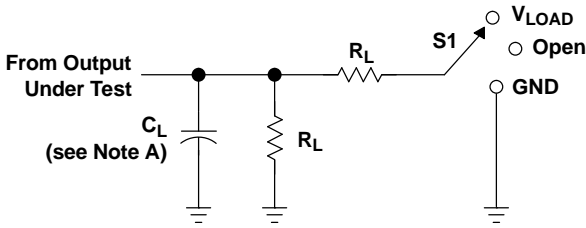
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$				120		125		150		MHz
$t_{\text{pd}}$	CLK	B	8	1.6	6.1	5.9		1.8	5.4	ns
		A (1B)	8	1.6	5.8	5.4		1.7	4.8	
		A (2B)	8	1.6	5.8	5.3		1.8	4.8	
		A ( $\overline{\text{SEL}}$ )	11	2.5	7.3	6.5		2.4	5.8	
$t_{\text{en}}$	CLK	B	12	2.7	7.2	6.8		2.6	6.1	ns
		A	9	2	6.2	5.6		1.8	5.1	
$t_{\text{dis}}$	CLK	B	10	2.8	7.2	6.1		2.5	5.9	ns
		A	9	2	6.5	5.4		2.1	5	

**OPERATING CHARACTERISTICS**

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}, f = 10\text{ MHz}$	87	120	pF
	Outputs disabled		80.5	118	

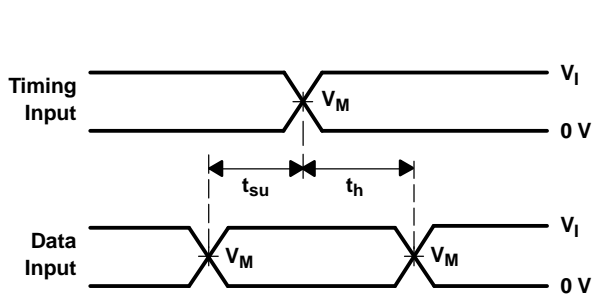
PARAMETER MEASUREMENT INFORMATION



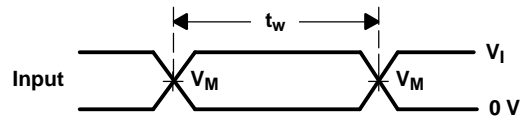
LOAD CIRCUIT

TEST	S1
$t_{pd}$ $t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PZH}$	Open $V_{LOAD}$ GND

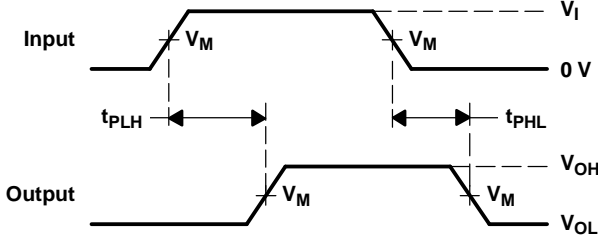
$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



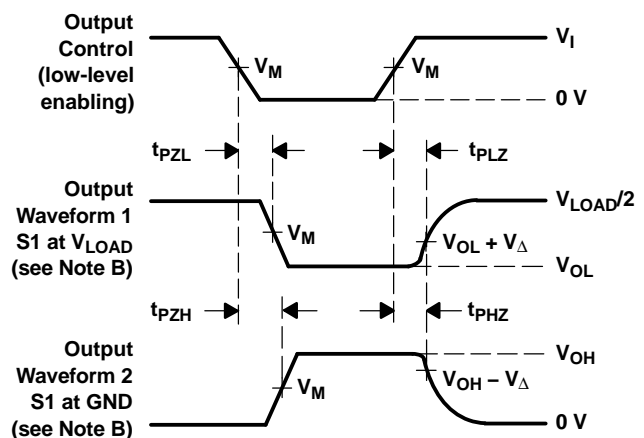
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVCH162268DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162268	<a href="#">Samples</a>
SN74ALVCH162268GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162268	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH162268GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH162268GR	TSSOP	DGG	56	2000	367.0	367.0	45.0

# MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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