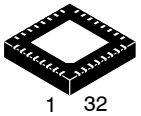
NCV53480

Low-Power OOK/FSK/ASK ISM Band Transceiver

ON Semiconductor®

http://onsemi.com



NQFP 32, 6x6
CASE 560AR

MARKING DIAGRAM

NCV53480−C = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package
CCCCC = Country of Origin*
(*Not required if assembled in USA)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

General Description

The NCV53480 ASSP is a low power OOK/FSK/ASK transceiver designed for operation in the ISM band from 260 MHz to 470 MHz. It is intended for use in narrowband, low data rate applications in the range of 1 kbps to 60 kbps. The receiver architecture is low−IF, and contains image reject filtering to provide 40 dB of image reject. The IF filter is fully integrated on chip with selectable bandwidth settings of 100 kHz, 200 kHz, and 300 kHz. The transmitter output power is programmable from −20 to 10 dBm.

On−chip digital circuitry can be configured to have the part perform periodic channel polling on up to 3 channels, with full control of the polling interval and active receive time for each channel. Additional register control can be used to have the part wake based on a pattern, energy level, or detected ID.

Features

- Single Supply Operation from 2.2 V to 3.63 V
- Temperature Range: −40°C to +125°C
- Simultaneous OOK/FSK (De)modulation
- No External Switch Needed Between LNA Input and PA Output
- Low Current Consumption Mode (< 1 μA)
- Programmable Frequency Band from 280 MHz to 434 MHz with Multichannel Operation (3 Channels)
- Continuous Receive Current Consumption < 10 mA
- FSK Receiver Sensitivity −109 dBm at 10 kbps NRZ
- OOK Receiver Sensitivity −118 dBm at 1 kbps NRZ
- Wake−On−Pattern and Wake−On−Energy capability
- Programmable Data Rates Up to 60 kbps
- Sniff−Mode Utilizing Patented Quick−Start Oscillator
- 128 Bit Receive Buffer
- 18 mA Continuous Transmit Mode at 10 dBm Output Power
- Programmable Output Power from −20 dBm to +10 dBm
- Dual Configurations for Sniffing, Receiving and Transmitting To and From Different Sources
- Internal Self−Calibration Routines
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Two−Way Keyless Entry
- TPMS
- Remote Control
- Remote Sensing
- Automatic Meter Reading
- Consumer Electronics
- Home and Building Automation
- Wireless Security Systems
- Telemetry

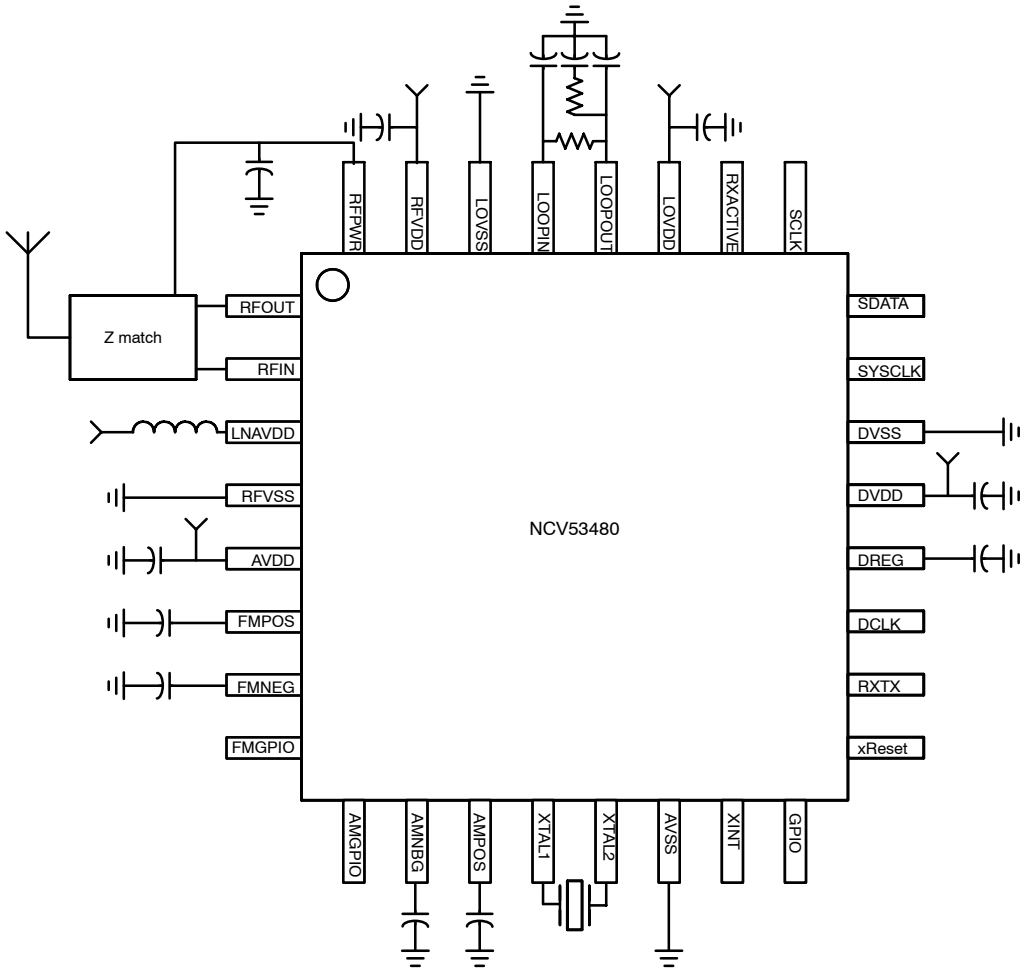


Figure 1. Pinout

Table 1. ORDERING INFORMATION

Part No.	Package	Shipping†
NCV53480MN1G−C	NQFP−32 (Pb−Free)	40 Units / Tube
NCV53480MN1R2G−C	NQFP−32 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

BLOCK DIAGRAM, PINOUT TABLE AND PAD DESCRIPTION

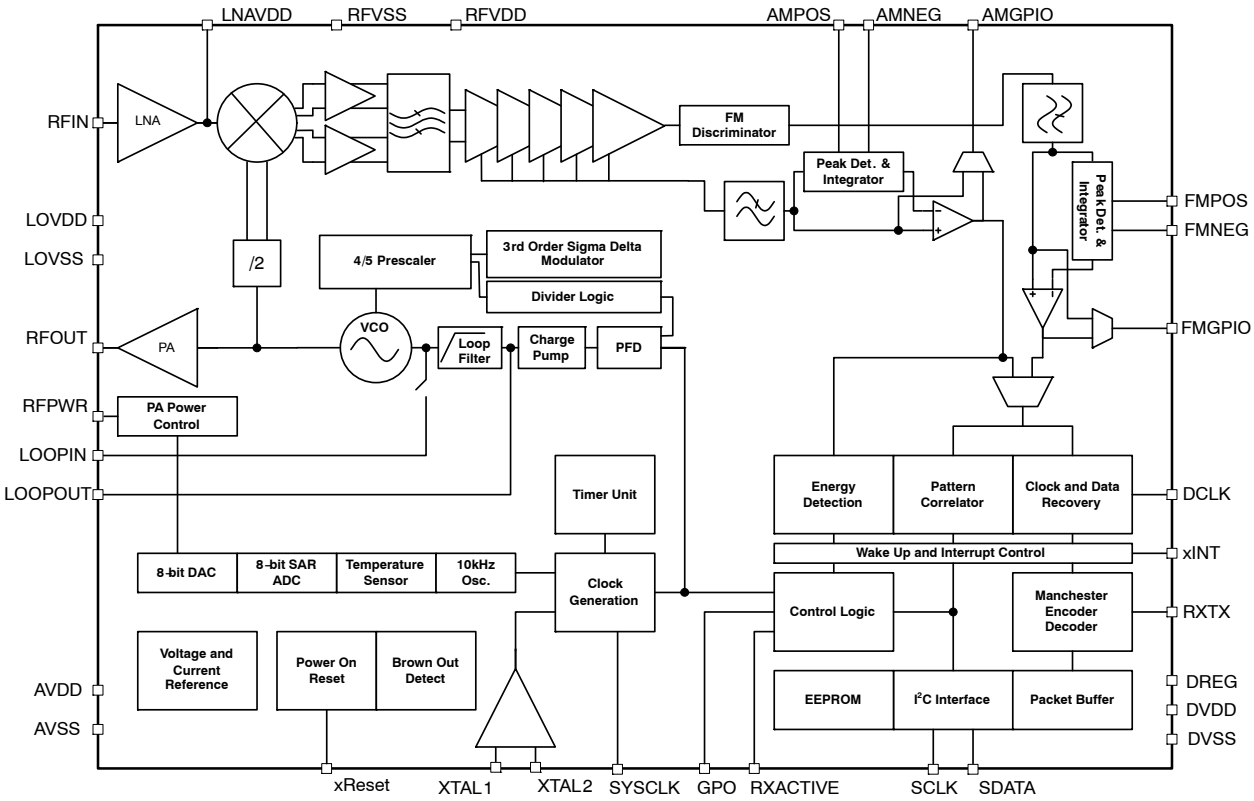


Figure 2. Block Diagram

Table 2. PINOUT AND DESCRIPTION

Pin	Name	Pad Description
1	RFOUT	RF Output
2	RFIN	RF Input
3	LNAVDD	LNA Supply Connection
4	RFVSS	V_{SS} for the RF Section
5	AVDD	V_{DD} for the Analog Section
6	FMPOS	External Cap Connection for the FM Peak Detector, or for the RC Integrator (See FSK Detector Section)
7	FMNEG	External Cap Connection for the FM Negative Peak Detector
8	FMGPIO	Multi−Function Pin Can Provide Analog FM out, FSK Sliced Data Out, and is Used as an Input for FSK Transmit.
9	AMGPIO	Multi−Function Pin Can Provide Analog RSSI, ASK Sliced Data Out, and is Used as an Input for ASK Transmit.
10	AMNEG	External Cap Connection for the AM Negative Peak Detector
11	AMPOS	External Cap Connection for the AM Peak Detector, or for the RC Integrator (See ASK Detector Options)
12	XTAL1	Crystal Oscillator Input Pin
13	XTAL2	Crystal Oscillator Output Pin
14	AVSS	V_{SS} for the Analog Section
15	xINT	Active low output for interrupt of external micro−processor during a receive event
16	GPO	General Purpose Output
17	xReset	Open Drain Digital IO. This Signal Will Go Active (‘0’) During a POR, or Can Be Pulled Active (‘0’) to Reset the Part.
18	RXTX	Recovered Data from the CDR in Receive Mode. Transmit Data for Synchronous Transmit Mode.
19	DCLK	Recovered Clock from the CDR in Receive Mode. Baud Clock for Synchronous Transmit Mode.
20	DREG	External capacitor connection for the internal digital regulator
21	DVDD	V_{DD} for the Digital Section
22	DVSS	V_{SS} for the Digital Section
23	SYSCLK	General Purpose Digital Output that can be Configured to Provide a System Clock to an External Micro−Processor
24	SDATA	Data Pin for the Serial I^2C Register Interface
25	SCLK	Clock pin for the serial I^2C Register Interface
26	RXACTIVE	Pin Used to Indicate the Device is in Receive
27	LOVDD	V_{DD} for the PLL
28	LOOPOUT	Charge Pump Output to External Loop Filter
29	LOOPIN	VCO Control Input When External Loop Filter is Selected
30	LOVSS	V_{SS} for the PLL
31	RFVDD	V_{DD} for the RF Section
32	RFPWR	Transmitter Power Supply for Output Power Regulation

DC SPECIFICATIONS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
DVDD	Digital DC Supply Voltage (Note 1)	−0.4	4.0	V
AVDD	Analog DC Supply Voltage (Note 1)	−0.4	4.0	V
RFVDD	RF DC Supply Voltage (Note 1)	−0.4	4.0	V
Vin	Input Pin Voltage (Note 1)	−0.4	4.0	V
Iin	Input Pin Current	−100	100	mA
MaxRFin	Input RF Level		+10	dBm
ESD	Human Body Model (Note 2)		2	kV
Tstrg	Storage Temperature	−40	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Time limit at maximum V_{DD} must be less than 100 milliseconds.
2. The RFOUT passes up to 1.25 kV.

DC CHARACTERISTICS

Table 4. DC CHARACTERISTICS (Typical Application Circuit, 50 Ω System Impedance, unless otherwise noted) (V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C) Operating outside the recommended operating ranges for extended periods of time may affect device reliability

Parameter	Description	Min	Typ	Max	Unit
VOLTAGE SUPPLY					
DVDD	Digital DC supply voltage	2.2		3.63	V
AVDD	Analog DC supply voltage	2.2		3.63	V
RFVDD	RF DC supply voltage	2.2		3.63	V
GROUND					
RFVSS	RF Ground Pin	0	0	0	V
AVSS	Analog Ground Pin	0	0	0	
DVSS	Digital Ground Pin	0	0	0	
POR					
POR	POR Ramp Rate	0		0.1	V/msec
CURRENT CONSUMPTION					
IDDS	Standby current		1.2		mA
	Sleep mode		1		μA
TRANSMIT CURRENT					
+10 dBm	V_{DD} = 3.3 V as PA reference		18		mA
RECEIVER CURRENT					
Base Receiver	Clock and data recovery off.		10		mA
Wake−On−Pattern	Part configured with ASK detector, pattern correlator, and clock and data recovery enabled.		10.5		mA
REGULATORS					
Digital Regulator		2.0	2.1	2.15	V
DAC					
Dref	DAC reference voltage	1.95	2	2.025	V
DDNL/INL	Differential non−linearity and integral non−linearity.		0.5	1	LSB
LOGIC INPUTS					
VINH	Input High Voltage	0.7 * DVDD		DVDD	V
VINL	Input Low voltage	0		0.3 * DVDD	V
IIN	Input current (input high/input low)	−1		1	μA
LOGIC OUTPUTS					
VOH	Output high voltage	0.8*DVDD		DVDD	
VOL	Output low voltage	0		0.2*DVDD	

STARTUP TIMING

Table 5. STARTUP TIMING

Symbol	Parameter	Description	Min	Typ	Max	Unit
T_{Ready}	Without Quick−Start	Time from low−power standby to crystal enabled, ready for instruction.		10		ms
	With Quick−Start			30		μs
T_{RX}	Without Quick−Start	Time for receiver startup (does not include data filter setting dependant settling time) from low−power state.		10		ms
	With Quick−Start			120		μs
T_{TX}	Without Quick−Start	Time for transmitter startup, ready for data transmission from a low−power state.		10		ms
	With Quick−Start			120		μs
$T_{RXTX}/T_{RXRX}/T_{TXRX}/T_{TXTX}$		Receive to transmit and transmit to receive switching time and channel switching time.		120		μs

RF SPECIFICATIONS

Table 6. OSCILLATORS CHARACTERISTICS (Typical Application Circuit, 50 Ω System Impedance, unless otherwise noted) (V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C)

Parameter	Description	Min	Typ	Max	Unit
CRYSTAL OSCILLATOR					
Frequency	Crystal oscillator is selectable between 20 MHz or 24 MHz		20 / 24		MHz
INTERNAL IC OSCILLATOR					
Frequency	IC oscillator operating frequency	9.95	10.0	10.05	KHz
Temperature Coefficient				500	ppm/C
PHASE−LOCKED LOOP (PLL)					
PLL Frequency Range	PLL Frequency Range	174		470	MHz
Phase Noise at 10 kHz Offset			−80		dBc/Hz
Phase Noise at 100 kHz Offset			−70		
PLL Lock Time	Using internal loop filter		40		μs

Table 7. RECEIVER CHARACTERISTICS (Typical Application Circuit, 50 Ω System Impedance, unless otherwise noted)
(V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C

Parameter	Description	Min	Typ	Max	Unit
RF Frequency Range	Min frequency is 300 MHz with 24 MHz crystal	260		470	MHz
ON OFF KEYING (BER = 1E−3, FRF = 434 MHz, LNA and PA matched separately)					
Sensitivity	IF bandwidth = 100 kHz. 1 kbps with NRZ encoding		−118		dBm
Sensitivity	IF bandwidth = 300 Khz. 1 kbps with NRZ encoding.		−116		dBm
IF Filter Bandwidth		85 180 260	100 200 300	115 220 340	kHz
IF Filter Center		475	500	535	kHz
Image Rejection			35		dB
CHANNEL FILTERING					
1st Adjacent Channel Rejection	Desired signal (1 kbps OOK), IFBW = 100 kHz, 3 dB above input sensitivity level, CW Interferer power level increased until BER = 10E−3, interferer 100 kHz from desired		25		dB
Co−Channel Rejection			−10		dB
RECEIVED SIGNAL STRENGTH INDICATION (RSSI)					
Range		−120		−60	dBm
RSSI Gain			22.5		mV/dB

Table 8. TRANSMITTER CHARACTERISTICS (Typical Application Circuit, 50 Ω system impedance, unless otherwise noted)
(V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C)

Parameter	Description	Min	Typ	Max	Unit
Transmit Power	V_{DD} = 3.0 V, T_A = 25°C, V_{DD} as PA reference		10		dBm
Power variation vs. Temp			±1		dB
Power variation vs. V_{DD}	Using RFPWR for regulated reference		±1		dB
	Using V_{DD} as the PA reference		+2/ −3.5		

3. Supply current, output power, and efficiency are greatly dependent on board layout and PAOUT match.

Table 9. MODULATION CHARACTERISTICS (Typical Application Circuit, 50 Ω System Impedance, unless otherwise noted)
(V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C)

Parameter	Description	Min	Typ	Max	Unit
AMPLITUDE SHIFT KEYING (ASK)					
ASK post detection bandwidth filter		0.6		40	kHz
FREQUENCY SHIFT KEYING (FSK)					
Conversion Gain			2.5 5.0 7.5 10		mV/kHz
FVoff	Input referred frequency offset		20		kHz
FSK Filter Cutoff	Filter cutoff frequency which sets the post detection bandwidth of the receiver		72 36 24 18 12 9 6 3		kHz

INTERNAL BLOCK DIAGRAMS AND DESCRIPTION

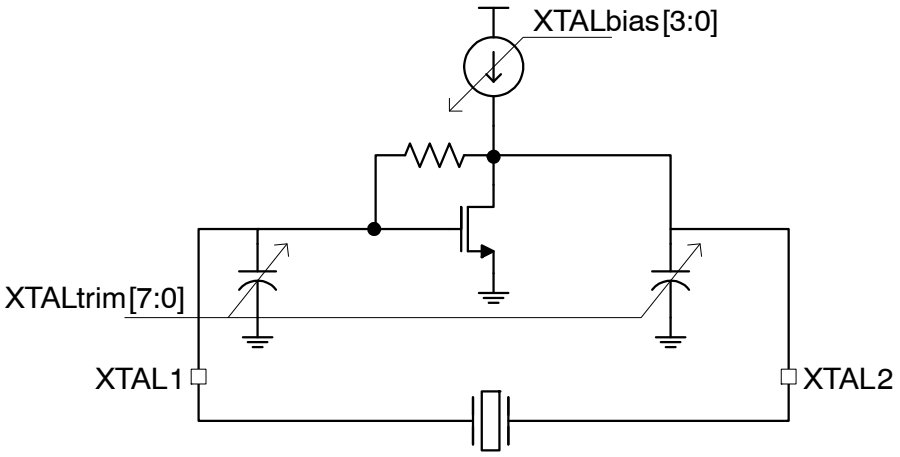


Figure 3. Crystal Oscillator

The internal crystal oscillator circuitry can be used with one of two inexpensive, readily available frequencies: 20 MHz, and 24 MHz. The XTAL Select bit of the General Options register needs to be set correctly based upon the crystal used. An on chip 8−bit capacitive DAC is connected to the crystal pins provide the load caps for the crystal, and allow fine tuning of the crystal frequency. The 8−bit control for the caps is located in the Crystal Trim register. The full scale range for the internal capacitors is 40 pF, the set value should be chosen such that the series value added to any PCB capacitance adds to the load capacitance specified for the crystal.

The current reference for the crystal oscillator amplifier is adjustable via the XTAL Current Trim register. By default, the device is set to 0x8. This provides sufficient gain for crystals with a load specified as 16 pF. For crystals requiring higher values of load capacitance, this setting may need to be increased to ensure reliable startup.

On power−up, the crystal oscillator is enabled, XTALbias is set to 0xF, and the internal load caps are set to 0x40. This ensures proper startup regardless of crystal. Once the device has been powered, then internal state machine will write the values stored in EEPROM for the bias and load−cap trim into the trim registers.

Table 10. CRYSTAL SPECIFICATION

Parameter	Min	Typ	Max	Unit	Notes
Tolerance			50	ppm	
R		20	30		
C	4.4	8.8		fF	
Lm		5	10	mH	The lower the better
C_p			7.0	pF	
C_{load}		10	16	pF	

SYSCLK Output

The NCV53480 can be used to provide a system clock to other external devices for device synchronization. The General Options register contains the control bits for selecting the SYSCLK output frequency.

The output can also be disabled when the NCV53480 is not required to provide a clock output. On power−up or reset, the SYSCLK pin is enabled and defaults to the crystal frequency divided by 160.

Quick−Start Oscillator (QSO)

To save power, and remove timing uncertainty from crystal startup, the NCV53480 includes ON Semiconductor's patented Quick−Start oscillator technology. The Quick−Start oscillator is an internal oscillator trimmed to the crystal frequency. Upon crystal start, the Quick−Start oscillator drives the crystal to quickly build energy in the motional inductance of the crystal, reducing startup time from milliseconds to microseconds.

To use the Quick−Start oscillator, it first needs to be calibrated by writing the Command Register to the Quick−Start Calibration instruction. All of the circuitry for the calibration is on board. During the calibration, the user can poll Status Register A to determine when it has completed by monitoring the Busy bit. After completion, the user should also check the RC/QS calibration bit of Status Register A to ensure the calibration was successful. Once calibrated, the Quick−Start oscillator is automatically enabled and will be used to assist in crystal startup anytime the part transitions from a low power mode to a high power mode. The calibration value is in the Quick Start Trim register, and is stored in EEPROM. The Quick−Start Calibrated bit of the Receiver Trim register stores whether the Quick−Start has been calibrated.

The figure below shows a crystal startup sequence using the Quick−Start oscillator.

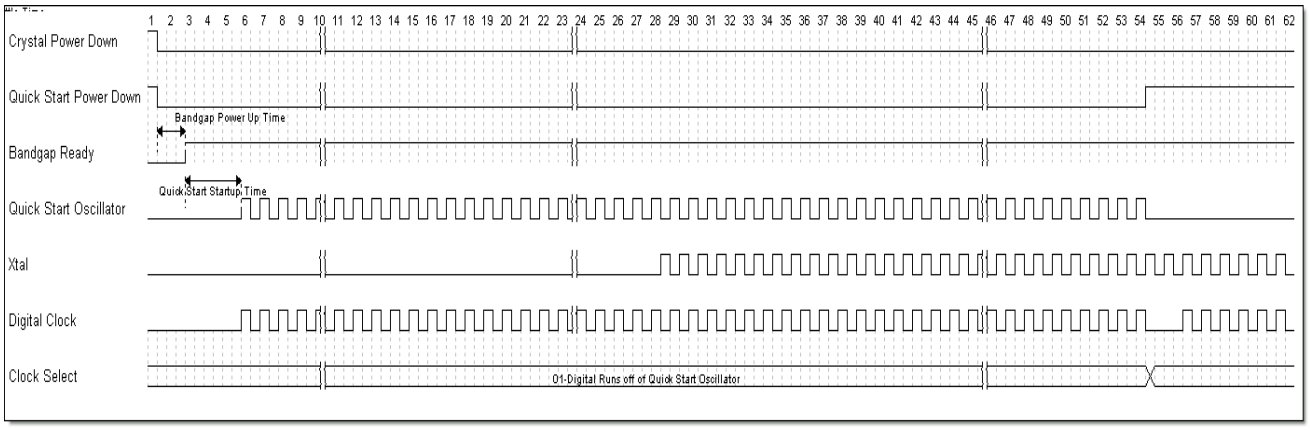


Figure 4. Quick−Start Cycle

To detect that the crystal oscillator has been properly started after a quick start cycle, a frequency and phase detector are utilized. These two detectors operate on the output of the QSO and the output of the crystal oscillator. The frequency detector counts for 400 cycles of the QSO. During that time, a similar counter counts the number of crystal clock cycles. When the QSO counter is finished, if the crystal counter is off by more than 10%, a quick start fail interrupt will occur. The phase detector is a cycle slip phase detector with a slight modification so that it will not trigger until there have been 10 edges of the QSO detected without any edges of the crystal oscillator occurring during that time. The phase detector can be enabled/disabled via bit 1 of register 0x5E.

The outputs of the two counters which form the frequency detector during startup of the crystal oscillator can also be used to adaptively trim the QSO. This is enabled via bit 0 of register 0x5E. When enabled, the output of the crystal counter is used to adjust up or down by one code the trim word for the QSO. If the crystal oscillator counter is greater than the QSO counter, the QSO trim is incremented. Similarly, if the crystal oscillator counter is less, the QSO is decremented. And finally, if they are both 400, no change to the trim is made.

If the adaptive trim function is not used, it is recommended to monitor the temperature sensor and re−calibrate the QSO when the temperature change exceeds 20°C from the last calibration for optimum performance.

A note on the QSO trim register: When the compensation is enabled, the actual trim value presented to the QSO, and the value read from the QSO trim register will differ. Recalibrating the QSO will reset the offset added by the compensation algorithm to 0.

Should the Quick−Start oscillator ever fail to start the crystal, the circuit is disabled and an interrupt is issued to the external controller. Status Register B can be used to determine the cause of the interrupt. In addition to providing an interrupt on fail, the Quick−Start oscillator continues to run in parallel with the crystal oscillator and is used to provide the system clock to ensure the integrity of the whole system. The figure below shows the crystal startup if the Quick−Start oscillator is un−calibrated or if it fails to start.

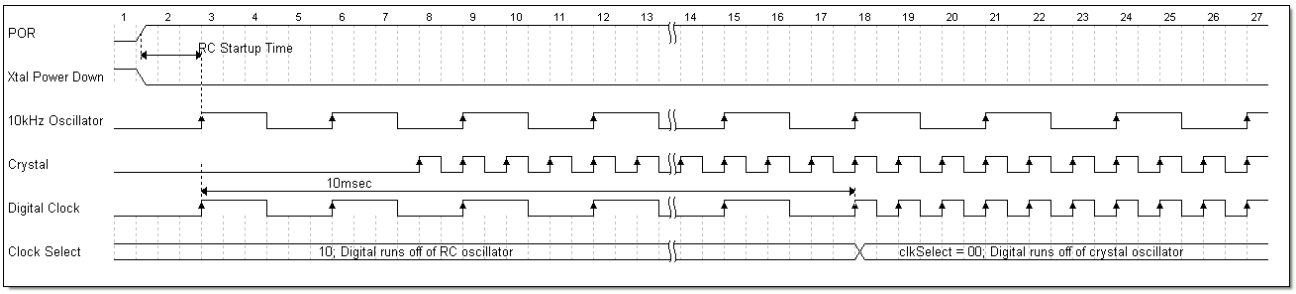


Figure 5. Natural Crystal Startup

10 kHz Oscillator

In addition to the crystal oscillator, a 10 kHz internal IC oscillator is included on chip to provide timing for receiver polling functions in Sniff−Mode. This oscillator is not factory trimmed, so to provide greater accuracy for polling functions, it can be trimmed by writing the Command Register to the RC Calibrate instruction. For applications which require poll timing accuracy better than ±6%, the oscillator should be re−calibrated with changes in temperature.

The 10 kHz Oscillator is calibrated against the crystal frequency to < 0.5% error. The calibration value is in the 10 kHz Oscillator Trim register, and is stored in EEPROM.

Temperature Sensor

An on chip temperature sensor is included in the NCV53480. The analog voltage from the sensor can be pinned out on the AMGPIO pin or using the on−board 8−bit ADC, a digital word can be read from the Temperature ADC register after executing a conversion instruction. The voltage for the temperature sensor is V_{temp} = 1 + (T − 27)/128. The ADC output code for the temperature sensor will be T_{code} = 128 + (T − 27).

To save power, the sensor is not always active. It will be active when one of the following is true:

- The part is in receive
- The Analog Test Mux register is set to output the Temperature sensor voltage on the AMGPIO pin
- An ADC conversion instruction is issued

The sensor offset is factory trimmed at 27°C to ± 1.5C. In addition to the trimmed error, the slope of the sensor is ± 5%.

ADC

The on board 8−bit DAC used for PA output power control and OOK level detection is also utilized to provide an 8−bit SAR ADC. This ADC is used primarily for best channel selection in multi−channel Sniff−Mode, but can also be used to provide a digitized output of the temperature sensor.

To perform a conversion of the temperature sensor without placing the device into multi−channel Sniff−Mode, perform the following:

1. Set any one of bits 1, 2, or 3 to a ‘1’ in either the configuration A or configuration B Sniff Configuration registers
2. Write the Command Register to the ADC conversion command.
3. Read the sensor value in the Temperature ADC register once the conversion is complete

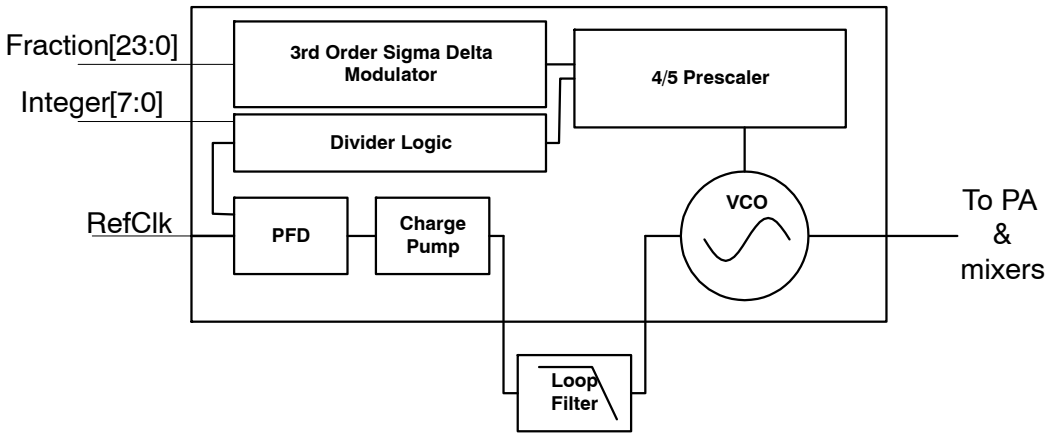


Figure 6. Fractional−N PLL

The NCV53480 uses a Sigma−Delta Fractional−N divider with a ring oscillator to provide continuous coverage of the 280−434 MHz ISM band. The lower frequency limit is 300 MHz with a 24 MHz crystal and 250 MHz with a 20 MHz crystal. In transmit mode, the VCO operates at the RF frequency, and the reference is the crystal frequency. In receive mode, the VCO operates at 2/3 of the RF frequency, and to simplify programming the part, the reference frequency is 2/3 the crystal frequency. This allows the same Integer and Fraction to be used for both receive and transmit, and reduces the number of register writes to switch between transmit and receive to just a single write. The 500 kHz offset for receive is calculated internally.

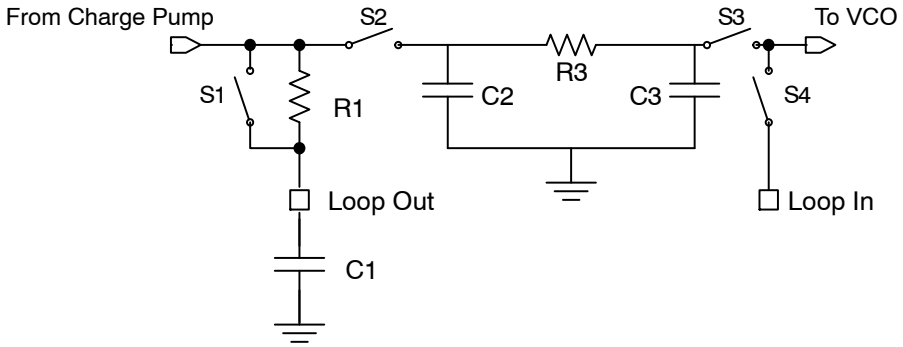


Figure 7. Loop Filter

As shown in Figure 7 above, the loop filter for the PLL can be configured in two ways by setting bit 4 of the RF PLL Trim register. The first is internal mode where S1 and S4 are open, and S1 and S3 are closed. Note that even in internal mode, C1 is still external to reduce total system cost. In external mode, S1 and S4 are closed while S2 and S3 are open allowing complete flexibility in loop filter design.

The table below shows the values of the internal loop filter components and the recommended value for C1 when using internal mode.

Table 11. INTERNAL LOOP FILTER VALUES

Component	R1	C1	C2	R3	C3
Value	1k	2 nF	150 pF	1k	80 pF

The following table provides the parameters of the VCO and charge pump for designing external loop filters.

Table 12. VCO PARAMETERS

Paramter	Kvco	Icp	Fref
Value	800 MHz/V	22.5 μA – 40 μA (Note 4)	$F_{crystal}$

4. Selectable by bits[2:0} of the RF PLL Trim Register

When using the internal loop filter, the charge pump current setting in the RF PLL Trim register should be set according to the following table based on the combination of output and crystal frequency. This will provide a 200 kHz loop bandwidth compatible with the Lock Detection circuitry.

Table 13. CHARGE PUMP CURRENTS

	250 MHz – 300 MHz	300 MHz – 350 MHz	350 MHz– 400 Mhz	400 MHz – 450 MHz
20 MHz	25 μA	30 μA	35 μA	37.5 μA
24 MHz	NA	25 μA	27.5 μA	32.5 μA

When using an external loop filter bandwidth less than approx 100 kHz, the sample time for the lock detection circuit will occur before lock is achieved, and a PLL is Unlocked flag will be set in the Status Register A. See the Lock Detection Section for further detail, and how to disable the lock checking.

Lock Detection

A digital lock detection circuit is built into the NCV53480. The output of this block is used to gate PA operation until the PLL has achieved lock. By default, this circuit is disabled after lock has been achieved. If a PLL loop bandwidth is used which doesn't allow for PLL lock with the default timing of 130 μsec lock will fail and the transmitter will be disabled. To circumvent this, setting the Infinite PLL Lock Time bit in the General Options register will over−ride the lock detect signal, and leave the lock detection on continuously. Pin GPO can be configured to output the lock detect signal for external monitoring using the GPO configuration register.

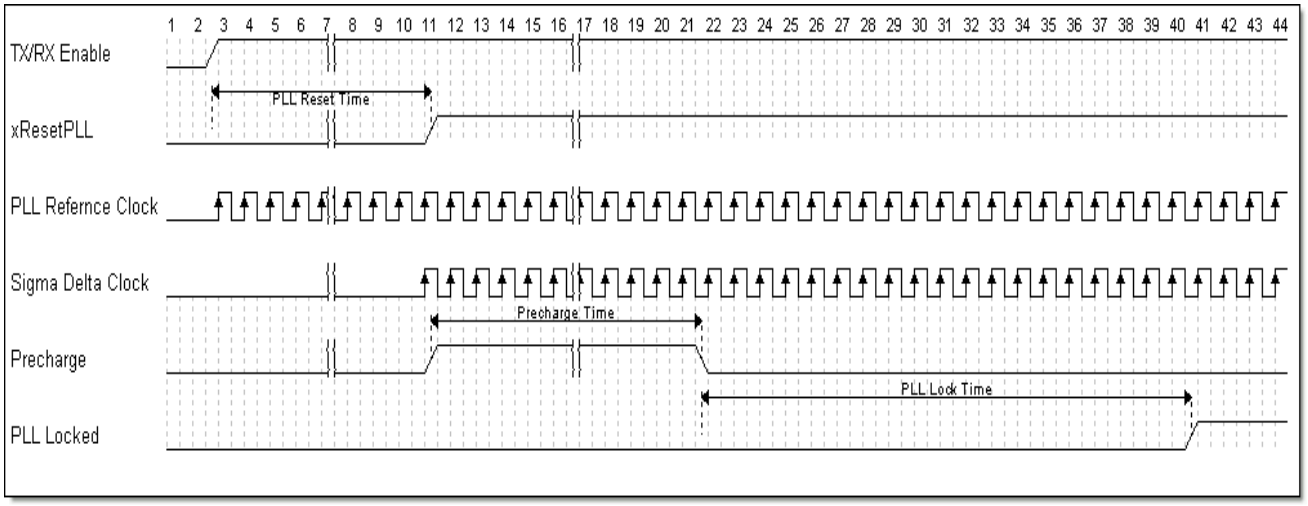


Figure 8. PLL Lock Detect

Transmitter

RF Output

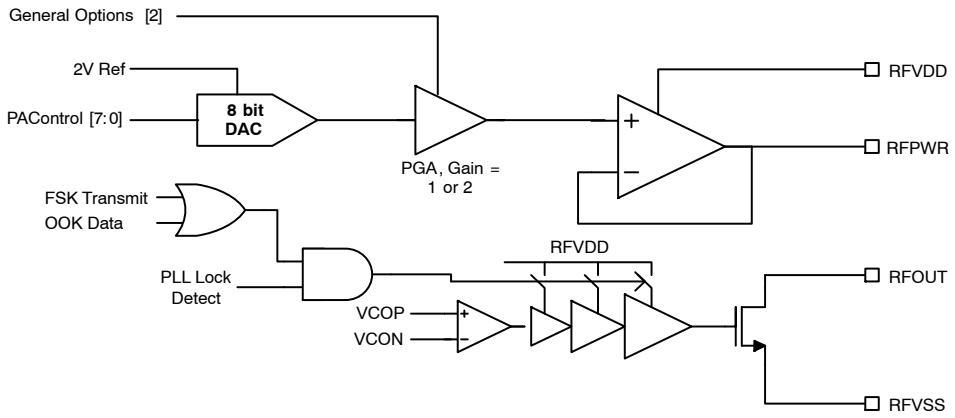


Figure 9. PA Control

The Power Amplifier (PA) of the NCV53480 is a single ended open drain amplifier, which has been designed to deliver up to 10 dBm into a 50 Ω load. The RFPWR pin is used to provide a voltage reference for the PA circuitry, and can be programmed to adjust the output power. The input to the buffer for the RFPWR pin can be either an 8−bit DAC referenced to 2.0 V or the DAC can be run through a 2x buffer allowing voltages up to 3 V on the RFPWR pin. The DAC mode provides a constant voltage over all temperature and voltage conditions, resulting in output power which varies just ±1 dB. The high gain mode, allows for maximum output power and efficiency (10 dBm). When using the 2x gain mode, the RFPWR pin will track V_{DD} if V_{DD} is less than the desired RFPWR voltage setting.

When the device is in receive mode, RFPWR is driven to ground, and the gate of the PA is grounded, facilitating a combined RX/TX match without the need for an external switch.

Asynchronous Transmit

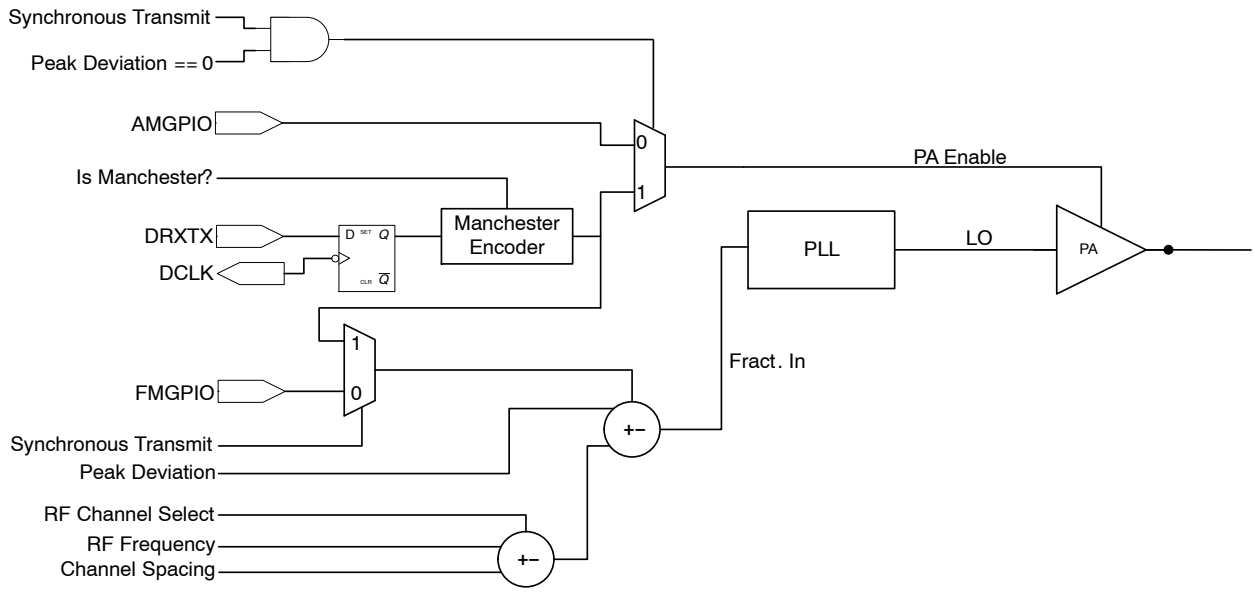


Figure 10. Transmit Control

In asynchronous transmit, the transmit portion of the state machine simply turns on the device with the PLL running, with the AMGPIO and FMGPIO pins configured as inputs. The AMGPIO pad controls the PA enable and the FMGPIO controls the frequency word into the PLL. For AM only transmit, the Peak Deviation register should be set to zero and the FMGPIO pin can be driven high, low or left floating (an internal pull−up is enabled). For FM only transmit, the AMGPIO pin should be driven high to enable the PA. For simultaneous transmit, the AMGPIO and FMGPIO can toggle independently of each other, but the PA will only be enabled when the AMGPIO is driven to a ‘1’. In asynchronous transmit the DCLK will be driven to a ‘1’, signifying when the PLL has gained lock.

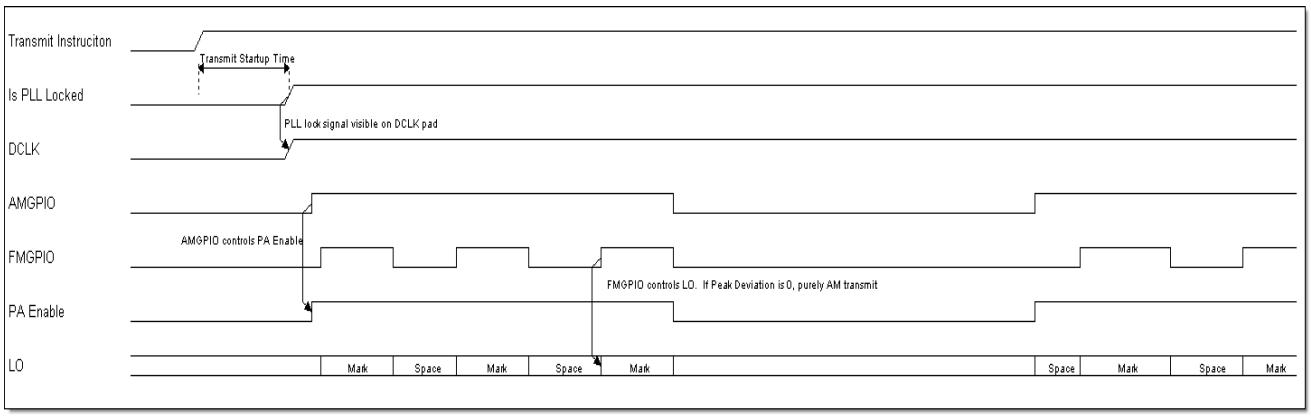


Figure 11. Asynchronous Transmit

Synchronous Transmit

In synchronous transmit the NCV53480 will provide a baud clock on the DCLK pin. The external micro−controller can use this pin to time the data rate, without the use of additional timers. In this mode of operation simultaneous OOK and FSK transmit is not supported. If the Peak Deviation register is zero then OOK modulation is assumed. If the Peak Deviation register is non−zero then FSK modulation is assumed. The below figures show synchronous OOK and synchronous FSK transmit. An internal state machine handles the necessary Manchester encoding, if Manchester is enabled via the Payload Encoding bit in the Transceiver Options register.

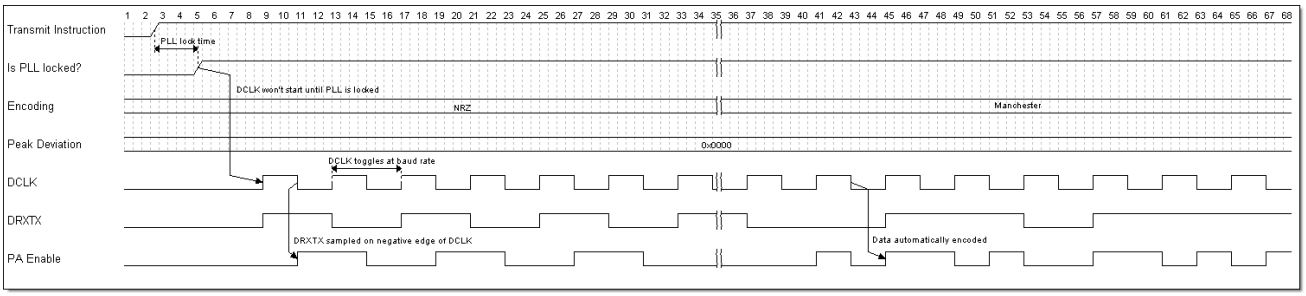


Figure 12. Synchronous OOK Transmit

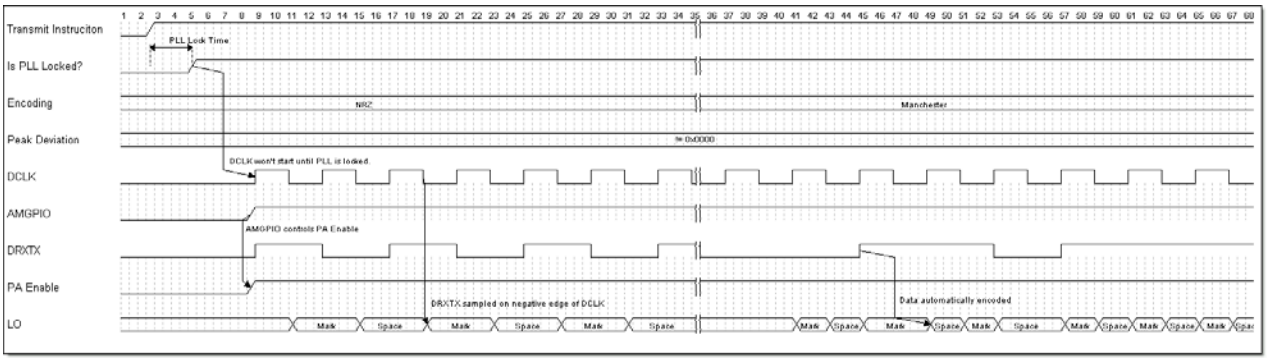


Figure 13. Synchronous FSK Transmit

Receiver

The NCV53480 is a fully monolithic image reject low−IF receiver. The low IF architecture saves considerable power, while the absence of the DC correction necessary for zero−IF reduces timing complexity and permits OOK modulation. The receiver provides outputs to an FSK detector, and an OOK detector.

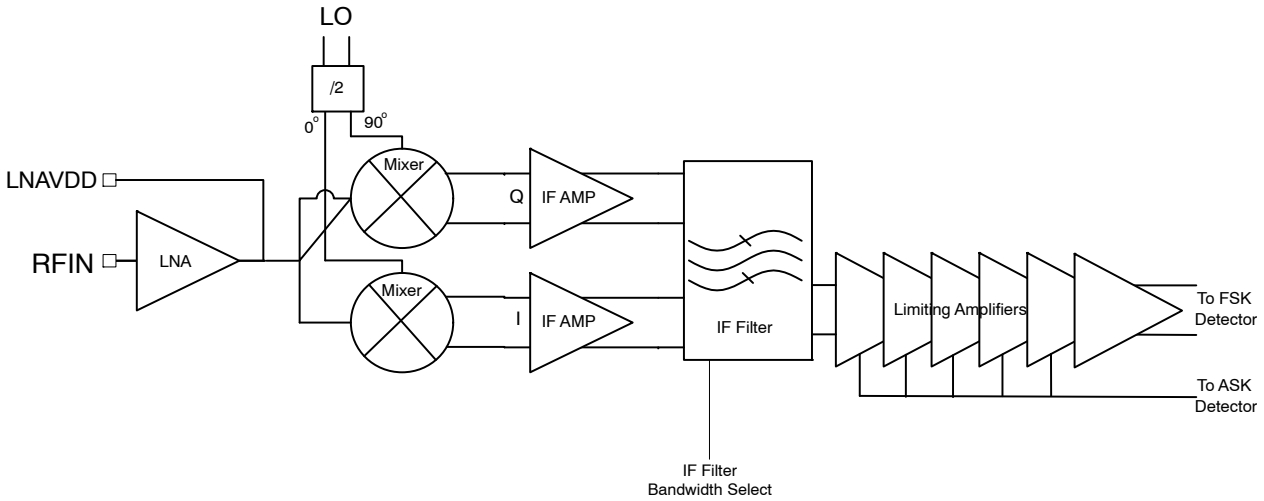


Figure 14. Receive Chain

The single ended LNA is followed by dual mixers, which perform a quadrature down conversion. The LNA is a common gate amplifier requiring a DC path to ground external to the device. The output of the LNA is connected to the pin LNAVDD. This pin should be connected to V_{DD} through an appropriately sized inductor for maximum sensitivity. See the RX/TX Matching Section for matching specifications. For reduced cost/performance, this pin can simply be connected to V_{DD} through a 1 kΩ resistor.

IF Filter

Following the first IF amplifiers, a complex (I,Q) bandpass filter provides both image reject, and channel selection. This filter has selectable bandwidths of 100 kHz, 200 kHz, and 300 kHz and is set by the IF Bandwidth bits of the Receive Options register. The filter roll−off is equivalent to a 5th order low−pass filter centered at the IF frequency of 500 kHz.

Limiting Amplifiers and RSSI

The limiting amplifiers which follow the IF channel selection filter also provide a log−linear current output which is summed onto a resistor to provide a RSSI voltage output. The analog RSSI output is available on the AMGPIO pin, and is fed to the OOK demodulator for data slicing. The digital level output of the limiting amplifiers is fed directly into the FSK detector.

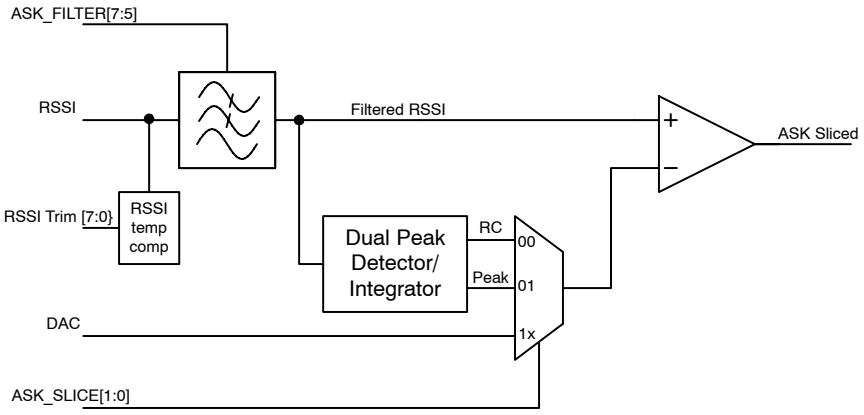


Figure 15. OOK Detector

OOK detection is done using full wave current output rectifiers in each stage of the log amp. These currents are summed onto an internal resistor to create the RSSI signal. The RSSI signal is then filtered and fed into the positive input of the data slice comparator. The reference input to the comparator can be either a DC level from the DAC, a RC integrated version of RSSI, or the midpoint of a dual peak detector. Both the filtered RSSI and the sliced data are available on the AMGPIO pin using the AMGPIO Configuration bits in the Receive Options register.

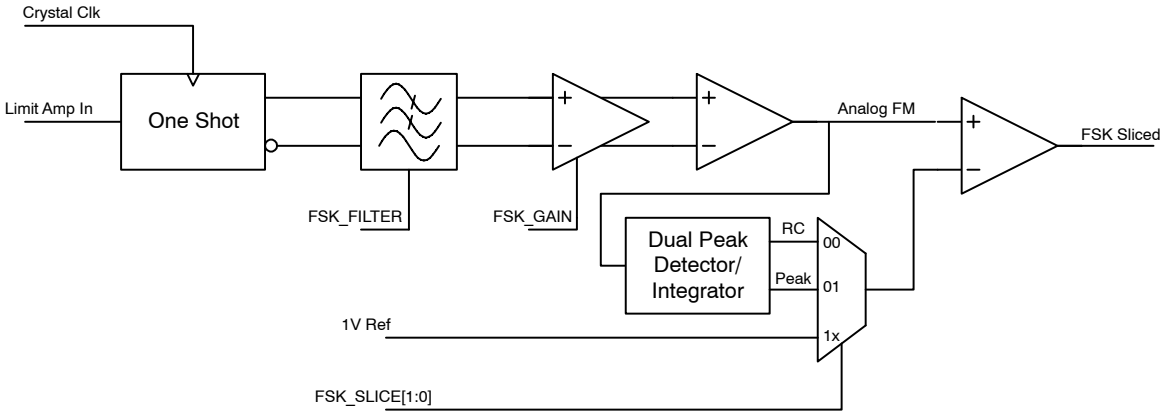


Figure 16. FSK Detector

For FSK detection, the IF signal is limited, and then fed to a one−shot detection block. The output of the one shot discriminator is then filtered by a 3rd order Chebyshev filter, and can then be amplified through the FSK gain block. Finally, data is recovered by comparing the output of the detector to one of three selectable references: 1 V reference (representing the RF frequency center), the mid point of a dual peak detector, or to an RC integrator. Both the discriminator output and the sliced data are available on the FMGPIO pin using the FMGPIO Configuration bits in the Receive Options register.

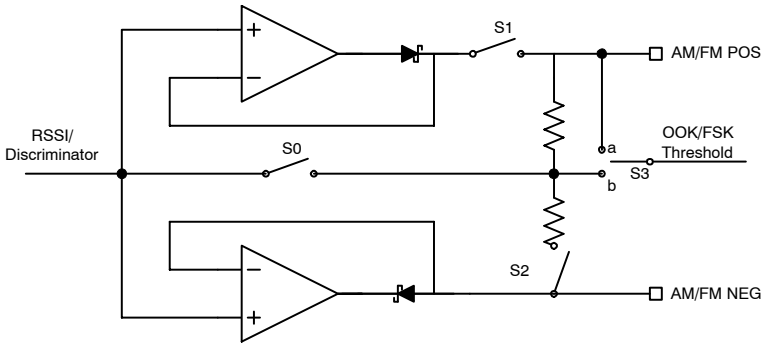


Figure 17. Dual Peak Detector/Integrator

The dual peak detector and integrator in both the OOK and FSK detection blocks are identical. The figure above illustrates the circuitry in this block. In the case where dual peak detection is used to set a threshold at the midpoint of the positive and negative peaks on the output of the detector, S1 and S2 are closed, and S3 is switched to position “b”. The simple resistive divider between the two peak detectors determines the threshold output. For this mode of operation, the capacitors should be sized at 2*TL/1M, where TL is the longest period of no data change, and 1M is the size of the internal resistors.

For RC integrator mode, switch S0 is closed, and S3 is switched to position “a”. The threshold is then simply a low pass version of the input signal. For optimal operation, the capacitor value for this configuration should be chosen to be 3*TL/1M, where TL is again the longest period of no data change.

FSK Squelch

Bit 2 of register 0x5E is used to enable the FSK Squelch function. This function will gate operation of the FSK detection circuitry until RSSI exceeds the threshold programmed in the energy threshold register (0x16, 0x36). A block diagram of this functionality is shown below. Note, the Energy Threshold register setting is common to both this function and the OOK detector when using the programmable DAC setting as a threshold for the OOK slick comparator.

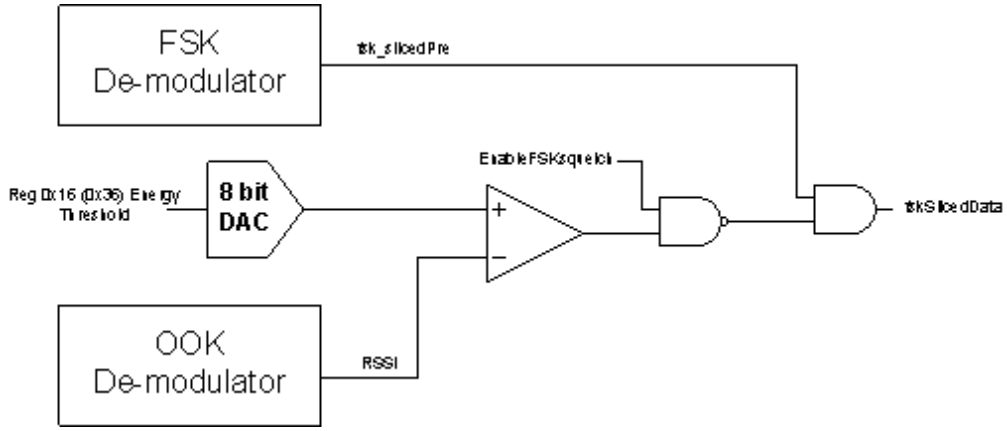


Figure 18.

Receiver Configuration

The NCV53480 receiver's level of autonomy can be configured from simple receiver providing continuous analog outputs to intelligent receiver buffering packets and issuing interrupts to an external controller.

From the top level, the receiver contains two available configurations, Configuration A and Configuration B. These configurations are completely independent from one another, for example, Configuration A can setup the receiver for OOK data detection at 1 kbps Manchester, and Configuration B can setup for FSK at 18 kbps. Further, Configuration A could setup the radio to search for a specific pre−amble, and once found qualify a Chip ID, buffer in 64 bits of data then interrupt an external controller, while Configuration B could simply put the radio in a state where the FM discriminator analog output is available to an external controller on the FMGPIO pin.

Further automation and power reduction of the NCV53480 is achieved by using Sniff−Mode. In Sniff−Mode 3 timers are available:

1. Control receive interval with the settings of Configuration A
2. Control receive interval with the settings of Configuration B
3. How often to do a clear channel assessment.

Additional timers in Sniff−Mode determine the length of time the receiver stays active in either Configuration A and Configuration B.

Note: The following sections apply to both Configuration A and Configuration B.

Receive Mode

The Receive Mode bits in the Transceiver Options register determine the way the receiver will operate. With these bits set to 00, the device will enter normal receive, the selected detectors will be enabled, and if enabled recovered clock and data will be available. All output will be continuous in this state until another command is issued.

Wake−On−Energy

Setting the Receive Mode bits to 01 enables Wake−On−Energy mode. With this mode enabled, the device can issue an interrupt to an external controller upon receiving a signal with RSSI energy greater than the value specified in the Energy Threshold register. When Wake−On−Energy is selected, the Receive Dwell Timer register determines how long the receiver will stay active looking for energy to surpass the energy threshold. When setting the Receive Dwell Timer to 0x00 the receiver will impulse sample for energy. Using this mode of operation with the Receive Dwell Timer set to impulse sample minimizes the receiver on time.

The clock and data recovery block, if enabled, is initially off in Wake−On−Energy mode. Once a threshold has been achieved, the CDR is then enabled. Additional functionality is available once the Wake−On−Energy mode has been selected. Upon finding energy greater than the threshold, the part can then begin searching for a specified Chip ID (CDR must be enabled). This pattern can be up to 32−bits long in Wake−On−Energy mode and is the concatenation of the Wake Pattern and Chip ID registers. The length of the pattern to search for is set in the Pattern and ID Length register. The Code Dwell Time register controls how long the device stays on looking for the pattern after energy has been found. If this timer expires the device returns to Sniff mode. If the pattern has been found, an interrupt can be issued to an external controller to handle the payload data on the DCLK and DRXTX pins. Alternatively the NCV53480 can automatically buffer in the next N bits, where N is set by the Packet Length register. If buffered packet is enabled (anything non−zero in Packet Length register), the interrupt to the external micro−controller will occur after buffering in the packet.

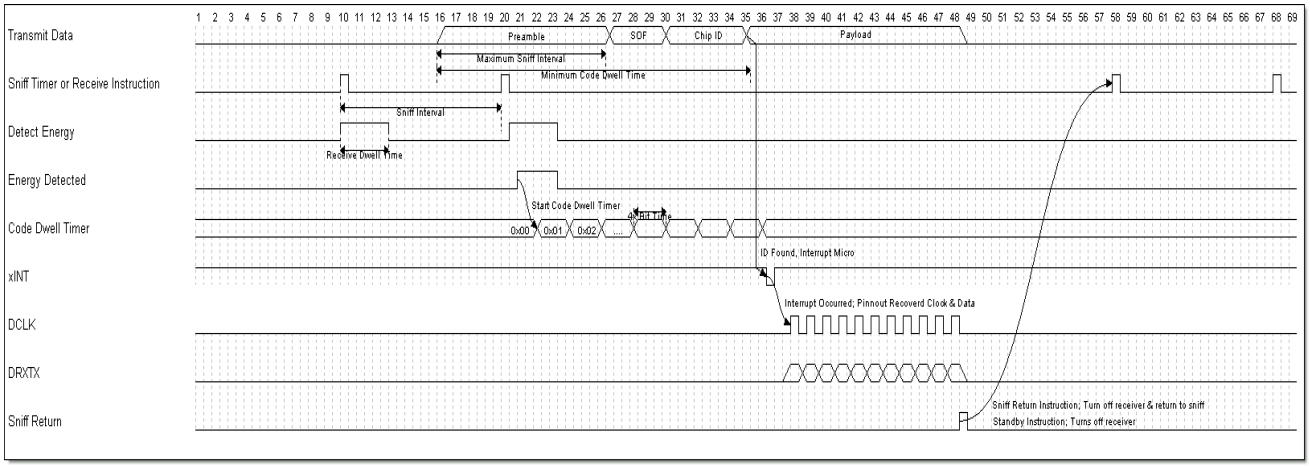


Figure 19. Wake−On−Energy

Wake−On−Pattern

In this mode of operation, enabled by setting Receive Mode bits to 10, the NCV53480 uses an over−sampling operation to find a sequence of bits matching the pattern in the Wake Pattern and Chip ID registers. The Pattern and ID Length register is used to set the length of pattern(s) the part will look for, and the Pattern and ID Threshold register is used to set how well each bit must match the expected. Setting this threshold low can result in false wake−ups, while setting it high will result in reduced sensitivity for Wake−On−Pattern functions. Section Pattern and ID Correlator explains, in detail how this correlation functionality operates.

It is possible to set up the part in this mode in two different ways. The first is to simply find a single sequence with a length from 1 to 16 bits. The second is to find a sequence matching the value in Wake Pattern register, and then after some time find a sequence matching the Chip ID register. The later mode of operation is useful for first finding a repeating pre−amble, and then qualifying a Chip ID before either buffering in the packet or interrupting an external controller.

There are two timers used in Wake−On−Pattern Mode. The first is the Receive Dwell Timer which functions similar to the way it does in Wake−On−Energy mode. It determines how long the receiver should stay active searching for the Wake Pattern. The second timer, Code Dwell Timer, starts once the wake pattern has been found, and determines how long the receiver will stay active looking for the chip id. If the wake pattern is a long repeating preamble such as 1001001001. and the part is configured to look for 1001, each time the device finds the wake pattern, the code dwell timer is reset. In this way, it is possible for the receiver to stay active during long pre−ambles waiting for the chip id to arrive. If both timers time out before finding its target, the part will return to Standby mode.

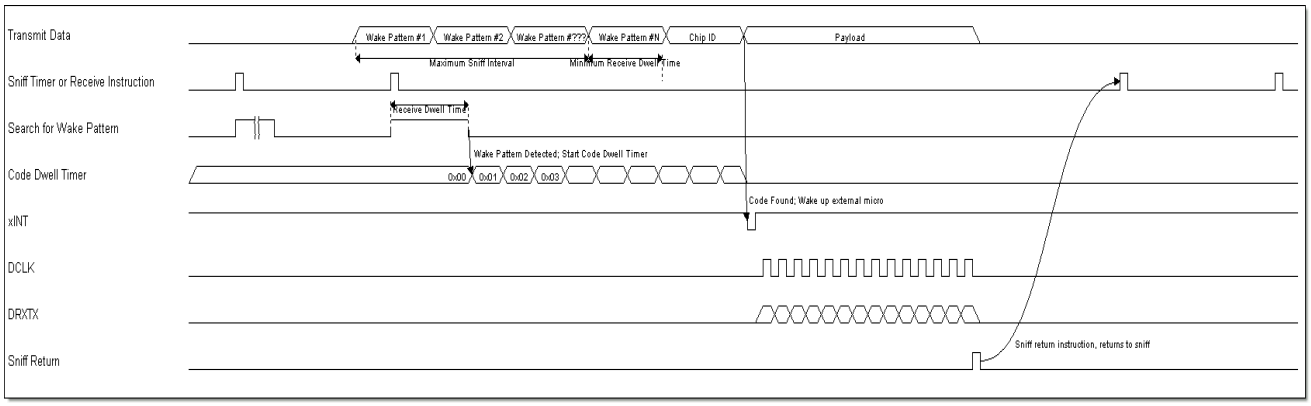


Figure 20. Wake−On−Pattern

Sniff−Mode

In the preceding sections describing Wake−On−Energy and Wake−On−Pattern, it was noted that the receiver simply returns to a low power state should the receiver not find the desired signal before the associated timers expired. Sniff−Mode configures the receiver to automatically return to receive mode at a specified interval, greatly reducing the burden on the external controller, and also reducing overall power consumption.

So as an example: Configuration A is configured to stay on for 10 ms (Receive Dwell) searching for a 5 bit Wake Pattern. By writing the Command register to the Receive Instruction, the part will enable the receiver and look for the wake pattern. If after 10 ms the wake pattern has not been found, the part will simply return to Standby and the controller will need to issue the next command. If however the Configuration A: Sniff Configuration register has been set to 0x03, and the Command register is written to the Sniff−Mode Instruction, the part will similarly enter receive and look for the wake pattern, the difference being that if after 10 ms the wake pattern has not been found, the part will automatically re−enable the receiver at an interval determined by the Configuration A Sniff Interval without intervention from the external controller.

Upon finding either, or both depending on configuration, the wake pattern and chip id the device will issue an interrupt to the external controller. Alternatively the NCV53480 can be configured to buffer in the next N bits as determined by the Packet Length register before issuing an interrupt.

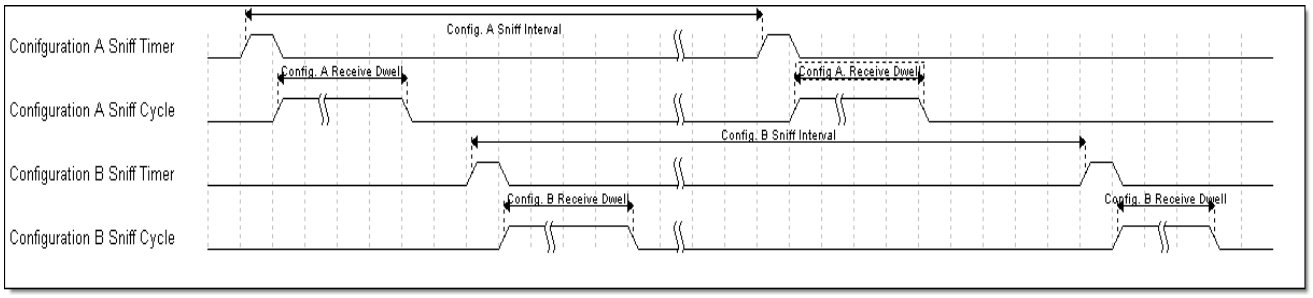


Figure 21. Sniff Cycles

The figure above shows an indicative timing diagram for Sniff−Mode with both Configuration A and Configuration B enabled. Note that Configuration A and Configuration B Sniff Intervals and Receive Dwell values are independent. Note in the timing diagram only the intervals and receive dwell timer are shown, not the chip id dwell, nor the payload receive portions.

Dual Configurations in Sniff−Mode

Using Sniff−Mode, it is possible to have the receiver autonomously enter receive using both the Configuration A and Configuration B device configurations. The NCV53480 has independent Sniff−Mode Configuration registers for Configuration A and Configuration B allowing the two to operate independently from one another. So the radio can be setup to enter receive mode every 20 ms using Configuration A, and also enter receive every 10 seconds using Configuration B.

When a collision occurs between the Configuration A and Configuration B Sniff−Mode timers, Configuration A always has precedence, and the Configuration B timer will be queued until after Configuration A completes its cycle.

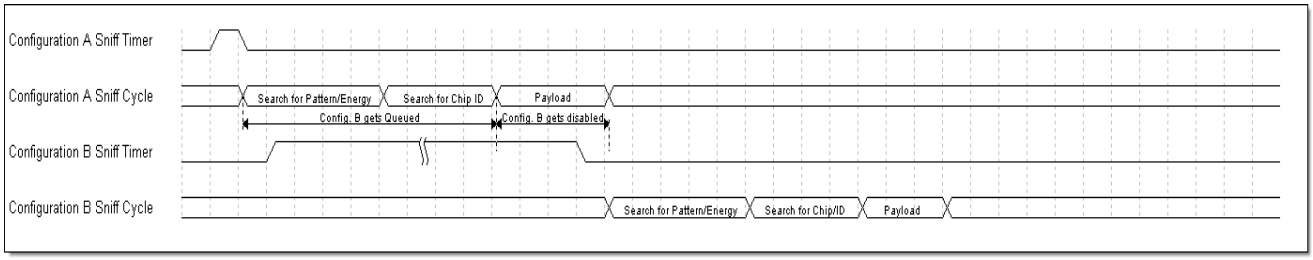


Figure 22. Configuration B Queued

The figure above shows that if the Configuration B Sniff timer overflows while Configuration A is active searching for either energy in Wake−On−Energy mode, or searching for the wake pattern in Wake−On−Pattern mode, then Configuration B will be queued until Configuration A has completed. If Configuration A receives a valid payload during this time, then Configuration B will be disabled such that the receive buffer is not corrupted by the Configuration B Sniff Cycle.

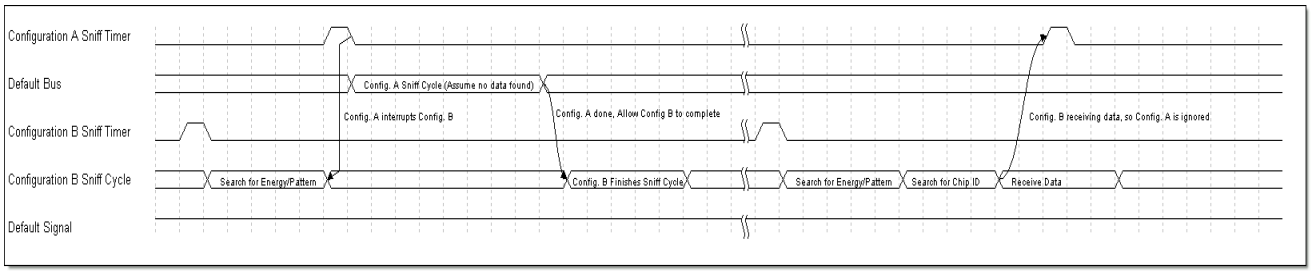


Figure 23. Configuration B Interrupted

If the Configuration A Sniff timer overflows while Configuration B is active searching for either energy in Wake−On−Energy Mode or searching for the wake pattern in Wake−On−Pattern mode, then Configuration A will interrupt the Configuration B Sniff cycle. If Configuration A completes its Sniff cycle without receiving a payload then Configuration B will re−start once Configuration A is complete.

If the Configuration A Sniff timer overflows while Configuration B is actively receiving data, such that Configuration B detected energy in Wake−On−Energy mode or the wake pattern in Wake−On−Pattern mode, then Configuration A will be disabled such that the receive buffer will not be corrupted by the Configuration A Sniff Cycle.

Multi−Channel Operation and Best Channel Selection

The NCV53480 also contains the ability to use multiple channels in both regular receive, and in Sniff−Mode. The channels are defined as ± Channel Spacing from the programmed RF Frequency. For a regular receive instruction, the desired channel is selected by the RF Channel Select bits of the Command register. For Sniff−Mode, the desired channel can be selected in one of two ways:

- Explicitly by enabling just a single Channel Enable bit in the Sniff−Mode Configuration register.
- On the fly by having the radio scan up to three channels and selecting the channel with the lowest noise floor.

When more than one channel is enabled in the Sniff−Mode Configuration register, the radio enables the ADC Poll Timer to automatically scan the enabled channels and select the one which has the lowest noise floor. The channel with the lowest noise floor is then used for all Sniff−Mode cycles until the next event on the ADC Poll Timer. This is not to say that Configuration A and Configuration B cannot operate on separate channels.

Example #1: If channels 1, 2, and 3 are enabled for Configuration A, and only channel 2 on Configuration B, when the Configuration A Sniff−Mode timer expires, it will go into receive mode on the channel with the lowest noise floor determined by the previous noise floor detection cycle. When the Configuration B Sniff−Mode timer expires, Configuration B will always operate on channel 2.

Example #2: Channels 1 and 2 enabled for Configuration A and channels 2, and 3 enabled for Configuration B. After the noise floor detection is completed, it is determined that channel 1 has the lowest floor, followed by 2, and finally 3. In this case Configuration A will operate on channel 1, and Configuration B will operate on channel 2.

Clock and Data Recovery

The Clock and Data Recover (CDR) is implemented using an All Digital Phase Lock Loop (ADPLL). The CDR uses an ADPLL to process the output from the FSK or ASK demodulator circuits to recover a clock signal, and provide a low jitter data output. This module is used for pattern detection and payload recovery. The CDR can recover data from 1 kbps to 60 kbps. In addition to the classical PLL for clock recovery, a fast phase alignment (FPA) feature allows the part to quickly acquire a coarse phase lock with the incoming data. This feature makes it possible to accurately acquire on as few as 4−bits.

To enable the receiver to quickly acquire lock on an incoming data stream, a fast phase alignment feature is implemented which will aid in acquisition by making a coarse phase adjustment to the PLL loop when a programmed sequence is initially detected from a sleep state. This sequence is set by the Start Detect Pattern register. While in an off state, only a minimum of the digital circuitry is enabled to look for the Start Detect Pattern to conserve power. This FPA functionality is only used in Wake−On−Energy mode.

In Wake−On−Pattern mode a separate correlator is used in which is clocked at 8x the set Data Rate. Once the incoming data reaches the threshold for the correlator, the full circuitry for the CDR operation is enabled, and the output phase is adjusted to be within 45 degrees based on the correlation. The start signal goes high, and can be used to gate the recovered clock signal.

Pattern and ID Correlator

The pattern correlator block uses the inputs from the Wake Pattern registers or the Chip Id registers to look for a specific sequence. Each bit set in the pattern/ID register is compared against the over sampled output of the selected demodulator. The output of the demodulator is sampled at 8x the data rate specified in the Data Rate registers.

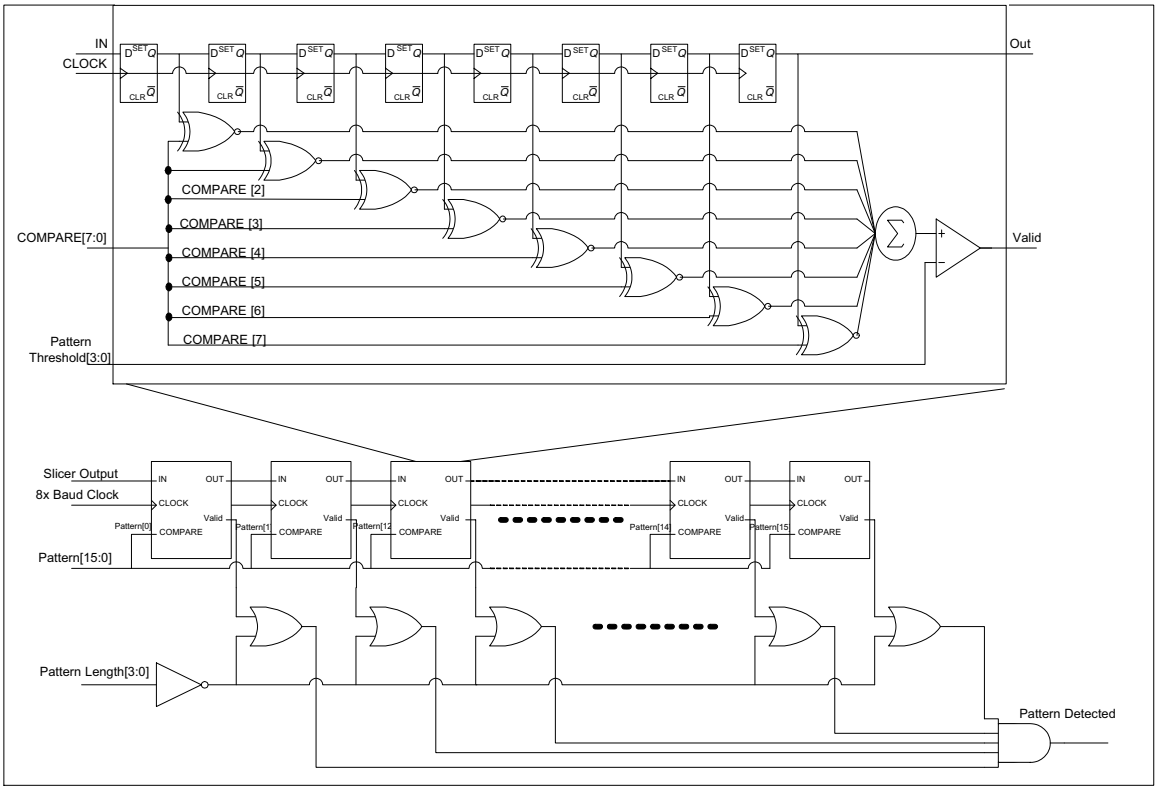


Figure 24. Pattern Correlator

The schematic above illustrates the basic blocks of the correlator. Each bit for comparison utilizes an 8−bit shift register feeding a bank of xnor gates, the other inputs of which come from either the Wake Pattern or Chip Id registers.

The COMPARE word for comparison is determined by the line code format chosen. The wake pattern encoding is specified by the Wake Pattern Encoding bits in the Pattern and ID threshold register. The chip id encoding is specified by the Payload Encoding bit in the Transceiver Options register. The following table shows what COMPARE[7:0] will be for the different line codes.

COMPARE [7:0]

RZ 1	1	1	1	1	0	0	0	0
RZ 0	0	0	0	0	0	0	0	0
Manchester 1	1	1	1	1	0	0	0	0
Manchester 0	0	0	0	0	1	1	1	1
NRZ 1	1	1	1	1	1	1	1	1
NRZ 0	0	0	0	0	0	0	0	0

Data In	1	1	0	1	0	0	0	1
Manchester 1	1	1	1	1	0	0	0	0
XNOR	1	1	0	1	1	1	1	0
SUM								6

Data is a Valid '1' if the Threshold is 6 or less

Figure 25. Correlator Encoding

The outputs of the xnor gates are then summed and compared to the threshold set in the Pattern and ID threshold register. An example is given in the table above: The input data from the demodulator is shown in the top row, the COMPARE value for the example is a Manchester ‘1’. The XNOR row shows the outputs of the xnor gates, the sum of which is 6, so for thresholds of 6 or less, the correlator will treat this input data as a valid ‘1’. For threshold of 7 the correlator will treat this as not correlated.

The final operation of the correlator is to AND all of the bit ‘valid’ signals. The number of bits to use in the correlator for either the wake pattern or the chip id is determined in the Pattern and ID length register.

Once a pattern has been detected, the block continues correlation of the wake pattern word, but then also begins looking for the chip id word. If correlation with the pre−amble is lost, and a chip id has not been found, the device returns to low power mode. An interrupt can be programmed to wake an external micro−processor after either the chip id word has been found or the ASIC has buffered in the packet.

In normal receive mode, the correlator will run continuously when enabled. In Sniff−Mode mode, however, because it is desirable for power consumption to have as short an on time as possible, and because the radio can and will wake up in the middle of a pre−amble out of phase with the programmed value, the contents of the incoming data shift register are circulated around the shift register to check for correlation prior to returning to sleep. This can be shown by the following:

Wake Pattern programmed to: 10000110

Incoming data at end of Sniff−Mode: 00110100

At the end of the Sniff−Mode cycle, the incoming data will be rotated through for comparison:

00110100 → 00011010 → 00001101→ 10000110. Which results in correlation with the desired wake pattern, and the radio will remain on searching for the chip id.

Device Reset and POR

The NCV53480 contains a POR and brownout POR function. After power is applied to the device and the supply exceeds the brownout threshold of 1.4 V, the internal reset for the chip will release < 80 ms later. During this time, the xReset pad will be held low. At any time during operation, if the supply dips below the 1.4 V threshold for the brownout POR, the part will be reset, and xReset will be pulled low. A small counter using the RC oscillator as its source guarantee the pulse width for the reset will nominally be between 100 μs and 200 μs.

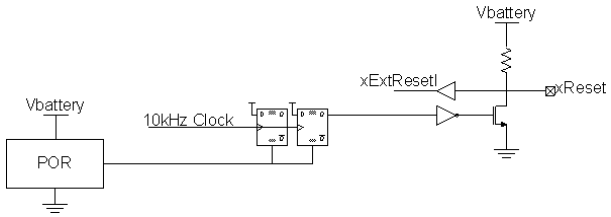


Figure 26.

In addition to the POR and brownout detectors, there are two methods to reset the NCV53480:

- xReset: Pulling the xReset pin low will reset the device with the exception of the digital control for the crystal oscillator and QSO control logic. This is to prevent the need to wait for the 10 ms crystal oscillator start−up timer after a reset.
- I^2C Serial Command: Issuing a serial reset command will reset the chip, inclusive of the oscillator logic, but does not reset the I^2C interface itself. If for some reason the serial interface were to become hung, such as by an external controller terminating a read mid−way through, the I^2C interface can be reset using the xReset.

I^2C Interface

The I^2C interface for the NCV53480 is compatible with standard and fast modes of operation. A control byte is the first byte received following the start condition from the master device. The control byte consists of a 7−bit device address and 1−bit command for read or write. For the NCV53480, the device address is '0110100' binary. The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. Following the start condition, the NCV53480 monitors the SDATA line checking the device type identifier being transmitted. Upon receiving its device address, the NCV53480 outputs an acknowledge signal on the SDATA line. Depending on the state of the R/W bit, the NCV53480 will select a read or write operation.

Single Register Write

Following the start condition from the master and the device address, the R/W bit, which is logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a register address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the register address to be written to. After receiving another acknowledge signal from the NCV53480, the master device will transmit the data word to be written, and the NCV53480 will acknowledge again. The write cycle ends with the master generating a stop condition. Figure 27 shows a pseudo−timing diagram for a single register write.

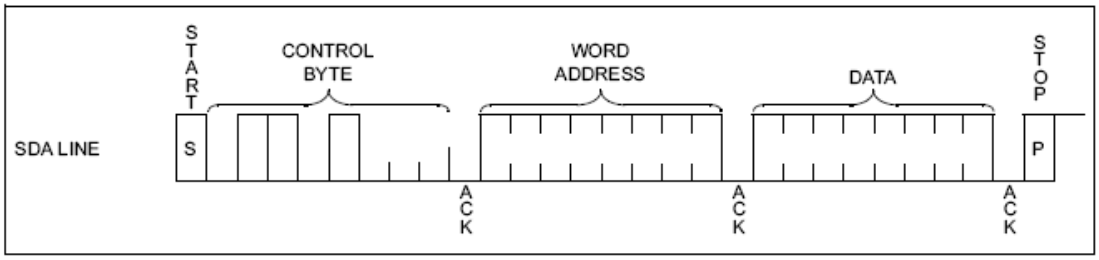


Figure 27. I^2C Single Register Write

Sequential Register Write

The write control byte, register address and first data byte are transmitted to the NCV53480 in the same way as in a byte write. However, instead of generating a stop condition, the master can continue to write register locations. Upon receipt of each word, the address is internally incremented by 1. If the master should transmit more words than the NCV53480 has address locations, the address will roll over. Figure 28 shows a pseudo−timing diagram for a sequential register write.

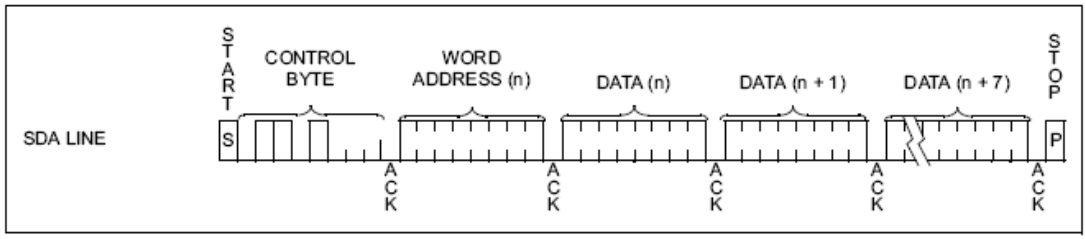


Figure 28. Sequential Register Write

Single Register Read

The single read operation allows the master to access the contents of any register in the device. The process to do so combine a portion of a single register write with a current address read. The sequence of operations is to send a start followed by device address and the R/W set to ‘0’ as in a write sequence. The address to read from is sent following an acknowledge from the slave. After the slave acknowledges the register address, the internal address counter is set to N, and to read the contents of the register, the same procedure for current address read is followed. Figure 29 shows a pseudo−timing diagram for a single register read.

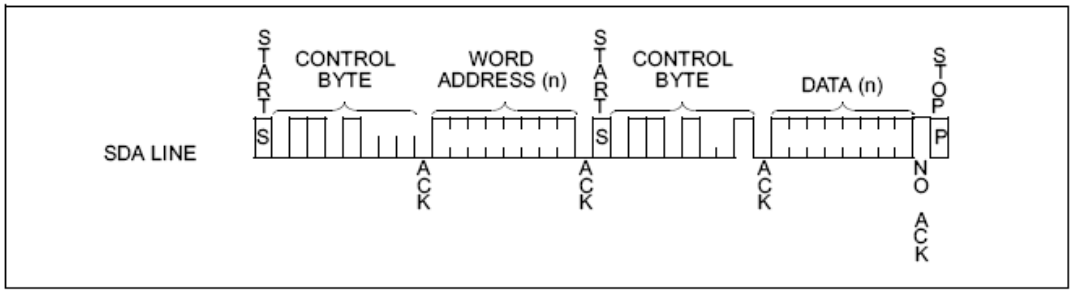


Figure 29. Single Register Read

Sequential Read

Sequential reads are performed in the same was as a random read, except that after the slave has transmitted the first data byte, the master issues an acknowledge, and not a stop bit. The acknowledge instructs the slave to transmit the contents of register N+1. After the master has received the contents of register N+X, the last register to be read, the master does not issue an acknowledge, and generates the stop bit. Figure 30 shows a pseudo−timing diagram for a sequential register read.

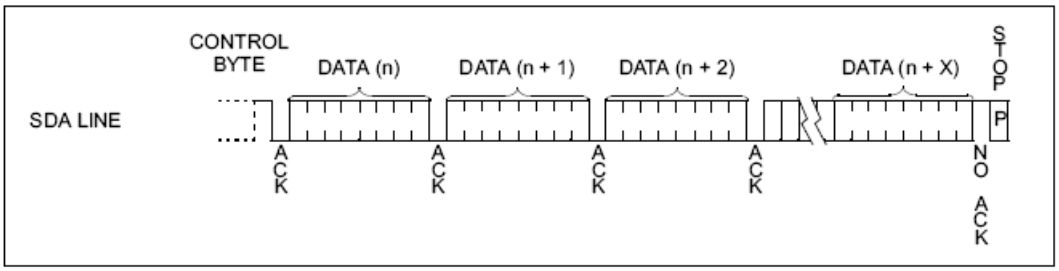


Figure 30. Sequential Register Read

Table 14. SERIAL INTERFACE REGISTERS

Read vs. Write	Register Addr.	Register Name	Description	POR Value	EE Addr.
GENERAL CONFIGURATION REGISTERS					
R/W	0x00	Command Register	Instruction Register	0x00	N/A
R	0x01	Status Register A	Status Register A	0x01	N/A
R	0x02	Status Register B	Status Register B	0x00	N/A
R	0x03	Status Register C	Status Register C	0x00	N/A
R/W	0x04	RF Divide	Integer portion of the RF frequency	0x00	N/A
R/W	0x05	RF Frequency <2>	Upper 8 bits of the RF frequency word	0x00	N/A
R/W	0x06	RF Frequency <1>	Middle byte of the RF frequency word	0x00	N/A
R/W	0x07	RF Frequency <0>	Lower byte of the RF frequency word	0x00	N/A
R/W	0x08	Peak Deviation <1>	Upper byte of the FM peak deviation	0x00	N/A
R/W	0x09	Peak Deviation <0>	Lower byte of the FM peak deviation	0x00	N/A
R/W	0x0A	Channel Space <1>	Upper byte of the Channel Spacing	0x00	N/A
R/W	0x0B	Channel Space <0>	Lower byte of the Channel Spacing	0x00	N/A
R/W	0x0C	General Options	General part configuration	0x02	N/A
R/W	0x0D	GPO Configuration	General Purpose Output Configuration	0x00	N/A
R/W	0x0E	ADC Poll Timer	ADC Poll Timer value	0x00	N/A
CONFIGURATION A REGISTERS					
R/W	0x10	Config.A: Sniff−Mode Options	Sniff Options	0x00	N/A
R/W	0x11	Config.A: Receive Options	General receive options	0x00	N/A
R/W	0x12	Config.A: Transceiver Options	General receive options	0x70	N/A
R/W	0x13	Config A: CDR Options	Clock and data recovery options	0x00	N/A
R/W	0x14	Config.A: Sniff Interval	Set the time for the interval of the sniff function	0x00	N/A
R/W	0x15	Config.A: Receive Dwell	Length of receiver dwell in Sniff−Mode	0x00	N/A
R/W	0x16	Config.A: Energy Threshold	RSSI threshold for wake on Energy	0x00	N/A
R/W	0x17	Config.A: Wake Pattern <1>	Upper byte of the wake pattern	0x00	N/A
R/W	0x18	Config.A: Wake Pattern <0>	Lower byte of the wake pattern	0x00	N/A
R/W	0x19	Config.A: Chip ID <1>	Upper byte of the wake code	0x00	N/A
R/W	0x1A	Config.A: Chip ID <0>	Lower byte of the wake code	0x00	N/A
R/W	0x1B	Config.A: Pattern and ID Threshold	Threshold of pattern and ID correlation	0x00	N/A
R/W	0x1C	Config.A: Pattern and ID Length	Length of wake pattern and chip id.	0x00	N/A
R/W	0x1D	Config.A: Code Dwell Timer	Code dwell time out value.	0x00	N/A
R/W	0x1E	Config.A: Packet Length	Packet length register	0x00	N/A
R/W	0x1F	Config.A: Data Rate<1>	Upper byte of the data rate register	0x00	N/A
R/W	0x20	Config.A: Data Rate<0>	Lower byte of the data rate register	0x00	N/A
R/W	0x21	Config.A: CDR Coefficients	CDR loop filter coefficients.	0x00	N/A
R/W	0x22	Config.A: Start Detect Threshold	Sets the CDR oversampled correlator threshold	0x00	N/A
R/W	0x23	Config.A: Start Detect Pattern	Sets the pattern for the CDR correlator	0x00	N/A
R/W	0x24	Config.A: ASK Detector Config	ASK data filter bandwidth and slicing options	0x00	N/A
R/W	0x25	Config.A: FSK Detector Config	FSK data filter bandwidth and slicing options	0x00	N/A

Table 14. SERIAL INTERFACE REGISTERS

Read vs. Write	Register Addr.	Register Name	Description	POR Value	EE Addr.
CONFIGURATION B REGISTERS					
R/W	0x30	Config.B: Sniff−Mode Options	Sniff Options	0x00	N/A
R/W	0x31	Config.B: Receive Options	General receive options	0x00	N/A
R/W	0x32	Config.B: Transceiver Options	General receive options	0x70	N/A
R/W	0x33	Config.B: CDR Options	Clock and data recovery options	0x00	N/A
R/W	0x34	Config.B: Sniff Interval	Set the time for the interval of the sniff function	0x00	N/A
R/W	0x35	Config.B: Receive Dwell	Length of receiver dwell in Sniff−Mode	0x00	N/A
R/W	0x36	Config.B: Energy Threshold	RSSI threshold for wake on Energy	0x00	N/A
R/W	0x37	Config.B: Wake Pattern <1>	Upper byte of the wake pattern	0x00	N/A
R/W	0x38	Config.B: Wake Pattern <0>	Lower byte of the wake pattern	0x00	N/A
R/W	0x39	Config.B: Chip ID <1>	Upper byte of the wake code	0x00	N/A
R/W	0x3A	Config.B: Chip ID <0>	Lower byte of the wake code	0x00	N/A
R/W	0x3B	Config.B: Pattern and ID Threshold	Threshold of pattern and ID correlation	0x00	N/A
R/W	0x3C	Config.B: Pattern and ID Length	Length of wake pattern and chip id.	0x00	N/A
R/W	0x3D	Config.B: Code Dwell Timer	Code dwell time out value.	0x00	N/A
R/W	0x3E	Config.B: Packet Length	Packet length register	0x00	N/A
R/W	0x3F	Config.B: Data Rate<1>	Upper byte of the data rate register	0x00	N/A
R/W	0x40	Config.B: Data Rate<0>	Lower byte of the data rate register	0x00	N/A
R/W	0x41	Config.B: CDR Coefficients	CDR loop filter coefficients.	0x00	N/A
R/W	0x42	Config.B: Start Detect Threshold	Sets the CDR oversampled correlator threshold	0x00	N/A
R/W	0x43	Config.B: Start Detect Pattern	Sets the pattern for the CDR correlator	0x00	N/A
R/W	0x44	Config.B: ASK Detector Config	ASK data filter bandwidth and slicing options	0x00	N/A
R/W	0x45	Config.B: FSK Detector Config	FSK data filter bandwidth and slicing options	0x00	N/A
EEPROM REGISTERS					
R/W	0x50	PA Control	Output power setting and mode selection	0xE0	0x00
R/W	0x51	Crystal Trim	Internal trim cap setting for crystal oscillator	0x40	0x01
R/W	0x52	Quick Start Trim	Quick start oscillator trim setting	0x80	0x02
R/W	0x53	10k Oscillator Trim	Trim register for the 10KHz IC oscillator	0x80	0x03
R/W	0x54	Analog Trim	Bandgap voltage and reference current trim	0x88	0x04
R/W	0x55	Filter Trim	Filter reference current and voltage trim	0x88	0x05
R/W	0x56	Receiver Trim	Image reject and IF amplifier trim	0x88	0x06
R/W	0x57	RF PLL Trim	Gain/Bandwidth correction trim	0x88	0x07
R/W	0x58	Antenna Trim	Antenna trim register	0x88	0x08
R/W	0x59	RSSI Trim	Temperature correction and resistor trim	0x80	0x09
R/W	0x5A	FSK Offset Trim	FSK detector input offset and BW trim	0x88	0x0A
R/W	0x5B	XTAL Current Trim	XTAL current and kicker slope adjust trims	0xFA	0x0B
R/W	0x5C	LNA and Temp Trim	LNA and temperature sensor trim.	0x88	0x0C
R/W	0x5D	IPtat Trim	IPtat trim	0x80	0x0D
R/W	0x5E	Miscellaneous	User available location	0x00	0x0E
R	0x5F	Check Sum	EEPROM checksum value		0x0F

Table 14. SERIAL INTERFACE REGISTERS

Read vs. Write	Register Addr.	Register Name	Description	POR Value	EE Addr.
EEPROM REGISTERS					
R/W	0x60	EE Unlock	This register must be written to 0x95 to write EE	0x6A	N/A
ADC REGISTERS					
R	0x6A	Temperature ADC	Temperature ADC result		N/A
R	0x6B	Channel 1ADC	Channel 1 RSSI ADC result		N/A
R	0x6C	Channel 2 ADC	Channel 2 RSSI ADC result		N/A
R	0x6D	Channel 3 ADC	Channel 3 RSSI ADC result		N/A
PACKET DATA REGISTERS					
R	0x70	Packet Data<15>	Most significant byte of packet data	0x00	N/A
R	0x7X	Packet Data <14:1>	Packet data bytes 14 through 1.	0x00	N/A
R	0x7F	Packet Data<0>	Least significant byte of packet data.	0x00	N/A
ANALOG TEST MODE REGISTERS					
R/W	0x80	Analog Test Mux		0x00	N/A
R/W	0x81	RF Test Mux		0x00	N/A
R/W	0x82	PLL Test Mode		0x00	N/A
R/W	0x83	Analog Test Mode		0x00	N/A
R/W	0x84	Empty		0x00	N/A
DIGITAL TEST MODE REGISTERS					
R/W	0x90	Digital Test Mode A		0x00	N/A
R/W	0x91	Digital Test Mode B		0x00	N/A
R/W	0x92	Digital Test Mux A		0x00	N/A
R/W	0x93	Digital Test Mux B		0x00	N/A
R/W	0x94	Digital Test Mux C		0x00	N/A
REVISION CONTROL REGISTER					
R	0xA0	ON Rev Code	ON Revision code	0x55	N/A

Table 15. REGISTER TABLE

Command Register

The command register is used to control the state of the part as the name implies. The lower 4 bits control what functional state the part is in. Bits 7 and 6 when used with a receive or transmit command control on which of the three channels the specified action should occur, i.e. writing register 0x00h to the value 0x81 puts the part into receive mode on the RF Channel Spacing above the center frequency programmed into the part.

COMMAND REGISTER: LOCATION 0x00

Bit	Bit Name	State	Comment
7:6	Receive & Transmit RF Channel Select	11	Use Frequency specified
		10	High Side Channel, RF frequency + Channel Spacing Value (Channel 3)
		01	Low Side Channel, RF frequency − Channel Spacing Value (Channel 1)
		00	Default, (Channel 2)
5:4			
3:0	Command Bits	0000	Standby− Put the part into standby mode
		0001	Receive Configuration A − Put part into receive mode using Config. A.
		0010	Receive Configuration B − Put part into receive mode using Config. B.
		0011	
		0100	Sniff−Mode − Put the part into Sniff−Mode
		0101	Transmit Configuration A: Put part into transmit mode using Config. A.
		0110	Transmit Configuration B: Put part into transmit mode using Config. B.
		0111	
		1000	ADC Conversion
		1001	
		1010	Write EE −Write current register values to EE
		1011	Read EE − Refresh register values from EE
		1100	Quick−Start Cal − Perform a calibration of the quick start oscillator
		1101	RC Cal − Perform a calibration of the 10 kHz oscillator
		1110	Reserved.
		1111	Full Reset − Reset the part

Status Register A

This register is used to provide an external micro−processor with information regarding the current state of the part as well as to provide status on calibration status.

STATUS REGISTER A: LOCATION 0x01

Bit	Bit Name	State	Comment
I	PLL Status	1	PLL is Locked
		0	PLL is NOT locked
6	PLL Lock Failed	1	PLL Failed to Lock
		0	PLL did Lock
5	RC/QS calibration fail	1	Indicates that either the RC or QS oscillator failed to calibrate
		0	
4	EEPROM Checksum Failed	1	Indicates the EEPROM data is corrupt
		0	
3			
2			
1			
0	Busy	1	Device is busy, new commands will be ignored
		0	Ready for command

Status Register B

This register is used to provide an external micro−processor with information regarding the current state of the part.

STATUS REGISTER B: LOCATION 0x02

Bit	Bit Name	State	Comment
7:6	Interrupt Status	11 10 01 00	Quick Start Cycle Failed. Recalibrate the Quick Start oscillator. Receive data on Configuration A Receive data on Configuration B No interrupt
5			
4			
3:2	Clock Select	11	N/A
		10	Digital section is being clocked off of the 10kHz oscillator
		01	Digital section is being clocked off of the Quick Start oscillator
		00	Digital section is being clocked off of the crystal
1:0	Quick Start Status	11	The Quick Start cycle is complete and has failed. The user should recalibrate the Quick Start
		10	The Quick Start cycle is complete and has succeeded.
		01	The Quick Start cycle hasn't started.
		00	Quick Start has not been calibrated

Status Register C

This register is used to provide an external micro−processor with information regarding the channel noise floor information.

STATUS REGISTER C: LOCATION 0x03

Bit	Bit Name	State	Comment
7:6			
5			
4			
3:2	Configuration A current channel	11	N/A
		10	High Side Channel, RF frequency + Channel Spacing Value
		01	Low Side Channel, RF frequency − Channel Spacing Value
		00	Default, Use Frequency specified
1:0	Configuration B current channel	11	N/A
		10	High Side Channel, RF frequency + Channel Spacing Value
		01	Low Side Channel, RF frequency − Channel Spacing Value
		00	Default, Use Frequency specified

RF Divider

Setting the RF channel frequency is done through the RF Divider register, along with the RF Frequency 2, 1, and 0 registers. The RF Divider register is used to specify the integer portion of the divide value, and the RF Frequency 2, 1, and 0 registers are used to specify the fraction. The values are calculated as follows,

$$\text{DivideVal} = \frac{F_{Channel}}{F_{Crystal}\text{MHz}}$$

where $F_{Channel}$ is the desired RF center frequency. The value for the RF Divider register is found by,

$$\text{Integer} = \text{round}(\text{DivideVal})$$

where Integer is the value used for RF Divider. The last step is to calculate the fractional value. This is done as,

$$\text{Fraction} = (\text{DivideVal} - \text{Integer}) \cdot 262147$$

where Fraction is the value to be used in the RF Frequency 2, 1, and 0 registers. As an example, if the desired RF channel frequency is 308 MHz, and the crystal is 20 MHz

$$\text{DivideVal} := \frac{F_{RF}}{F_{Crystal}} = 15.4$$

$$\text{Integer} := \text{round}(\text{DivideVal}) = 15$$

$$\text{Fraction} := \text{round}\left[(\text{DivideVal} - \text{Integer}) \cdot 262147\right] = 104859$$

For this example, the RF Divider register is written to 0x0F, RF Frequency 2 is written to 0x01, RF Frequency 1 to 0x99, and RF Frequency 0 to 0x9B.

RF DIVIDER: LOCATION 0x04

Bit	Name	Comment
7:0	RF Divider	00h through 0Bh : not allowed 1Ah : divide by 26 1Bh : divide by 27 –––––––––– 4Ah : divide by 74 4Bh : divide by 75 4Ch through FFh : not allowed

RF Frequency <2>

RF FREQUENCY<2>: LOCATION 0x05

Bit	Name	Comment
7:0	RF Freq.[23:16]	Upper 8 Bits of the RF Fraction

RF Frequency <1>

RF FREQUENCY<1>: LOCATION 0x06

Bit	Name	Comment
7:0	RF Freq.[15:8]	Center 8 Bits of the RF Fraction

RF Frequency <0>

RF FREQUENCY<0>: LOCATION 0x07

Bit	Name	Comment
7:0	RF Freq.[7:0]	Lower 8 Bits of the RF Fraction

Peak Deviation <1>

The peak deviation for FSK transmit is determined by the Peak Deviation <1> and Peak Deviation <0> registers. Calculation of the value for the peak deviation is straight forward. The following example is for a peak deviation of 20 kHz, using a 20 MHz crystal.

$$\text{PeakDev} := \text{round}\left(\frac{\frac{\text{PeakDeviation}}{F_{\text{Crystal}}}}{262147}\right) = 262$$

The result of this operation is entered into the Peak Deviation registers.

PEAK DEVIATION<1>: LOCATION 0x08

Bit	Name	Comment
7:0	Peak Deviation [15:8]	Upper 8 bits of the peak deviation

Peak Deviation <0>

PEAK DEVIATION<0>: LOCATION 0x09

Bit	Name	Comment
7:0	Peak Deviation [7:0]	Lower 8 bits of the peak deviation

Channel Space <1>

The Channel Offset Spacing is determined by the Channel Spacing<1> and Channel Spacing<0> registers. Calculation of the value for the channel spacing is the same as the Peak Deviation register.

CHANNEL SPACING<1>: LOCATION 0x0A

Bit	Name	Comment
7:0	Channel Spacing[15:8]	Upper 8 bits of the peak deviation

Channel Space <0>

CHANNEL SPACING<0>: LOCATION 0x0B

Bit	Name	Comment
7:0	Channel Spacing[7:0]	Lower 8 bits of the peak deviation

General Options

GENERAL OPTIONS: LOCATION 0x0C

Bit	Bit Name	State	Comment
[7:5]	System Clock Select	111	Off
		110	Crystal divided by 2
		101	Crystal divided by 4
		100	Crystal divided by 8
		011	Crystal divided by 16
		010	Crystal divided by 40
		001	Crystal divided by 80
		000	Crystal divided by 160, Default value
4	Infinite PLL Lock Time	1	The PLL lock detection circuit runs continuously until the PLL locks.
		0	The output of the PLL lock detection circuit is latched at 130 μs. If the PLL isn't locked within that time, then the PLL Failed Lock signal is set.
3			
2	PA Reference	1	Gain 2.0
		0	Gain 1.0
1	Standby Mode	1	Crystal oscillator enabled
		0	Low−power, all circuits disabled
0	XTAL Select	1	Using a 24 MHz crystal
		0	Using a 20 MHz crystal

GPO Configuration

GPO CONFIGURATION: LOCATION 0x0D

Bit	Bit Name	State	Comment
7			
6			
5			
4			
3:0	GPO Configuration	1111	
		1110	
		1101	
		1100	ADC is busy
		1011	Doing a Configuration A Sniff Cycle
		1010	Doing a Configuration B Sniff Cycle
		1001	Configuration B Sniff Timer overflowed
		1000	Is doing any Sniff Cycle
		0111	Energy is detected
		0110	Quick−Start cycle failed
		0101	Configuration A Sniff Timer overflowed
		0100	Cystal is powered down
		0011	PLL failed to lock
		0010	PLL locked successfully
		0001	Transmitter enable
		0000	Off, Default

ADC Poll Time

Specifies the frequency at which the part will wake−up in Sniff−Mode to determine which channel has the lowest noise floor. The timer is clocked of a 1 Hz clock. If this value is written to 0xFF then this noise floor detection function is disabled.

ADC POLL TIME: LOCATION 0x0E

Bit	Name	Comment
7:0	ADC Poll Time	

Sniff Configuration

SNIFF CONFIGURATION: LOCATIONS 0x10 AND 0x30 FOR CONFIGURATION A AND CONFIGURATION B, RESPECTIVELY

Bit	Bit Name	State	Comment
7			
6			
5			
4	Sniff Interval Resolution	1	100ms
		0	500us
3	Channel 3 Enable	1	Enables reception on Channel 3 if, channel 3 has the lowest noise floor
		0	Reception on Channel 3 is disabled
2	Channel 2 Enable	1	Enables reception on Channel 2 if, channel 2 has the lowest noise floor
		0	Reception on Channel 2 is disabled
1	Channel 1 Enable	1	Enables reception on Channel 1 if, channel 1 has the lowest noise floor
		0	Reception on Channel 1 is disabled
0	Enable Sniff	1	Enables the sniff cycle
		0	Sniff cycle is disabled

Receive Options

RECEIVE OPTIONS: LOCATIONS 0x11 AND 0x31 FOR CONFIGURATION A AND CONFIGURATION B, RESPECTIVELY

Bit	Bit Name	State	Comment
7:6	AMGPIO Configuration	1x	Analog RSSI Out
		01	Sliced
		00	Off, Pin configured as digital Out, driven High, unless in transmit
5:4	FMGPIO Configuration	1x	Analog Discriminator Out
		01	Sliced
		00	Off, Pin configured as digital Out, driven High, unless in transmit
3	FM Detector	1	Enabled
		0	Disabled
2	ASK Detector	1	Enabled
		0	Disabled
1:0	IF Bandwidth	11 10 01 00	N/A 300 kHz IF Bandwidth 200 kHz IF Bandwidth 100 kHz IF Bandwidth

Transceiver Options

TRANSCEIVER OPTIONS: LOCATIONS 0x12 AND 0x32 FOR CONFIGURATION A AND CONFIGURATION B, RESPECTIVELY

Bit	Bit Name	State	Comment
7:4	CDR Manchester Re−Align Threshold		If this value is set to N and the CDR module receives N+1 invalid Manchester bits out of 16 bits, then the CDR will adjust the NCO by +180° to re−align to the Manchester data. Setting this value to 0 will disable this functionality. This functionality is always disabled if the Payload Encoding (Bit 3) is set to NRZ.
3	Payload Encoding	1	Payload is Manchester encoded
		0	Payload is NRZ encoded
2:1	Receive Mode	11	Invalid
		10	Wake−On−Pattern
		01	Wake−On−Energy
		00	Normal Receive
0	Transmit Mode	1	Inputs are synchronized to baud clock
		0	Inputs are asynchronous

CDR Options

The sample clock frequency should be set such that it is high as possible without overflowing certain accumulators in the CDR. The Sample Clock Frequency * Data Rate should be less than or equal to 400. For example, for a data rate of 19.2 kbps using a 20 MHz crystal the user should select the Sample Clock Frequency to be Crystal divided by 4, since 5 MHz < 19.2 kHz * 400.

CDR OPTIONS: LOCATIONS 0x13 AND 0x33 FOR CONFIGURATION A AND CONFIGURATION B, RESPECTIVELY

Bit	Bit Name	State	Comment
7	CDR Enabled	1	CDR enabled with input as selected in bit 6
		0	
6	CDR/Correlator Input	1	FSK
		0	ASK
5:4	Activity Check<1:0>	11	16 bits
		10	8 bits
		01	4 bits
		00	Disabled
3:0	Sample Clock	1111	Crystal divided by 512
		1110	Crystal divided by 256
		1101	Crystal divided by 160
		1100	Crystal divided by 128
		1011	Crystal divided by 80
		1010	Crystal divided by 64
		1001	Crystal divided by 40
		1000	Crystal divided by 32
		0111	Crystal divided by 20
		0110	Crystal divided by 16
		0101	Crystal divided by 10
		0100	Crystal divided by 8
		0011	Crystal divided by 5
		0010	Crystal divided by 4
		0001	Crystal divided by 2
		0000	Crystal

Sniff−Mode Interval

This register sets the time for the interval of the Sniff−Mode function. The resolution of the timer is specified in the Sniff Configuration register, and is based off of the 10 kHz low power oscillator. The Sniff−Mode interval time will be Sniff−Mode Interval * Sniff−Mode Interval Resolution.

Receive Dwell Timer

Length of time the receiver remains active during a Sniff−Mode cycle or after a receive instruction checking for the either the presence of energy or the wake pattern. If this value is 0x00 then the receiver will impulse sample to detect energy in Wake−On−Energy mode. If this value is 0xFF then the receiver will stay on until either energy is detected or the wake pattern found depending on mode. This timer is clocked at 10 kHz in Wake−On−Energy mode, and by the baud clock Wake−On−Pattern mode.

Energy Threshold

RSSI threshold used for ASK data slicing during a Sniff−Mode event. Also used for data slicing of the ASK when DAC mode is specified for the ASK Slice mode in the ASK Configuration register.

Wake Pattern <1:0>

If the receive mode is Wake−On−Pattern this register defines a sequence the receiver will check for during a Sniff−Mode or receive cycle. The sequence can be defined as NRZ, Manchester, or RZ in Pattern Threshold register independent of the data type for the ensuing ID or packet data. The bit interval remains the same as the data rate programmed into the device for clock and data recovery.

If the receive mode is Wake−On−Energy this register defines the upper two bytes of the chip id the receiver will check during a Sniff−Mode or receive cycle.

The full 16−bit sequence need not be used, and the length of a pattern the receiver will check for is set in the Pattern and ID Length register.

Chip ID <1:0>

If the receive mode is Wake−On−Pattern this register defines a sequence the receiver will check for once the wake pattern has been detected.

If the receive mode is Wake−On−Energy this register defines the lower two bytes of the chip id the receiver will check during a Sniff−Mode or receive cycle.

The full 16−bit sequence need not be used, and the length of a ID the receiver will check for is set in the Pattern and ID Length register.

Pattern and ID Threshold

This register controls how well each incoming bit must match the expected value in order to be considered valid.

PATTERN & ID THRESHOLD: LOCATIONS 0x1B AND 0x3B FOR CONFIGURATION A AND CONFIGURATION B, RESPECTIVELY

Bit	Bit Name	State	Comment
7:6	Wake Pattern Encoding	11	Invalid
		10	RZ
		01	Manchester
		00	NRZ
5:3	Pattern Threshold		0x7 is full correlation, 0x4 is 50% and will give best sensitivity
2:0	ID Threshold		0x7 is full correlation, 0x4 is 50% and will give best sensitivity

Pattern and ID Length

If the receive mode is Wake−On−Pattern this register controls how many bits the device will try to correlate for both the Wake Pattern and Chip ID. Each setting is N+1, meaning a setting of 0xF will use all 16 bits for either the wake pattern or the chip id.

If the receive mode is Wake−On−Energy the concatenation of these nibbles will specify the chip id length to be used. For example if the entire register contains 0x1F, then a chip id length of 32 is assumed. If the register contains 0x0 then the wake on id function is disabled.

PATTERN & ID LENGTH: LOCATIONS 0x1C AND 0x3C FOR CONFIGURATION A AND CONFIGURATION B, RESPECTIVELY

Bit	Bit Name	State	Comment
7:4	ID Length	0−F	Set the length of the Chip ID to find
3:0	Pattern Length	0−F	Set the length of the Pre−amble to find

Code Dwell Timer

This timer runs at 4x the bit time, so it's defined in nibbles. To have the receiver on all of the time checking for the Chip ID, set this register to 0xFF.

Packet Length

Length of packet to be buffered in expressed in bits, when set to 0x00, buffered packet is disabled. Maximum is 128.

Data Rate<1:0>

The Data Rate<1>, and Data Rate<0> registers are used to set the data rates. The following equation is used to calculate the value for the data rate register,

$$CUST\_DR = DataRate \cdot \frac{2^{22}}{F_{sample\_clock}}$$

where DataRate is the desired data rate, and F_{sample_clock} is the frequency selected in the CDR Options register.

CDR Coefficients

The clock and data recovery loop filter coefficients. See the below table for recommended loopfilter coefficients for some common data rates.

CDR COEFFICIENTS: LOCATION 0x21 AND 0x41 FOR CONFIGURATION A AND CONFIGURATION B, RESPECTIVELY

Data Rate	Recommend Loopfilter Coefficients
1.2 kbps	0x18
2.4 kbps	0x18
4.8 kbps	0x18
9.6 kbps	0x18
19.2 kbps	0x18
57.6 kpbs	0x22

Start Detect Threshold

This sets the clock and data recovery module's oversample correlator threshold. The default and recommended value is 25. This value is only used in Wake−On−Energy mode. If this value is set to 0 then the Fast Phase Alignment portion of the CDR is disabled, and the part operates in a "free−run" mode of operation.

Start Detect Pattern

This sets the clock and data recovery module's oversampled correlator pattern. The value in this register is the value the CDR correlator will search for. This value is only used in Wake−On−Energy mode. It is recommended a value of 0x33 is used for NRZ encoding and 0x66 for Manchester encoding If the recommended values are set in the Start Detect Pattern register then a start of frame (SOF) of 0x55 is recommended for NRA and 0xA5 for Manchester.

ASK Detector Configuration

This register contains options for the ASK detector. The ASK data filter value setting selects the bandwidth of the low pass filter operating on RSSI. The ASK slice setting chooses the comparator reference for slicing the ASK data. Maximum sensitivity is achieved using the averaging mode.

ASK DETECTOR CONFIG: LOCATIONS 0x24 AND 0x44 FOR CONFIGURATION A AND CONFIGURATION B, RESPECTIVELY

Bit	Bit Name	State	Comment
7:5	ASK data filter value	111	38.4 kHz @ 24 MHz crystal; 32 kHz @ 20 MHz crystal
		110	19.2 kHz @ 24 MHz crystal; 16 kHz @ 20 MHz crystal
		101	9.6 kHz @ 24 MHz crystal; 8 kHz @ 20 MHz crystal
		100	4.8 kHz @ 24 MHz crystal; 4 kHz @ 20 MHz crystal
		011	2.4 kHz @ 24 MHz crystal; 2 kHz @ 20 MHz crystal
		010	1.2 kHz @ 24 MHz crystal; 1 kHz @ 20 MHz crystal
		001	600 Hz @ 24 MHz crystal; 500 Hz @ 20 MHz crystal
		000	300 Hz @ 24 MHz crystal; 250 Hz @ 20 MHz crystal
4			
3			
2			
1:0	ASK Slice	1x	DAC
		01	Dual Peak Detector
		00	RC integrator

FSK Detector Configuration

FSK Filter sets the post−detection bandwidth of the FSK detector. Similar to ASK mode, the output of the discriminator can either be sliced against a fixed reference, or against an average input signal. The fixed mode will be sensitive to Frequency offsets, while the average mode will provide the greatest sensitivity.

FSK DETECTOR CONFIG: LOCATIONS 0x25 AND 0x45 FOR CONFIGURATION A AND CONFIGURATION B, RESPECTIVELY

Bit	Bit Name	State	Comment
7:5	FSK Filter	111	72 kHz
		110	36 kHz
		101	24 kHz
		100	18 kHz
		011	12 kHz
		010	9 kHz
		001	6 kHz
		000	3 kHz
4			
3:2	FSK GAIN	11	2.5 mV/kHz
		10	5.0 mV/kHz
		01	7.5 mV/kHz
		00	10 mV/kHz
!:0	FSK SLICE	1x	1 V reference
		01	Dual Peak Detector
		00	RC integrator

PA Control

The output power control register.

PA CONTROL: LOCATION 0x50

Bit	Bit Name	State	Comment
7:0	DAC Value		An 8 bit DAC with a 2 V reference

Crystal Trim

Crystal trim register, minimum value is minimum capacitance/maximum frequency, max value (0xFF) is maximum capacitance (~40 pF) minimum frequency.

Quick−Start Trim

Trim register for the quick start oscillator, 0x00 is minimum frequency, 0xFF is maximum frequency. The Quick−Start Oscillator trim a can be automatically trimmed via an onboard state machine.

10k Oscillator Trim

Trim register for the 10kHz oscillator. 0x00 is minimum frequency, 0xFF is maximum frequency. The 10k Oscillator trim a can be automatically trimmed via an onboard state machine.

Analog Reference Trim

ANALOG REFERENCE TRIM: LOCATION 0x54

Bit	Bit Name	State	Comment
7:4	Bandgap trim		ON trimmed parameter
3:0	Iref trim		ON trimmed parameter

Filter Trim

IF FILTER TRIM: LOCATION 0x55

Bit	Bit Name	State	Comment
7:4	IF Center		IF Center Frequency Trim, 0xF is max, ON trimmed parameter
3:0	IF Bandwidth		IF Bandwidth Trim, 0xF is max, ON trimmed parameter

Receiver Trim

RECEIVER TRIM: LOCATION 0x56

Bit	Bit Name	State	Comment
7	Quick−Start calibrated	1	The Quick−Start has been calibrated successfully.
		0	The Quick−Start hasn't been calibrated, or the calibration failed.
6	LNA Gain Mode	1	High gain mode
		0	Low gain mode.
5:0	IR Amplitude Trim		ON trimmed parameter

RF PLL Trim

RF PLL TRIM: LOCATION 0x57

Bit	Bit Name	State	Comment
7:4	Image Reject Phase Trim		ON trimmed parameter
3	Internal Filter	1	Use internal loop filter
		0	Use external loop filter
2:0	Charge Pump Current	7	40 μA
		6	37.5 μA
		5	35 μA (Nominal Design setting for 434 MHz)
		4	32.5 μA
		3	30 μA
		2	27.5 μA
		1	25 μA (Nominal Design setting for 315 MHz)
		0	22.5 μA

Antenna Trim

The antenna trim register controls an internally variable shunt capacitance on the RF pin. Both the transmit and receive trims control the same capacitance, the value in the upper nibble is applied in Transmit, the lower nibble in receive. At setting 0x0, capacitance is 0 pF, and at setting 0xF the capacitance is ~4 pF

ANTENNA TRIM: LOCATION 0x58

Bit	Bit Name	State	Comment
7:4	Transmit Antenna Trim		
3:0	Receive Antenna Trim		

RSSI Trim

The RSSI trim register is ON trimmed. The register allows adjustment of the slope, offset, and temperature compensation for the RSSI signal. The temperature compensation can be disabled in the analog test mode register.

RSSI TRIM: LOCATION 0x59

Bit	Bit Name	State	Comment
7:6	RSSI Temp Trim	11	41 nA/C Current
		10	36 nA/C Current
		01	31 nA/C Current
		00	26 nA/C Current
5:4	RSSI Offset Trim	11	+100 mV
		10	0
		01	−100 mV
		00	−200 mV
3:0	RSSI Res Trim		RSSI Resistor Trim

FSK Offset Trim

The FSK offset trim register is used to center the Discriminator output at 1 V when an RF signal at the desired RF is applied.

FSK OFFSET TRIM: LOCATION 0x5A

Bit	Bit Name	State	Comment
7:4	FSK Filter Trim		0x0 is min bandwidth, 0xF is maximum bandwidth
3:0	FSK Offset Trim		0x0 is min, 0xF is max

XTAL Current Trim

This register is used to control the current of the crystal oscillator, coarse adjust for the Quick Start oscillator and temperature slope adjustment for the quick start oscillator.

XTAL CURRENT TRIM: LOCATION 0x5B

Bit	Bit Name	State	Comment
7:4	XTAL Current Trim		
3:2 1:0	Quick Start Temperature Compensation		

LNA Output and Temperature Sensor Trim

LNA & TEMPERATURE TRIM: LOCATION 0x5C

Bit	Bit Name	State	Comment
7:4	Temperature Sensor Trim		
3:0	LNA Output Trim		

IPtat Trim

IPTAT TRIM: LOCATION 0x5D

Bit	Bit Name	State	Comment
7:6	IF Filter Temperature Compensation Scale Factor	11	2.5x
		10	2x
		01	1.5x
		00	1x
5	IF Filter Temperature Compensation Hot Adjustment	1	Increased
		0	Normal
4	IF Filter Temperature Compensation Cold Adjustment	1	Increased
		0	Normal
3:0	IPtat Trim		ON trimmed parameter

Miscellaneous

Miscellaneous configuration items.

Bit	Bit Name	State	Comment
7:4	User Data		Available for user storage
2	Enable FSK Squelch	1	Enabled
		0	Disabled
1	QSO Cycle Slip Enable	1	Enabled
		0	Disabled
0	Enable QSO auto−compensation	1	Enabled
		0	Disabled

Check Sum

This is the check sum value for the EEPROM for checking the data validity of the array.

EE Unlock

This value allows writing to the eeprom. The register should be written to 0x95 for the device to write the eeprom. Once the eeprom has been written, this register should be re−written to its default value.

Temperature ADC data

TEMPERATURE ADC DATA: LOCATION 0x6A

Bit	Name	Comment
7:0	Temperature Data	Temperature Sensor ADC reading

Channel 1 ADC data

TEMPERATURE ADC DATA: LOCATION 0x6B

Bit	Name	Comment
7:0	Channel 1 Data	Channel 1 ADC reading

Channel 2 ADC data

TEMPERATURE ADC DATA: LOCATION 0x6C

Bit	Name	Comment
7:0	Channel 2 Data	Channel 2 ADC reading

Channel 3 ADC data

TEMPERATURE ADC DATA: LOCATION 0x6D

Bit	Name	Comment
7:0	Channel 3 Data	Channel 3 ADC reading

Packet <15:0>

These registers contain the packet data that has been buffered into the part if the Packet Length register is non−zero.

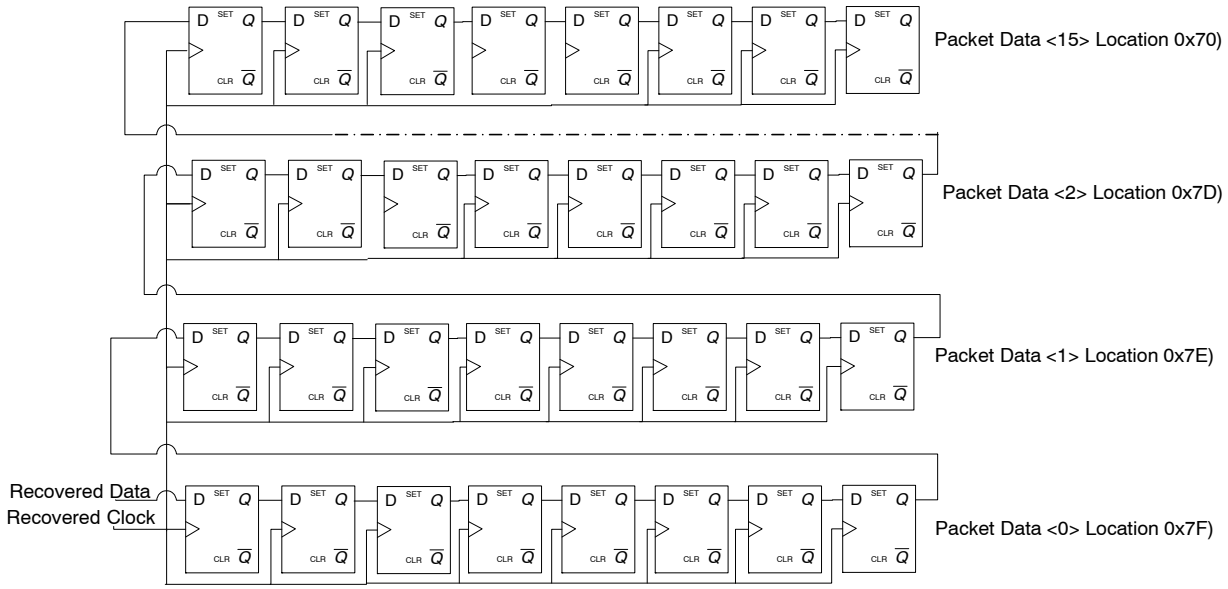


Figure 31. Packet Data Organization

The packet data is shifted into a 128−bit shift register. The data comes from the output of the clock and data recovery circuit and is clocked by the recovered baud clock. The first bit received will be the first bit shifted in, and will be the MSB in register location 0x70 if the packet length is 128.

Analog Test Mux

ANALOG TEST MUX: LOCATION 0x80

Bit	Signal	State	Comment
[7:4] FMGPIO		F	
		E	
	AM testInput	D	FMGPIO as input pin to AM detector
		C	
		B	
	iptat_master	A	
	I2 μA	9	2uA current from the master bias block
		8	
	AM input	7	AMGPIO pad as input to FMGPIO buffer
	FMfilterVDD	6	
	VregKicker	5	
	VregBE	4	
	FM threshold	3	
	FM follower neg	2	
	FM follower pos	1	
	FM Discriminator	0	Default Condition
[3:0] AMGPIO		F	
		E	
	FM test input	D	Input pin to FSK threshold setting block
		C	
	EE cell currents	B	Mux must be selected this way when using the EE test modes to measure cell currents
	Inputs from PLL	A	Controlled by PLL test mode (charge−pump Iptat and loop filter)
	Kicker reference current	9	
		8	
	FM input	7	FMGPIO pad as input to AMGPIO buffer
	2 V reference	6	Internal 2.1 V regulator for the Kicker
	1 V reference	5	
	DAC	4	Output is controlled by ‘Power’ setting in TX, Slice Threshold in RX
	Bandgap	3	Bandgap output voltage
	AM threshold	2	
	Temperature Sensor	1	
	Filtered RSSI	0	Default Condition

RF Test Mux

RF TEST MUX: LOCATION 0x81

Bit	Signal	State	Comment
7			
6			
5			
4	PLL Test Mode	1	Integer divide
		0	Fractional divide
[3:0] RFPWR		F	
		E	
		D	
		C	
		B	
	IFfilter BW	A	Regulator for the Bandwidth portion of the IF filter
	IFfilter Center	9	Regulator for the center frequency portion of IF filter
	Limit Amp 3	8	Regulator for the last stage of the Limit Amp
	Limit Amp 2	7	Regulator for the second two stages of the Limit Amp
	Limit Amp 1	6	Regulator for the first two stages of the Limit Amp
	IF AMP Reg	5	Regulator for the IF amplifiers
	Mixer Reg	4	Regulator for the mixer
	PLL Digital Reg	3	Regulator for the “digital” portion of the RF PLL
	PLL Analog Reg	2	Regulator for the “analog” portion of the RF PLL
	PA Reg	1	Regulator for the PA pre−drive circuitry
	DAC	0	Default Condition

PLL Test Mode

PLL TEST MODE: LOCATION 0x82

Bit	Bit Name	State	Comment
7	Reset	1	hold the divider, sigma delta, reference clk gen, and phase detector in reset
6	sigDelTest	1	Enable the sigma delta test mode . Sigma delta and pn code driven direcly from the refclk input.
5	Invert PLL Mode	1	When in RX PLL runs in TX mode. When in TX PLL runs in RX mode
		0	When in RX PLL runs in RX mode. When in TX PLL runs in TX mode
4	pd_cp	1	power down the charge pump. (also disables the pfd)
3	LP_bufferEnable	1	Turn on the buffer and enable its output on testNode2
2	iptat_testEn	1	Enable the iptat test current on the testNode2 output
1	ForceSource	1	Turn on the source current from the charge pump (also shuts off the pfd) (The loop filter will need to be set to external for measurement)
		0	
0	ForceSink	1	Turn on the sink current from the charge pump (also shuts off the pfd) (The loop filter will need to be set to external for measurement)
		0	

Analog Test Mode

ANALOG TEST MODE: LOCATION 0x83

Bit	Bit Name	State	Comment
7	PreCharge	1	Force PreCharge High for detector measurements
		0	
6	IF filter Bypass Mode	1	Bypass the IF filter for JIC
		0	
5		1	
		0	
4		1	
		0	
3		1	
		0	
2	FSK Test Digital In	1	xInterrupt pin used as digital input to FSK detector Block
		0	
1	RSSI Temperature Comp Disable	1	
		0	
0			

Digital Test Mode A

DIGITAL TEST MODE A: LOCATION 0x90

Bit	Bit Name	State	Comment
7	Auto Increment Disable	1	Disable the auto−increment feature of the I2C module
		0	
6	Kill digital Clock	1	Gate the clock going to the digital
		0	
5	Crystal Bypass	1	Bypass the crystal module and drive directly via the XTAL1 pad.
		0	
4:3	Pad Test	11	Pull−up Test
		10	Enable pad test A (Pull−Ups Disabled)
		01	Enable pad test B (Pull−Ups Disabled)
		00	Normal
2	EE BIST Start	1	Start the EEPROM BIST.
		0	
1	EE BIST Bad	1	If this bit is ever a ‘1’, it signifies the EEPROM BIST failed.
		0	
0	EE BIST done	1	Will go to a ‘1’ once the BIST is complete.
		0	

Digital Test Mode B

It will be necessary it test to write the lower two bits of this register. Due to clock gating elements in the design the user must write a dummy instruction to the command register to overwrite the lower two bits in this register. A value of 0x0E written to the command register will allow the user to write this register manually.

DIGITAL TEST MODE B: LOCATION 0x91

Bit	Bit Name	State	Comment
7	Overdrive Slice Data	1	AM and FMGPIO configured as inputs directly to correlator/CDR
		0	
6	10k Oscillator is xtal	1	The 10 kHz oscillator is muxed to be the cystal oscillator. This is used in testing the 10k oscillator clock dividers
		0	Normal mode of operation.
5			
4			
3			
2			
1	Continuous Kick Mode	1	Enable continuous kick mode
		0	Off
0	Kicker Clamped	1	Kicker is clamped
		0	Off

Digital Test Mux A

DIGITAL TEST MUX A: LOCATION 0x92

Bit	Signal	State	Comment
SYSCLK [7:4]		F	
	Xtal	E	
	Kicker	D	
	CDR Start	C	
	Wake on Pat Start	B	
	PLL Lock Failed	A	
	isPLLlocked	9	
	PLLrefCLK	8	Output of the PLL reference divider
	one shot	7	Output of the FSK discriminator One Shot
	Latchclk	6	Clock to the Limit Amp Output comparator/Latch
	AM filter Clk	5	Clock to the AM data Filter
	Sample Clock	4	
		3	
	Delta Sigma Clk	2	PLL feedback clock that drives the sigma delta
		1	
	Normal	0	Default Condition

DIGITAL TEST MUX A: LOCATION 0x92

Bit	Signal	State	Comment
xInt [3:0]	CheckSumFailed	F	
	kickerDone	E	A kick cycle is complete
	rcOscDiv10000	D	RC Oscillator divided by 10000
	xtalDiv2000	C	XTAL divided by 2000
	xtalDiv512	B	XTAL divided by 512
	xtalDiv160	A	XTAL divided by 160
		9	
	fractOut	8	Output of the Sigma Delta Modulator
	dataI	7	Output of the limit amp comparator
		6	
		5	
		4	
	clk10k	3	Output of the 10 KHz RC oscillator
	AM Slice Data	2	Output of the RSSI comparator
		1	
	Normal	0	Default Condition

Digital Test Mux B

DIGITAL TEST MUX B: LOCATION 0x93

Bit	Signal	State	Comment
DCLK [7:4]	CPENA	F	EE Charge Pump Enable
	kickerFail	E	A kick cycle failed.
	RC calibration Done	D	
	Detect Energy	C	
	PNcode (RFPLL)	B	PN code that modulates noise in the sigma delta
	preCharge	A	
		9	
	PAenable	8	
		7	
		6	
	All ID Match	5	
	ManchesterDecodedCLK	4	
	WakeOnPatter 8xBCLK	3	
	WakeOnPattern BCLK	2	
	recovered Clock	1	
	Normal	0	Default Condition

DIGITAL TEST MUX B: LOCATION 0x93

Bit	Signal	State	Comment
DRXTX [3:0]	EEBistBAD	F	
	xtal PD	E	
	BufferDone	D	
	Cfg A Sniff Timer Overflow	C	
	CodeDwellTimerOver	B	
	EnergyDwellOverflow	A	
	PacketTimer Overflow	9	
	TXdata (Encoded)	8	
	PLL locked Internal	7	
	KickerPD	6	
	Cfg B Sniff Timer Overflow	5	
	!CDRData	4	
	CDRData ^ Baud Clock	3	
	FM Slice Data	2	
	Recovered Data	1	
	Normal	0	Default Condition

Digital Test Mux C

DIGITAL TEST MUX C: LOCATION 0x94

Bit	Signal	State	Comment
RXactive [7:4]	EEbistDone	F	
	BGready	E	
	RC calibration fail	D	
	Energy Present	C	
	Kicker Ring/FSK Squelch Comp	B	When FSK squelch is enabled, this output becomes the output of the Squelch comparator.
	Receive is Awake	A	
	Sniffer is Awake	9	
	xResetPLL	8	
	isIDfound	7	
	PLL Acquire	6	
	All Pattern Match	5	
	ManchesterIsLocked	4	
	Recovered Data	3	
	isInSniff	2	
	isInTransmit	1	
	Normal	0	Default Condition
[3:0]		F	
		E	
		D	
		C	
		B	
		A	
		9	
		8	
		7	
		6	
		5	
		4	
		3	
		2	
		1	
		0	Default Condition

ON Rev Code

This value specifies the revision code for the NCV53480 ASIC.

RX/TX MATCHING1

The LNA and PA of the NCV53480 can either be matched to independent ports, or combined into a single port. The Independent RX Matching Section will show independent matching for the RFIN port, the Independent TX Matching Section will show matching for the RFOUT port, the Combined RX/TX Match Section shows combined matching, and finally the Matching to Small Loop Antenna Section shows an example matching circuit using a printed loop antenna.

Independent RX Matching

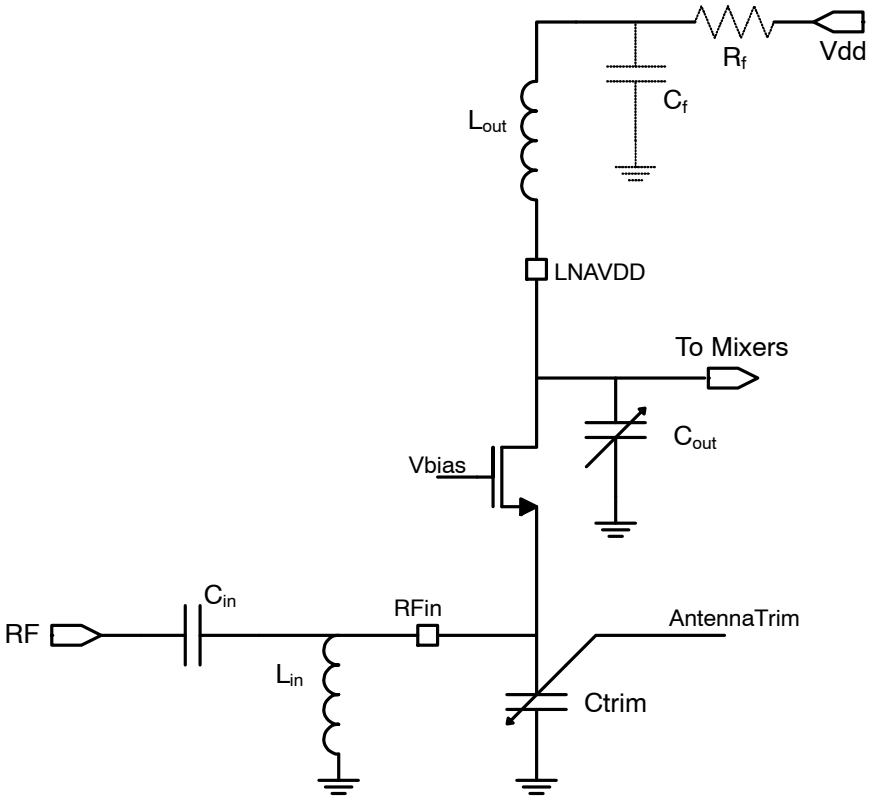


Figure 32. Independent Receive Match

The figure above shows the matching circuitry for the LNA. C_{in} and Lin form the input match to a 50 Ω source, while L_{out} tunes the LNA output. The chart below gives typical values for these components when the LNA is in high gain mode (Set by bit 6 of the Receiver Trim register).

	Cin	Lin	Lout
433.92 MHz	5 pF	18 nH	51 nH
315 MHz	10 pF	27 nH	100 nH

The LNA output node is nearly as sensitive as the LNA input, so it is important to keep this node clean of clock harmonics or other unwanted noise that may be present on the board. The dashed components Cf and Rf are optional and can be used to filter any noise that may be present on the supply. R_f should be kept less than 100 Ω (or replaced by an inductor) to avoid compressing the supply of the LNA too severely. C_f should be sized to provide the desired low pass corner frequency.

The integrated trimmable capacitors Ctrim and Cout can be used to fine tune the input match and output resonant circuits respectively. Ctrim can be adjusted with the lower 4 bits of the Antenna Trim register, and Cout adjusted with the lower 4 bits of the LNA and Temp Trim register. Ctrim decreases with increasing code from 5 pF to 2.4 pF, and Cout increases with increasing code from 2.1 pF to 2.9 pF. The input resistance of the LNA is 125 Ω in high gain mode, and 150 Ω in normal mode. This resistance is in parallel with the given C_{trim} capacitance values.

Independent TX Matching

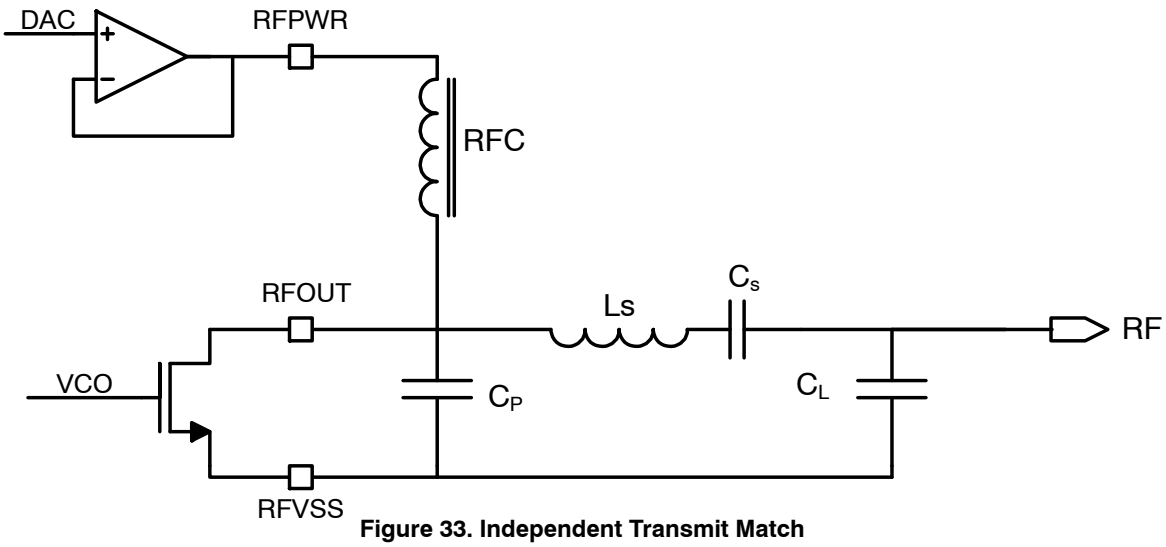


Figure 33. Independent Transmit Match

The figure to the above shows the matching network for the RF output to drive a given load impedance.Component values for matching to a 50 Ω load at selected frequency's are provided in Table 16.

Table 16.

	RFC	L_s	C_s	C_P	C_L
315 MHz	>400 nH	110 nH	5 pF	0.5 pF	0 pF
433.92 MHz	>270 nH	62 nH	6 pF	1 pF	0 pF

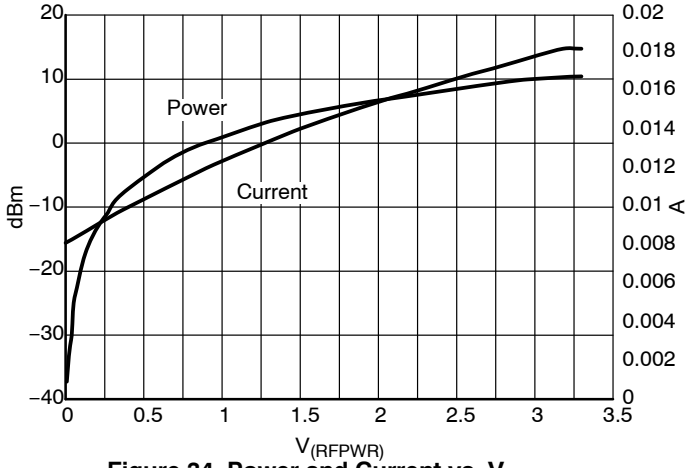


Figure 34. Power and Current vs. $V_{(RFPWR)}$ Gain of 2 Mode

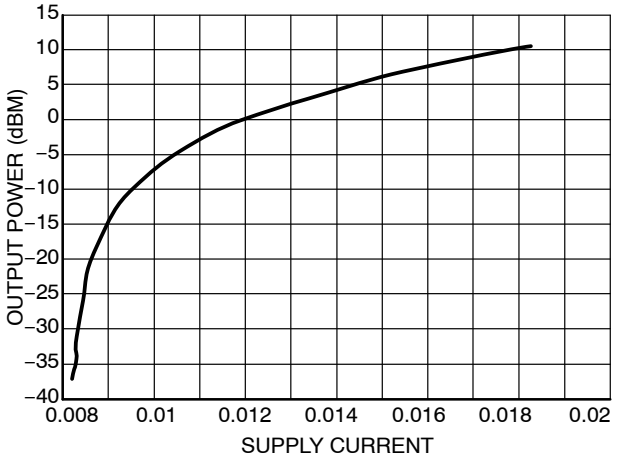


Figure 35. Power vs Current Current Gain of 2 Mode

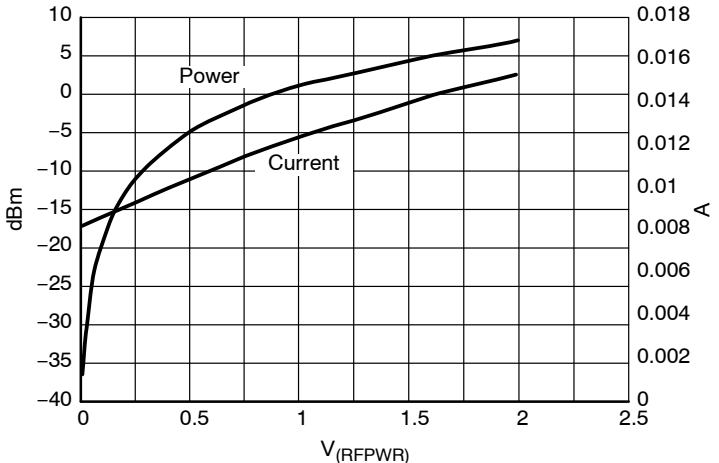


Figure 36. Power and Current vs. $V_{(RFPWR)}$ Gain of 1 Mode

Combined RX/TX Match

The RFIN and RFOUT pins can be shorted together using the matching network given in the TX Matching section to provide a single RF port without the need for an external RX/TX switch. In this configuration, the achievable RF output power will be slightly less due to the increased capacitance on the output net due to the LNA input. The RFPWR pin is pulled to ground internally during receive to provide the necessary DC path for the LNA input to ground.

For applications where it is desirable to have the RFIN and RFOUT ports separated to facilitate the addition of an external LNA, PA, or SAW filter network, the RXactive pin is provided for control of these external devices. The pin as its name implies is high during receive, and low otherwise. The current sink/source capability of the RXactive pin is limited to ±1 mA.

Matching to Small Loop Antenna

In many applications, the radiating antenna will not be a 50 Ω antenna, but rather a small printed loop antenna. In this case, the Antenna itself will form the inductor Ls and load resistance shown as Rrad. Typical values for Ls for a printed copper loop are between 40nH and 100nH, while Rrad is less than 1 Ω. This leads to having a very high Q tank, and hence a high output impedance seen by the PA at resonance which can cause damage to the device due to excessive voltage swings if care is not taken. Increasing the value of Cp will reduce the impedance transformation ratio and protect the device from damage.

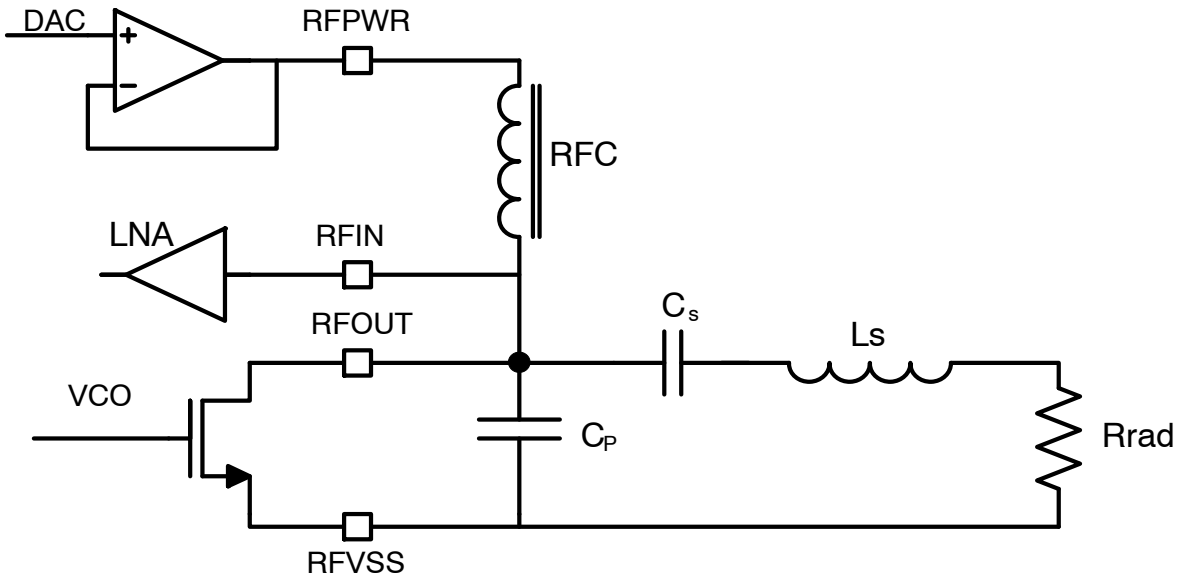


Figure 37. Loop Antenna Mat

Matching Tips

While matching the LNA input is straightforward and can be done quickly with the suggested network and the use of a network analyzer, matching the PA output is less straightforward. A good way to optimize the PA match is to utilize the frequency agility of the NCV53480. A simple application which sweeps the RF frequency of the NCV53480 while using a spectrum analyzer and DMM to measure the output power and supply current draw can quickly provide a designer with the necessary information to refine the matching network. The graph below shows such a sweep performed on a device with the match listed in Table 16 for 433.92 MHz. Notice that the points of maximum output power and minimum current draw do not coincide. The point of minimum current draw will always be slightly higher in frequency than the peak power point. So, while this match can deliver approximately the same amount of power at 400 MHz as it can at 450 MHz, the current consumption will be 25% higher at 400 Mhz than at 450 MHz. To adjust the frequency of the PA match, start with the match from the table closest to the desired frequency, then adjust the values of Ls and Cs using F = 1/sqrt(LC) keeping Ls as large as practical for maximum Q. Keep in mind that PCB trace will add ~1 nH per mm, so keep traces short.

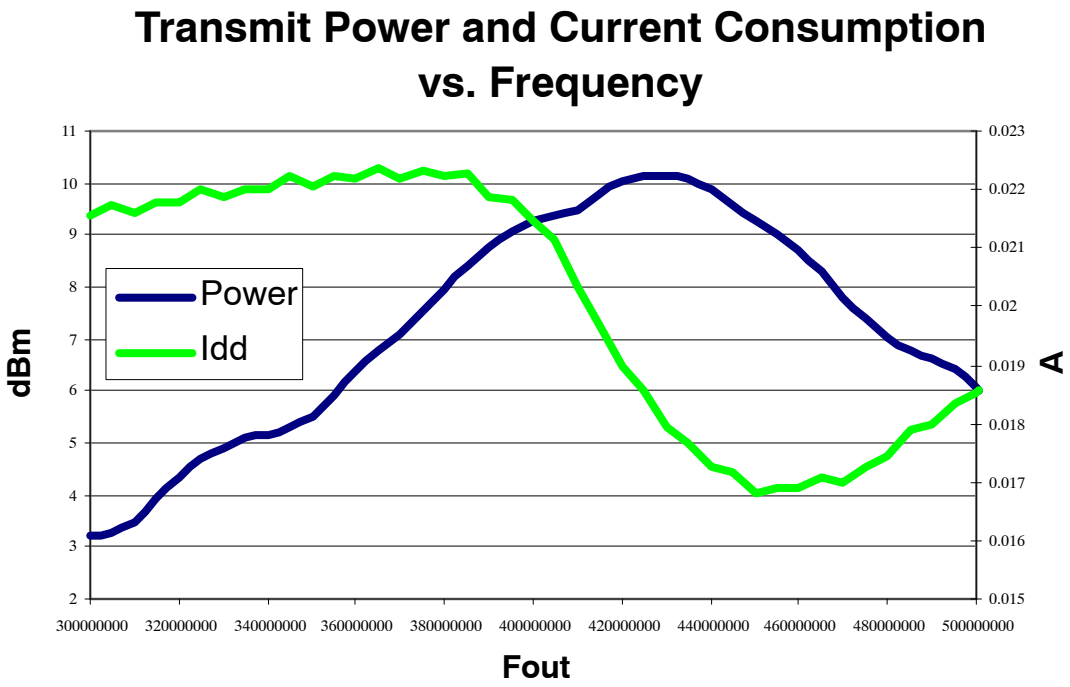


Figure 38. Transmit Power vs. Current Consumption

Checking the resonance of the LNA output can also be done utilizing a simple program. The plot below shows the RSSI output amplitude as the codes for Ctrim and Cout are swept through the values 0−15. From this, Ctrim should be set to 0xD, and Cout set to 0x5 for maximum sensitivity.

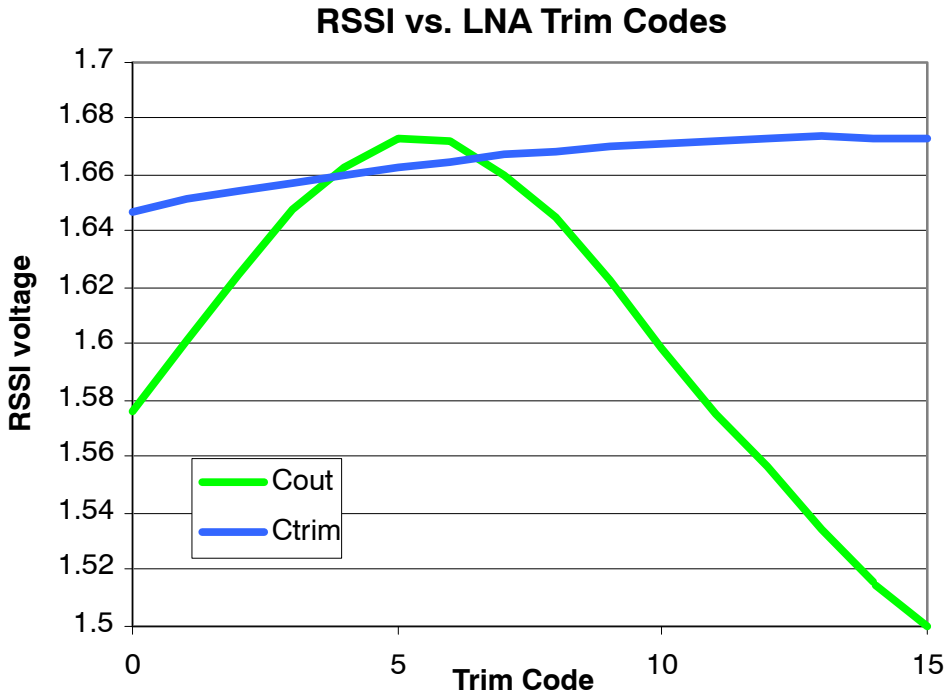


Figure 39. RSSI vs. LNA Trim Code

NCV53480 TRIMMED PARAMETERS USER GUIDE

The NCV53480 transceiver includes a number of blocks which include trim. Most of these are used by ON Semiconductor to maximize performance and yield by trimming of internal components, and are trimmed at silicon final test. A few of these parameters can be used to maximize performance and yield by trimming out external component variation at board level final test.

The table below lists all of the trim registers, a short description, whether these are trimmed by ON Semiconductor or left for the user, and what the value for the user trimmed parameters is set to at final silicon test. For those registers which contain functions trimmed both by ON Semiconductor and the user, please take care to preserve the trimmed values for the ON Semiconductor trimmed parameters when modifying these registers.

Table 17. TRIMMED PARAMETER REGISTER LOCATIONS

Working Register Addr.	Name	Bits	Description	Trimmed by?	Factory Set Value
0x50	PA Control	7:0	Output power setting and mode selection	User	0x80
0x51	Crystal Trim	7:0	Internal capacitive DAC trim setting	User	0x80
0x52	Quick Start Trim	7:0	Quick Start oscillator trim	User	0x80
0x53	10k Oscillator Trim	7:0	10kHz oscillator trim	User	0x80
0x54	Analog Trim	7:0	Internal voltage and current reference	ON	Trimmed
0x55	Filter Trim	7:0	IF filter center and bandwidth trim	ON	Trimmed
0x56	Receiver Trim	7	Quick Start is Calibrated (auto set after cal)	Device	0x0
		6	LNA High Gain Mode	User	0x1
		5:0	IR Trim	ON	Trimmed
0x57	RF PLL Trim	7:4	IR Trim	ON	Trimmed
		3	Use Internal Loop Filter	User	0x1
		2:0	Charge Pump Current	User	0x5
0x58	Antenna Trim	7:0	Transmit and Receive Antenna Trim	User	0x88
0x59	RSSI Trim	7:0	RSSI Trim	ON	Trimmed
0x5A	FSK Offset Trim	7:0	FSK detector input offset and BW trim	ON	Trimmed
0x5B	XTAL Current Trim	7:4	XTAL current Trim	Both	0x8
		3:0	QSO T−comp trim	ON	Trimmed
0x5C	LNA and T−sense	7:4	Temperature sensor trim	ON	Trimmed
		3:0	LNA Output trim	User	0x8
0x5D	Iptat Trim	7:0	Internal I−reference trim	ON	Trimmed
0x5E	User Data	7:0	Bits 7:4 are available for user storage	User	0xA0

PA Control

Please refer to the RX/TX matching section of the NCV53480 datasheet

Crystal Trim

Please refer to the Crystal Oscillator section on page 9 of the datasheet for information about this circuitry.

To trim, start by powering up the NCV53480 in its default state. In this state, the system clock on the SYSCLK pin will be set as a divide by 160 from the crystal clock. Monitor this frequency and adjust register 0x51 until the desired frequency is achieved. Increasing the value in register 0x51 will increase the capacitance of the internal capacitive DAC's, thus lowering the frequency. Decreasing this value will do the opposite.

Quick Start Trim

The Quick Start Oscillator is used for quickly starting the crystal oscillator in poling applications. There is an internal calibration circuit for doing this. Please refer to page 10 of the datasheet.

10kHz Oscillator Trim

Please refer to page 11 of the datasheet for a description of, and instructions on calibration of this oscillator.

Receiver Trim

Bit 6 of this register controls the current bias for the LNA. Setting this to a ‘1’, uses 500 μA additional current and provides an additional 3 dB of sensitivity (default setting). Setting this to a ‘0’ reduces the LNA current and sensitivity, but increases the IIP3 performance of the radio by ~ 5 dB. When setting or clearing this value, take precautions to preserve the data stored in the other bit locations.

RF PLL Trim

Bits 7:4 of this register are trimmed by ON Semiconductor. Bits 3:0 are available to be set depending on the user application. Please refer to Pages 11−12 for information on setting the value for this bit. When changing the values of bits 3:0, take precautions to preserve the data stored in bits 7:4.

Antenna Trim

Refer to the RX/TX matching section beginning on page 52 of the NCV53480 datasheet.

XTAL Current Trim

Bits 3:0 of this register are ON trimmed and care should be taken to maintain these values. Bits 7:4 control the bias current for the crystal oscillator and may be modified by the user to provide more or less gain for the crystal oscillator amplifier. By default, this value is set to 8. Refer to page 9 of the datasheet for additional information.

LNA and Temperature Sensor

Bits 7:4 are trimmed by ON Semiconductor. Bits 3:0 are available for the user to trim the LNA output resonant tank circuit. Please refer to the RX/TX matching section beginning on page 50 of the NCV53480 datasheet for further information.

PAD PARAMETRICS AND CURRENT LEVELS

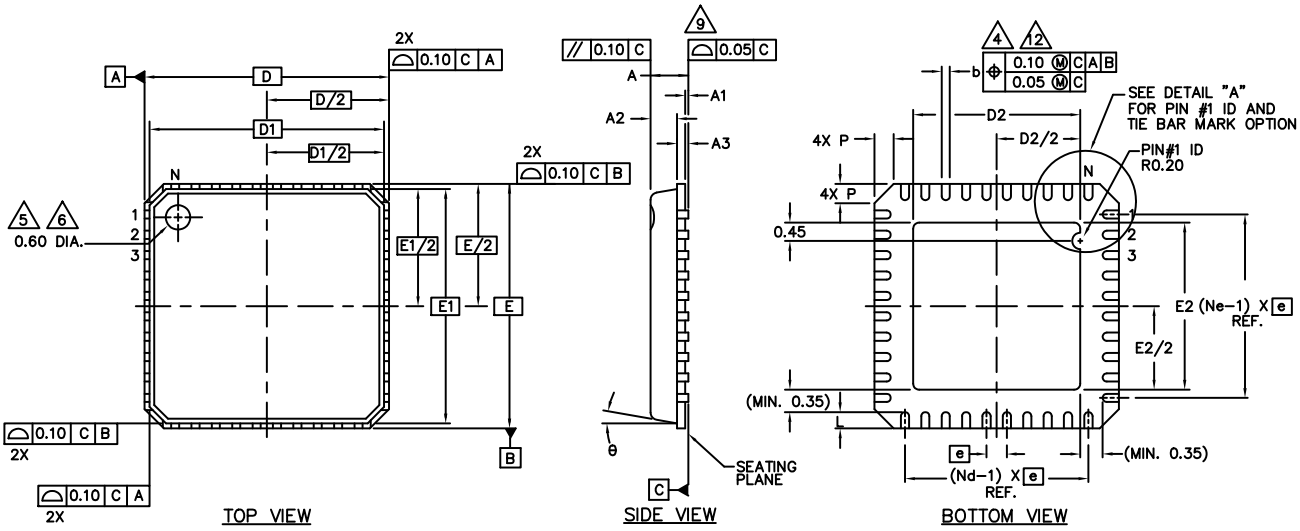
Table 18. PAD PARAMETRICS

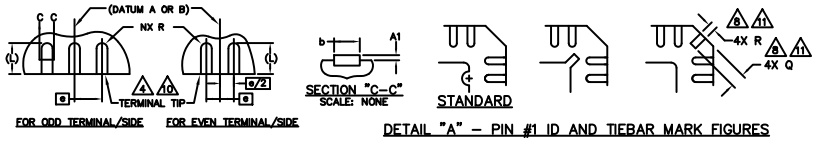
Pin#	Name	Type (Note 5)	Vil (max) V (Note 6)	Vih (min) V (Note 6)	Iil (min/max) µa (Note 6, 7)	Iih (min/max) µa (Note 6, 7)	Vol (max) V (Note 6)	Voh (min) V (Note 6)	Iol (max) mA (Note 6, 7)	Ioh (min) mA (Note 6, 7)	Notes (Note 8)
1	RFOUT	AO									
2	RFIN	AI									
3	LNAVDD	AO									
4	RFVSS	P									
5	AVDD	P									
6	FMPOS	AO									
7	FMNEG	AO									
8	FMGPIO	ADIO	0.3 * V_{DD}	0.7 * V_{DD}	−27/−75	−1.0/+1.0	0.2 * V_{DD}	0.8 * V_{DD}	1.0	−1.0	SU
9	AMGPIO	AO	0.3 * V_{DD}	0.7 * V_{DD}	−27/−75	−1.0/+1.0	0.2 * V_{DD}	0.8 * V_{DD}	1.0	−1.0	SU
10	AMNEG	AO									
11	AMPOS	ADIO									
12	XTAL1	AI									
13	XTAL2	AO									
14	AVSS	P									
15	xINT	DO					0.2 * V_{DD}	0.8 * V_{DD}	1.0	−1.0	
16	GPO	DO					0.2 * V_{DD}	0.8 * V_{DD}	2.0	−2.0	
17	xReset	DIO	0.3 * V_{DD}	0.7 * V_{DD}	−27/−75	−1.0/+1.0	0.2 * V_{DD}	0.8 * V_{DD}	1.0	−1.0	SU
18	RXTX	DIO	0.3 * V_{DD}	0.7 * V_{DD}	−27/−75	−1.0/+1.0	0.2 * V_{DD}	0.8 * V_{DD}	1.0	−1.0	SU
19	DCLK	DIO	0.3 * V_{DD}	0.7 * V_{DD}	−27/−75	−1.0/+1.0	0.2 * V_{DD}	0.8 * V_{DD}	1.0	−1.0	SU
20	DREG	P									
21	DVDD	P									
22	DVSS	P									
23	SYSCLK	DO					0.2 * V_{DD}	0.8 * V_{DD}	2.0	−2.0	
24	SDATA	DIO	0.3 * V_{DD}	0.7 * V_{DD}	−27/−75	−1.0/+1.0	0.2 * V_{DD}	0.8 * V_{DD}	1.0	−1.0	SU
25	SCLK	DI	0.3 * V_{DD}	0.7 * V_{DD}	−27/−75	−1.0/+1.0	0.2 * V_{DD}	0.8 * V_{DD}	1.0	−1.0	SU
26	RXACTIVE	DO					0.2 * V_{DD}	0.8 * V_{DD}	2.0	−2.0	
27	LOVDD	P									
28	LOOPOUT	AI									
29	LOOPIN	AO									
30	LOVSS	P									
31	RFVDD	P									
32	RFPWR	AO									

5. Buffer Type: A = analog, D = Digital, I = Input, O = Output, IO = Bi−directional, P = Power
6. Symbol: Iil and Iih are tested at V_{DD} = VDDmax Volts. Not tested at less than room temperature.
   Vol, Iol are tested at typical.
   Voh, Ioh are tested at typical.
7. Limits: Polarity on currents indicates direction of current: (+) for sinking and (−) for sourcing
8. PU = Pullup, PD = Pulldown, ST = Schmitt, SU = Schmitt & Pullup, SD = Schmitt & pulldown

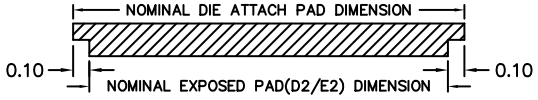
PACKAGE DIMENSIONS

NQFP 32, 6x6
CASE 560AR
ISSUE O





GENERAL ; NOMINAL EXPOSED PAD(D2/E2) DIMENSION = NOMINAL DIE ATTACH PAD DIMENSION−0.20



<DIE ATTACH PAD X−SECTION VIEW>

PACKAGE DIMENSIONS

NQFP 32, 6x6
CASE 560AR
ISSUE O

SYMBOL	PITCH VARIATION A			NOTE
	MIN.	NOM.	MAX.	
e	0.80 BSC			
N	20			3
Nd	5			3
Ne	5			3
L	0.50	0.60	0.75	
b	0.28	0.33	0.40	4
D2	SEE EXPOSED PAD VARIATION: B			
E2	SEE EXPOSED PAD VARIATION: B			

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e	0.65 BSC			
N	28			3
Nd	7			3
Ne	7			3
L	0.50	0.60	0.75	
b	0.23	0.28	0.35	4
D2	SEE EXPOSED PAD VARIATION: B,C			
E2	SEE EXPOSED PAD VARIATION: B,C			

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	32			3
Nd	8			3
Ne	8			3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	SEE EXPOSED PAD VARIATION: D			
E2	SEE EXPOSED PAD VARIATION: D			

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	36			3
Nd	9			3
Ne	9			3
L	0.50	0.60	0.75	
b	0.18	0.23	0.30	4
D2	SEE EXPOSED PAD VARIATION: B,C			
E2	SEE EXPOSED PAD VARIATION: B,C			

* NOT DESIGNED YET
** DESIGNED BUT NOT TOOLED UP

SYMBOL	PITCH VARIATION E			NOTE
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	40			3
Nd	10			3
Ne	10			3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	SEE EXPOSED PAD VARIATION: C,D,E			
E2	SEE EXPOSED PAD VARIATION: C,D,E			

SYMBOL	PITCH VARIATION F			NOTE
	MIN.	NOM.	MAX.	
e	0.40 BSC			
N	48			3
Nd	12			3
Ne	12			3
L	0.30	0.40	0.50	
b	0.15	0.20	0.25	4,12
D2	SEE EXPOSED PAD VARIATION: *			
E2	SEE EXPOSED PAD VARIATION: *			

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	10
A2	0.60	0.65	0.70	
A3	0.20 REF.			
D	6.00 BSC			
D1	5.75 BSC			
E	6.00 BSC			
E1	5.75 BSC			
θ	0	–	12°	
P	0.24	0.42	0.60	
Q	0.30	0.40	0.65	8,11
R	0.13	0.17	0.23	8,11

<STANDARD>

SYMBOLS		D2			E2			NOTE
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	A	2.80	2.90	3.00	2.80	2.90	3.00	
	B	3.60	3.70	3.80	3.60	3.70	3.80	
	C	4.00	4.10	4.20	4.00	4.10	4.20	
	D	4.20	4.30	4.40	4.20	4.30	4.40	
	E	4.30	4.40	4.50	4.30	4.40	4.50	

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
10. APPLIED ONLY FOR TERMINALS.
11. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.
12. FOR 0.40mm LEAD PITCH, THE LEAD POSITION TOLERANCE MUST BE 0.07mm AT THE ACTUAL MEAN VALUE OF BODY SIZE.

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