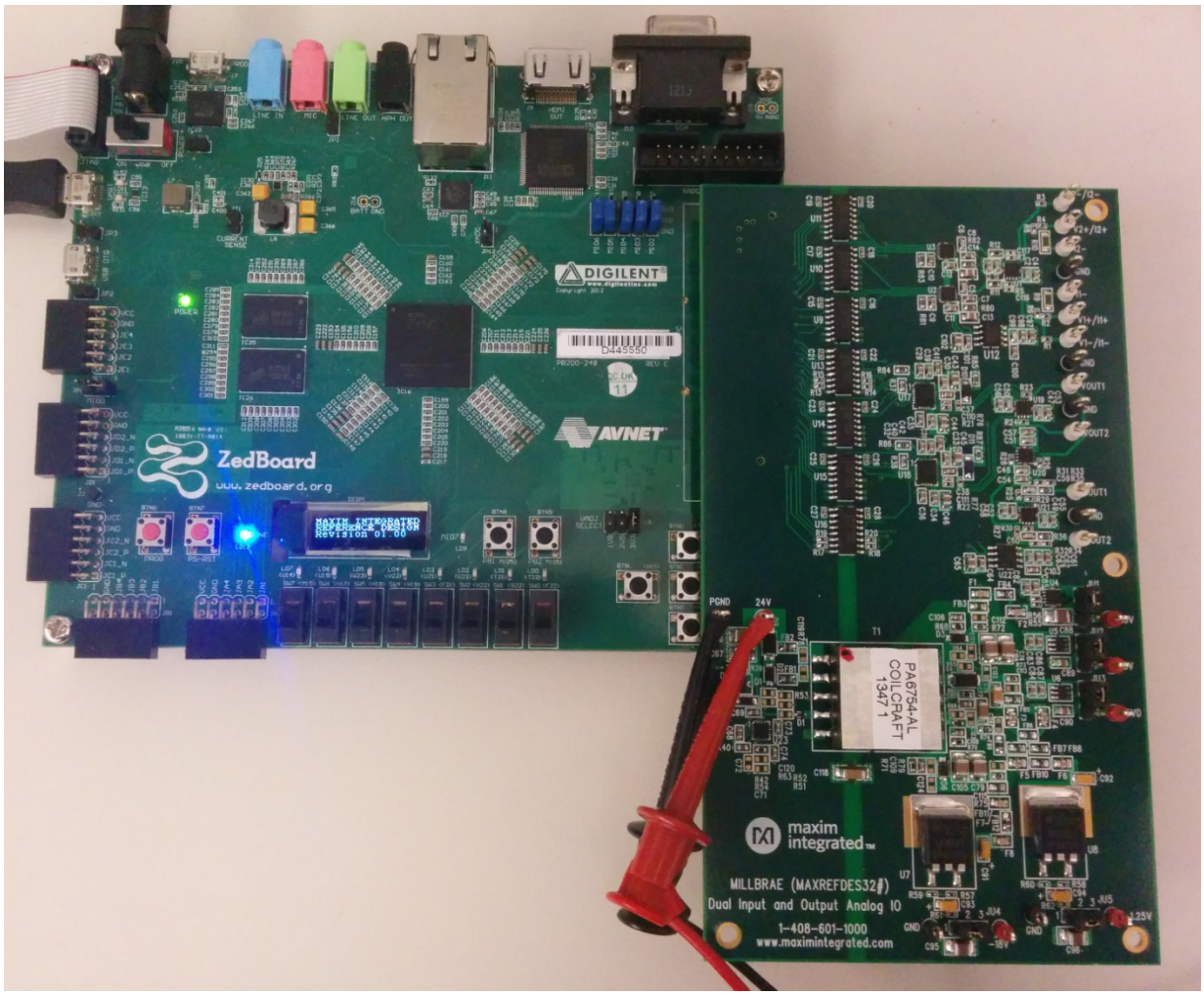
MAXREFDES32# ZedBoard Quick Start Guide

Rev 0; 5/14



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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1. Required Equipment

- MAXREFDES32# board
- ZedBoard™ Rev C development kit
- Industrial sensor or signal source
- To run the binary from SD card:
  - Host PC with Windows® OS with Terminal Software installed (HyperTerminal) and one USB port
  - Cypress USB-UART bridge device driver
  - 4GB FAT32 formatted SD card
- To run the software from the Xilinx® SDK:
  - PC with Windows OS with Xilinx PlanAhead™/SDK version 14.2 or later and two USB ports
  - License for Xilinx EDK/SDK (free WebPACK™ license is OK)
  - Xilinx Platform Cable USB II-compatible JTAG device

2. Overview

The MAXREFDES32 ZedBoard software can be downloaded to the ZedBoard board via two methods:

- (Easiest) Boot from an SD card containing a binary file that loads the necessary CPU bootloader, FPGA bitstream, and MAXREFDES32# executable file. This approach is explained in detail in Section 3 of this document.
- (Flexible) Use the Xilinx SDK to download the board bitstream and executable file. This approach allows the source code to be modified. This approach is explained in detail of Section 4 of this document.

3. Boot from an SD Card

The steps below describe how to download the binary image (BOOT.BIN), install on an SD card, and begin using the MAXREFDES32 system.

1) Download the latest BOOT.BIN file from the MAXREFDES32# page.
2) Obtain a FAT32 formatted 4GB SD card such as the one provided with the ZedBoard.
3) Copy the BOOT.BIN file onto the SD card. A USB-to-SD adapter is normally required to do this on a PC with Windows OS (Figure 1).
4) Ensure the SD card is the BOOT.BIN file. **Note that if using the Avnet supplied SD card, it comes pre-installed with a Linux test image. This image needs to be removed.**
5) Remove the SD card from the host PC. Make sure the ZedBoard is powered off, and insert the SD card in the ZedBoard (Figure 2).
6) Configure the ZedBoard boot source jumpers to boot from SD (Figure 3 and Figure 4).

7) Connect the MAXREFDES32# reference design board to the J1 FMC™ connector (Figure 5).
8) Connect a Micro-USB cable to ZedBoard USB connector J14. Connect the 12V power supply to the ZedBoard and slide the SW8 power switch to the on position. If the BOOT.BIN file has loaded successfully, the on-board display will show the message **MAXIM INTEGRATED REFERENCE DESIGN Revision XX.XX**.
   a) The ZedBoard utilizes the Cypress USB-UART bridge IC. If Windows cannot automatically install the driver for the Cypress USB-UART bridge IC, the driver is available for download from www.cypress.com/?rID=63794. The driver is WHQL certified for the default Cypress VID / PID of 0x04B4 / 0x0008.
9) Open HyperTerminal or similar Terminal program on the PC. Find the appropriate COM port, usually a higher number port, such as COM4, or COM6, and configure the connection for 115200, n, 8, 1, none (flow control).
10) The MAXREFDES32 software will display a menu (Figure 6).
11) Use the menu selections to choose ADC conversion or signal replication.



Figure 1. USB-SD and SD Card

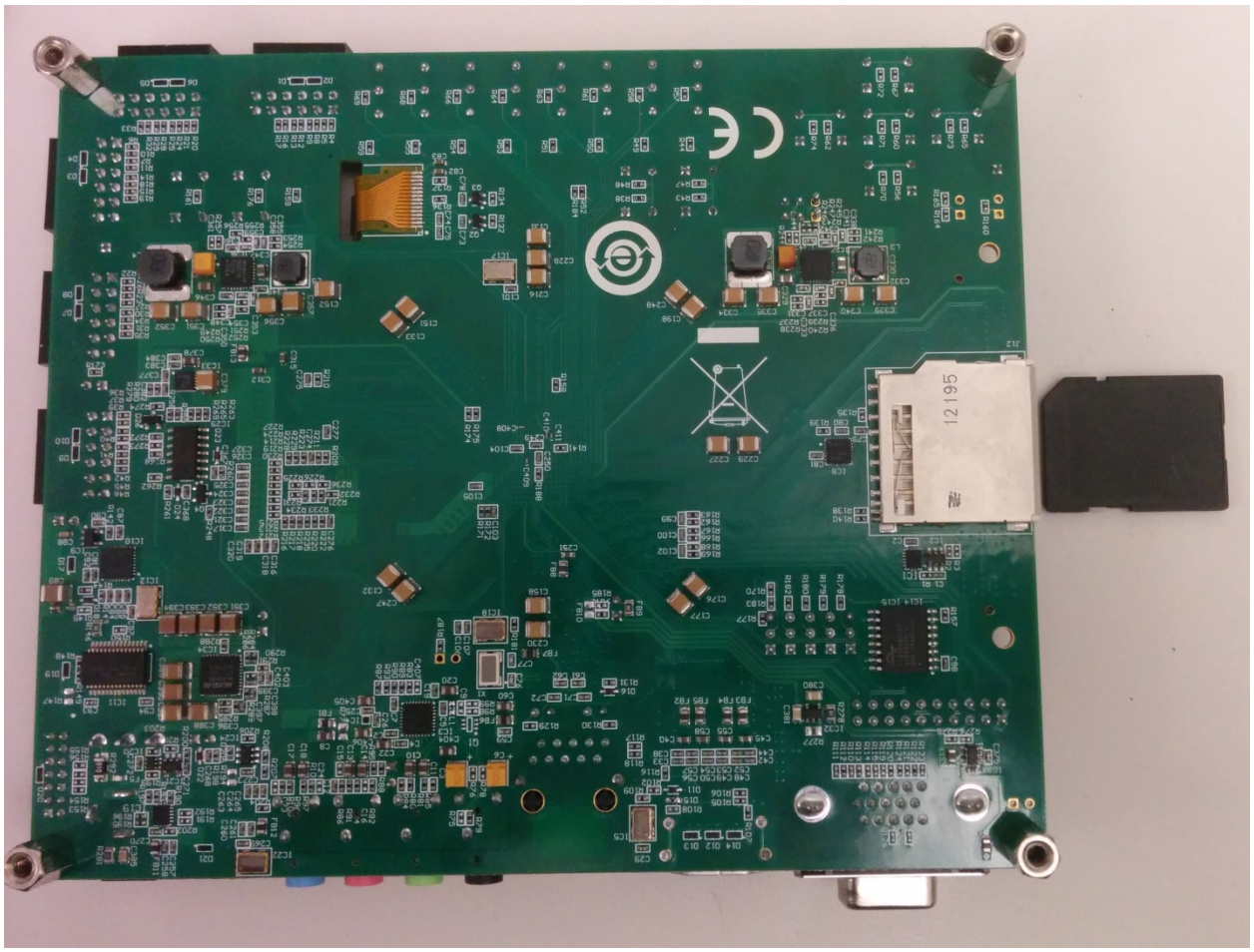
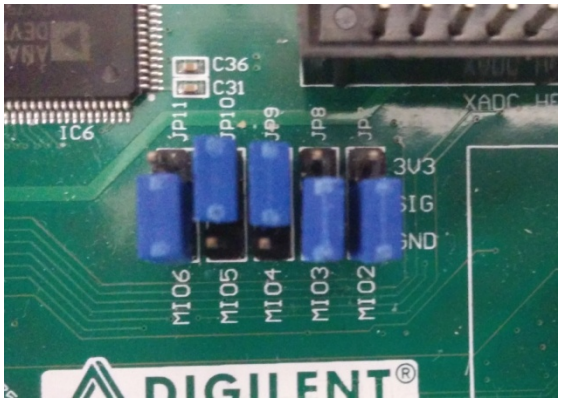


Figure 2. ZedBoard SD Card Slot



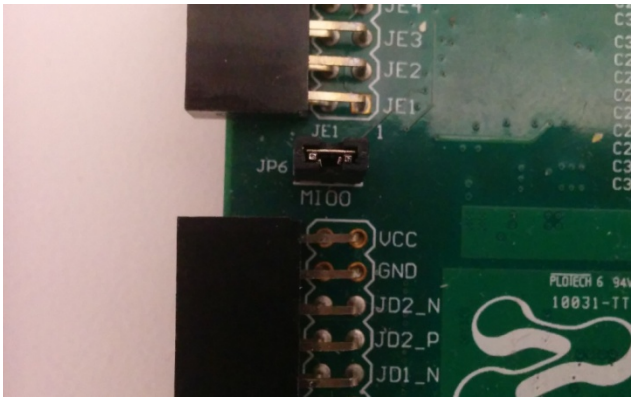


Figure 3 and Figure 4. ZedBoard Boot from SD Jumper Settings

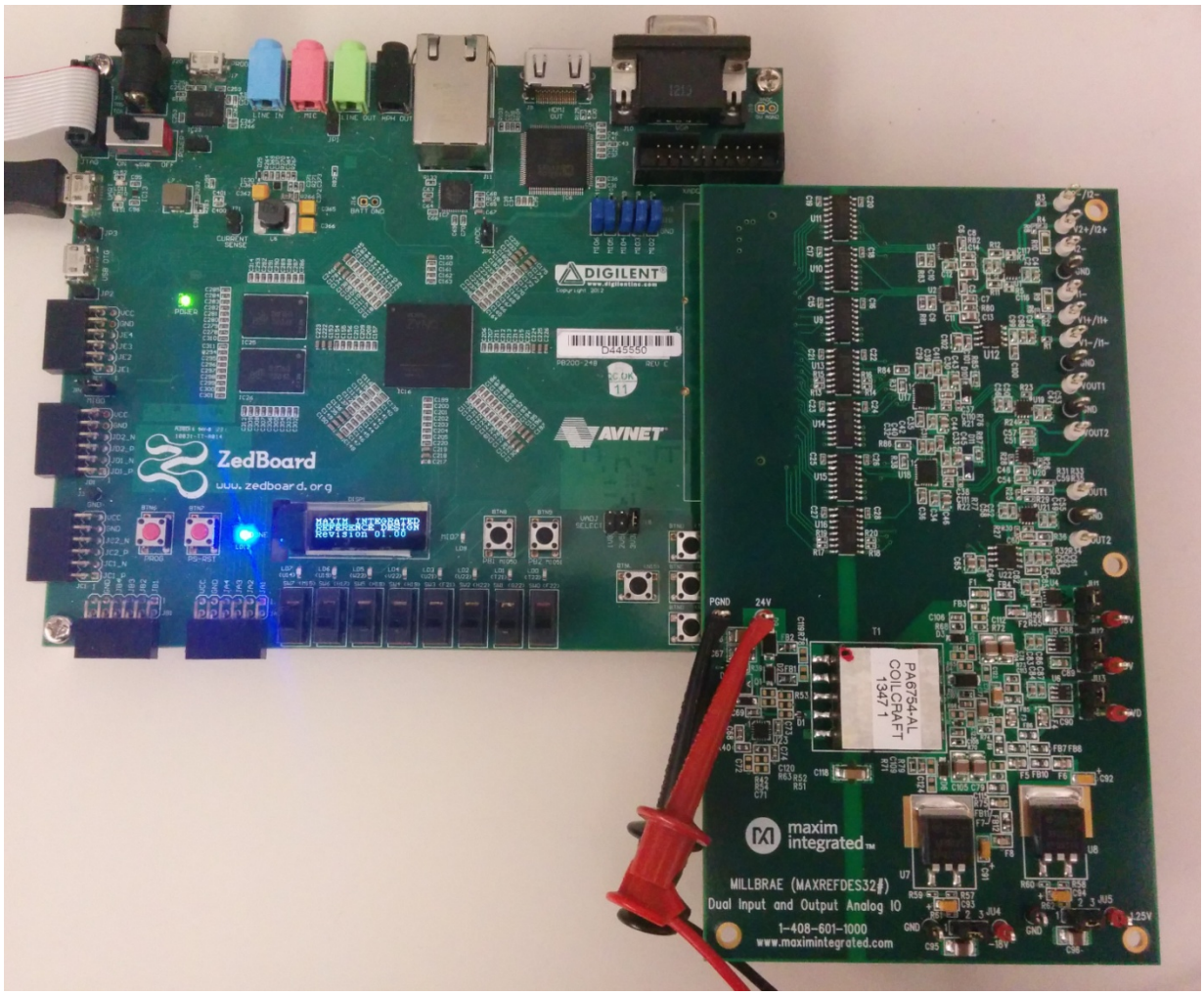


Figure 5. MAXREFDES32# Board Connected to ZedBoard Kit

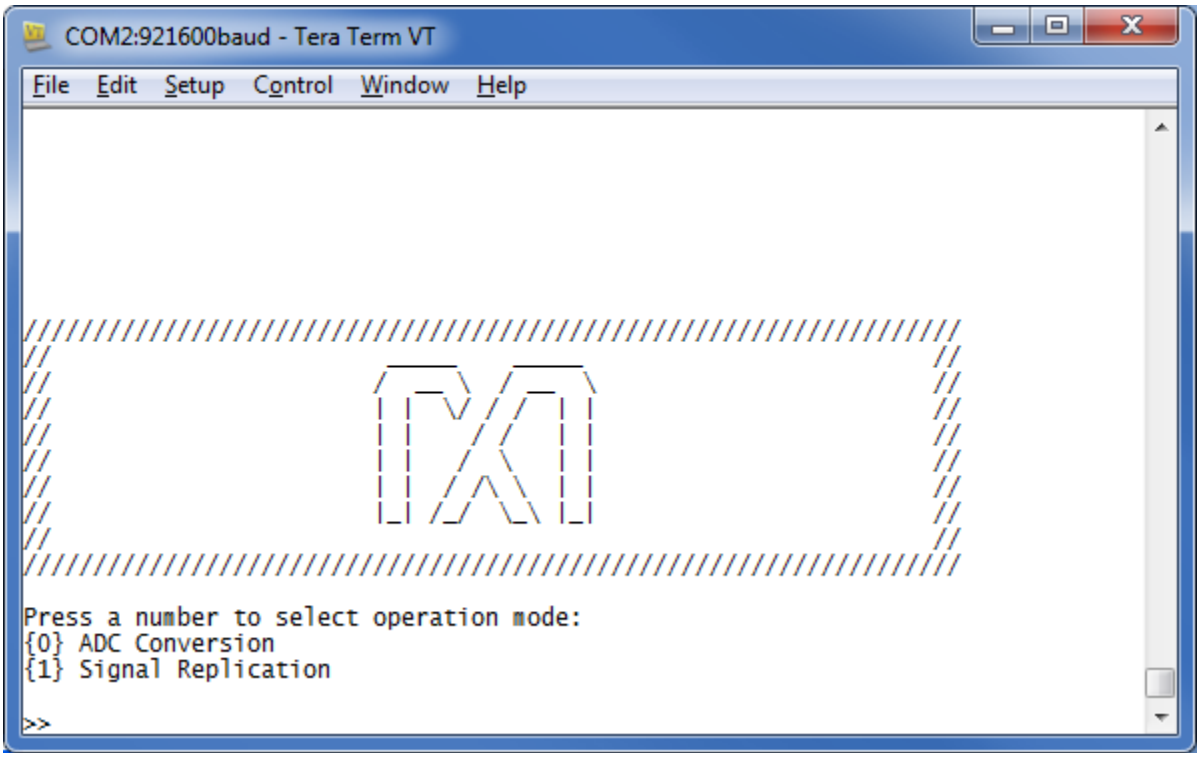


Figure 6. MAXREFDES32 Main Menu

4. Download Demonstration from Xilinx SDK

Below is a high-level overview of the steps required to quickly get the MAXREFDES32# design running by downloading and running the FPGA project. Detailed instructions for each step are provided in the following pages.

1) Connect the MAXREFDES32# board to the J1 FMC connector of a ZedBoard as shown in Figure 5.
2) Download the latest **RD32V01_00.ZIP** file located at the MAXREFDES32# page.
3) Extract the **RD32V01_00.ZIP** file to a directory on your PC.
4) Open the Xilinx SDK.
5) Download the bitstream (.BIT) file to the board. This bitstream contains the FPGA hardware design and software bootloader.
6) Use Xilinx SDK to download and run the executable file (.ELF) on one of the two ARM® Cortex™-A9 processors.

5. Included Files

The top level of the hardware design is a Xilinx PlanAhead Project (.PRR) for Xilinx PlanAhead version 14.2. The Verilog-based arm_system_stub.v module provides FPGA/board net connectivity, and instantiates the wrapper that carries both the Zynq® Processing System and AXI_MILLBRAE custom IP core that interface to the FMC connector. This is supplied as a Xilinx software development kit (SDK) project that includes a demonstration software application to evaluate the MAXREFDES32# subsystem reference design. The lower level c-code driver routines are portable to the user's own software project.

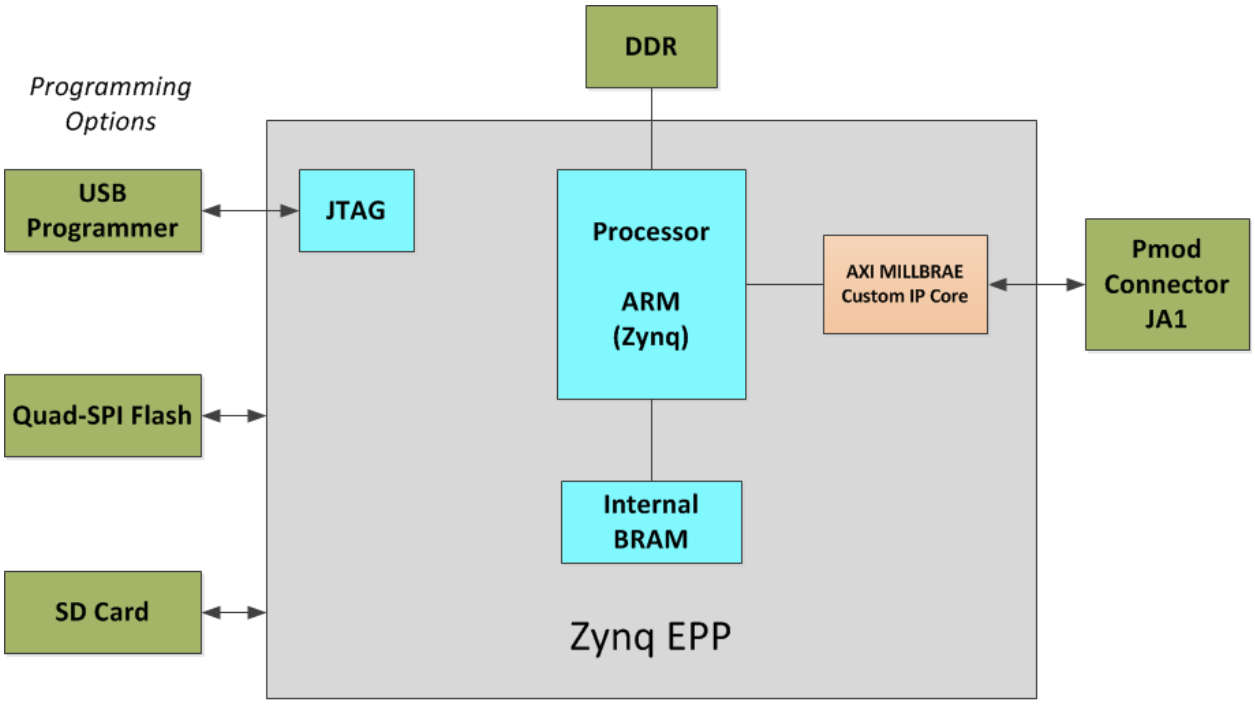


Figure 7. Block Diagram of FPGA Hardware Design

6. Procedure

1. Install a 2-pin header on the J18 connector on the ZedBoard if the 3V3 header is missing.
2. Configure the ZedBoard boot source jumpers as shown in Figure 8, and remove the shunt on JP6.

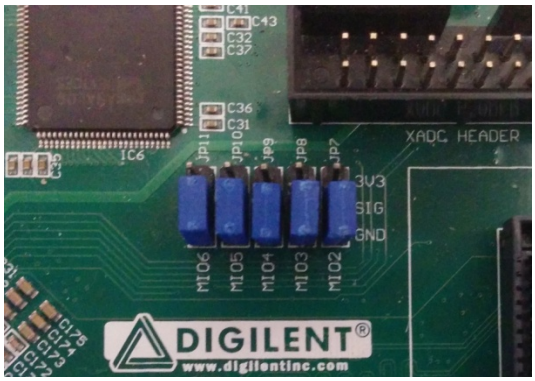


Figure 8. JTAG Mode Jumper Settings

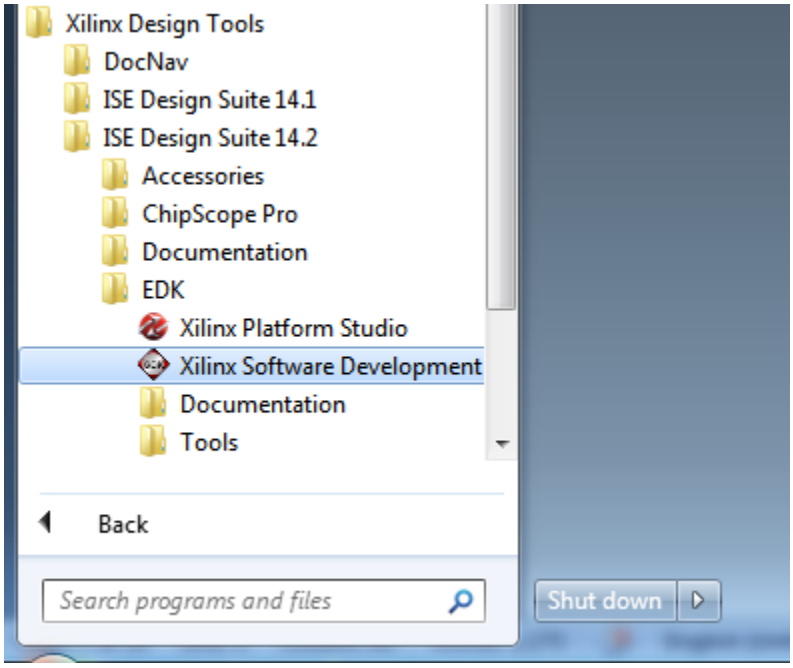
3. Remove any shunt on 1V8 and 2V5 headers, and install a shunt on the 3V3 header.
4. Connect the MAXREFDES32# board to the J1 FMC connector of the ZedBoard as shown in Figure 5.
5. Power up the ZedBoard by sliding the SW8 switch on the ZedBoard to the ON position.
6. Download the latest **RD32V01_00.ZIP** file at **www.maximintegrated.com/AN5883**. All files available for download are available at the bottom of the page.
7. Extract the **RD32V01_00.ZIP** file to a directory on your PC. The location is arbitrary but the maximum path length limitation in Windows (260 characters) should not be exceeded.

   In addition, the Xilinx tools require the path to not contain any spaces.

   C:\Do Not Use Spaces In The Path\RD32V01_00.ZIP (This path has spaces.)

   For the purposes of this document, it will be **C:\designs\maxim\RD32V01_00**. See **Appendix A: Project Structure and Key Filenames** in this document for the project structure and key filenames.

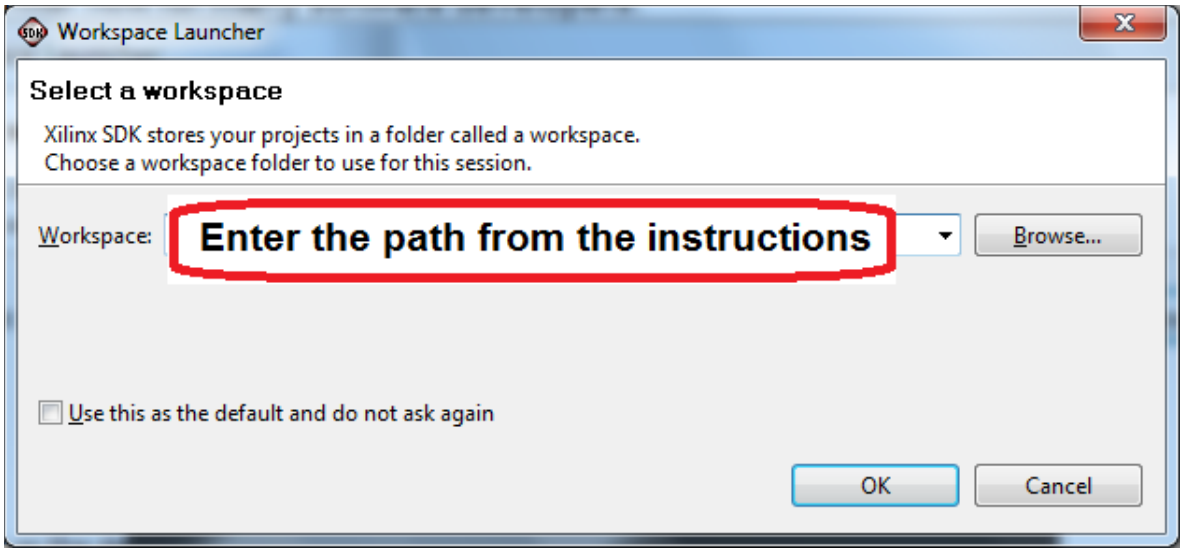
8. Open the **Xilinx Software Development Kit (SDK)** from the Windows **Start** menu.



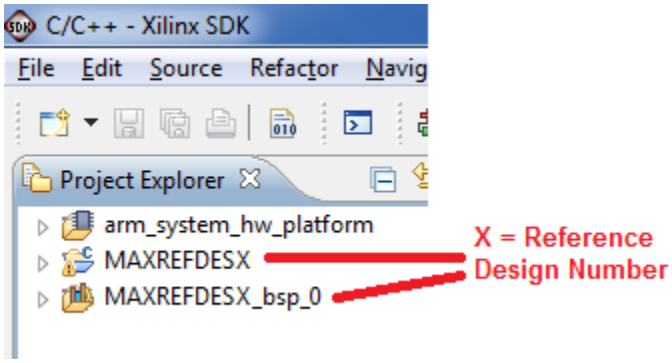
9. SDK will prompt for a workspace directory, which is the location where the software project is located. For this example, it is:

C:\designs\maxim\RD32V01_00\RD32_ZED_V01_00\Design_Files\top.sdk\SDK\SDK_Export

Click **OK** and SDK will open. The Xilinx SDK is based on an Eclipse™-based IDE, so it will be a familiar flow for many software developers.



10. Review the SDK IDE. The **Project Explorer** in the upper left tab should have three components as shown in the image below. If all three subfolders are present, you can skip the next step.

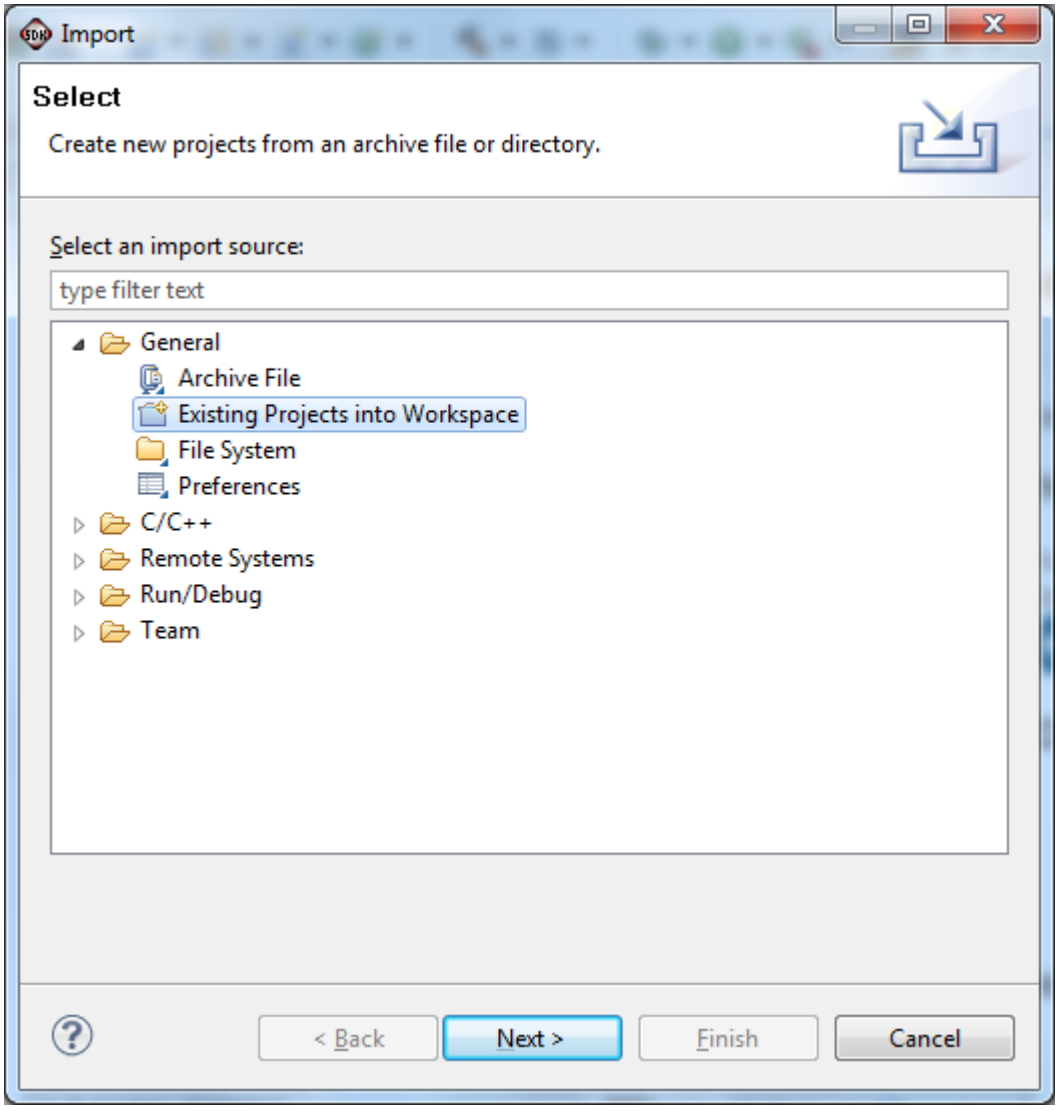


11. If the **Project Explorer** does not contain these three subfolders, launch the **File | Import** menu, expand the **General** folder, and select **Existing Projects into Workspace**. Click **Next**. Set the root directory to:

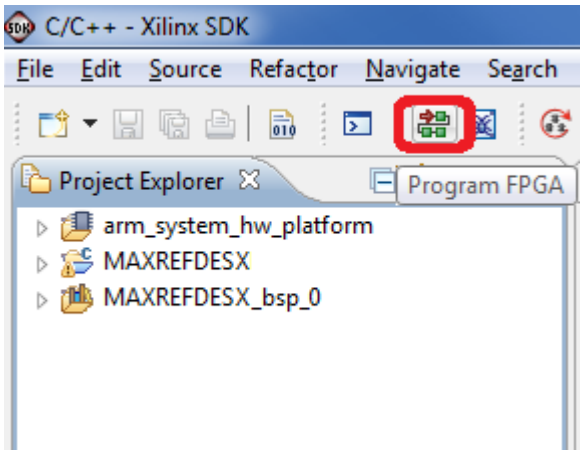
    C:\designs\maxim\RD32V01_00\RD32_ZED_V01_00\Design_Files\top.sdk\SDK\SDK_Export

    and the missing projects should appear in SDK **Project Explorer** with their checkboxes checked.

    Click **Finish** to import the projects.



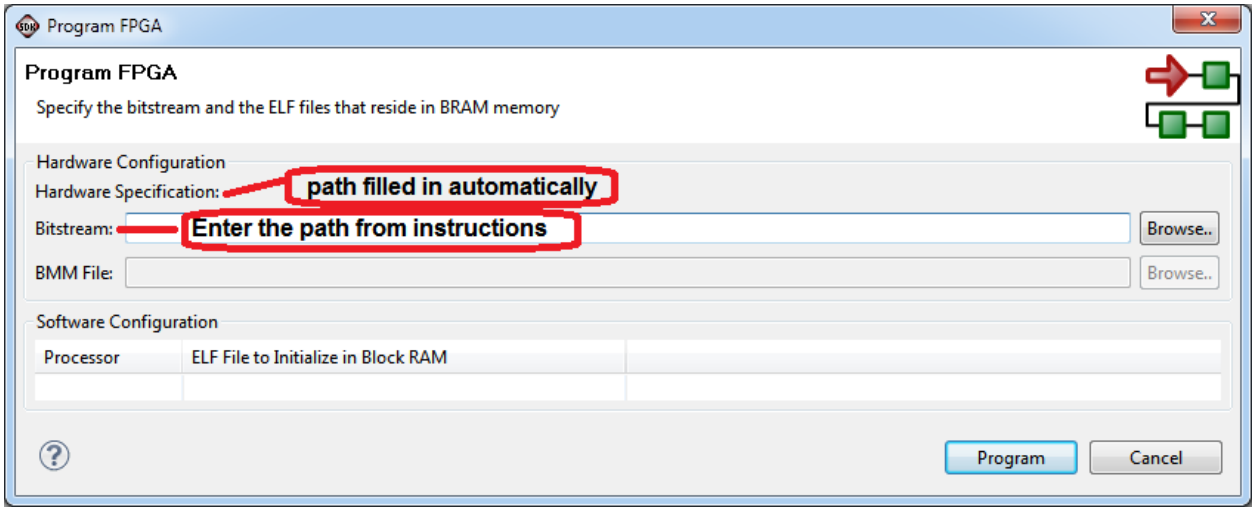
12. To download the bitstream (.BIT) file to the board, click on the **Program FPGA** icon (which looks like a green chain of devices).



The **Program FPGA** dialog box appears. From here, an FPGA bitstream (.BIT) file is selected. Be sure to select the .BIT file by using the paths below.

Bitstream:
C:\designs\maxim\RD32V01_00\RD32_ZED_V01_00\Design_Files\top.sdk\SDK\SDK_Export\arm_system_hw_platform

Press **Program**.



It takes approximately 10 seconds to download the FPGA, then a message box indicating **FPGA configuration complete** appears.

13. Setup of the terminal program to run on the PC using the following steps. Before loading the executable firmware file on the FPGA, the terminal program on the PC should be running. The example firmware running on the FPGA communicates with the PC via a USB port set up to emulate a serial port (UART). To establish this communication link, the PC must be configured with the appropriate Windows drivers. A suitable terminal program such as Tera Term or HyperTerminal should be invoked.

    The ZedBoard utilizes the Cypress USB-UART bridge IC. If the Windows cannot automatically install the driver for the Cypress USB-UART bridge IC, the driver is available for download from (http://www.cypress.com/?rID=63794). The driver is WHQL certified for the default Cypress VID / PID of 0x04B4 / 0x0008.

    Once installed, Windows will assign a previously unused COM port. Use the Windows **Control Panel | System | Device Manager** to determine the COM port number. (It will be named Cypress Serial.) Make a note of which COM port this is. That information is needed in the next step.

    Next, a terminal emulation program needs to be installed and launched. For Windows XP® and earlier systems, the HyperTerminal program is the usual choice. However, since HyperTerminal was eliminated from Windows 7, it may be necessary to locate an alternative. Several are available; one good choice is called Tera Term (http://ttssh2.sourceforge.jp/). Whatever terminal program you choose, the communication should be set up by opening the COM port number previously described above and the port configured as:

    bits per second: **115,200**;

    data bits: **8**;

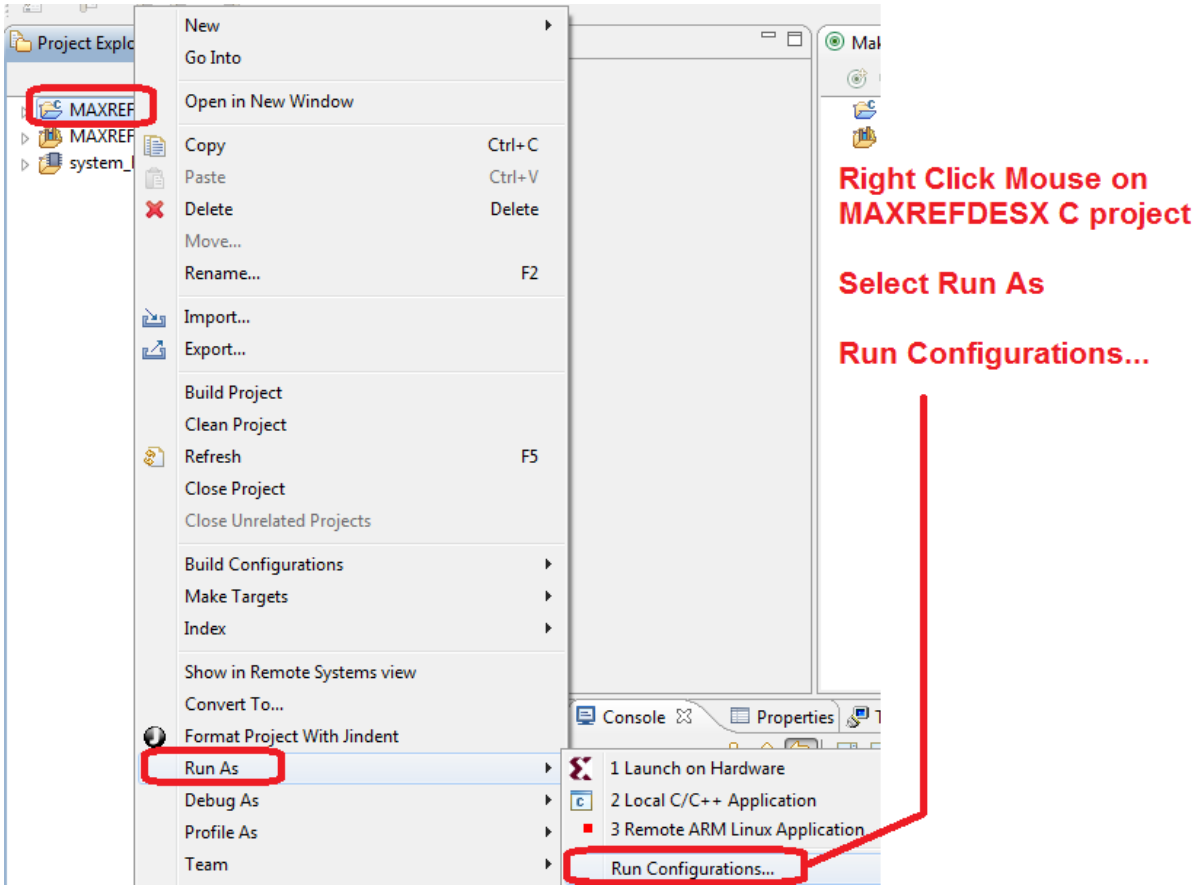
    parity: **none**;

    stop bits: **1**;

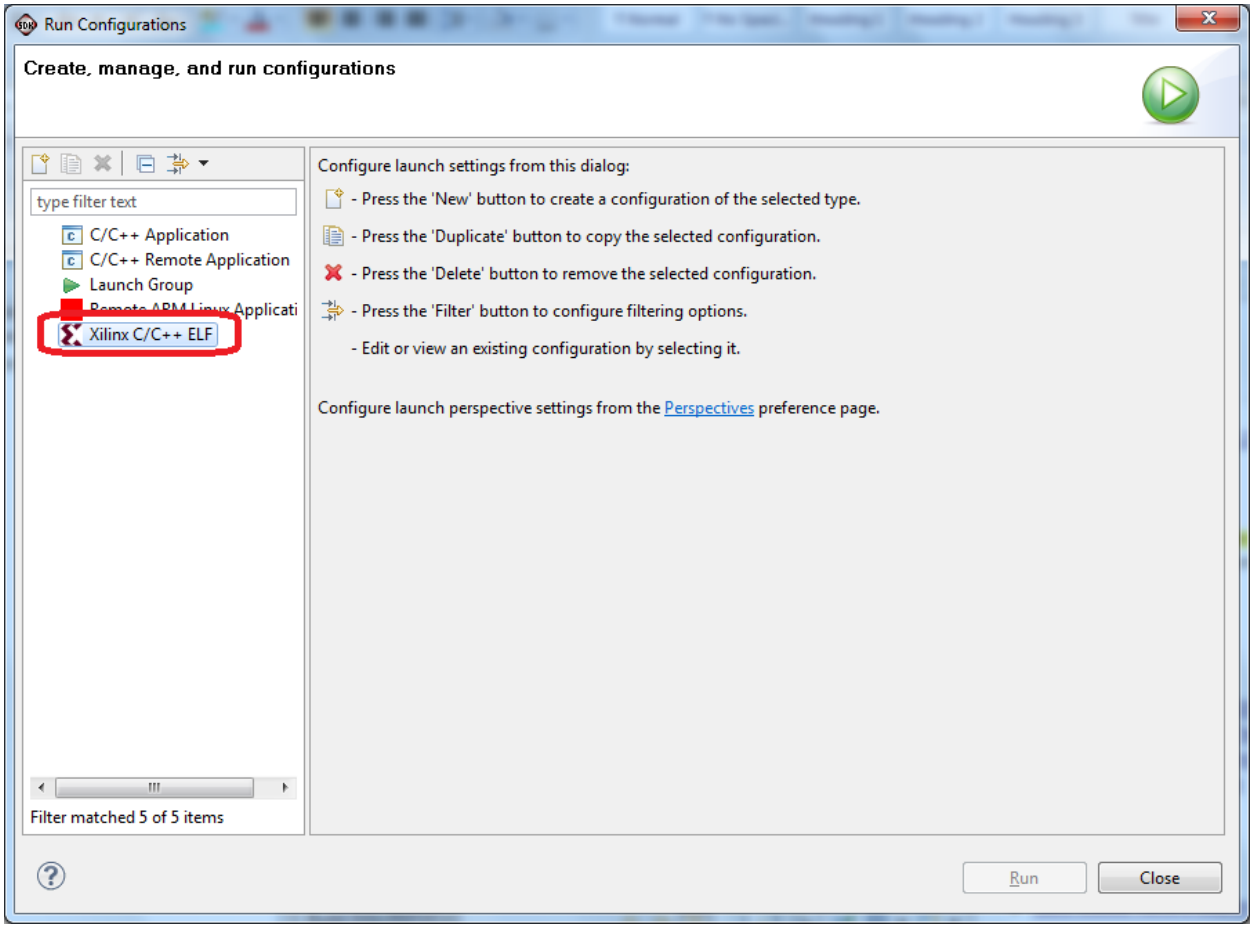
    flow control: **none**.

14. Use the Xilinx SDK to download and run the executable ELF (.ELF) file on the ARM Cortex-A9 processor using the following steps.

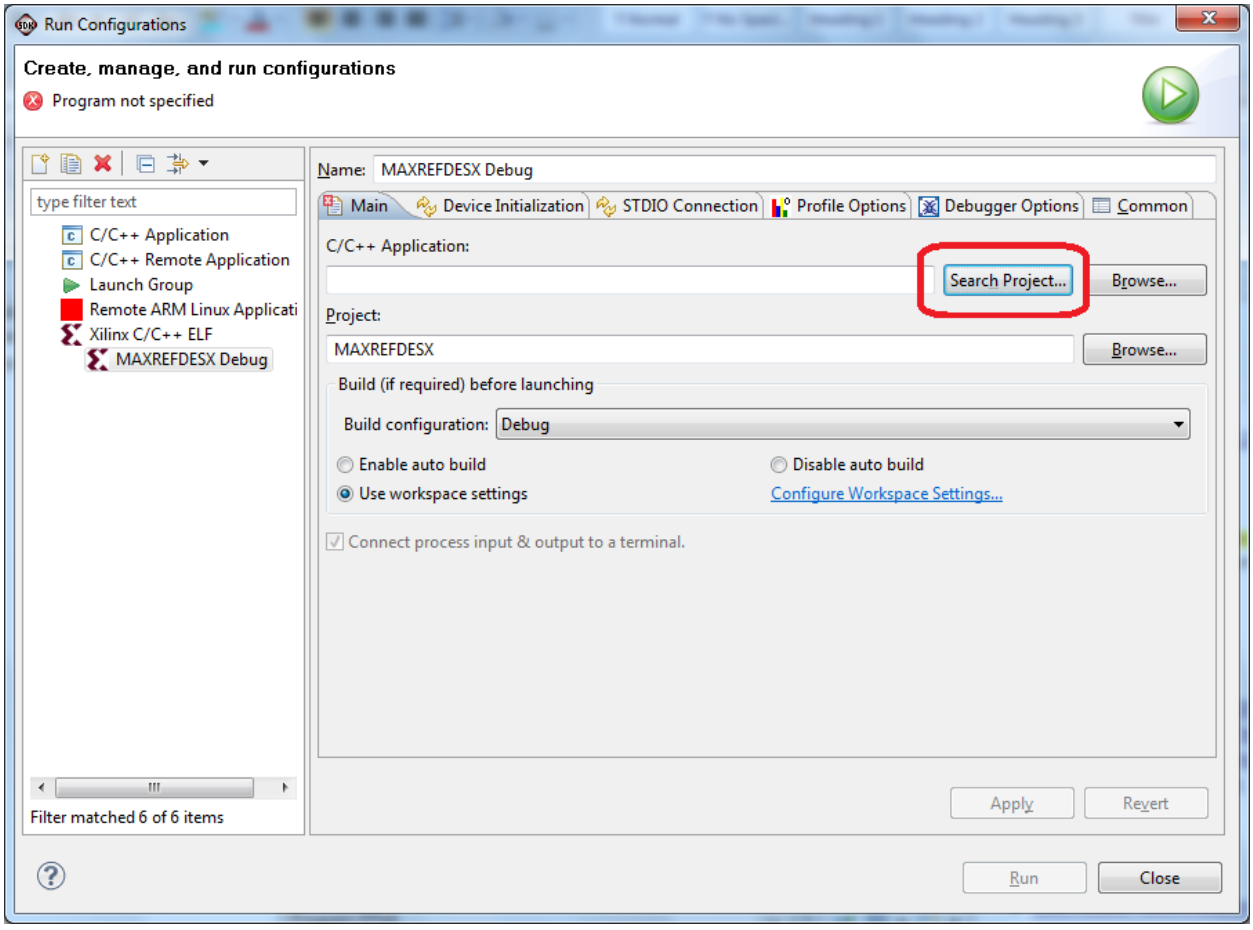
    Right-click the mouse while the **MAXREFDES32 C** project is selected, choose the **Run As** menu, and then **Run Configurations…** menu as shown below.



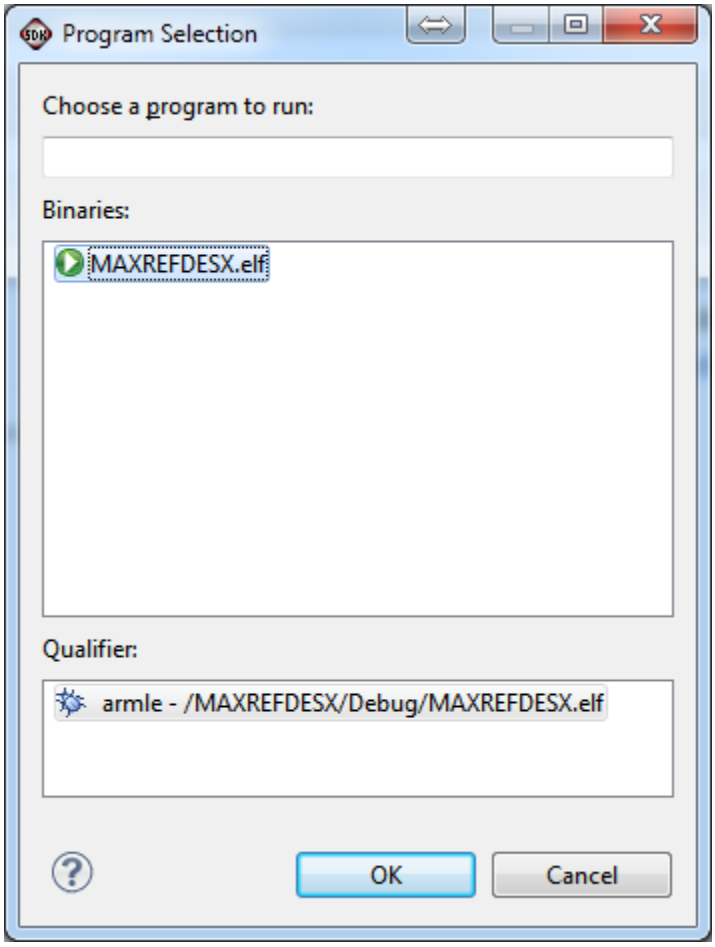
Next, double-click the mouse on the **Xilinx C/C++ ELF** menu.



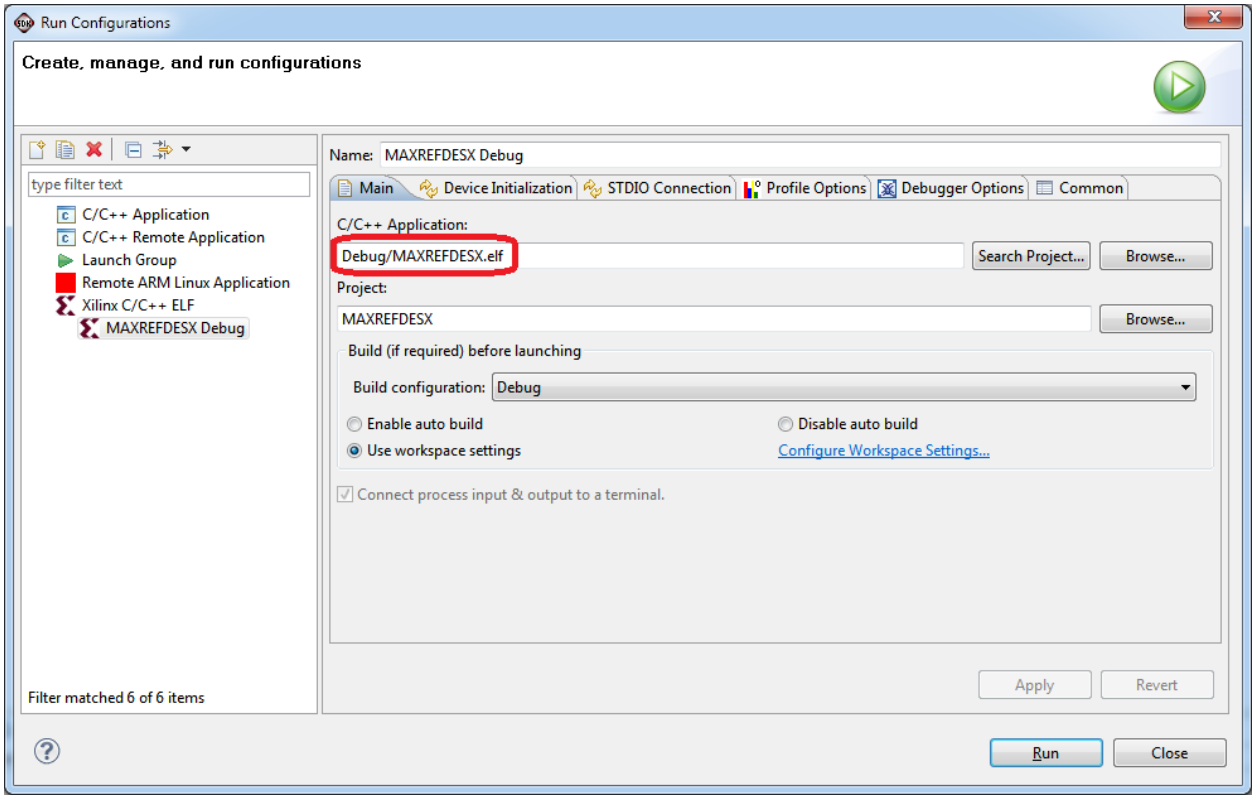
Next, press the **Search Project** button.



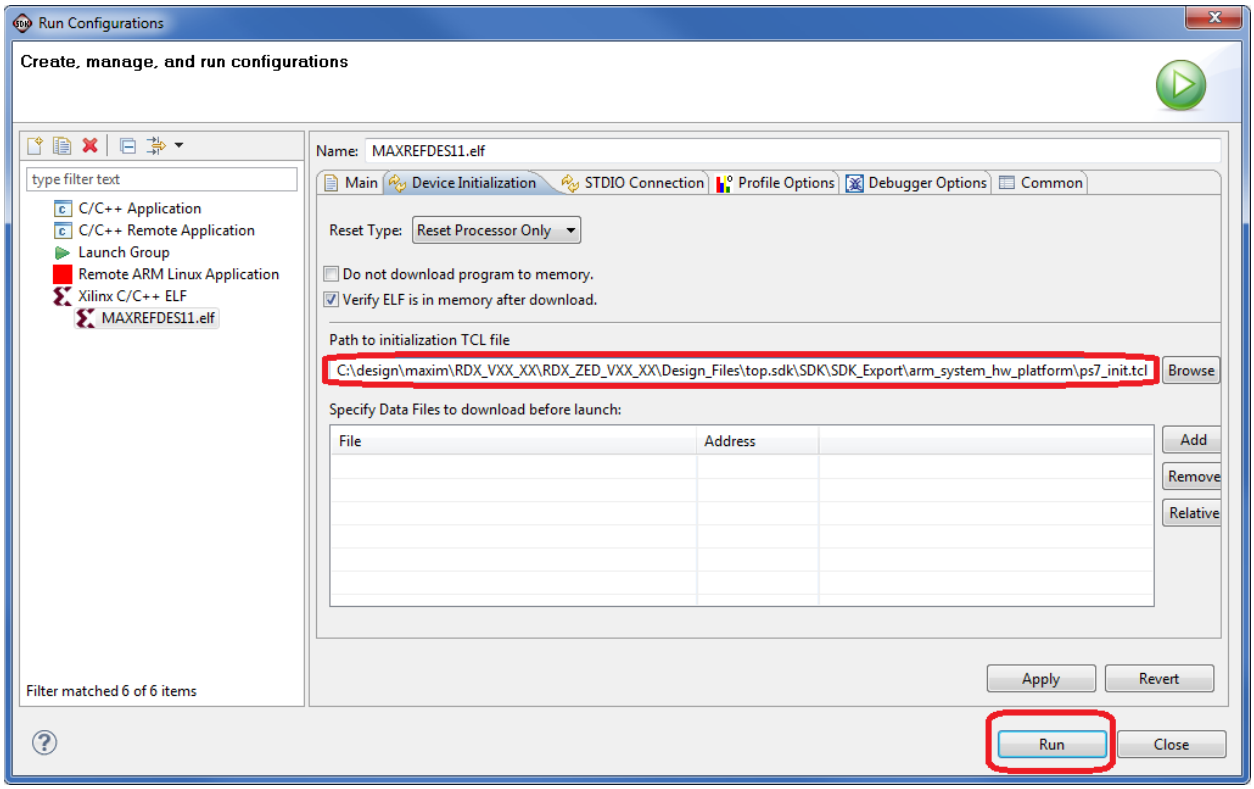
Double-click on the **MAXREFDES32.elf** binary.



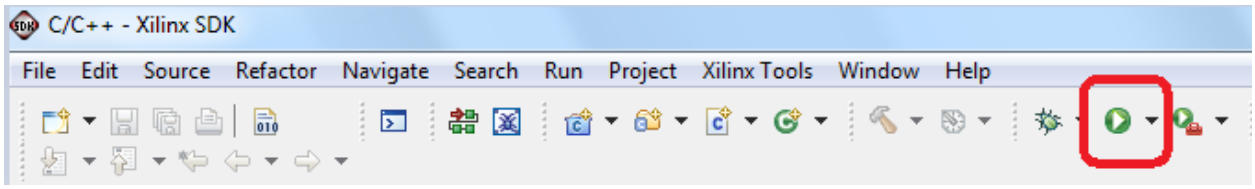
Verify the application is selected on the **Main** tab.



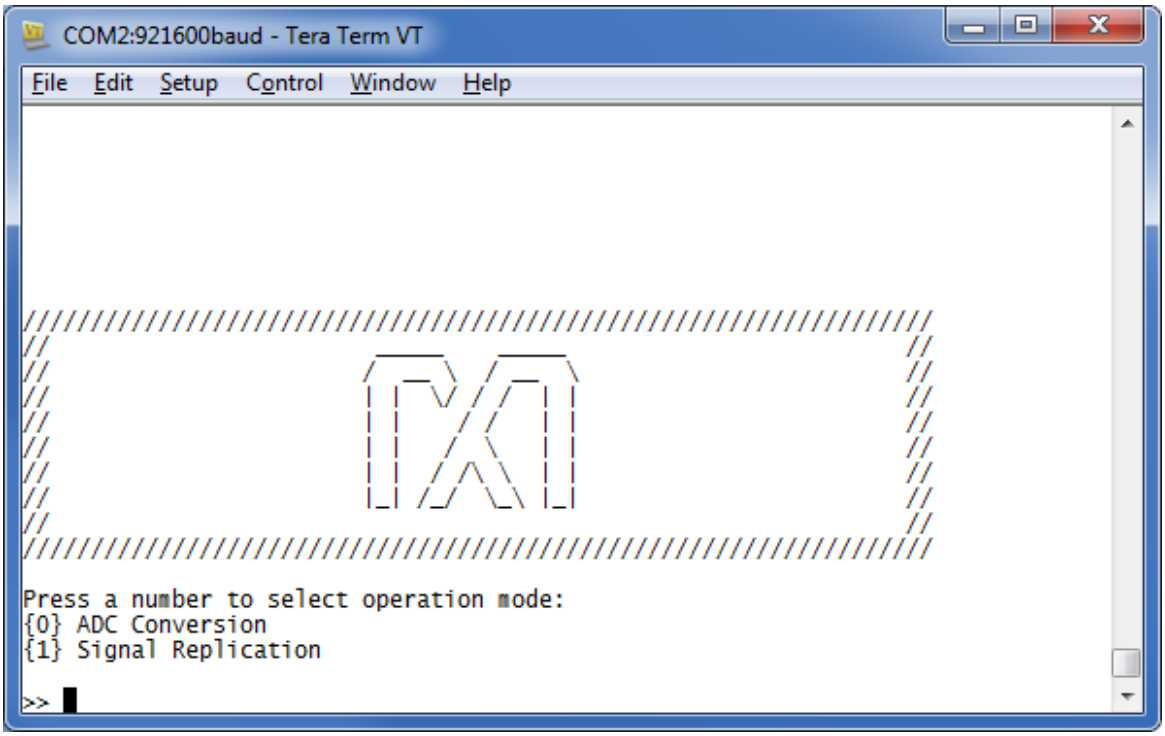
On the **Device Initialization** tab, click **Browse…** button to select the right initialization TCL file and press the **Run** button.



Once the Debug/MAXREFDES32 configuration is set up once, you just need to press the **Run** button if you ever want to run the program again.

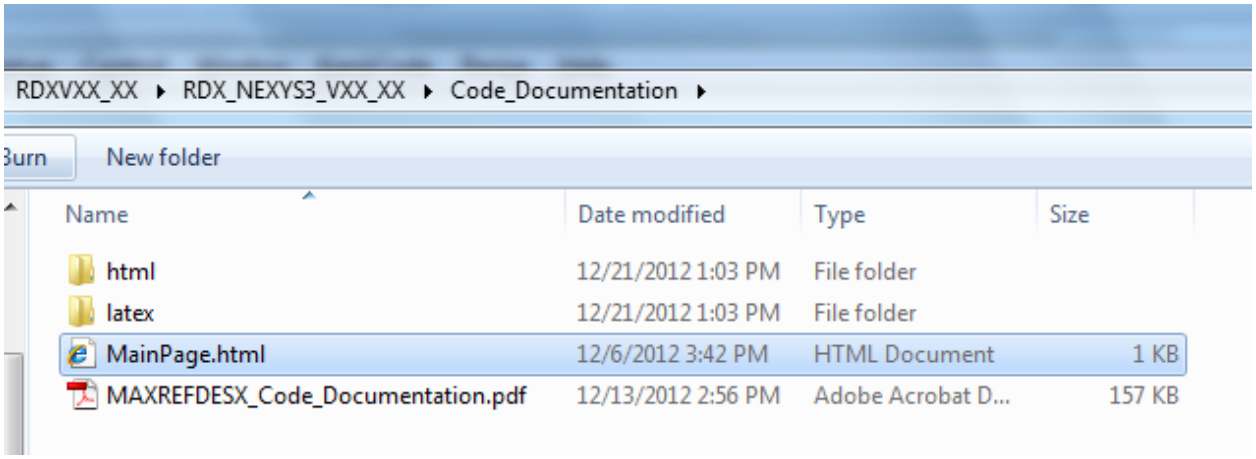


At this point, the application will be running on the Cortex-A9 and the terminal program should show the menu below. Make the desired selections by pressing the appropriate keys on the keyboard. For example, to select Signal Replication, press **1**.



7. Code Documentation

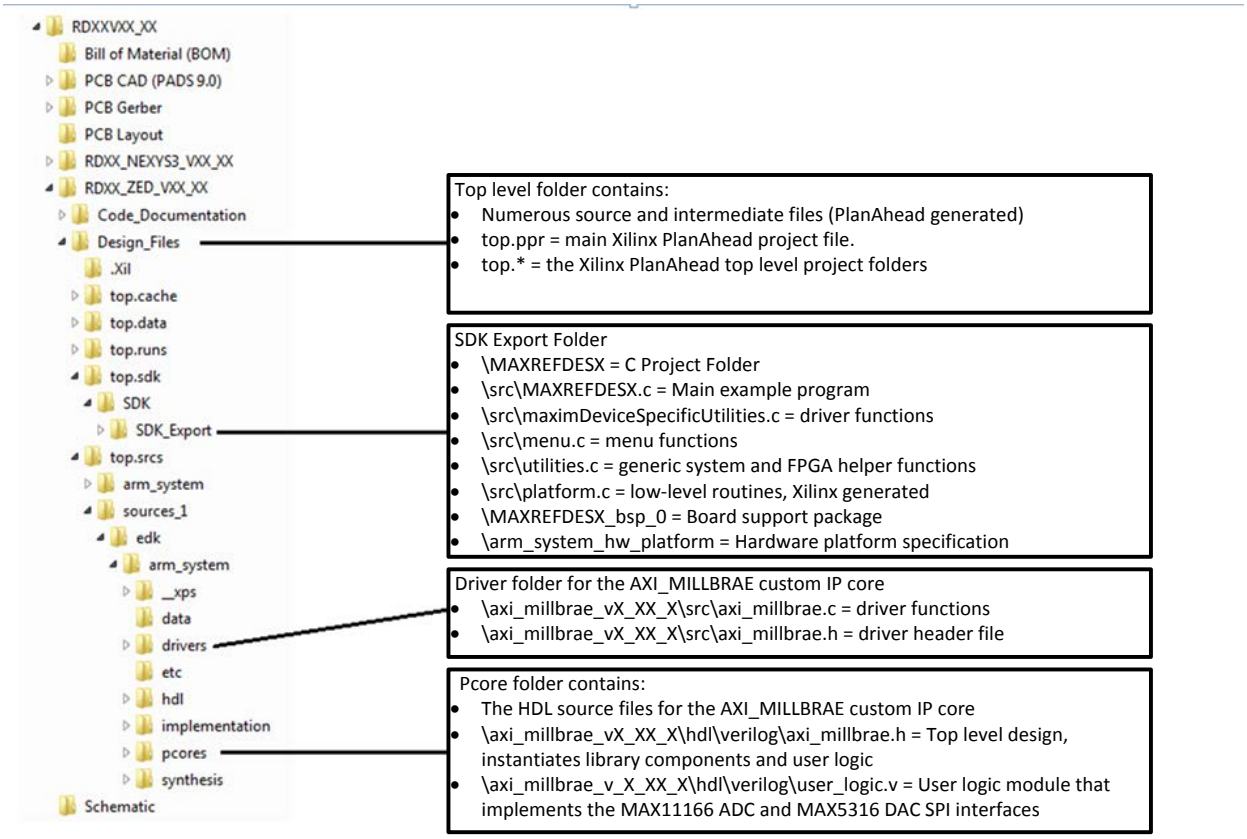
Code documentation can be found at:
C:\...\RD32V01_00\RD32_ZED_V01_00\Code_Documentation



To view the code documentation in HTML format with a browser, open the **MainPage.html** file.

To view the code documentation in .PDF format with a PDF reader, open the **MAXREFDES32_Code_Documentation.pdf** file.

8. Appendix A: Project Structure and Key Filenames



9. Trademarks

ARM is a registered trademark of ARM Ltd.
Cortex is a trademark of ARM Ltd.
Eclipse is a trademark of Eclipse Foundation, Inc.
FMC is a trademark of Digilent Inc.
PlanAhead is a trademark of Xilinx, Inc.
WebPACK is a trademark of Xilinx, Inc.
Windows is a registered trademark and registered service mark and Windows XP is a registered trademark of Microsoft Corporation.
Xilinx is a registered trademark and registered service mark of Xilinx, Inc.
ZedBoard is a trademark of ZedBoard.org.
Zynq is a registered trademark of Xilinx, Inc.

10. Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/14	Initial release	—