30µA I_Q, Dual, 2-Phase Synchronous Step-Down Controller

FEATURES

- **Wide Output Voltage Range: 0.8V ≤ V_{OUT} ≤ 10V**
- **Ultralow Operating I_Q: 30µA (One Channel On)**
- **Out-of-Phase Controllers Reduce Required Input Capacitance and Power Supply Induced Noise**
- **OPTI-LOOP® Compensation Minimizes C_{OUT}**
- **±1% Output Voltage Accuracy**
- **Wide V_{IN} Range: 4V to 36V Operation**
- **Phase-Lockable Fixed Frequency 140kHz to 650kHz**
- Selectable Continuous, Pulse Skipping or **Low Ripple** Burst Mode® Operation at Light Loads
- Dual N-Channel MOSFET Synchronous Drive
- Very Low Dropout Operation: 99% Duty Cycle
- Adjustable Output Voltage Soft-Start or Tracking
- Output Current Foldback Limiting
- Power Good Output Voltage Monitor
- Output Overvoltage Protection
- Low Shutdown I_Q: 4µA
- Internal LDO Powers Gate Drive from V_{IN} or V_{OUT}
- Small 5mm × 5mm QFN Package

APPLICATIONS

- Automotive Systems
- Battery-Operated Digital Devices
- Distributed DC Power Systems

DESCRIPTION

The LTC®3826 is a high performance dual step-down switching regulator controller that drives all N-channel synchronous power MOSFET stages. A constant frequency current mode architecture allows a phase-lockable frequency of up to 650kHz. Power loss and noise due to the ESR of the input capacitor are minimized by operating the two controller output stages out of phase.

The 30µA no-load quiescent current extends operating life in battery powered systems. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC3826 features a precision 0.8V reference and a power good output indicator. A wide 4V to 36V input supply range encompasses all battery chemistries.

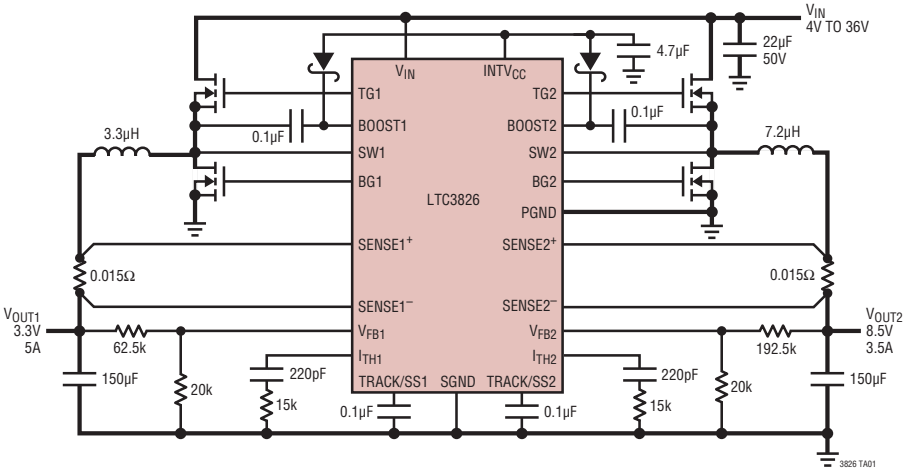
Independent TRACK/SS pins for each controller ramp the output voltage during start-up. Current foldback limits MOSFET heat dissipation during short-circuit conditions.

The PLLIN/MODE pin selects among Burst Mode operation, pulse skipping mode, or continuous inductor current mode at light loads. For a leaded package version (28-lead SSOP), see the LTC3826-1 data sheet.

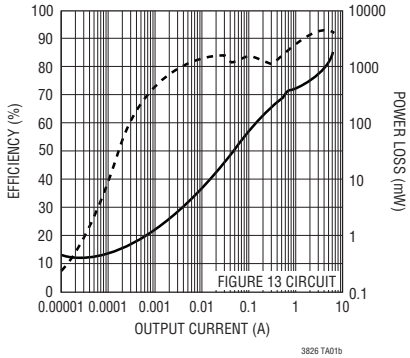
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Burst Mode and OPTI-LOOP are registered trademarks of Linear Technology Corporation.
All other trademarks are the property of their respective owners. Protected by U.S. Patents, including 5481178, 5929620, 6177787, 6144194, 5408150, 6580258, 6304066, 5705919.

TYPICAL APPLICATION

High Efficiency Dual 8.5V/3.3V Step-Down Converter



Efficiency and Power Loss vs Load Current

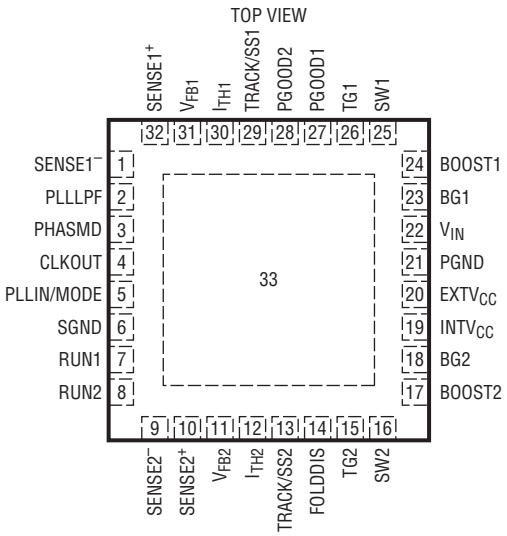


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Top Side Driver Voltages
(BOOST1, BOOST2) ..... 42V to –0.3V
Switch Voltage (SW1, SW2) ..... 36V to –5V
(BOOST1-SW1), (BOOST2-SW2) ..... 8.5V to –0.3V
RUN1, RUN2 ..... 7V to –0.3V
$SENSE1^+$, $SENSE2^+$, $SENSE1^–$,
$SENSE2^–$ Voltages ..... 11V to –0.3V
PLLIN/MODE, PLLLPF, Voltages ..... $INTV_{CC}$ to –0.3V
PHASMD, FOLDDIS, TRACK/SS1, TRACK/SS2
Voltages ..... $INTV_{CC}$ to –0.3V
$EXTV_{CC}$ ..... 10V to –0.3V
I_{TH1}, I_{TH2}, V_{FB1}, V_{FB2} Voltages ..... 2.7V to –0.3V
PGOOD1, PGOOD2 Voltages ..... 8.5V to –0.3V
Peak Output Current <10µs (TG1, TG2, BG1, BG2) 3A
Operating Temperature Range (Note 2).... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UH PACKAGE 32-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 33) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3826EUH#PBF	LTC3826EUH#TRPBF	3826	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LTC3826IUH#PBF	LTC3826IUH#TRPBF	3826	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3826EUH	LTC3826EUH#TR	3826	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LTC3826IUH	LTC3826IUH#TR	3826	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{RUN/SS1,2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
$V_{FB1,2}$	Regulated Feedback Voltage	(Note 4); $I_{TH1,2}$ Voltage = 1.2V	●	0.792	0.800	0.808	V
$I_{VFB1,2}$	Feedback Current	(Note 4)			–5	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 4V to 30V (Note 4)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔITH Voltage = 1.2V to 2V	 ● ●		 0.1 –0.1	 0.5 –0.5	 % %
$g_{m1,2}$	Transconductance Amplifier g_m	$I_{TH1,2}$ = 1.2V; Sink/Source 5mA (Note 4)			0.5		mmho
I_Q	Input DC Supply Current Sleep Mode (Channel 1 On) Sleep Mode (Channel 2 On) Shutdown Sleep Mode (Both Channels)	(Note 5) RUN1 = 5V, RUN2 = 0V, V_{FB1} = 0.83V (No Load) RUN1 = 0V, RUN2 = 5V, V_{FB2} = 0.83V (No Load) $V_{RUN1,2}$ = 0V RUN1,2 = 5V, V_{FB1} = V_{FB2} = 0.83V			 30 30 4 50	 50 50 10 75	 µA µA µA µA
UVLO	Undervoltage Lockout	V_{IN} Ramping Down	●		3.7	4	V
V_{OVL}	Feedback Overvoltage Lockout	Measured at $V_{FB1,2}$, Relative to Regulated $V_{FB1,2}$		8	10	12	%
I_{SENSE}	Sense Pins Total Source Current	(Each Channel) $V_{SENSE1-,2-}$ = $V_{SENSE1+,2+}$ = 0V			–220		µA
DF_{MAX}	Maximum Duty Factor	In Dropout		98	99.4		%
$I_{TRACK/SS1,2}$	Soft-Start Charge Current	$V_{TRACK1,2}$ = 0V		0.75	1	1.35	µA
$V_{RUN1,2}$ ON	RUN Pin ON Threshold	V_{RUN1}, V_{RUN2} Rising		0.5	0.7	0.9	V
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$V_{FB1,2}$ = 0.7V, $V_{SENSE1-,2-}$ = 3.3V	●	85	100	115	mV
TG1, 2 t_r TG1, 2 t_f	TG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 50 50	 90 90	 ns ns
BG1, 2 t_r BG1, 2 t_f	BG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 40 40	 90 80	 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			70		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			70		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			230		ns
$INTV_{CC}$ Linear Regulator							
$V_{INTVCCVIN}$	Internal V_{CC} Voltage	8.5V < V_{IN} < 30V, V_{EXTVCC} = 0V		5.0	5.25	5.5	V
V_{LDOVIN}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 0V			0.2	1.0	%
$V_{INTVCCEXT}$	Internal V_{CC} Voltage	V_{EXTVCC} = 8.5V		7.2	7.5	7.8	V
V_{LDOEXT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 8.5V			0.2	1.0	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.5	4.7		V
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				0.2		V
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	V_{PLLLPF} = Floating; PLLIN/MODE = DC Voltage		350	390	430	kHz
f_{LOW}	Lowest Frequency	V_{PLLLPF} = 0V; PLLIN/MODE = DC Voltage		220	250	280	kHz
f_{HIGH}	Highest Frequency	V_{PLLLPF} = $INTV_{CC}$; PLLIN/MODE = DC Voltage		475	530	585	kHz
$f_{SYNCMIN}$	Minimum Synchronizable Frequency	PLLIN/MODE = External Clock; V_{PLLLPF} = 0V			115	140	kHz
$f_{SYNCMAX}$	Maximum Synchronizable Frequency	PLLIN/MODE = External Clock; V_{PLLLPF} = 2V		650	800		kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{RUN/SS1, 2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PLLLPF}	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{PLLIN/MODE} < f_{OSC}$ $f_{PLLIN/MODE} > f_{OSC}$			 –5 5		 µA µA
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive		 –12 8	 –10 10	 –8 12	 % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3826E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3826I is guaranteed to meet performance specifications over the full –40°C to 85°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

$$T_J = T_A + (P_D \bullet 34\ °C/W)$$

Note 4: The LTC3826 is tested in a feedback loop that servos $V_{ITH1, 2}$ to a specified voltage and measures the resultant $V_{FB1, 2}$.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see minimum on-time considerations in the Applications Information section).

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency and Power Loss vs Output Current

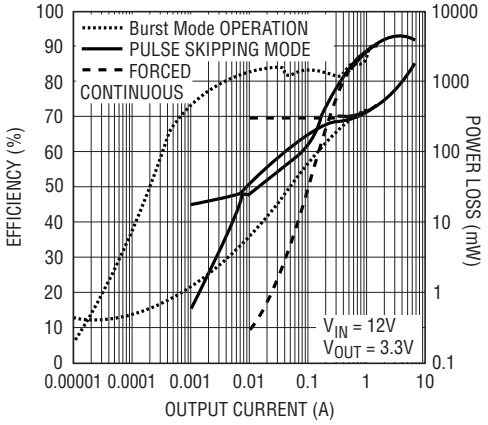


FIGURE 13 CIRCUIT

3826 G01

Efficiency vs Output Current

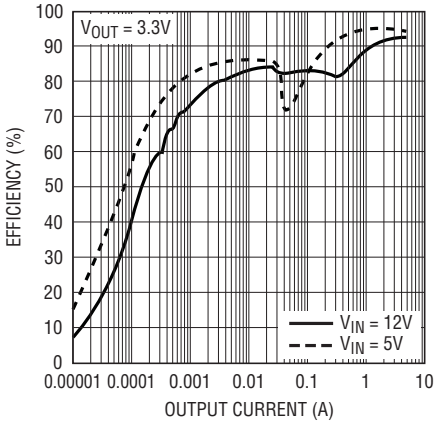


FIGURE 13 CIRCUIT

3826 G02

Efficiency vs Input Voltage

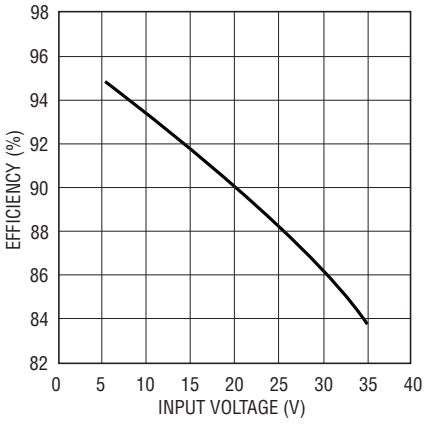
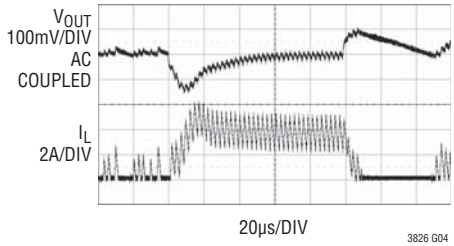


FIGURE 13 CIRCUIT

3826 G03

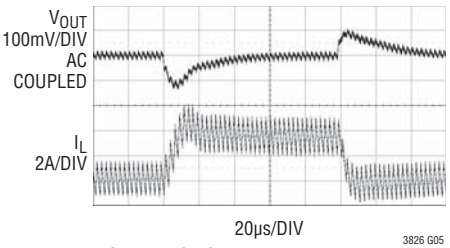
Load Step (Burst Mode Operation)



3826 G04

FIGURE 13 CIRCUIT
V_{OUT} = 3.3V

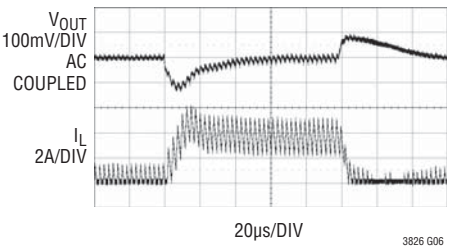
Load Step (Forced Continuous Mode)



3826 G05

FIGURE 13 CIRCUIT
V_{OUT} = 3.3V

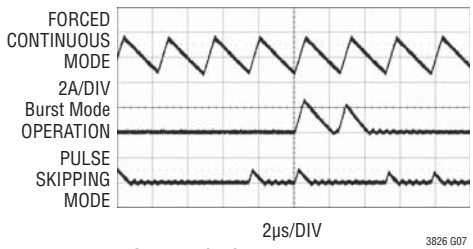
Load Step (Pulse Skipping Mode)



3826 G06

FIGURE 13 CIRCUIT
V_{OUT} = 3.3V

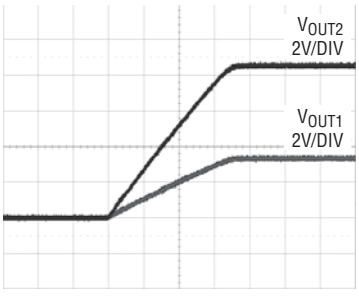
Inductor Current at Light Load



3826 G07

FIGURE 13 CIRCUIT
V_{OUT} = 3.3V
I_{LOAD} = 100µA

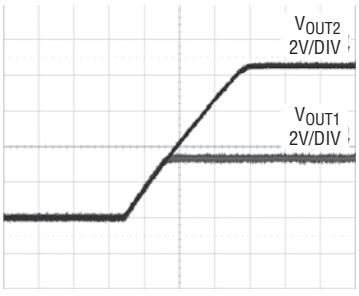
Soft-Start-Up



3826 G08

FIGURE 13 CIRCUIT

Tracking Start-Up

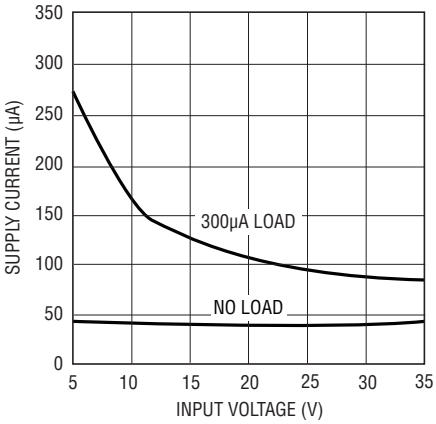


3826 G09

FIGURE 13 CIRCUIT

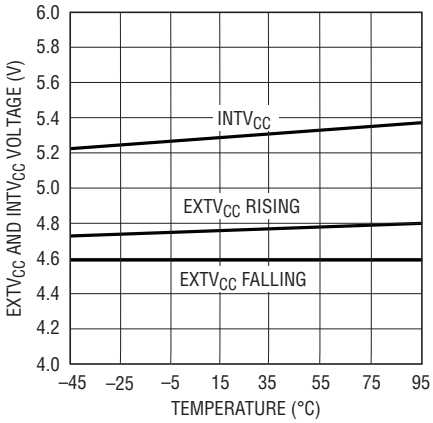
TYPICAL PERFORMANCE CHARACTERISTICS

Total Input Supply Current vs Input Voltage



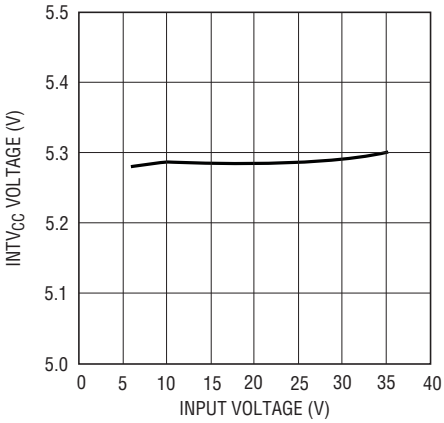
3826 G10

$EXTV_{CC}$ Switchover and $INTV_{CC}$ Voltages vs Temperature



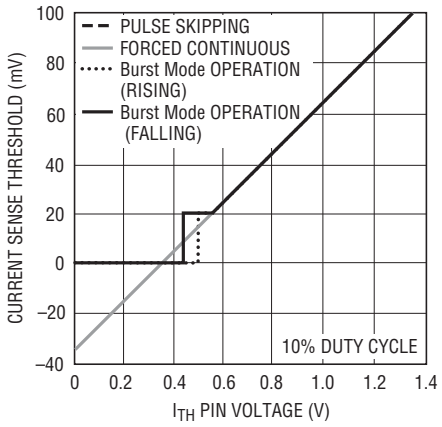
3826 G11

$INTV_{CC}$ Line Regulation



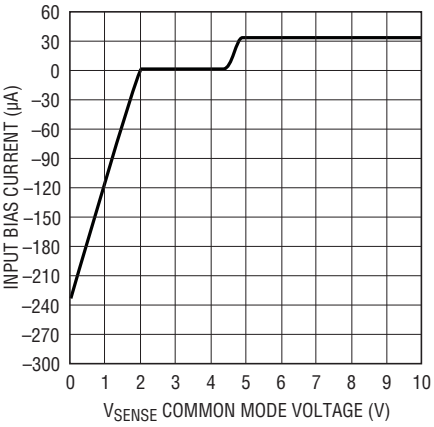
3826 G12

Maximum Current Sense Voltage vs I_{TH} Voltage



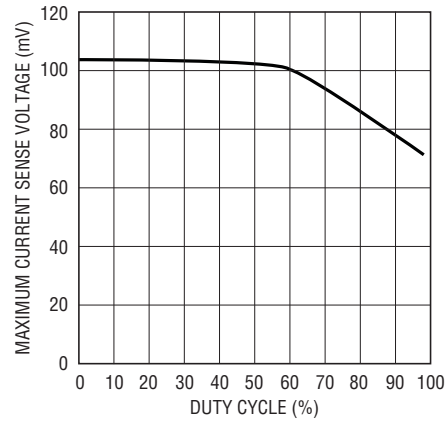
3826 G13

Sense Pins Total Input Bias Current



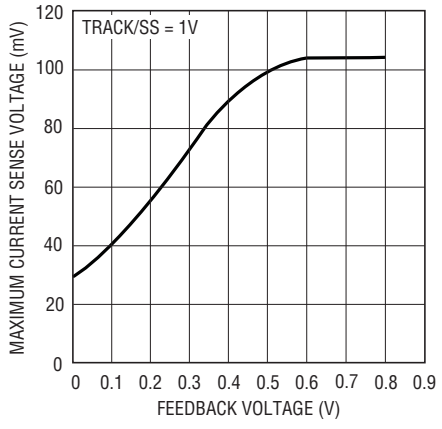
3826 G14

Maximum Current Sense Threshold vs Duty Cycle



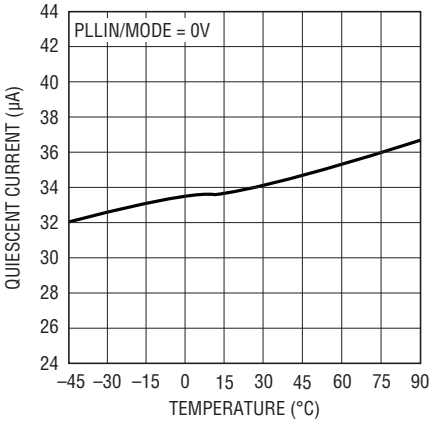
3826 G15

Foldback Current Limit



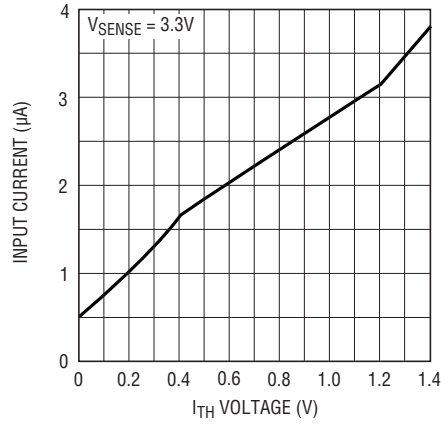
3826 G16

Quiescent Current vs Temperature



3826 G17

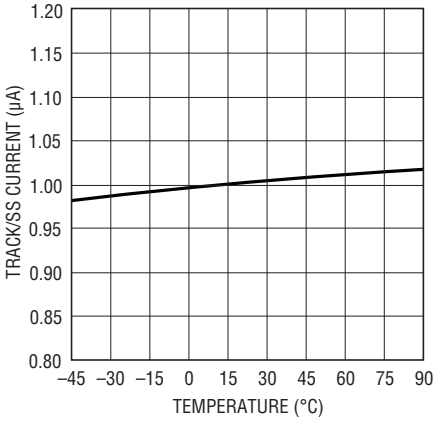
SENSE Pins Total Input Bias Current vs I_{TH}



3826 G18

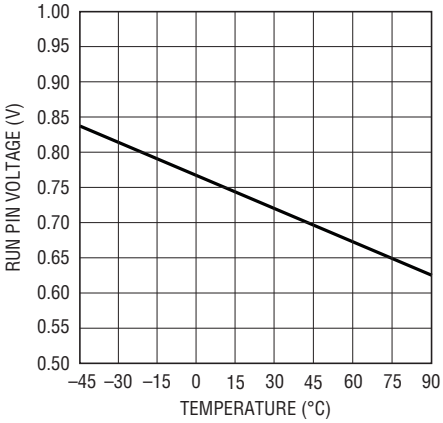
TYPICAL PERFORMANCE CHARACTERISTICS

TRACK/SS Pull-Up Current vs Temperature



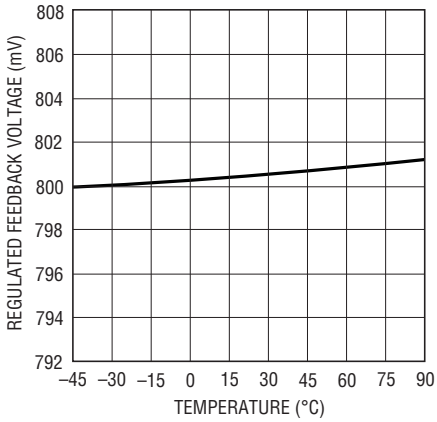
3826 G19

Shutdown (RUN) Threshold vs Temperature



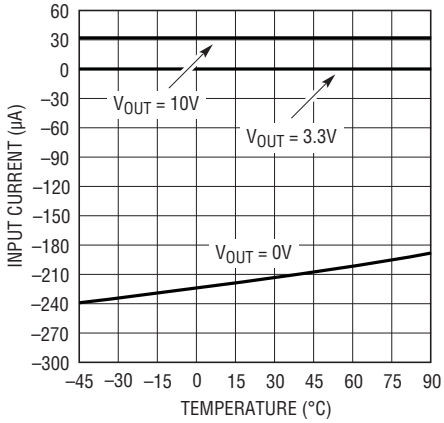
3826 G20

Regulated Feedback Voltage vs Temperature



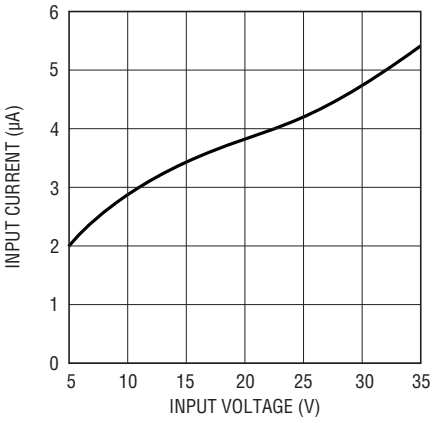
3826 G21

Sense Pins Total Input Bias Current vs Temperature



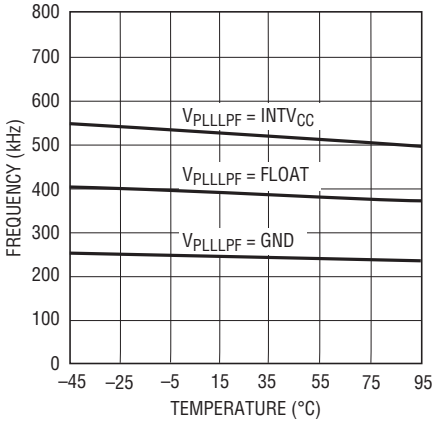
3826 G22

Shutdown Current vs Input Voltage



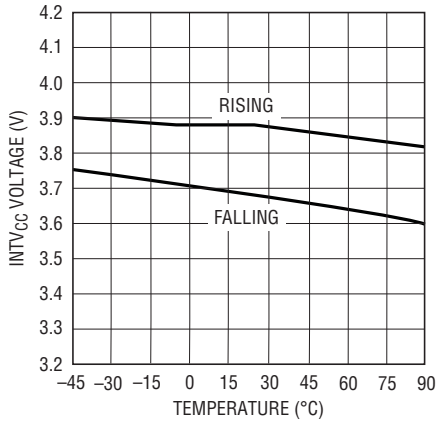
3826 G23

Oscillator Frequency vs Temperature



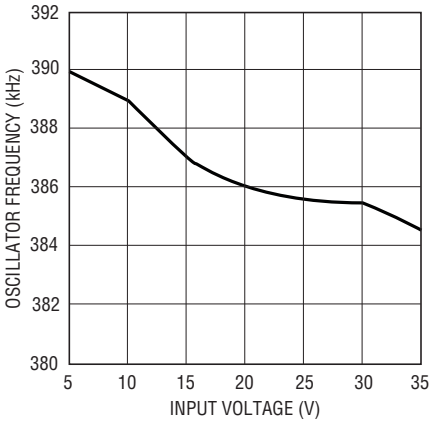
3827 G24

Undervoltage Lockout Threshold vs Temperature



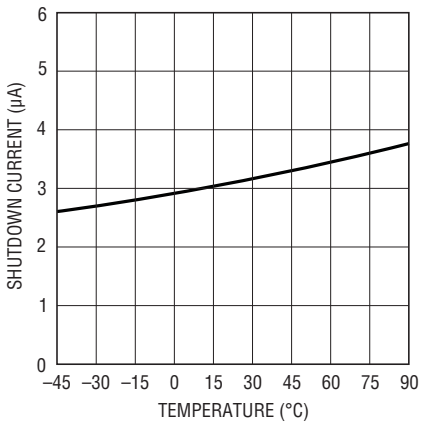
3826 G25

Oscillator Frequency vs Input Voltage



3826 G26

Shutdown Current vs Temperature



3826 G27

PIN FUNCTIONS

SENSE1⁻, SENSE2⁻ (Pins 1, 9): The (–) Input to the Differential Current Comparators.

PLLLPF (Pin 2): The phase-locked loop's lowpass filter is tied to this pin when synchronizing to an external clock. Alternatively, tie this pin to GND, $INTV_{CC}$ or leave floating to select 250kHz, 530kHz or 390kHz switching frequency.

PHASMD (Pin 3): Control Input to Phase Selector which determines the phase relationships between controller 1, controller 2 and the CLKOUT signal.

CLKOUT (Pin 4): Output Clock Signal available to daisy-chain other controller ICs for additional MOSFET driver stages/phases.

PLLIN/MODE (Pin 5): External Synchronization Input to Phase Detector and Forced Continuous Control Input. When an external clock is applied to this pin, the phase-locked loop will force the rising TG1 signal to be synchronized with the rising edge of the external clock. In this case, an R-C filter must be connected to the PLLLPF pin. When not synchronizing to an external clock, this input, which acts on both controllers, determines how the LTC3826 operates at light loads. Pulling this pin below 0.7V selects Burst Mode operation. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 0.9V and less than $INTV_{CC}$ –1.2V selects pulse skipping operation.

SGND (Pins 6, 33): Small Signal Ground common to both controllers, must be routed separately from high current grounds to the common (–) terminals of the C_{IN} capacitors. The Exposed Pad is SGND. It must be soldered to PCB ground for rated thermal performance.

RUN1, RUN2 (Pins 7, 8): Digital Run Control Inputs for Each Controller. Forcing either of these pins below 0.7V shuts down that controller. Forcing both of these pins below 0.7V shuts down the entire LTC3826, reducing quiescent current to approximately 4µA.

FOLDDIS (Pin 14): Foldback Current Disable Input Pin. Driving this pin high (to $INTV_{CC}$) disables foldback current limiting during short-circuit or overcurrent conditions.

$INTV_{CC}$ (Pin 19): Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be decoupled to power ground with a minimum of 4.7µF tantalum or other low ESR capacitor.

$EXTV_{CC}$ (Pin 20): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ Connection in the Applications Information section. Do not exceed 10V on this pin.

PGND (Pin 21): Driver Power Ground. Connects to the sources of bottom (synchronous) N-channel MOSFETs, anodes of the Schottky rectifiers and the (–) terminal(s) of C_{IN}.

V_{IN} (Pin 22): Main Supply Pin. A bypass capacitor should be tied between this pin and the signal ground pin.

BG1, BG2 (Pins 23, 18): High Current Gate Drives for Bottom (Synchronous) N-Channel MOSFETs. Voltage swing at these pins is from ground to $INTV_{CC}$.

BOOST1, BOOST2 (Pins 24, 17): Bootstrapped Supplies to the Top Side Floating Drivers. Capacitors are connected between the BOOST and SW pins and Schottky diodes are tied between the BOOST and $INTV_{CC}$ pins. Voltage swing at the BOOST pins is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

SW1, SW2 (Pins 25, 16): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

TG1, TG2 (Pins 26, 15): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ – 0.5V superimposed on the switch node voltage SW.

PGOOD1 (Pin 27): Open-Drain Logic Output. PGOOD1 is pulled to ground when the voltage on the V_{FB1} pin is not within ±10% of its set point.

PIN FUNCTIONS

PGOOD2 (Pin 28): Open-Drain Logic Output. PGOOD2 is pulled to ground when the voltage on V_{FB2} pin is not within ±10% of its set point.

TRACK/SS1, TRACK/SS2 (Pins 29, 13): External Tracking and Soft-Start Input. The LTC3826 regulates the $V_{FB1,2}$ voltage to the smaller of 0.8V or the voltage on the TRACK/SS1,2 pin. An internal 1µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to this pin allows the LTC3826 output to track the other supply during startup.

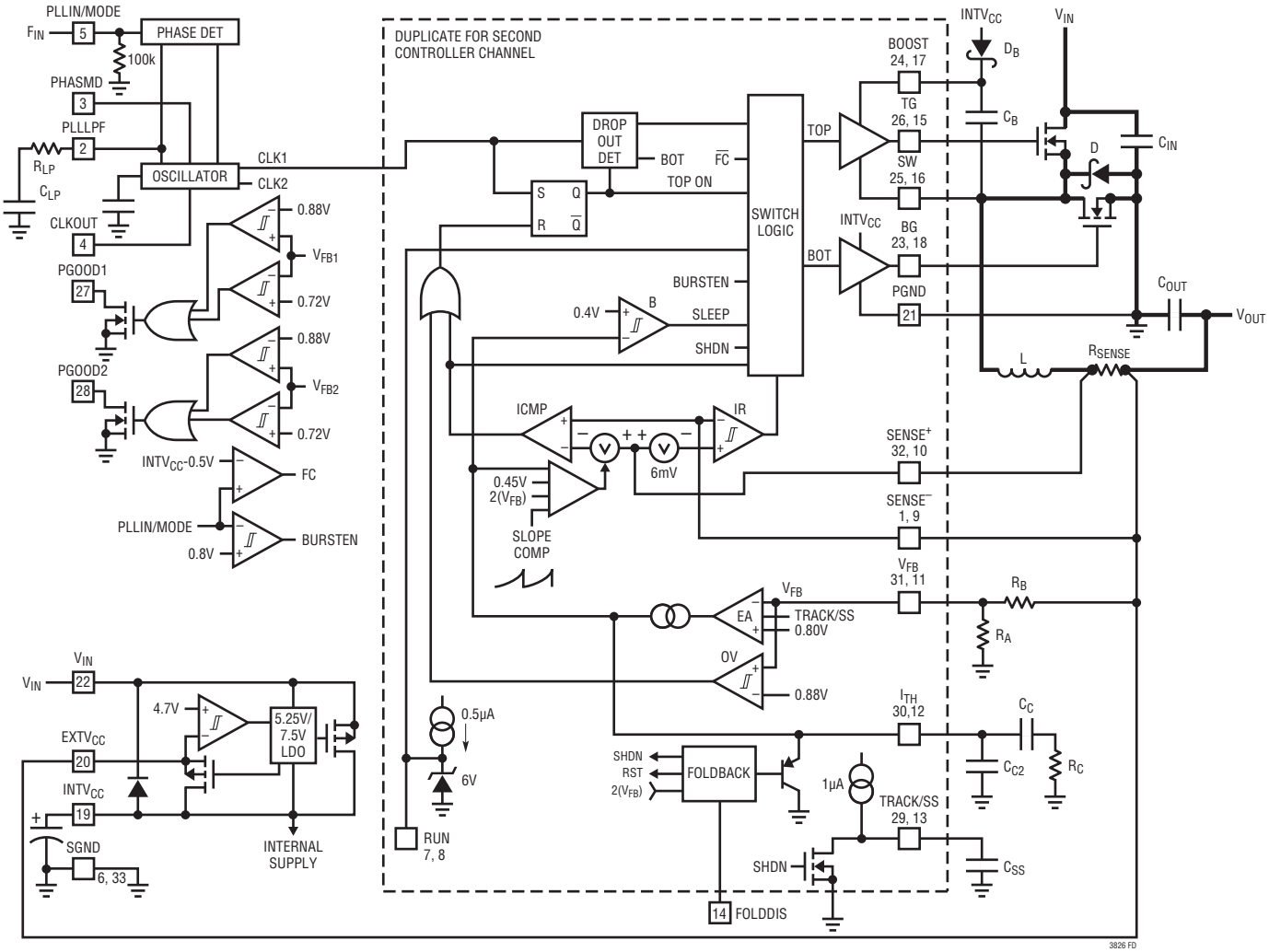
I_{TH1}, I_{TH2} (Pins 30, 12): Error Amplifier Outputs and Switching Regulator Compensation Points. Each associated channel's current comparator trip point increases with this control voltage.

V_{FB1}, V_{FB2} (Pins 31, 11): Receives the remotely sensed feedback voltage for each controller from an external resistive divider across the output.

SENSE1$^+$, SENSE2$^+$ (Pins 32, 10): The (+) Input to the Differential Current Comparators. The I_{TH} pin voltage and controlled offsets between the SENSE$^-$ and SENSE$^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

Exposed Pad (Pin 33): SGND. Must be soldered to the PCB.

BLOCK DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3826 uses a constant frequency, current mode step-down architecture with the two controller channels operating 180 degrees out of phase. During normal operation, each external top MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} trips and resets the latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin, (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 0.800V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the I_{TH} voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.7V, an internal 5.25V low dropout linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 4.7V, the 5.25V regulator is turned off and a 7.5V low dropout linear regulator is enabled that supplies $INTV_{CC}$ power from $EXTV_{CC}$. If $EXTV_{CC}$ is less than 7.5V (but greater than 4.7V), the 7.5V regulator is in dropout and $INTV_{CC}$ is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than 7.5V (up to an absolute maximum rating of 10V), $INTV_{CC}$ is regulated to 7.5V. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as one of the LTC3826 switching regulator outputs.

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one twelfth of the clock period every tenth cycle to allow C_B to recharge.

Shutdown and Start-Up (RUN1, RUN2 and TRACK/SS1, TRACK/SS2 Pins)

The two channels of the LTC3826 can be independently shut down using the RUN1 and RUN2 pins. Pulling either of these pins below 0.7V shuts down the main control loop for that controller. Pulling both pins low disables both controllers and most internal circuits, including the $INTV_{CC}$ regulator, and the LTC3826 draws only 4µA of quiescent current.

Releasing either RUN pin allows an internal 0.5µA current to pull up the pin and enable that controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the Absolute Maximum rating of 7V on this pin.

The start-up of each controller's output voltage V_{OUT} is controlled by the voltage on the TRACK/SS1 and TRACK/SS2 pin. When the voltage on the TRACK/SS pin is less than the 0.8V internal reference, the LTC3826 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 0.8V reference. This allows the TRACK/SS pin to be used to program a soft start by connecting an external capacitor from the TRACK/SS pin to SGND. An internal 1µA pull-up current charges this capacitor creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value.

Alternatively the TRACK/SS pin can be used to cause the start-up of V_{OUT} to "track" that of another supply. Typically, this requires connecting to the TRACK/SS pin an

OPERATION (Refer to Functional Diagram)

external resistor divider from the other supply to ground (see Applications Information section).

When the corresponding RUN pin is pulled low to disable a controller, or when V_{IN} drops below its undervoltage lockout threshold of 3.5V, the TRACK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, both controllers are disabled and the external MOSFETs are held off.

Light Load Current Operation (Burst Mode Operation, Pulse Skipping, or Continuous Conduction) (PLLIN/MODE Pin)

The LTC3826 can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse skipping mode, or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to a DC voltage below 0.7V (e.g., SGND). To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 0.9V and less than $INTV_{CC}$ – 1.2V.

When a controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-tenth of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is lower than the load current, the error amplifier EA will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.4V, the internal sleep signal goes high (enabling "sleep" mode) and both external MOSFETs are turned off. The I_{TH} pin is then disconnected from the output of the EA and "parked" at 0.425V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3826 draws. If one channel is shut down and the other channel is in sleep mode, the LTC3826 draws only 30µA of quiescent current. If both channels are in sleep mode, the LTC3826 draws only 50µA of quiescent current. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the I_{TH} pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous has the advantages of lower output ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode or clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop section), the LTC3826 operates in PWM pulse skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator I_{CMP} may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (PLLLPF and PLLIN/MODE Pins)

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching

OPERATION (Refer to Functional Diagram)

losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3826's controllers can be selected using the PLLLPF pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the PLLLPF pin can be floated, tied to $INTV_{CC}$, or tied to SGND to select 390kHz, 530kHz, or 250kHz, respectively.

A phase-locked loop (PLL) is available on the LTC3826 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. In this case, a series R-C should be connected between the PLLLPF pin and SGND to serve as the PLL's loop filter. The LTC3826 phase detector adjusts the voltage on the PLLLPF pin to align the turn-on of controller 1's external top MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's external top MOSFET is 180 degrees out of phase to the rising edge of the external clock source.

The typical capture range of the LTC3826's phase-locked loop is from approximately 115kHz to 800kHz, with a guarantee over all manufacturing variations to be between 140kHz and 650kHz. In other words, the LTC3826's PLL is guaranteed to lock to an external clock source whose frequency is between 140kHz and 650kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.2V (falling).

PolyPhase Applications (CLKOUT and PHASMD Pins)

The LTC3826 features two pins (CLKOUT and PHASMD) that allow other controller ICs to be daisy-chained with the LTC3826 in PolyPhase® applications. The clock output signal on the CLKOUT pin can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or multiple separate outputs. The PHASMD pin is used to adjust the phase of the CLKOUT signal as well as the relative phases between the two internal controllers, as summarized in Table 1. The phases are calculated relative to the zero degrees phase being defined as the rising edge of the top gate driver output of controller 1 (TG1).

Table 1

V_{PHASMD}	CONTROLLER 2 PHASE	CLKOUT PHASE
GND	180°	60°
Floating	180°	90°
$INTV_{CC}$	240°	120°

Output Overvoltage Protection

An overvoltage comparator guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{FB} pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Power Good (PGOOD1 and PGOOD2) Pins

Each PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the corresponding V_{FB} pin voltage is not within ±10% of the 0.8V reference voltage. The PGOOD pin is also pulled low when the corresponding RUN pin is low (shut down). When the V_{FB} pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 8.5V.

Foldback Current (FOLDDIS Pin)

When the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the V_{FB} voltage is keeping up with the TRACK/SS voltage) or when the FOLDDIS pin is pulled high to $INTV_{CC}$.

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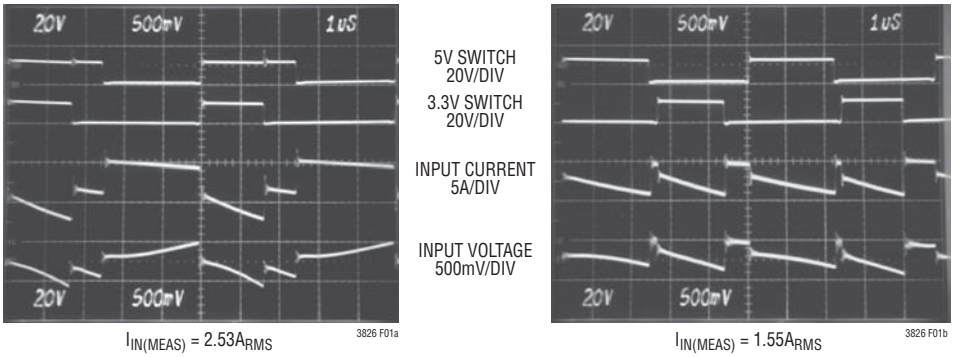
OPERATION (Refer to Functional Diagram)

THEORY AND BENEFITS OF 2-PHASE OPERATION

Why the need for 2-phase operation? Up until the 2-phase family, constant-frequency dual switching regulators operated both channels in phase (i.e., single-phase operation). This means that both switches turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor and battery. These large amplitude current pulses increased the total RMS current flowing from the input capacitor, requiring the use of more expensive input capacitors and increasing both EMI and losses in the input capacitor and battery.

With 2-phase operation, the two channels of the dual-switching regulator are operated 180 degrees out of phase. This effectively interleaves the current pulses drawn by the switches, greatly reducing the overlap time where they add together. *The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used, reduces shielding requirements for EMI and improves real world operating efficiency.*

Figure 1 compares the input waveforms for a representative single-phase dual switching regulator to the LTC3826 2-phase dual switching regulator. An actual measurement of the RMS input current under these conditions shows that 2-phase operation dropped the input current from $2.53A_{RMS}$ to $1.55A_{RMS}$. While this is an impressive reduction in itself, remember that the power losses are proportional to I_{RMS}^2, meaning that the actual power wasted is reduced by a factor of 2.66. The reduced input ripple voltage also means less power is lost in the input power



$I_{IN(MEAS)} = 2.53A_{RMS}$ (a)

$I_{IN(MEAS)} = 1.55A_{RMS}$ (b)

Figure 1. Input Waveforms Comparing Single-Phase (a) and 2-Phase (b) Operation for Dual Switching Regulators Converting 12V to 5V and 3.3V at 3A Each. The Reduced Input Ripple with the 2-Phase Regulator Allows Less Expensive Input Capacitors, Reduces Shielding Requirements for EMI and Improves Efficiency

OPERATION (Refer to Functional Diagram)

path, which could include batteries, switches, trace/connector resistances and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage.

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles which, in turn, are dependent upon the input voltage V_{IN} (Duty Cycle = V_{OUT}/V_{IN}). Figure 2 shows how the RMS input current varies for single-phase and 2-phase operation for 3.3V and 5V regulators over a wide input voltage range.

It can readily be seen that the advantages of 2-phase operation are not just limited to a narrow operating range, for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

The schematic on the first page is a basic LTC3826 application circuit. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE} and the inductor value. Next, the power MOSFETs are selected. Finally, C_{IN} and C_{OUT} are selected.

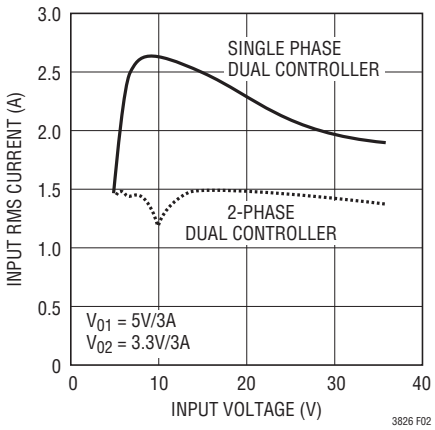


Figure 2. RMS Input Current Comparison

APPLICATIONS INFORMATION

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The current comparator has a maximum threshold of 100mV/R_{SENSE} and an input common mode range of SGND to 10V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the IC and external component values yields:

$$R_{SENSE} = \frac{80mV}{I_{MAX}}$$

When using the controller in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak output current level depending upon the operating duty factor.

Operating Frequency and Synchronization

The choice of operating frequency, is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The internal oscillator for each of the LTC3826's controllers runs at a nominal 390kHz frequency when the PLLLPF pin is left floating and the PLLIN/MODE pin is a DC low or high. Pulling the PLLLPF to $INTV_{CC}$ selects 530kHz operation; pulling the PLLLPF to SGND selects 250kHz operation.

Alternatively, the LTC3826 will phase-lock to a clock signal applied to the PLLIN/MODE pin with a frequency between 140kHz and 650kHz (see Phase-Locked Loop and Frequency Synchronization).

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 10% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance

APPLICATIONS INFORMATION

selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for each controller in the LTC3826: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the Gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

APPLICATIONS INFORMATION

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The optional Schottky diodes D3 and D4 shown in Figure 14 conduct during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3826, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC3826 2-phase operation can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The sources of the top MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the sources and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3826, is also suggested. A 10Ω resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

APPLICATIONS INFORMATION

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

Setting Output Voltage

The LTC3826 output voltages are each set by an external feedback resistor divider carefully placed across the output, as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

To improve the frequency response, a feed-forward capacitor, C_{FF} may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

SENSE+ and SENSE– Pins

The common mode input range of the current comparator is from 0V to 10V. Continuous linear operation is provided throughout this range allowing output voltages from 0.8V to 10V. The input stage of the current comparator requires that current either be sourced or sunk from the SENSE pins depending on the output voltage, as shown in the curve in Figure 4. If the output voltage is below 1.5V, current will flow out of both SENSE pins to the main output. In these cases, the output can be easily pre-loaded by the V_{OUT} resistor divider to compensate for the current comparator's negative input bias current. Since V_{FB} is servoed to the 0.8V reference voltage, R_A in Figure 3 should be chosen to be less than $0.8V/I_{SENSE}$, with I_{SENSE} determined from Figure 4 at the specified output voltage.

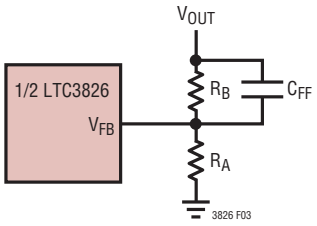


Figure 3. Setting the Output Voltage

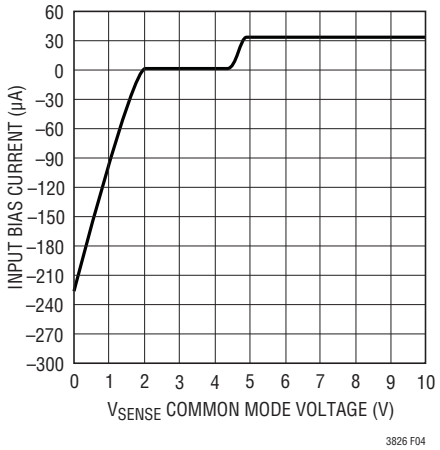


Figure 4. SENSE PIns Input Bias Current vs Common Mode (Output) Voltage

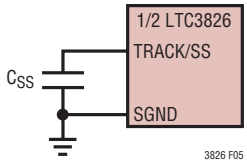


Figure 5. Using the TRACK/SS Pin to Program Soft-Start

Tracking and Soft-Start (TRACK/SS Pins)

The start-up of each V_{OUT} is controlled by the voltage on the respective TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal 0.8V reference, the LTC3826 regulates the V_{FB} pin voltage to the voltage on the TRACK/SS pin instead of 0.8V. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to "track" another supply during start-up.

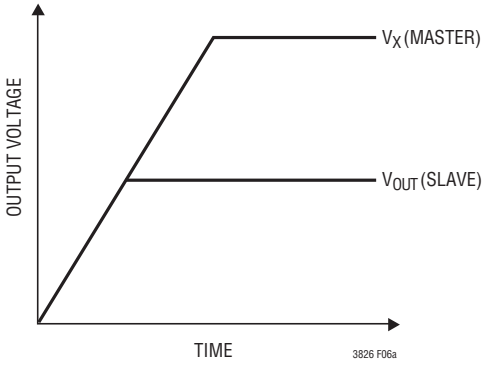
Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Figure 5. An internal 1µA current source charges up the capacitor, providing a linear ramping voltage at the TRACK/SS pin.

APPLICATIONS INFORMATION

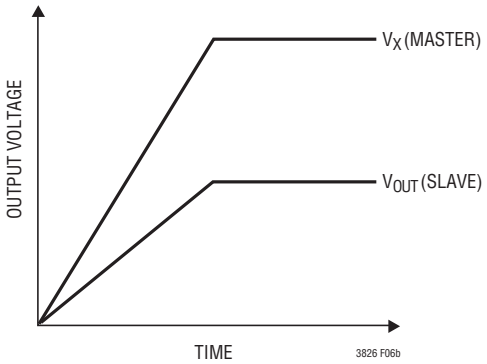
The LTC3826 will regulate the V_{FB} pin (and hence V_{OUT}) according to the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{1\mu A}$$

Alternatively, the TRACK/SS pin can be used to track two (or more) supplies during start-up, as shown qualitatively in Figures 6a and 6b. To do this, a resistor divider should be connected from the master supply (V_X) to the TRACK/SS pin of the slave supply (V_{OUT}), as shown in Figure 7.



(6a) Coincident Tracking



(6b) Ratiometric Tracking

Figure 6. Two Different Modes of Output Voltage Tracking

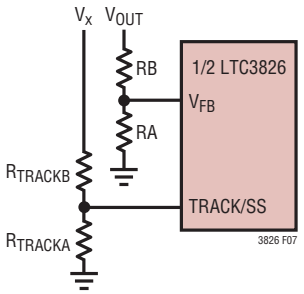


Figure 7. Using the TRACK/SS Pin for Tracking

During start-up V_{OUT} will track V_X according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B}$$

For coincident tracking ($V_{OUT} = V_X$ during start-up),

$R_A = R_{TRACKA}$

$R_B = R_{TRACKB}$

$INTV_{CC}$ Regulators

The LTC3826 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the $INTV_{CC}$ pin from either the V_{IN} supply pin or the $EXTV_{CC}$ pin, respectively, depending on the connection of the $EXTV_{CC}$ pin. $INTV_{CC}$ powers the gate drivers and much of the LTC3826's internal circuitry. The V_{IN} LDO regulates the voltage at the $INTV_{CC}$ pin to 5.25V and the $EXTV_{CC}$ LDO regulates it to 7.5V. Each of these can supply a peak current of 50mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. The ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND IC pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3826 to be exceeded. The $INTV_{CC}$ current, which is dominated by the

APPLICATIONS INFORMATION

gate charge current, may be supplied by either the 5.25V V_{IN} LDO or the 7.5V $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than 4.7V, the V_{IN} LDO is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet INTV_{CC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC3826 $INTV_{CC}$ current is limited to less than 24mA from a 24V supply when in the G package and not using the $EXTV_{CC}$ supply:

$T_J = 70°C + (24mA)(24V)(95°C/W) = 125°C$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (PLLIN/MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. The $EXTV_{CC}$ LDO attempts to regulate the $INTV_{CC}$ voltage to 7.5V, so while $EXTV_{CC}$ is less than 7.5V, the LDO is in dropout and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than 7.5V up to an absolute maximum of 10V, $INTV_{CC}$ is regulated to 7.5V.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from one of the LTC3826's switching regulator outputs ($4.7V \le V_{OUT} \le 10V$) during normal operation and from the V_{IN} LDO when the output is out of regulation (e.g., startup, short-circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Do not apply more than 10V to the $EXTV_{CC}$ pin and make sure than $EXTV_{CC} \le V_{IN}$.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency). For 5V to 10V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$T_J = 70°C + (24mA)(5V)(95°C/W) = 81°C$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ Left Open (or Grounded). This will cause $INTV_{CC}$ to be powered from the internal 5.25V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ Connected directly to V_{OUT}. This is the normal connection for a 5V to 10V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ Connected to an External supply. If an external supply is available in the 5V to 10V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements.
4. EXTVCC Connected to an Output-Derived Boost Network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V. This can be done with the capacitive charge pump shown in Figure 8.

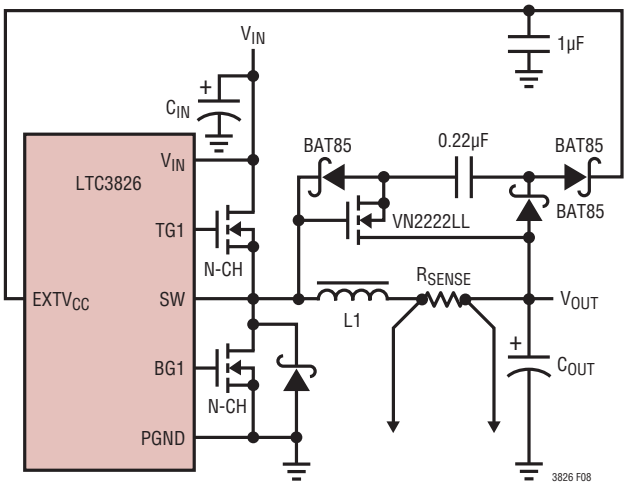


Figure 8. Capacitive Charge Pump for $EXTV_{CC}$

APPLICATIONS INFORMATION

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Fault Conditions: Current Limit and Current Foldback

The LTC3826 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 100mV to 30mV. Under short-circuit conditions with very low duty cycles, the LTC3826 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC3826 (≈230ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} (V_{IN}/L)$$

The resulting short-circuit current is:

$$I_{SC} = \frac{30mV}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}$$

Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator (OV) detects overvoltage faults greater than 10% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the OV condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes. A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

Phase-Locked Loop and Frequency Synchronization

The LTC3826 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the PLLIN/MODE pin. The turn-on of controller 2's top MOSFET is thus 180 degrees out of phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLLLPF pin. The relationship between the voltage on the PLLLPF pin and operating frequency, when there is a clock signal applied

APPLICATIONS INFORMATION

to PLLIN/MODE, is shown in Figure 9 and specified in the Electrical Characteristics table. Note that the LTC3826 can only be synchronized to an external clock whose frequency is within range of the LTC3826's internal VCO, which is nominally 115kHz to 800kHz. This is guaranteed to be between 140kHz and 650kHz. A simplified block diagram is shown in Figure 10.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the PLLLPF pin. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLLPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the PLLLPF pin is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF.

Typically, the external clock (on PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.2V.

Table 2 summarizes the different states in which the PLLLPF pin can be used.

Table 2

PLLLPF PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	250kHz
Floating	DC Voltage	390kHz
$INTV_{CC}$	DC Voltage	530kHz
RC Loop Filter	Clock Signal	Phase-Locked to External Clock

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3826 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

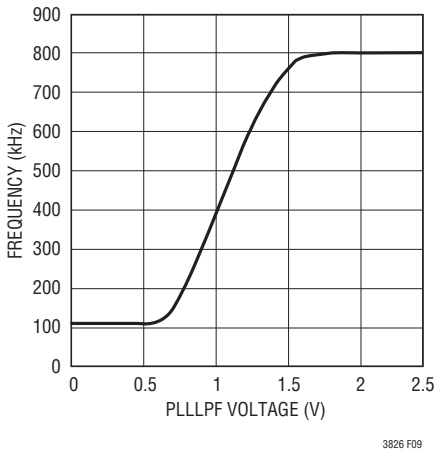


Figure 9. Relationship Between Oscillator Frequency and Voltage at the PLLLPF Pin When Synchronizing to an External Clock

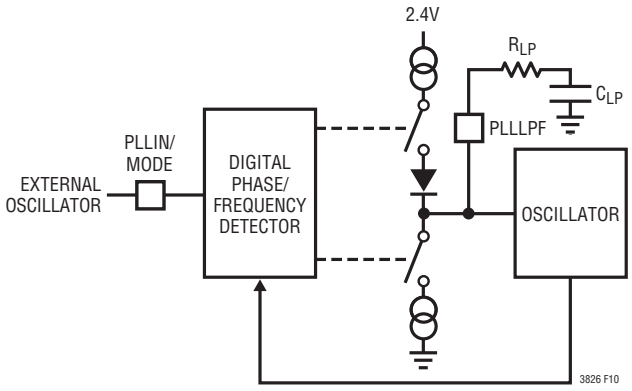


Figure 10. Phase-Locked Loop Block Diagram

APPLICATIONS INFORMATION

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3826 is approximately 230ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 250ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3826 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current has two components: the first is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents; the second is the current drawn from the 3.3V linear regulator output. V_{IN} current typically results in a small (<0.1%) loss.
2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T+Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

   Supplying $INTV_{CC}$ power through the $EXTV_{CC}$ switch input from an output-derived source will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.
3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)} = 30m\Omega$, $R_L = 50m\Omega$, $R_{SENSE} = 10m\Omega$ and $R_{ESR} = 40m\Omega$ (sum of both input and output capacitance losses), then the total resistance is $130m\Omega$. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

APPLICATIONS INFORMATION

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   Transition Loss = (1.7) $V_{IN}2\ I_{O(MAX)}\ C_{RSS}\ f$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. The LTC3728L 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. *The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in Figure 13 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the

APPLICATIONS INFORMATION

same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example for one channel, assume V_{IN} = 12V (nominal), V_{IN} = 22V (max), V_{OUT} = 1.8V, I_{MAX} = 5A, and f = 250kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the PLLLPF pin to GND, generating 250kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

A 4.7µH inductor will produce 23% ripple current and a 3.3µH will result in 33%. The peak inductor current will be the maximum DC value plus one half the ripple current, or 5.84A, for the 3.3µH value. Increasing the ripple current will also help ensure that the minimum on-time of 230ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}f} = \frac{1.8V}{22V(250kHz)} = 327ns$$

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

$$R_{SENSE} \le \frac{80mV}{5.84A} \approx 0.012\Omega$$

Choosing 1% resistors: R1 = 25.5k and R2 = 32.4k yields an output voltage of 1.816V.

The power dissipation on the top side MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, C_{MILLER} = 215pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{1.8V}{22V}(5)^2\left[1+(0.005)(50°C-25°C)\right]\bullet$$

$$(0.035\Omega)+(22V)^2\left(\frac{5A}{2}\right)(4\Omega)(215pF)\bullet$$

$$\left[\frac{1}{5-2.3}+\frac{1}{2.3}\right](300kHz) = 332mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{25mV}{0.01\Omega} - \frac{1}{2}\left(\frac{120ns(22V)}{3.3\mu H}\right) = 2.1A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(20) = 0.1. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = \frac{22V-1.8V}{22V}(2.1A)^2(1.125)(0.022\Omega)$$
$$= 100mW$$

which is less than under full-load conditions.

APPLICATIONS INFORMATION

C_{IN} is chosen for an RMS current rating of at least 3A at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.02\Omega(1.67A) = 33mV_{P-P}$$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 11. Figure 12 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs M1 and M3 located within 1cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.

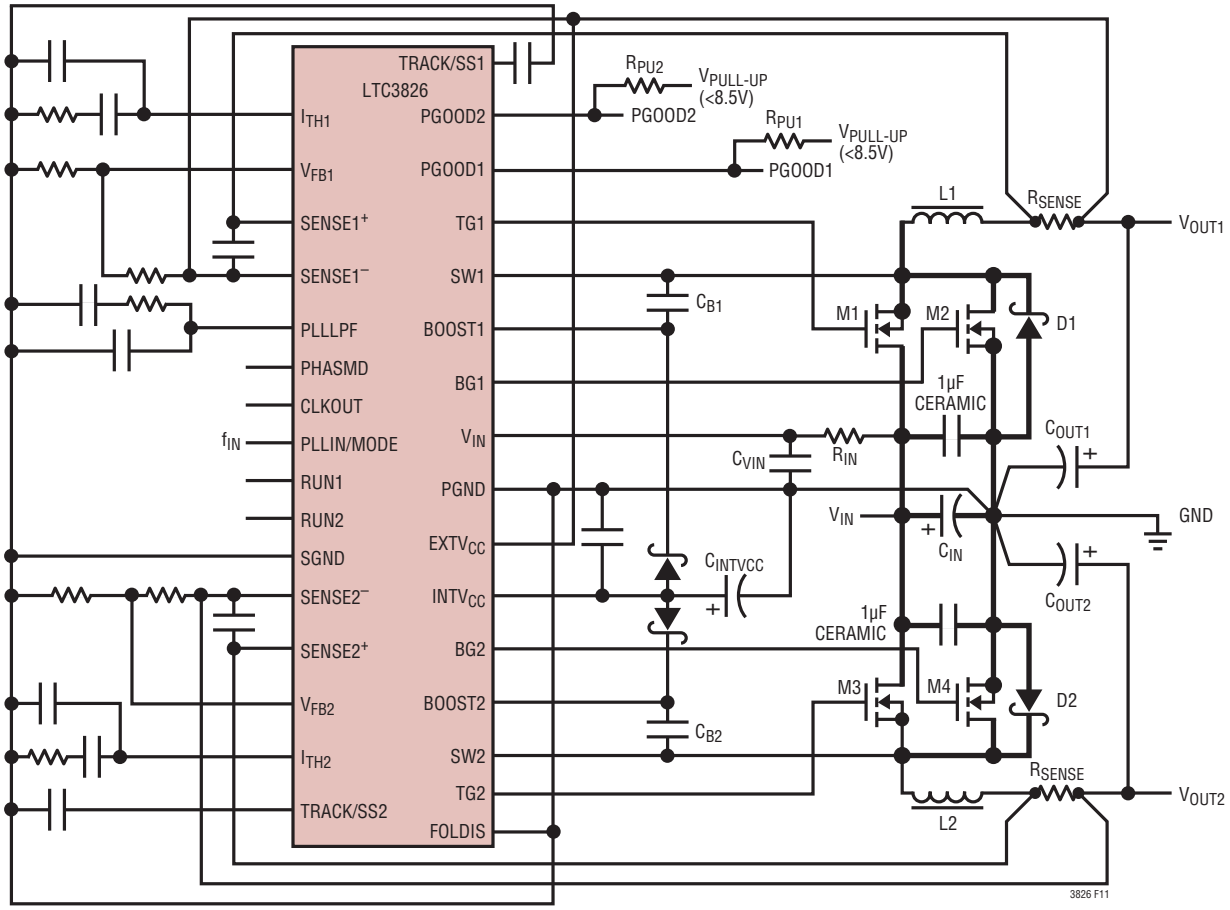


Figure 11. Recommended Printed Circuit Layout Diagram

APPLICATIONS INFORMATION

2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

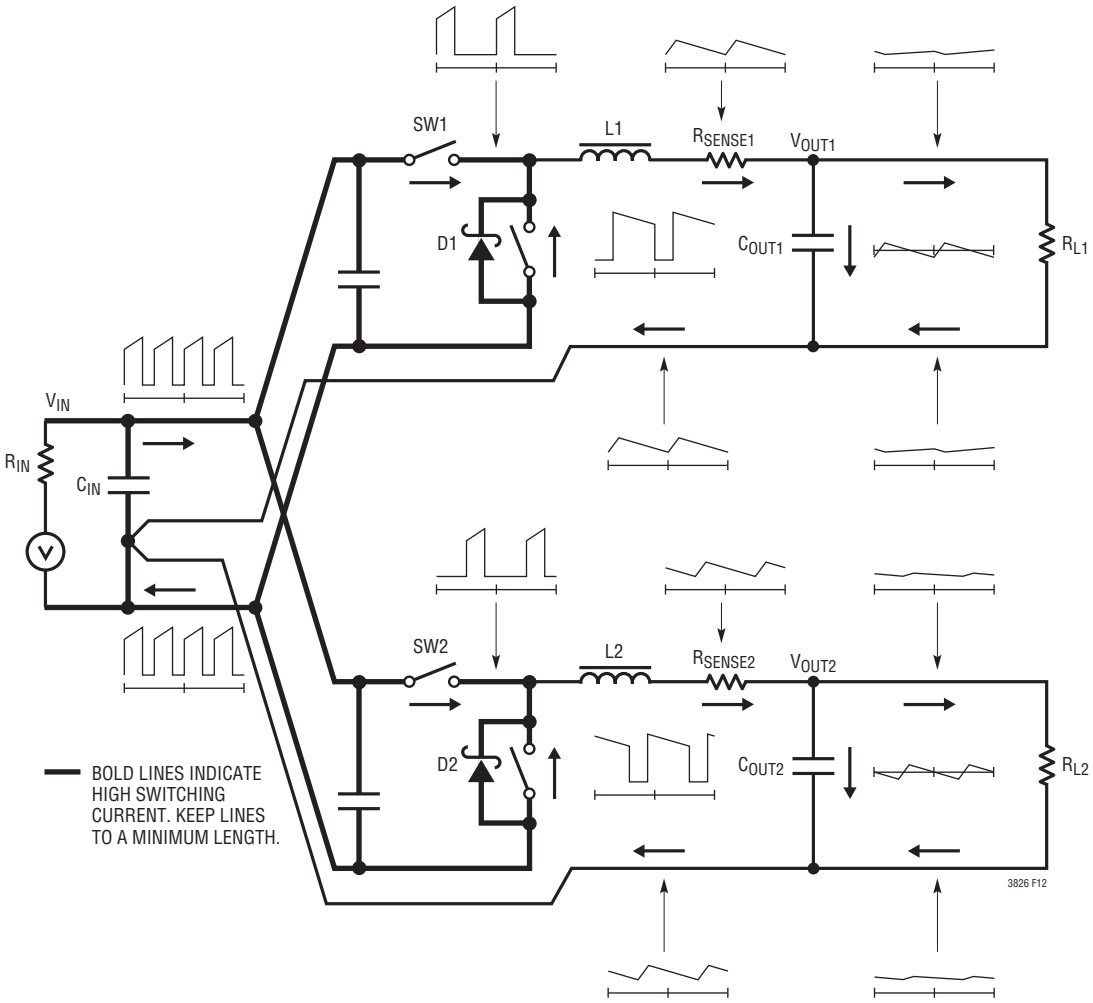


Figure 12. Branch Current Wavefoms

APPLICATIONS INFORMATION

3. Do the LTC3826 V_{FB} pins' resistive dividers connect to the (+) terminals of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.
6. Keep the switching nodes (SW1, SW2), top gate nodes (TG1, TG2), and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposites channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3826 and occupy minimum PC trace area.
7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

PC Board Layout Debugging

Start with one controller on at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

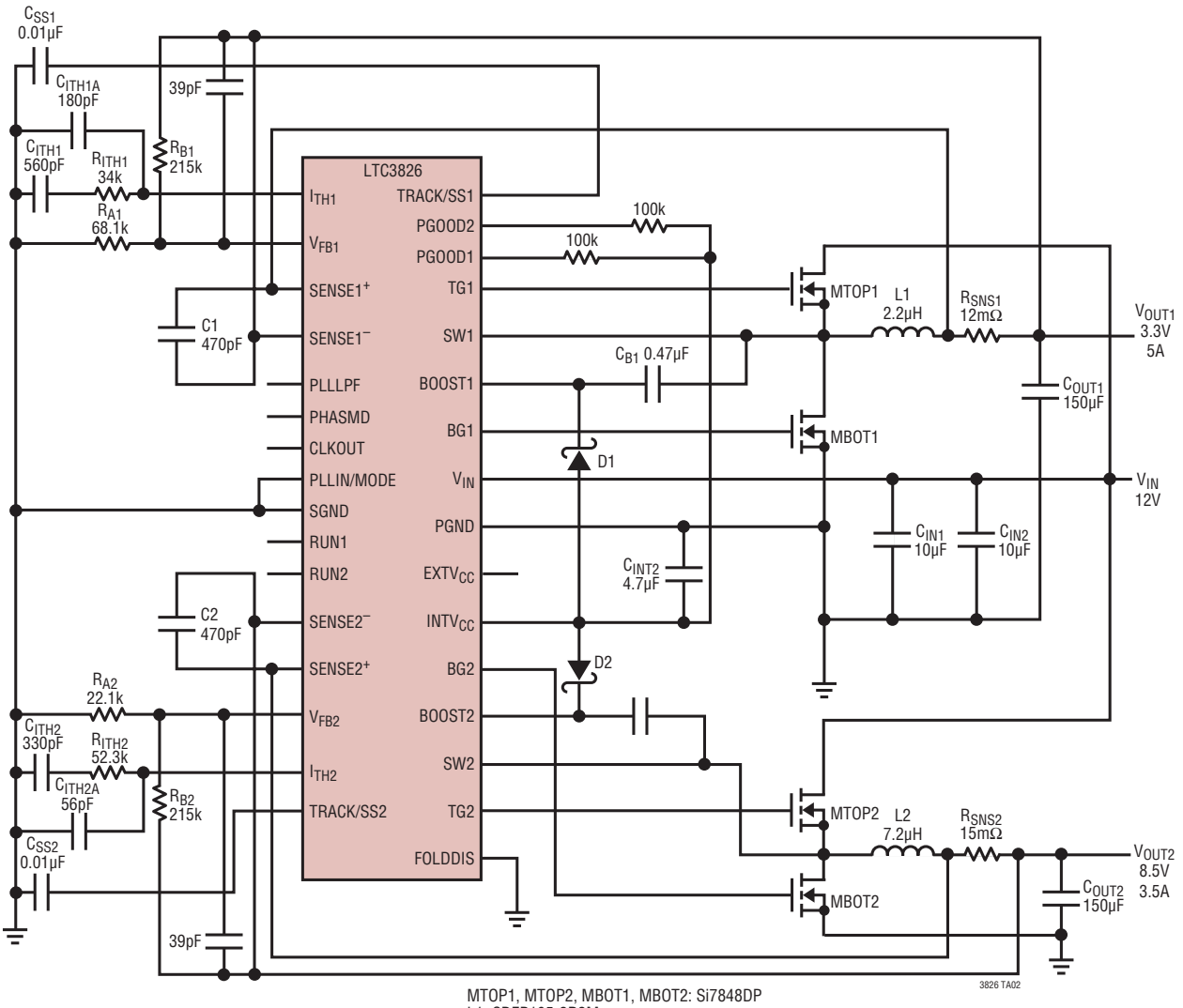
Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the under-voltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

APPLICATIONS INFORMATION

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

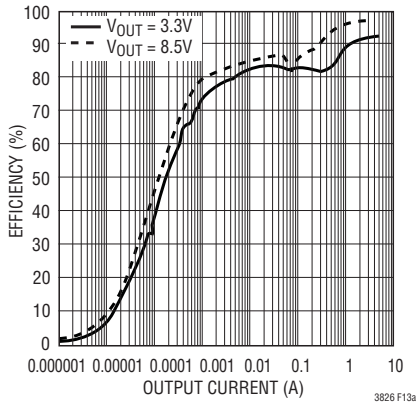
An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

TYPICAL APPLICATIONS

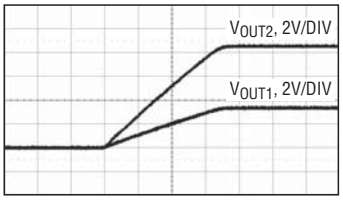


MTOP1, MTOP2, MBOT1, MBOT2: Si7848DP
L1: CDEP105-2R2M
L2: CDEP105-7R2M
C_{OUT1}, C_{OUT2} = SANYO 10TPD150M

Efficiency vs Output Current



Start-Up



SW Node Waveform

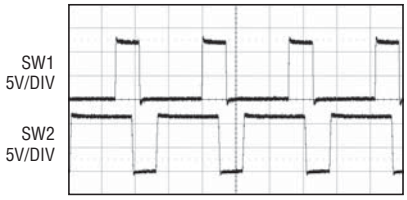
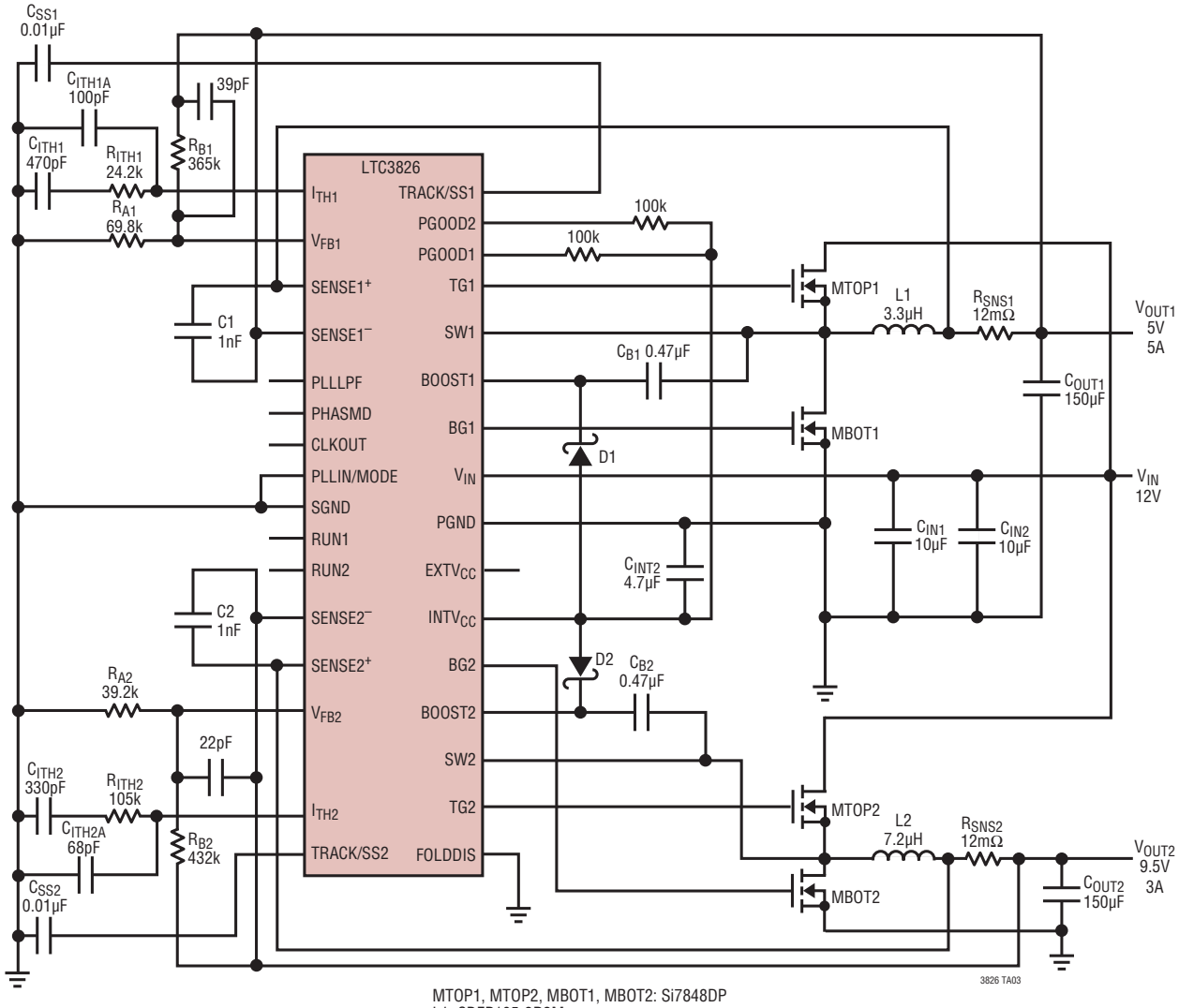


Figure 13. High Efficiency Dual 8.5V/3.3V Step-Down Converter

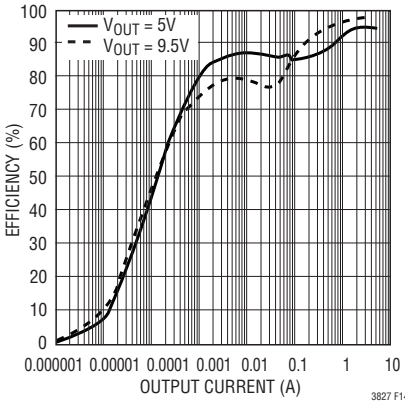
TYPICAL APPLICATIONS

High Efficiency Dual 5V/9.5V Step-Down Converter

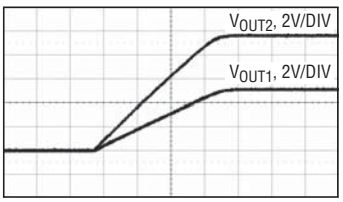


MTOP1, MTOP2, MBOT1, MBOT2: Si7848DP
L1: CDEP105-3R2M
L2: CDEP105-7R2M
C_{OUT1}, C_{OUT2} = SANYO 10TPD150M

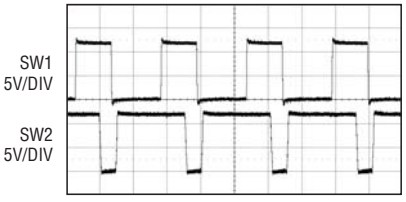
Efficiency vs Output Current



Start-Up

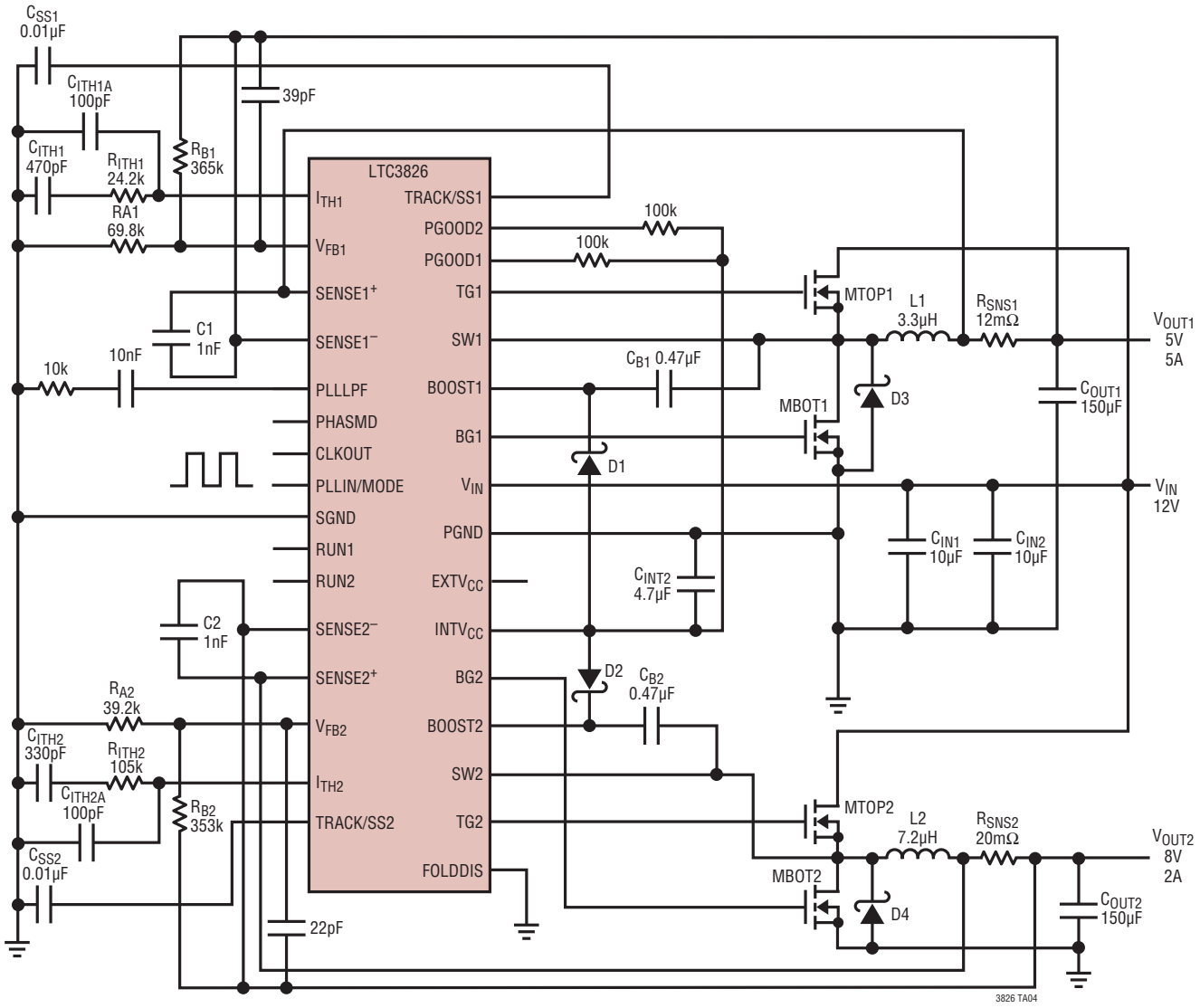


SW Node Waveform



TYPICAL APPLICATIONS

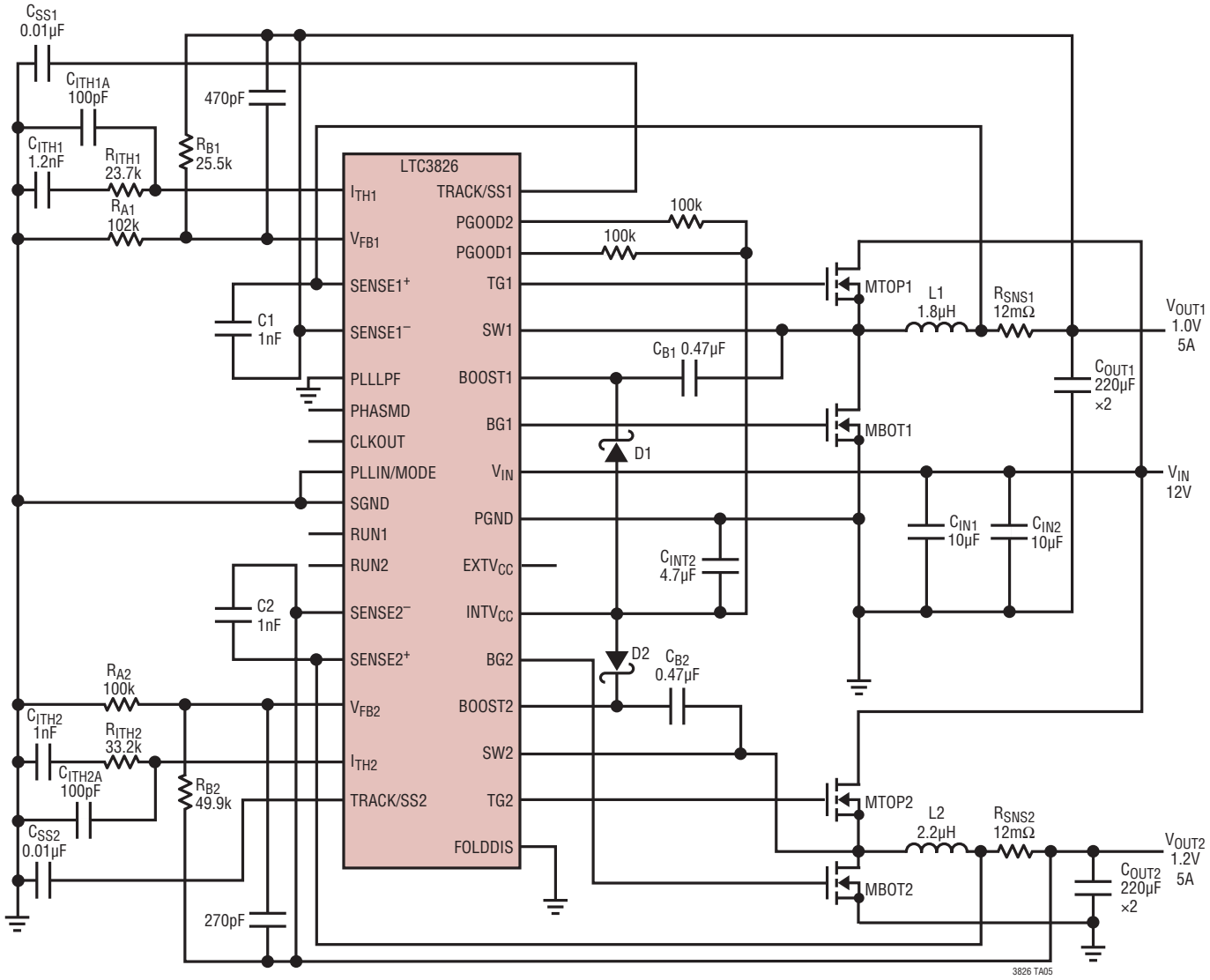
High Efficiency Synchronizable Dual 5V/8V Step-Down Converter



MTOP1, MTOP2, MBOT1, MBOT2: Si7848DP
L1: CDEP105-3R2M
L2: CDEP105-7R2M
C_{OUT1}, C_{OUT2} = SANYO 10TPD150M

TYPICAL APPLICATIONS

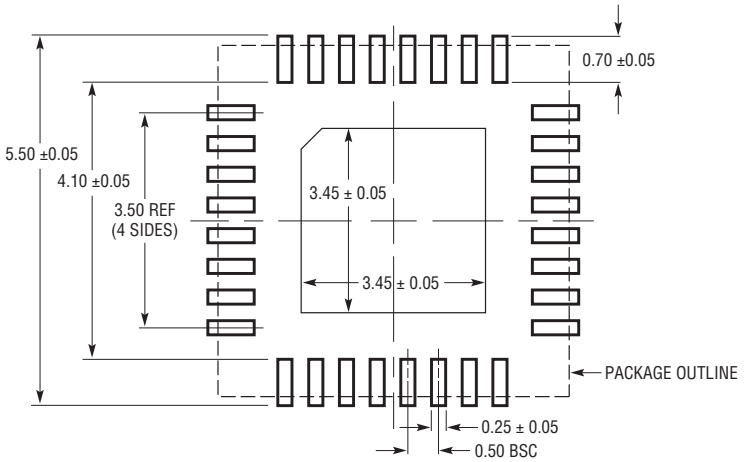
High Efficiency Dual 1.2V/1V Step-Down Converter



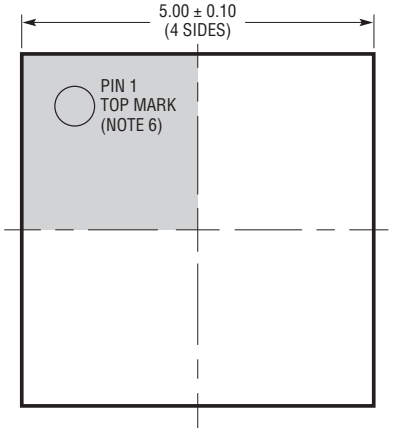
MTOP1, MTOP2, MBOT1, MBOT2: Si7848DP
L1: CDEP105-1R8M
L2: CDEP105-2R2M
C_{OUT1}, C_{OUT2} = SANYO 10TPD150M

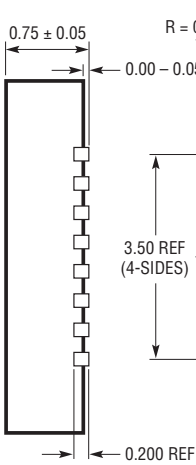
PACKAGE DESCRIPTION

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)

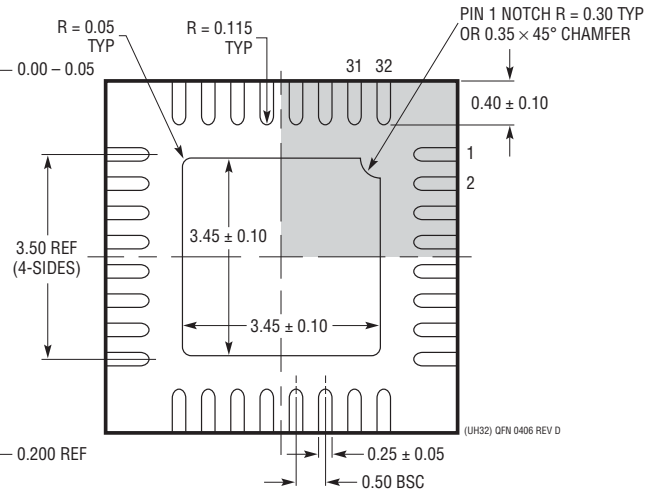


RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

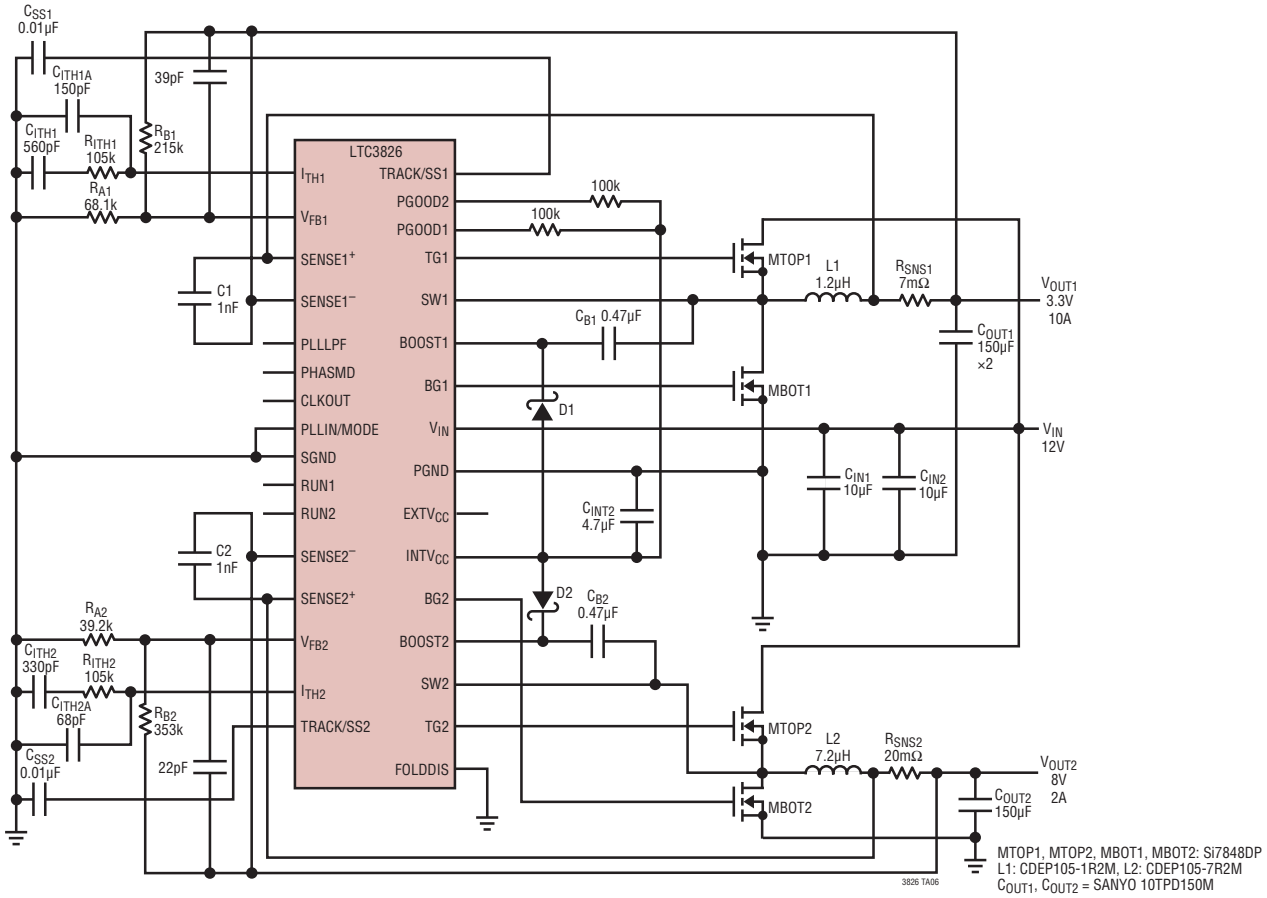


NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

High Efficiency Dual 3.3V/8V Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1735	High Efficiency Synchronous Step-Down Switching Regulator	Output Fault Protection, 16-Pin SSOP
LTC1778/LTC1778-1	No R_{SENSE}™ Current Mode Synchronous Step-Down Controllers	Up to 97% Efficiency, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ (0.9)(V_{IN}), I_{OUT} up to 20A
LT1976	High Voltage Step-Down Switching Regulator	3.3V ≤ V_{IN} ≤ 60V, 100µA Quiescent Current
LTC3708	Dual, 2-Phase, DC/DC Controller with Output Tracking	Current Mode, No R_{SENSE}, Up/Down Tracking, Synchronizable
LTC3727/LTC3727A-1	2-Phase Dual Synchronous Controller	0.8V ≤ V_{OUT} ≤ 14V; 4V ≤ V_{IN} ≤ 36V
LTC3729	20A to 200A, 550kHz PolyPhase Synchronous Controller	Expandable from 2-Phase to 12-Phase, Uses all Surface Mount Components, V_{IN} up to 36V
LTC3731	3- to 12-Phase Step-Down Synchronous Controller	60A to 240A Output Current, 0.6V ≤ V_{OUT} ≤ 6V, 4.5V ≤ V_{IN} ≤ 32V
LTC3827/LTC3827-1	Low I_Q Dual Synchronous Controller	4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, 80µA Quiescent Current
LTC3835/LTC3835-1	Low I_Q Synchronous Step-Down Controller	Single Channel LTC3827/LTC3827-1
LTC3845	Low I_Q Synchronous Step-Down Controller	4V ≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, 120µA Quiescent Current
LTC3850	Dual, 550kHz, 2-Phase Synchronous Step-Down Controller	Dual 180° Phased Controllers, V_{IN} 4V to 24V, 97% Duty Cycle, 4x4 QFN-28, SSOP-28

No R_{SENSE} is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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