TEXAS INSTRUMENTS

TAS5518-5152K8EVM

Evaluation Module for TAS5518 Digital Audio PWM Processor and TAS5152 Digital Amplifier Power-Output Stage

User's Guide

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SLEU074

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About This Manual

This manual describes the operation of the TAS5518-5152K8EVM evaluation module (EVM) from Texas Instruments (TI).

How to Use This Manual

This document contains the following chapters:

Chapter 1 - Overview

Chapter 2 - System Interfaces

Chapter 3 - Protection

Information About Cautions and Warnings

This manual may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From TI

Table 1 contains a list of data manuals that have detailed descriptions of the integrated circuits used in the design of TAS5518-5152K8EVM. The data manuals can be obtained at http://www.ti.com.

Table 1. Related Documentation From TI

PART NUMBER	LITERATURE NUMBER
TAS5518	SLES115
TAS5152	SLES127
TPA112	SLOS212
TPS3801K33	SLVS219
LM317M	SLVS297
TPS76733	SLVS208

Additional Documentation

- *TAS5518-5152K8EVM Application Report* (SLEA061)
- *PC Configuration Tool for TAS5518* (TAS5518 GUI Ver. 4.0 or later)
- General application notes

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Overview

The TAS5518-5152K8EVM PurePath Digital™ customer evaluation amplifier module demonstrates two audio integrated circuits, TAS5518 and TAS5152, from Texas Instruments (TI).

The TAS5518PAG is a high-performance 32-bit (24-bit input) multichannel PurePath Digital pulse-width modulator (PWM) based on Equibit™ technology, with a fully symmetrical AD modulation scheme. It accepts input sample rates from 32 kHz to 192 kHz. The device also has digital audio processing (DAP) that provides 48-bit signal processing, advanced performance, and a high level of system integration. The device has interfaces for headphone output and power supply volume control (PSVC).

The TAS5152DKD is a compact, high-power, digital amplifier power stage designed to drive a 4-Ω loudspeaker up to 125 W (10% THD+N). It contains integrated gate drivers, four matched and electrically isolated enhancement-mode N-channel power DMOS transistors, and protection/fault-reporting circuitry.

The DKD PowerPAD™ package top side allows heat transfer through a heatsink. The heatsink in this design is for evaluation purposes only.

This EVM, together with a TI input-USB board, is a complete 7-channel digital audio amplifier system that includes digital input (S/PDIF), analog inputs, interface to PC, and DAP features, such as digital volume control, input and output mixers, auto mute, equalization, tone controls, loudness, dynamic range compression, and PSVC output. There are configuration options for stereo line level output, stereo headphone output, and power-stage failure protection.

This 6.1 system is designed for home-theater applications, such as A/V receivers, DVD minicomponent systems, home theater in a box (HTIB), DVD receivers, or plasma display panels (PDPs).

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1.1 TAS5518-5152K8EVM Features

- Stereo-channel line output
- Stereo headphone output
- Self-contained protection system (short circuit and thermal)
- Standard inter-IC sound (I^2S) and inter-integrated circuit (I^2C)/control connector for TI input board
- Double-sided plated-through printed circuit board (PCB) layout

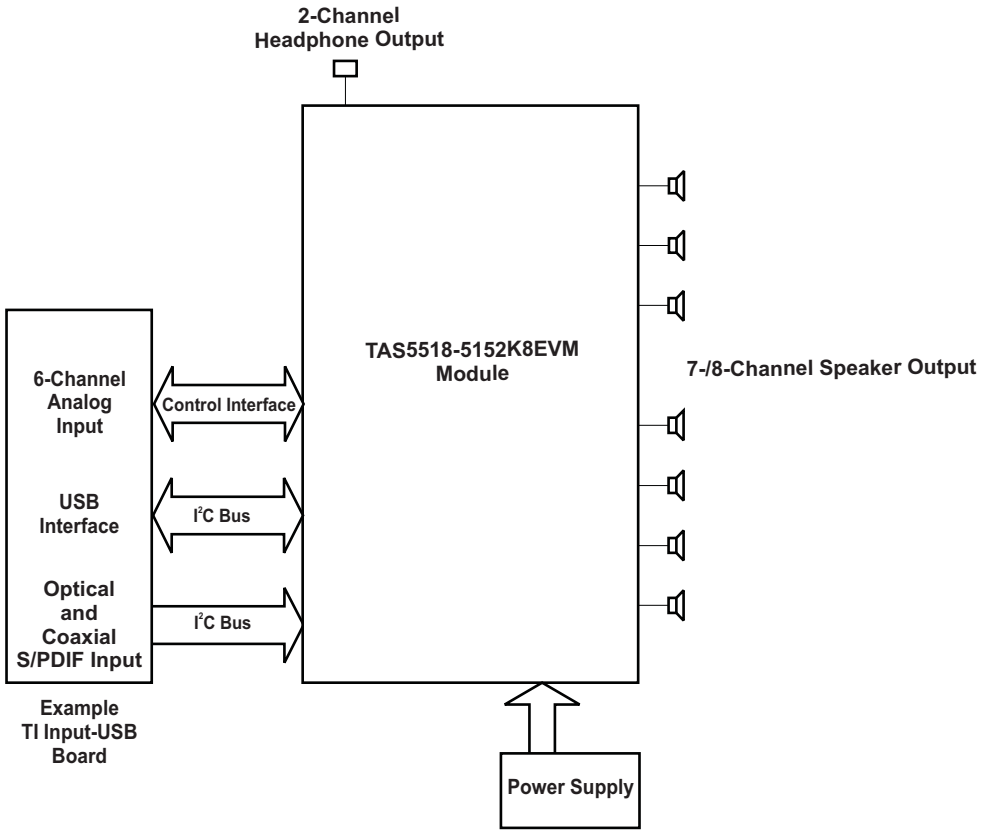

Figure 1-1. Integrated PurePath Digital™ Amplifier System

1.2 PCB Key Map

Physical structure for the TAS5518-5152K8EVM is shown in Figure 1-2.

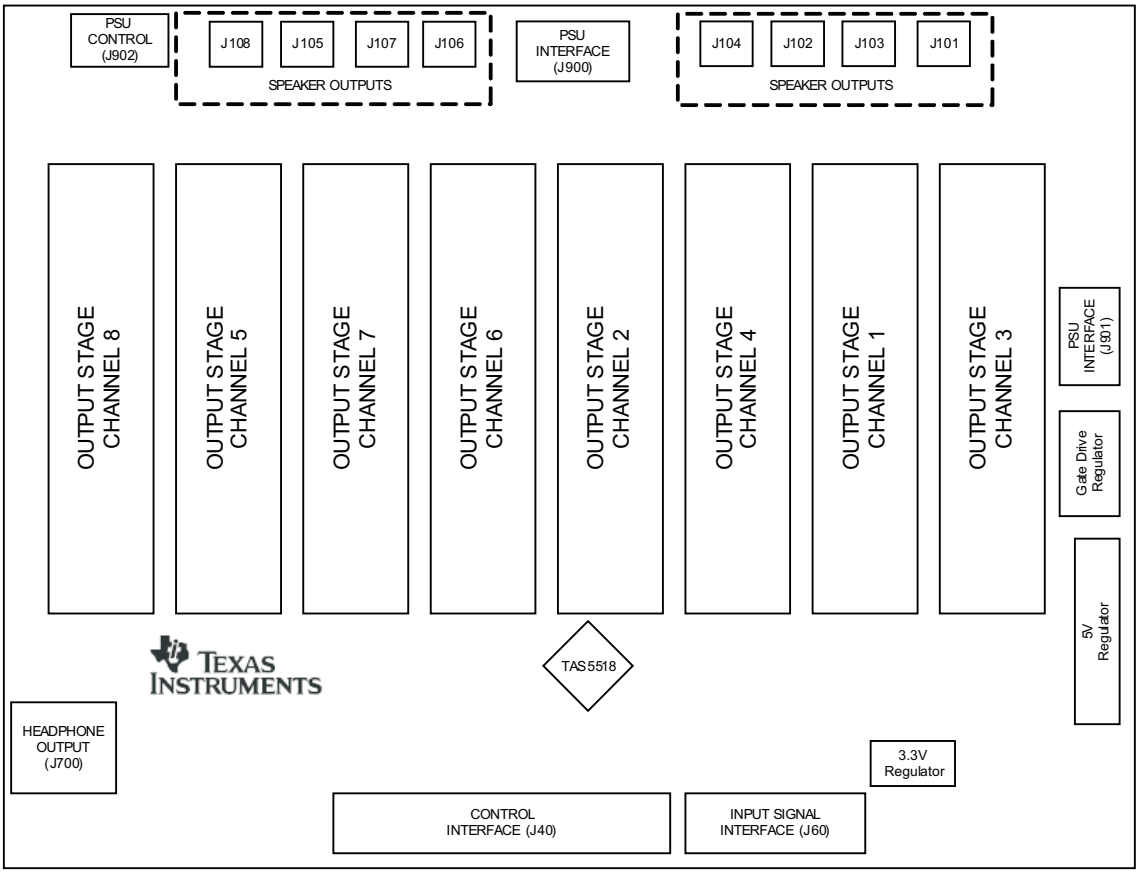

Figure 1-2. Physical Structure for TAS5518-5152K8EVM (Rough Outline)

System Interfaces

This chapter describes the TAS5518-5152K8EVM board, with regard to power supplies and system interfaces.

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2.1 Power Supply (PSU) Interface (J901 and J900)

The TAS5518-5152K8EVM module must be powered from external power supplies. High-end audio performance requires a stabilized power supply, with low ripple voltage and low output impedance.

Note: The length of power-supply cable must be minimized. Increasing the length of PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

Maximum output-stage supply voltage depends of the speaker load resistance. Check the recommended maximum supply voltage in the TAS5152 data sheet.

Table 2-1. Recommended Supply Voltages

DESCRIPTION	VOLTAGE LIMITATIONS (4-Ω LOAD)	CURRENT RECOMMENDATIONS
System power supply	15 V to 20 V	0.3 A
Output-stage power supply	0 V to 35 V	6 A(1)

(1) The rated current corresponds to two-channel full scale (80 W each), which is adequate for a standard eight-channel amplifier design.

The recommended TAS5152 power-up sequence is shown in Figure 2-1 . For proper TAS5152 operation, the $\overline{\text{RESET}}$ signal should be kept low during power up. $\overline{\text{RESET}}$ is pulled low during power up for 200 ms by the onboard reset generator (U73).

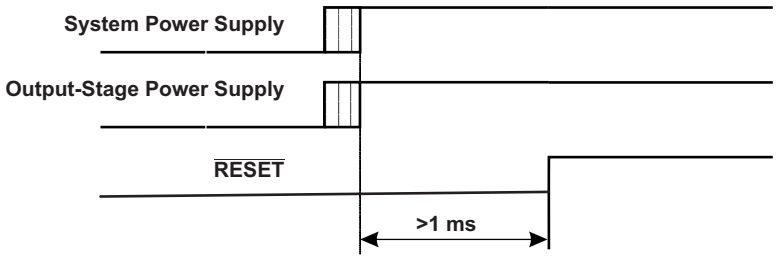

Figure 2-1. Recommended Power-Up Sequence

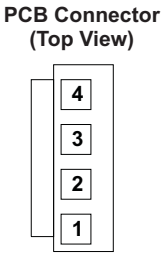

Figure 2-2. J901 and J900 Pin Numbers

Table 2-2. J901 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1	PVDD	Output-stage power supply
2	SYSTEM	System power supply
3	GND	Ground
4	GND	Ground

Table 2-3. J900 Pin Description(1)

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1	PVDD	Extra output-stage power supply
2	PVDD	Extras output-state power supply
3	GND	Extra ground
4	GND	Extra ground

(1) Optional – Use to decrease impedance to reach better performance

2.2 PSU Control Interface (J902)

This interface is used for onboard sensing of output supply voltage and for the power supply volume control (PSVC) signal.

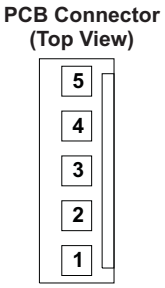

Figure 2-3. J902 Pin Numbers

Table 2-4. J902 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1	–	Reserved for future use
2	PVDD	Sense of output power supply
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bidirectional)
5	PSVC	Power supply volume control

2.3 Loudspeaker Connectors (J101–J107)

CAUTION

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g., through an oscilloscope).

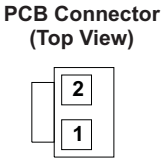

Figure 2-4. J101–J107 Pin Numbers

Table 2-5. J101–J107 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1	OUT-1	Speaker negative output
2	OUT-2	Speaker positive output

2.4 Headphone Connector (J700)

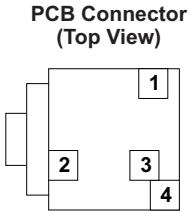

Figure 2-5. J700 Pin Numbers

Table 2-6. J700 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1	OUT-R	Right headphone output
2	GND	Ground
3	–	Reserved
4	OUT-L	Left headphone output

2.5 Control Interface (J40)

This interface connects the TAS5518-5152K8EVM board to a TI input-USB board.

Table 2-7. J40 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1, 3, 11, 17, 25, 26, 31, 32	GND	Ground
2, 8, 9, 13–16, 18, 19, 27–30	–	Reserved
4	$\overline{\text{RESET}}$	
5	$\overline{\text{BKND-ERR}}$	Backend error (or soft reset). Provides reduced click and pop reset, without resetting I^2C volume register settings.
6	$\overline{\text{MUTE}}$	Ramp volume from any setting to noiseless soft mute. Mute also can be activated by I^2C.
7	$\overline{\text{PDN}}$	Power down. The TAS5518 goes to power-down state when activated.
10	SDA	I^2C data clock
12	SCL	I^2C bit clock
20	$\overline{\text{SD}}$	Shutdown reporting. Activated if one or more TAS5152 has high current or high temperature (see Chapter 3).
21	$\overline{\text{SD}}$	Shutdown reporting. Activated if one or more TAS5152 has high current or high temperature Pin 21 connected to pin 20 (see Chapter 3).
22	$\overline{\text{OTW}}$	Overtemperature warning. Activated if one or more TAS5152 has reached temperature warning level.
23	$\overline{\text{OTW}}$	Overtemperature warning. Activated if one or more TAS5152 has reached temperature warning level. Pin 23 connected to pin 22.
24	$\overline{\text{HP-SEL}}$	Headphone select. Headphone active when LOW and inactive when HIGH. To use this pin, a 100-Ω resistor must be placed for R50.
33, 34	5 V	5-V dc power supply (output)

2.6 Digital Audio Interface (J60)

The digital audio interface contains digital audio signal data (I^2S), clocks, etc. Please refer to the *TAS5518 Data Manual* for signal timing and details not covered in this document.

Table 2-8. J60 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1, 3, 10, 12, 14, 16	GND	Ground
2	MCLK	Master clock input. Low-jitter system clock for PWM generation and reclocking. Ground connection from source to the TAS5518 must be a low-impedance connection.
3	GND	Ground
4	SDIN1	I^2S data 1, channel 1 and 2
5	SDIN2	I^2S data 2, channel 3 and 4
6	SDIN3	I^2S data 3, channel 5 and 6
7	SDIN4	I^2S data 4, channel 7 and 8
8, 9, 15	—	Reserved
11	SCLK	I^2S bit clock
13	LRCLK	I^2S left-right clock

Protection

This section describes the short-circuit protection and fault-reporting circuitry of the TAS5152 device.

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3.1 Short-Circuit Protection and Fault-Reporting Circuitry

The TAS5152 is a self-protecting device that provides fault reporting (including high-temperature protection and short-circuit protection). The TAS5152 is configured in back-end auto-recovery mode and, therefore, resets automatically after all errors (M1, M2, and M3 are set low). This means that the device restarts itself after an error and reports shortly through the $\overline{SD}$ error signal.

3.2 Fault Reporting

The $\overline{OTW}$ and $\overline{SD}$ outputs from the TAS5152 indicate fault conditions. Please refer to the *TAS5152 Data Manual* for a description of these pins.

Table 3-1. TAS5152 Warning/Error Signal Decoding

$\overline{OTW}$	$\overline{SD}$	DEVICE CONDITION
0	0	High-temperature error and/or high-current error
0	1	High-temperature warning
1	0	Undervoltage lockout or high-current error
1	1	Normal operation, no errors/warnings

The temperature warning signals at the TAS5518-5152K8EVM board are wired-OR to one temperature warning signal ($\overline{OTW}$– pin 22 in the control interface connector). Shutdown signals are wired-OR into one shutdown signal ($\overline{SD}$– pin 20 in the control interface connector).

The shutdown signals will activate with the temperature warning signal to give chip-state information as described in Table 3-1. Device fault-reporting outputs are open-drain outputs.°

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0-35 V and the output voltage range of 15-20 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75°C. The EVM is designed to operate properly with certain components above 75°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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