MP8040

High Current Power Half Bridge

The Future of Analog IC Technology™

DESCRIPTION

The MP8040 is a general purpose, high frequency half bridge power driver capable of driving a 9A load. The device integrates both top and bottom N-Channel MOSFET power switches and is fully protected from both sourcing and sinking current by a preset cycle-by-cycle current limit. It has a wide input voltage range from 7.5V to 25V.

The MP8040 features a low-current shutdown mode, input under-voltage protection, thermal shutdown, and fault flag signal output. It interfaces with standard logic signals and is available in a small 8-pin SOIC with exposed pad package.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV0041	3.5”X x 3.5”Y x 1.2”Z

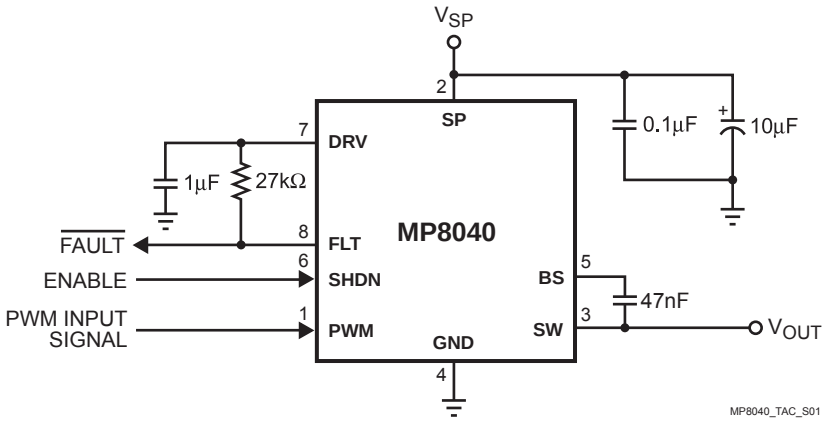
FEATURES

- ±9A Peak Current Output
- ±4.25A Continuous Current Output
- Up to 1.2MHz Switching Frequency
- Protected Integrated Power 100mΩ Switches
- All Switches Current Limited
- Integrated Under-Voltage Protection
- Integrated Thermal Protection
- 2.5µA Standby Mode
- True 2-Quadrant Operation
- Sources and Sinks Current
- Fault Indicator Output

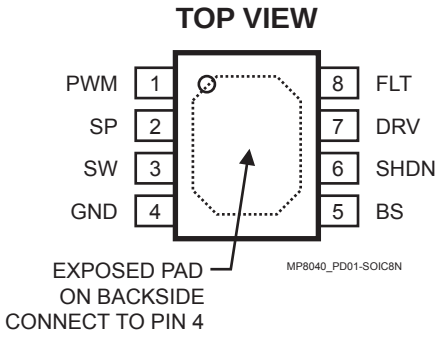
APPLICATIONS

- Class D Audio Driver
  - o 25W/4Ω/10% Output Power Single Ended
  - o 70W/4Ω/10% Output Power Full Bridge
- Full or Half Bridge DC-DC Switching Regulator
- Motor Driver

TYPICAL APPLICATION



PACKAGE REFERENCE



Part Number*	Package	Temperature
MP8040DN	SOIC8N (Exposed Pad)	–40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP8040DN–Z)
For Lead Free, add suffix –LF (eg. MP8040DN–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

SP Supply Voltage (V_{SP}) 28V
SW Pin Voltage ..... –0.3V to V_{SP}
SW to BS ..... –0.3V to +6V
Voltage at All Other Pins ..... –0.3V to +6V
Storage Temperature ..... –55°C to +150°C

Recommended Operating Conditions (2)

SP Supply Voltage (V_{SP}) ..... 7.5V to 24V
Peak Output Current ..... 9A Maximum
Operating Temperature ..... –40°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
SOIC8N	50	8	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{SP} = 12V, V_{SHDN} = 0V, T_A = +25°C, unless otherwise noted.

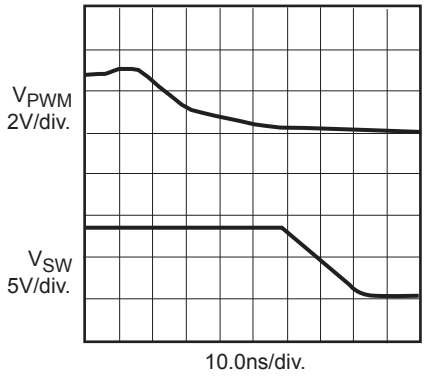
Parameter	Symbol	Condition	Min	Typ	Max	Units
SP Operating Current				1.5	2.5	mA
SP Shutdown Current		V_{SHDN} = 2V		2.5	10	µA
SHDN, SP Threshold Low					1	V
SHDN, SP Threshold High			2			V
SHDN, SP Input Bias Current				1		µA
SW On Resistance		V_{SP} = 7.5V, High-Side and Low-Side		0.1		Ω
SW Current Limit (4)		V_{PWM} = 5, (Sinking)		9		A
		V_{PWM} = 0, (Sourcing)		9		A
SW Switching Frequency		V_{PWM} = 0 to 2V, 50% Duty Cycle			1.2	MHz
SW Maximum Duty Cycle (5)		V_{SP} = 7.5V, V_{PWM} = 2V, C_{SW} 100nF, f_{SW} = 3.3kHz		99.5		%
SW Rise/Fall Time		V_{PWM} = 0 to 5V		20		ns
PWM Pulse Width		V_{PWM} = 0 to 2V, High or Low Pulse	200			ns
PWM to SW Delay Time Rising		V_{PWM} = 0 to 5V		70		ns
PWM to SW Delay Time Falling		V_{PWM} = 5 to 0V		70		ns
Thermal Shutdown Temperature (4)		T_J Rising, Hysteresis = 20°C		160		°C

Notes:
4) Not production tested.
5) SW drives low for 1.5µs every 300µs to charge the BS to SW capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

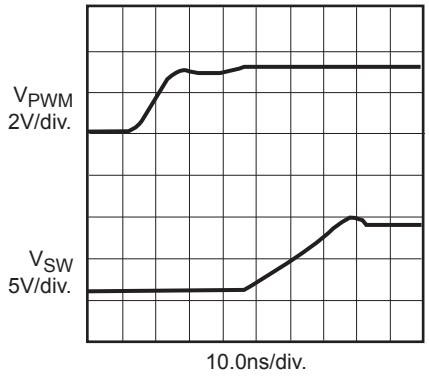
Circuit of Figure 4, T_A = +25°C, unless otherwise noted.

Delay Time
SW Falling (V_{SP}=8V)



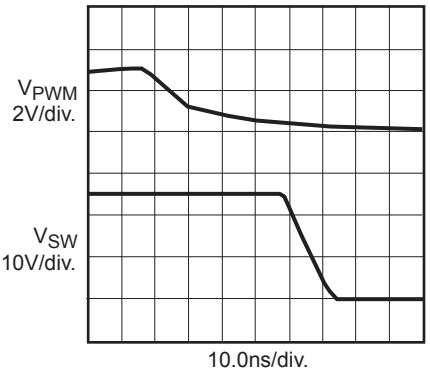
MP8040-TPC01

Delay Time
SW Rising (V_{SP}=8V)



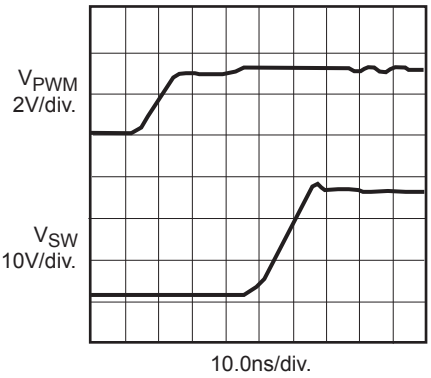
MP8040-TPC02

Delay Time
SW Falling (V_{SP}=25V)



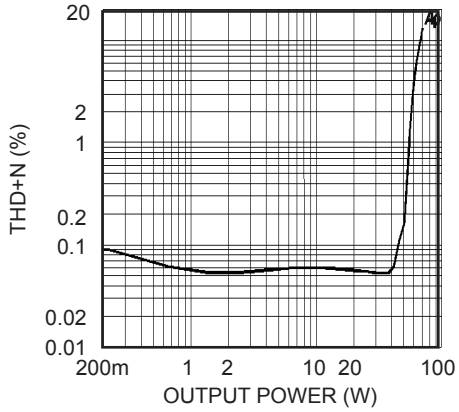
MP8040-TPC03

Delay Time
SW Rising (V_{SP}=25V)



MP8040-TPC04

THD+N vs Output Power
(V_{SP}=24V) Bridged Output into 4Ω
(Class D Application using closed loop circuit)



MP8040-TPC05

PIN FUNCTIONS

Pin #	Name	Description
1	PWM	Driver Logic Input. Drive PWM with the signal that controls the MP8040 output. Drive PWM high to turn on the high-side switch; drive PWM low to turn on the low-side switch.
2	SP	Power Supply Input. Connect SP to the positive side of the input power supply. Bypass SP to GND as close to the IC as possible.
3	SW	Switched Output. SW is the power output of the MP8040. Connect the output LC filter to SW. SW is valid approximately 100µs after SP goes high.
4	GND	Ground. (Note: Connect the exposed pad on the bottom side to Pin 4).
5	BS	Bootstrap Supply. BS powers the high-side gate of the MP8040. Connect a 0.1µF or greater capacitor between BS and SW.
6	SHDN	Shutdown Input. SHDN enables/disables the MP8040. Drive SHDN low to turn on the MP8040, drive it high to turn it off. If not used, connect SHDN to GND.
7	DRV	Gate Drive Supply Bypass. The voltage at DRV is supplied from an internal regulator from SP. DRV powers the internal circuitry and internal MOSFET gate drives. Bypass DRV to GND with a 0.1µF to 10µF capacitor.
8	FLT	Fault Output. Active-low, open drain. A low output at FLT indicates that the MP8040 has detected a fault and has shutdown. Connect FLT to DRV through a 100kΩ resistor.

OPERATION

The MP8040 is a general purpose, power driver. It takes a logic input and drives a half bridge comprised of 0.1Ω high-side and low-side N-Channel MOSFET switches. It operates at frequencies up to 1.2MHz, can accept a DC supply voltage as high as 25V, and produce peak output current as high as 9A.

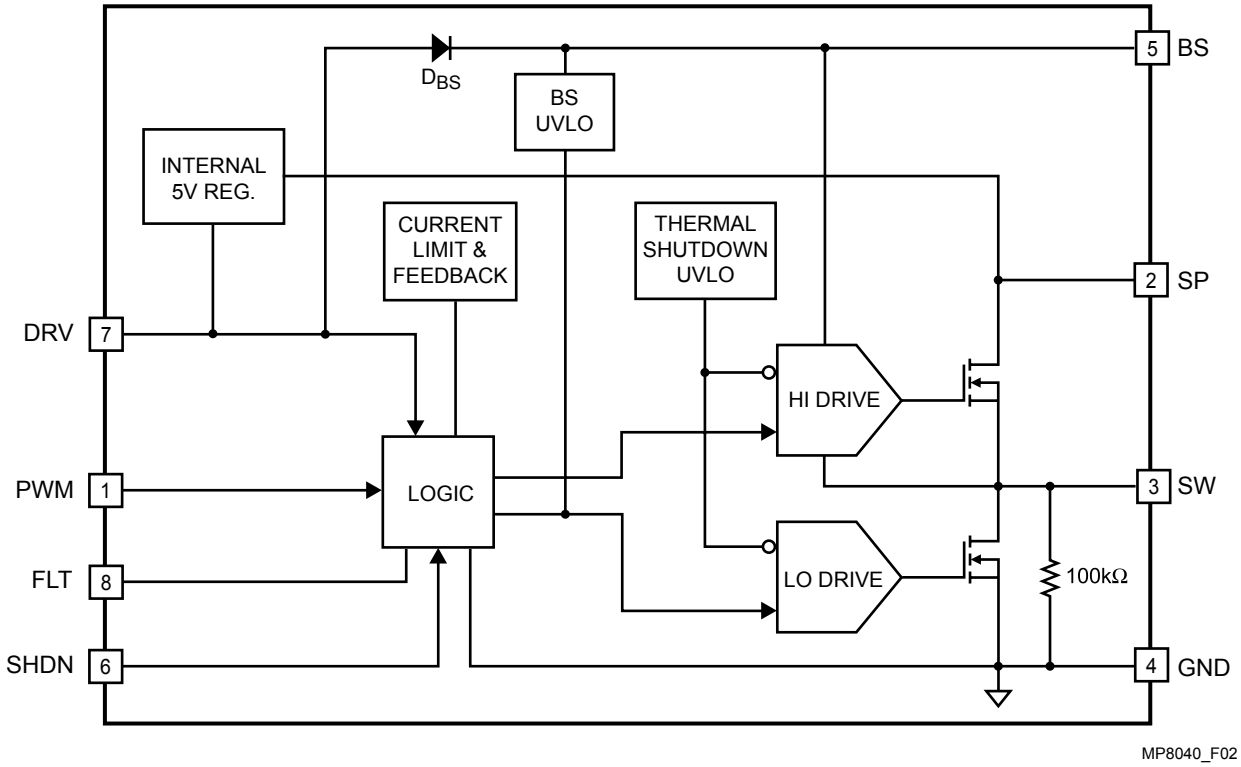


Figure 1—Function Block Diagram

SW Output

The SW output drives the load. It is controlled by the logic input signal at PWM. When the signal at PWM is high (above 2V), the high-side switch is turned on. When the signal at PWM is low (less than 0.4V), the low-side switch is turned on.

The MP8040 uses internal N-Channel MOSFETs for both the high-side and low-side switches. The high-side MOSFET gate drive is powered from the voltage between SW and BS, allowing BS to rise above the SP input voltage to power the high-side MOSFET. To do this a bootstrap capacitor is connected between SW and BS. When the low-side switch is on, the capacitor is internally charged from the voltage at DRV, which is also internally generated. There is a dead time region (typically 40ns) where both the upper and lower switches are off (see Figure 2).

Both the high-side and low-side switches have internal current limits to prevent failure due to excessive load current. Once the current limit is reached, both output switches are turned off and the fault output is asserted (driven low).

Shutdown

The MP8040 includes a 2.5μA shutdown mode. When SHDN is high, both output switches are turned off and the input current drops to 2.5μA. When the MP8040 is shutdown, the internally generated voltage at DRV drops to 0V, and the fault output (FLT) is asserted (driven low). If the shutdown mode is not used, connect SHDN directly to GND.

Fault Output

The MP8040 includes a fault indicator output (FLT). This is an active-low open drain output. The MP8040 detects faults due to over-current (>9A), over-temperature (>160°C), under-voltage at SP (<6.5V), or if the part is disabled. Connect FLT to DRV or to an external voltage up to 6V through a 27kΩ or greater resistor. When any of the 3 fault conditions are detected, both output switches are turned off and the SW output is high-impedance.

Thermal Shutdown

The MP8040 includes a thermal overload protection circuit. If the die temperature rises above 160°C, the output switches are turned off and the fault output is asserted. Once the thermal overload circuit is tripped, the die temperature must drop below 140°C before automatically restarting.

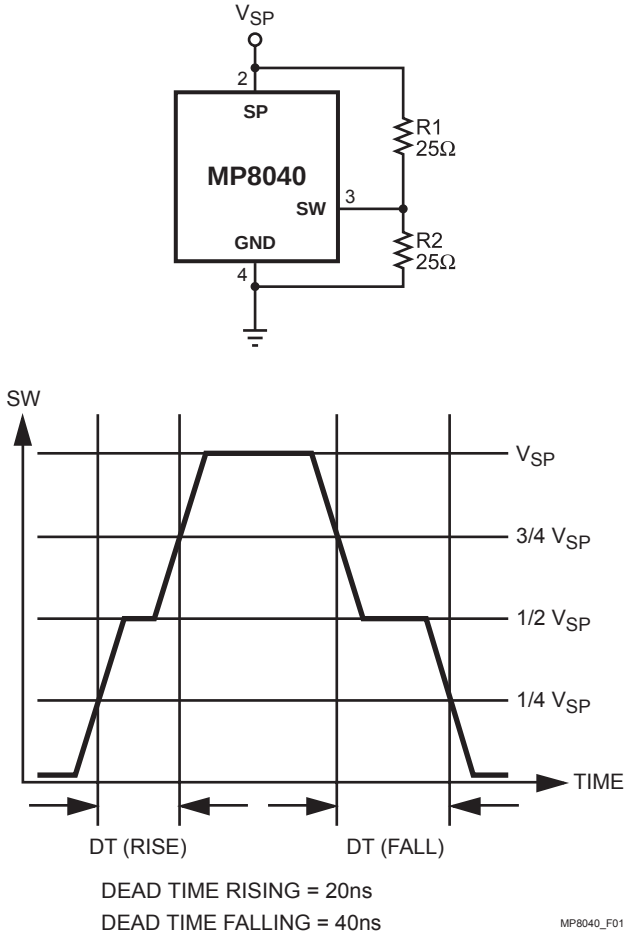


Figure 2—Dead Time

TYPICAL APPLICATION CIRCUITS

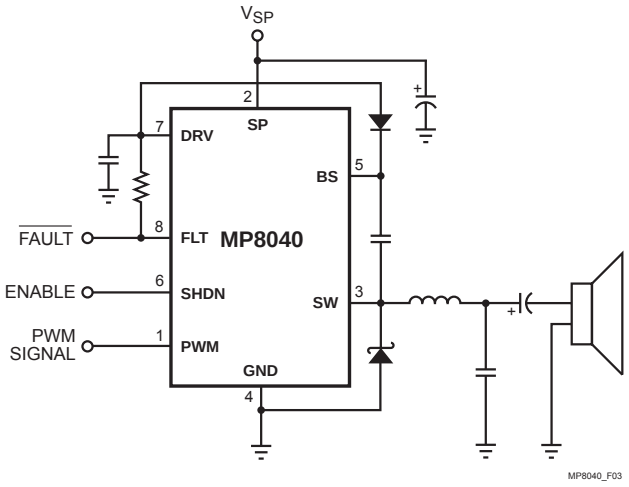


Figure 3—Single Ended Audio Amplifier

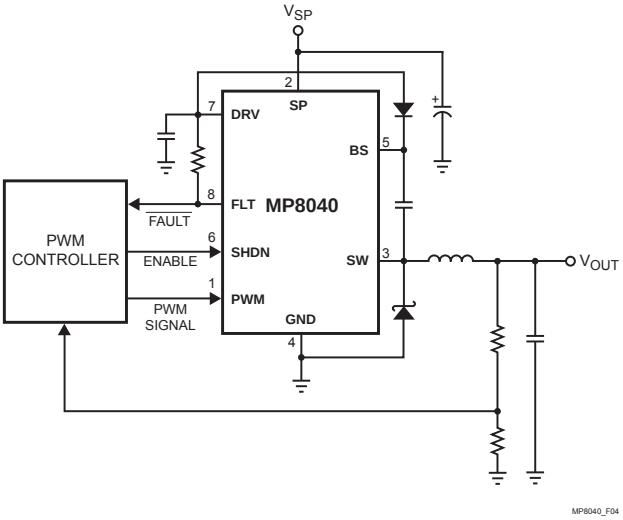


Figure 4—General Purpose DC to DC Converter

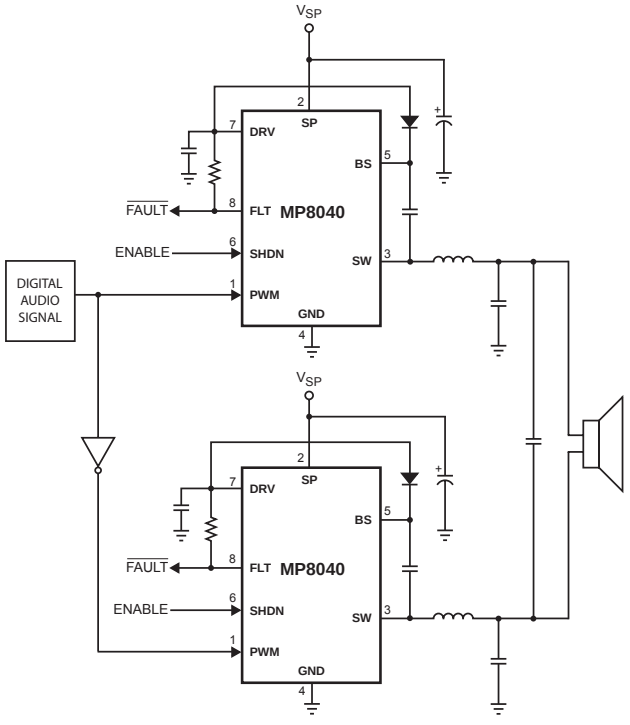


Figure 5—80W Full Bridge Audio Amplifier

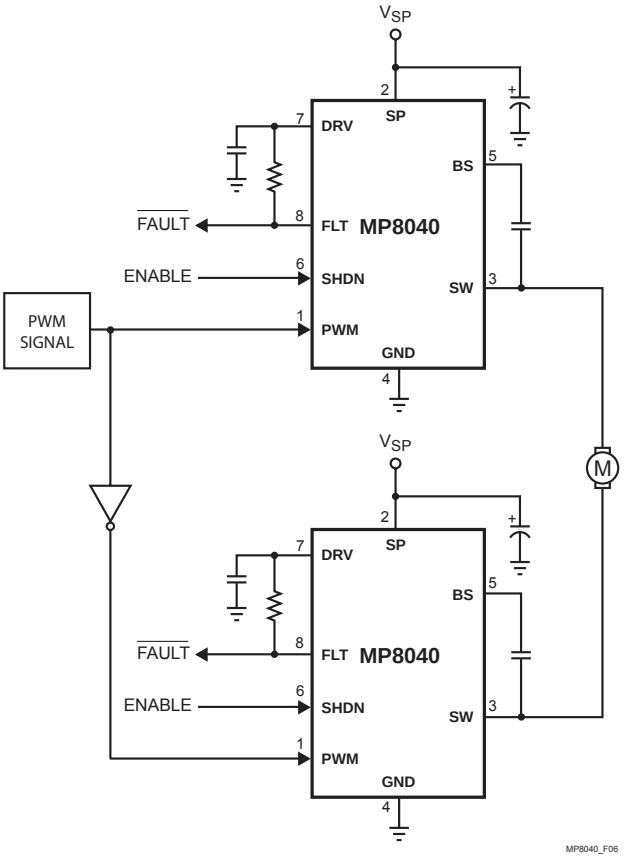


Figure 6—Full Bridge Motor Driver

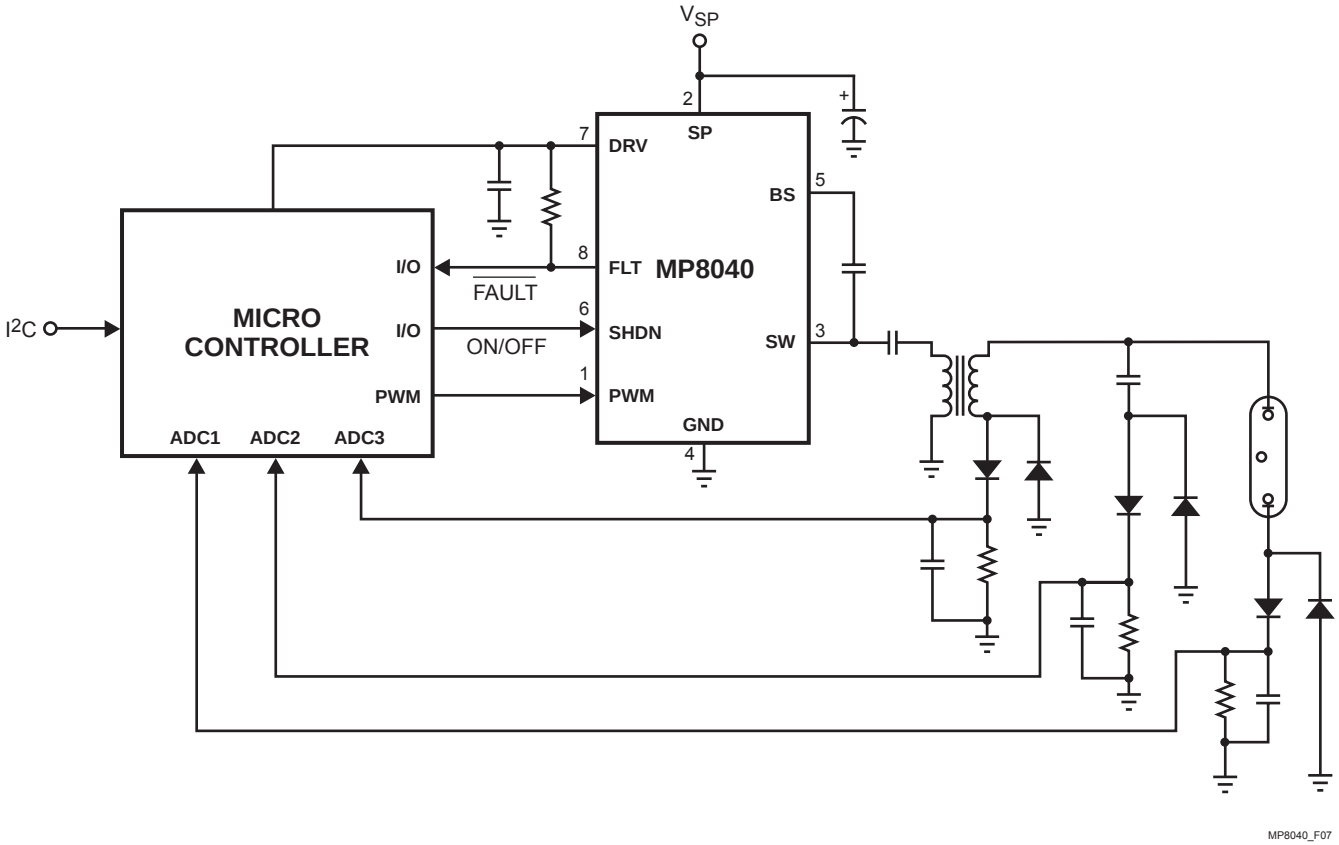
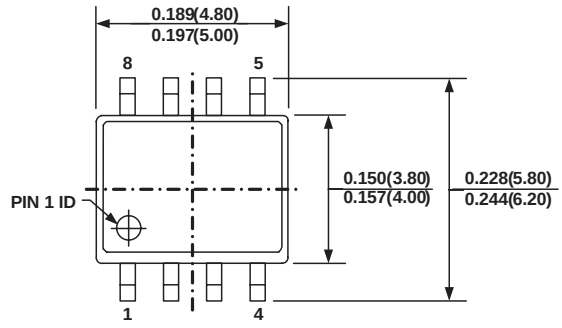


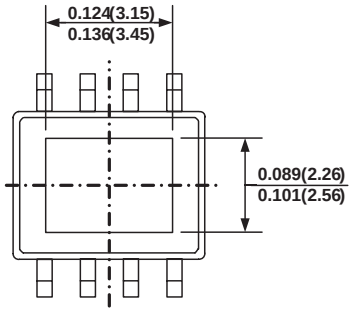
Figure 7—CCFL Driver Circuit

PACKAGE INFORMATION

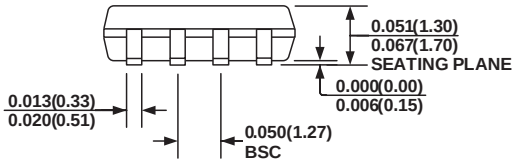
SOIC8N (EXPOSED PAD)



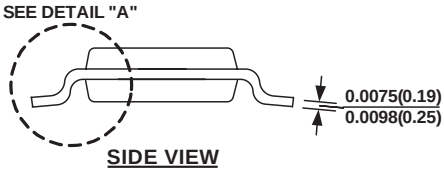
TOP VIEW



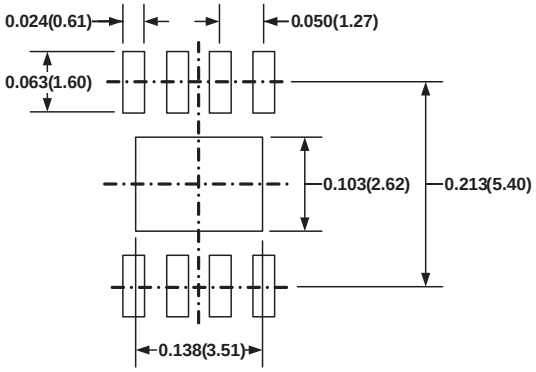
BOTTOM VIEW



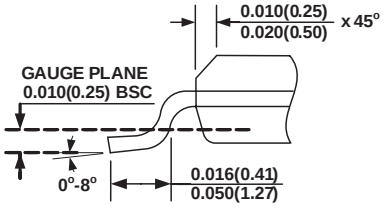
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"