MC100LVEL40

3.3/5V ECL Differential Phase-Frequency Detector

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Description

The MC100LVEL40 is a three state phase frequency−detector intended for phase−locked loop applications which require a minimum amount of phase and frequency difference at lock. Advanced design significantly reduces the dead zone of the detector. For proper operation, the input edge rate of the R and V inputs should be less than 5 ns. The device is designed to work with a 3.3 V power supply.

When the reference (R) and the feedback (FB) inputs are unequal in frequency and/or phase the differential up (U) and down (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

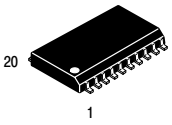
For application information, refer to AND8040/D, “Phase Lock Loop Operation.”

The 100 Series Contains Temperature Compensation.

Features

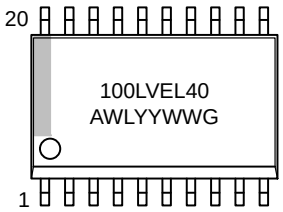
- 250 MHz Typical Bandwidth
- PECL Mode Operating Range:
  V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = −3.0 V to −5.5 V
- Internal Input Pulldown Resistor
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



SO−20
DW SUFFIX
CASE 751D

MARKING DIAGRAM



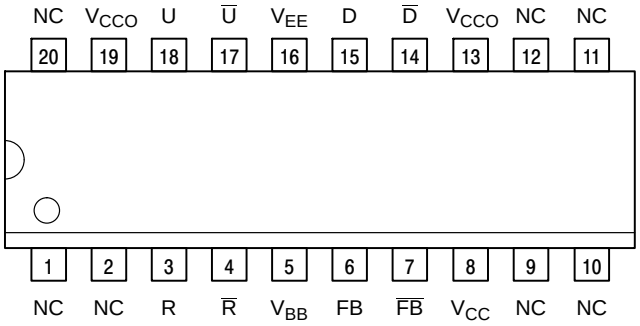
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20−Lead Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
U, $\overline{U}$	ECL Up Differential Outputs
D, $\overline{D}$	ECL Down Differential Outputs
FB, $\overline{FB}$	ECL Feedback Differential Inputs
R, $\overline{R}$	ECL Reference Differential Inputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

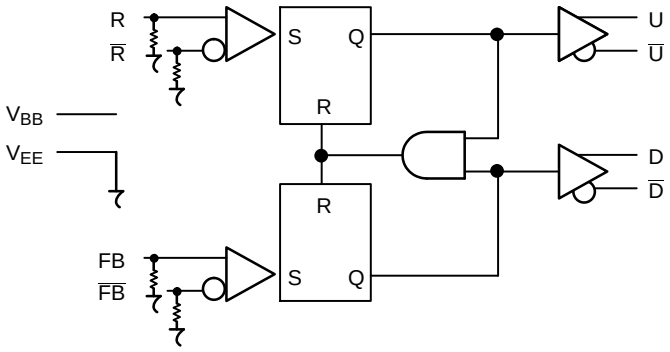


Figure 2. Logic Diagram

Table 2. ATTRIBUTES

Characteristics		Value	
ESD Protection	Human Body Model	> 2 kV	
Moisture Sensitivity (Note 1)		Pb Pkg	Pb−Free Pkg
	SOIC−20	Level 1	Level 3
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
Transistor Count		356 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 to 0 −6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−20 SOIC−20	90 306	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	SOIC−20	30 to 35	°C/W
T_{sol}	Wave Solder Pb Pb−Free			265 265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		38	45		38	47		38	47	mA
V_{OH}	Output HIGH Voltage (Note 3)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 3)	1470	1605	1745	1490	1595	1380	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single−Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7) Vpp < 500 mV Vpp ≧ 500 mV	 1.3 1.5		 3.3 3.3	 1.2 1.4		 3.3 3.3	 1.2 1.4		 3.3 3.3	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{R}$, $\overline{FB}$	0.5 −300			0.5 −300			0.5 −300			μA μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ± 0.3 V.
3. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2 V.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Table 5. LVNECL DC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V (Note 5)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		38	45		38	47		38	47	mA
V_{OH}	Output HIGH Voltage (Note 6)	−1085	−1005	−880	−1025	−955	−880	−1025	−955	−880	mV
V_{OL}	Output LOW Voltage (Note 6)	−1830	−1695	−1555	−1810	−1705	−1620	−1810	−1705	−1620	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1810		−1475	−1810		−1475	−1810		−1475	mV
V_{BB}	Output Voltage Reference	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7) Vpp < 500 mV Vpp ≧ 500 mV	 −2.0 −1.8		 −0.4 −0.4	 −2.1 −1.9		 −0.4 −0.4	 −2.1 −1.9		 −0.4 −0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{R}$, $\overline{FB}$	0.5 −300			0.5 −300			0.5 −300			μA μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ± 0.3 V.
6. All loading with 50 Ω resistor to V_{CC} − 2 V.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Table 6. AC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0 V; V_{EE} = −3.3 V (Note 8)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Fmax	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay R to U, FB to D	430 1200		630 1400	450 1250		650 1450	480 1370		680 1590	ps
V_{PP}	Input Swing (Differential Configuration) (Note 9)	150		1000	150		1000	150		1000	mV
t_{JITTER}	Cycle−to−Cycle Jitter		TBD			TBD			TBD		ps
t_r, t_f	Output Rise/Fall Times	175		475	175		475	175		475	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

8. V_{EE} can vary ± 0.3 V.
9. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40.

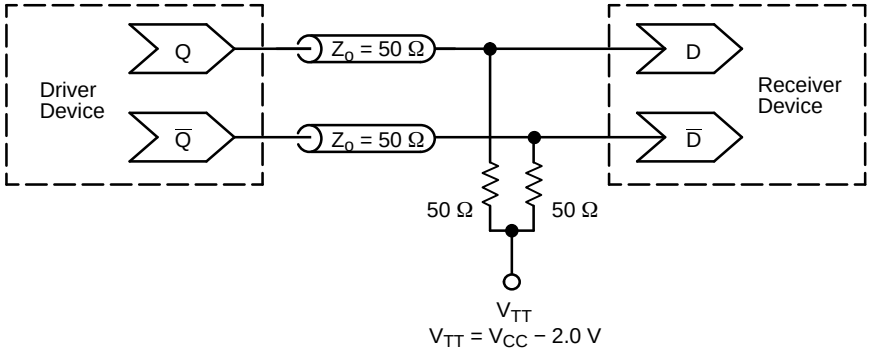


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL40DWG	SOIC−20 (Pb−Free)	38 Units / Rail
MC100LVEL40DWR2G	SOIC−20 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

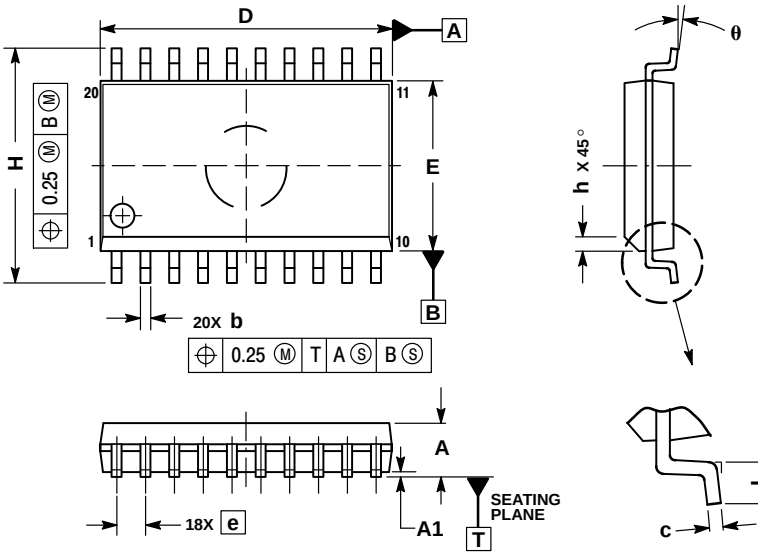
AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

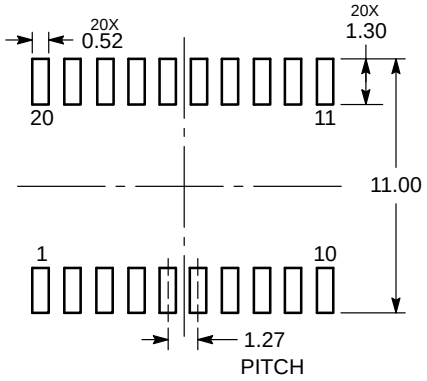
SOIC−20 WB
CASE 751D−05
ISSUE H



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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