

Evaluation Board User's Guide

ADC12L080, 12-Bit, 80 Msps A/D Converter

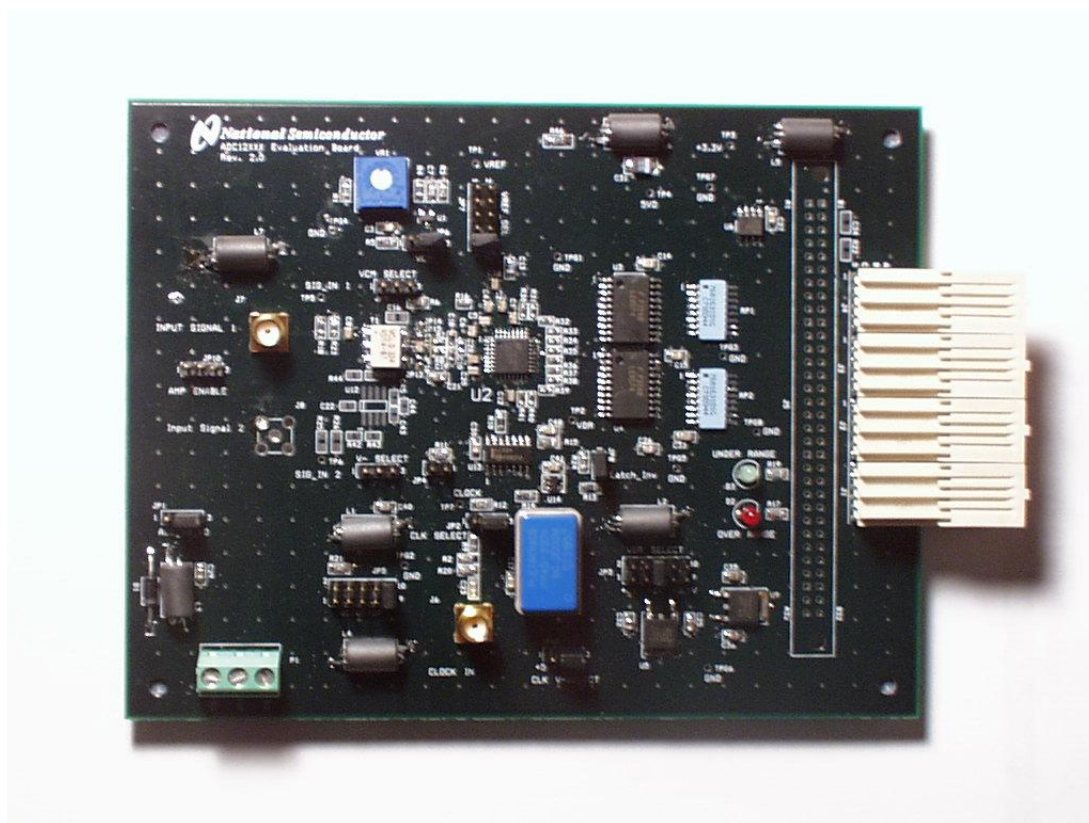


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1.0 Introduction

This ADC12L080 Design Kit (consisting of an Evaluation Board and this manual) is designed to ease evaluation and design-in of National Semiconductor's ADC12L080 12-bit Analog-to-Digital Converter, which operates at speeds up to 80 Msps.

The evaluation board can be used in either of two modes. In the Manual mode suitable test equipment can be used with the board to evaluate the ADC12L080 performance. In the Computer mode evaluation is simplified by connecting the board to the WaveVision™ Digital Interface Board (order number WAVEVSN BRD 4.0), which is connected to a personal computer through a USB port and running WaveVision™ software, operating under Microsoft Windows. The software can perform an FFT on the captured data upon command and, in addition

to a frequency domain plot, shows dynamic performance in the form of SNR, SINAD, THD and SFDR. The WaveVision™ software is available on National's web site at <http://www.national.com/appinfo/adc/wv4.html>.

The signal at the Analog Input to the board is digitized and is available at pins A7 through A18 of J5 and pins B4 through B15 of the WaveVision™ (WV4) connector.

2.0 Board Assembly

The ADC12L080 Evaluation Board comes pre-assembled. Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement and to the Evaluation Board schematic in *Section 8*.

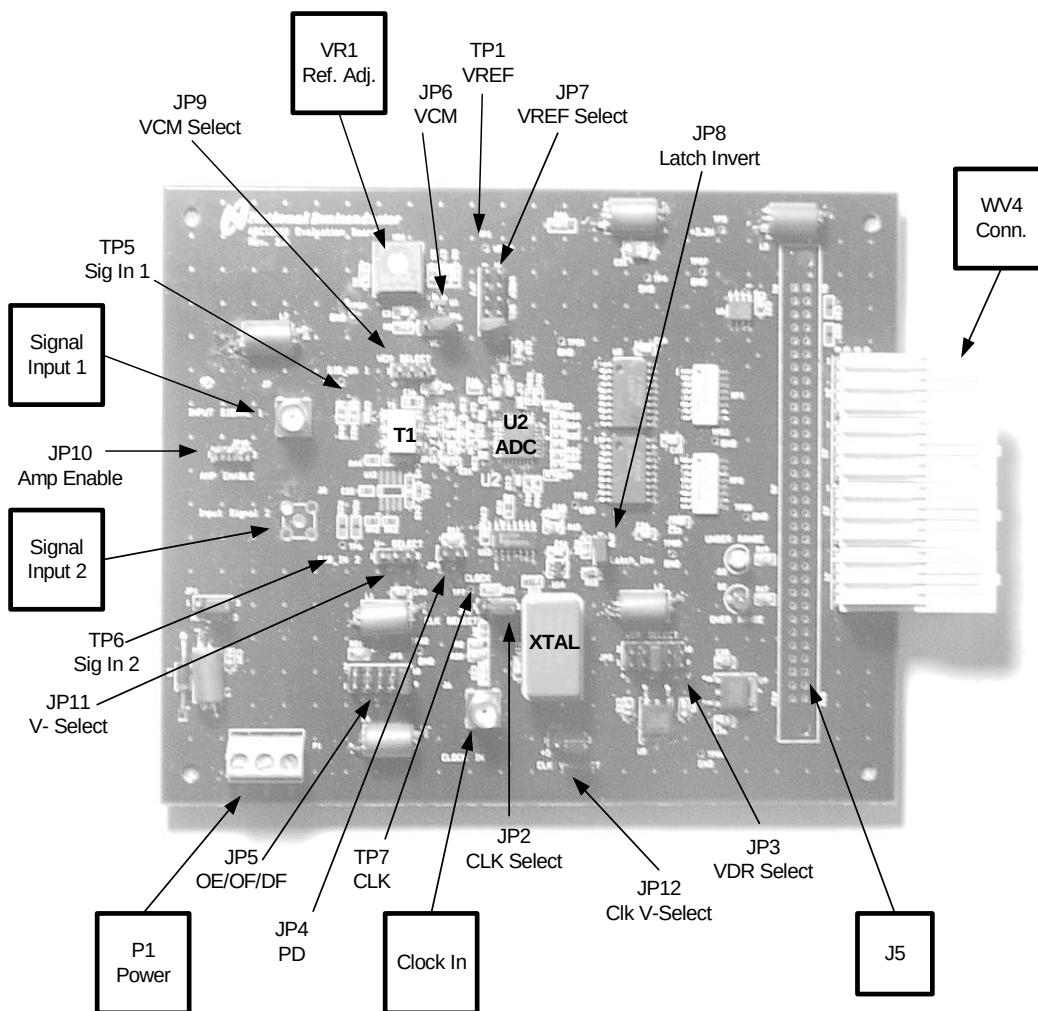


Figure 1. Component and Jumper Locations

3.0 Quick Start

Refer to *Figure 1* for locations of jumpers, test points and major components. The board is configured by default to use a crystal clock source, internal 1.0V reference, and offset binary output data format. Refer to Section 4.0 and the Appendix for more information on jumper settings.

For **Stand-Alone** operation:

1. Install an appropriate crystal into socket Y1. While the oscillator may be soldered to the board, using a socket will allow you to easily change clock frequencies.
2. Connect a clean +5V power supply to pin 1 of Power Connector P1. Pin 2 is ground. Pin 3 of P1 is used to supply -5V to the amplifier circuit (U12) and is not populated on this board.
3. Connect a signal from a 50-Ohm source to Input Signal 1 connector J7. The ADC input signal can be observed at TP5. Because of isolation resistor R18 and the scope probe capacitance, the input signal at TP5 may not have the same frequency response as the ADC input. Be sure to use a bandpass filter before the Evaluation Board.
4. Adjust the input signal amplitude as needed to ensure that the signal does not over-range by examining a histogram of the output data.
5. The digitized signal is available at pins A7 through A18 of J5 and pins B4 through B15 of the WaveVision4 connector. See board schematic of *Section 8*.

For **Computer Mode** operation:

1. Connect the evaluation board to the WaveVision™ Digital Interface Board. See the WaveVision™ Board Manual for operation of that board. Connect the WaveVision™ board to the computer using a USB cable.
2. Connect a clean +5V power supply to pin 1 of Power Connector P1. Pin 2 is ground. Pin 3 of P1 is used to supply -5V to the amplifier circuit (U12) and is not used on this board. The WaveVision™ board gets power from the ADC12L080 Evaluation Board, therefore it does not require a separate power supply.
3. Connect a signal from a 50-Ohm source to Input Signal 1 connector J7. The ADC input signal can be observed at TP5. Because of isolation resistor R18 and the scope probe capacitance, the input signal at TP5 may not have the same frequency response as the ADC input. Be sure to use a bandpass filter before the Evaluation Board.
4. Adjust the input signal amplitude as needed to ensure that the signal does not over-range by examining a histogram of the output data with the WaveVision™ software.
5. See the WaveVision™ Board Manual for instructions for gathering and analyzing data.

4.0 Functional Description

The ADC12L080 Evaluation Board schematic is shown in *Section 8*. A list of test points and jumper settings can be found in the Appendix.

4.1 Input (signal conditioning) circuitry

The input signal to be digitized should be applied to SMA connector J7. This 50 Ohm input is intended to accept a low-noise sine wave signal of 2V peak-to-peak amplitude. To accurately evaluate the dynamic performance of this converter, the input test signal will have to be passed through a high-quality bandpass filter with at least 14-bit equivalent noise and distortion characteristics.

Signal transformer T1 provides single-ended to differential conversion. The voltage V_{RM} from the ADC, or an adjustable voltage from VR1 sets the common mode of the input signal by biasing the center tap of the secondary of T1. When VR1 is used, the voltage should be set within the acceptable range of the ADC, 0.5 to 2.0V. Jumper JP6 selects the source of the common mode voltage. The default setting is to use V_{RM} from the ADC. Solder jumpers JP15 and JP16 must be shorted when using the Transformer T1 circuit. Solder jumpers JP13 and JP14 must be open.

There is an alternate signal path using Input Signal 2 connector J8, with amplifier U12 (National Semiconductor LMH6550) providing the single-ended to differential conversion. Solder jumpers JP13 and JP14 must be shorted when using the amplifier circuit. Solder jumpers JP15 and JP16 must be open. Select a common mode voltage with JP9. Set JP11 to select the negative supply for U12. It can be set to ground or a -5V supply from P1 pin 3. (This option is not applicable on the ADC12L080 Evaluation Board.)

It may be necessary to increase the value of input capacitors C18 and C19 for testing at low input frequencies. For Nyquist operation, the RC poles of the input RC composed of R7 and C18 plus the 8pF and of R8 and C19 plus 8pF should be approximately equal to the ADC clock frequency. The 8pF is the ADC input capacitance. For higher input frequencies, these RC poles should be about twice the input frequency.

4.2 ADC reference circuitry

The ADC12L080 can use an internal 1.0V reference, or an external reference. The reference is selected using jumper JP7.

The default position for JP7 is pins 9 and 10, which selects the internal 1.0V reference.

An adjustable reference circuit is provided on the board. The simple circuit here is not temperature stable and is not recommended for your final design solution. The reference circuit will generate a voltage in the range of 0 to 2.4V. The ADC12L080 is specified to operate with V_{REF} in the range of 0.8 to 1.5 V, with a nominal value of 1.0V. The reference voltage can be monitored at test point TP1 and is set with VR1. This circuit can also be used as a common mode voltage source (see section 4.1). Short pins 5 and 6 on JP7 to use this reference.

4.3 ADC clock circuit

The clock signal applied to the ADC is selected with jumper JP2. A standard crystal oscillator can be installed in a socket at Y1 (or a surface mount crystal may be installed) and selected with jumper JP2 pins 2 and 3 shorted together (default). To use a different clock source, connect the signal to connector J6 and select

pins 1 and 2 of jumper JP2. The ADC clock frequency can be monitored at test point TP7. Note that any external clock source must have TTL/CMOS levels. Also, if using an external clock, the oscillator at Y1 should be removed.

4.4 Digital Data Output

The digital output data from the ADC12L080 is available at the WV4 connector, a 96-pin Euro connector shown as J1-J4 on the schematic. Series resistors RP1 and RP2 isolate the ADC from the load circuit to reduce noise coupling into the ADC.

4.5 Power Supply Connections

Power to this board is supplied through power connector P1. The only supply needed is +5V at pin 1 plus ground at pin 2. If the amplifier circuit of U12 is used, a -5V supply may be applied to P1 pin 3.

When using the ADC12L080 Evaluation Board with the the WaveVision™ Digital Interface Board, a 5V logic power supply for the interface board is passed through the WV4 connector to the Digital Interface Board.

4.6 Power Requirements

Voltage and current requirements for the ADC12L080 Evaluation Board mode are:

For the ADC12L080, ADC12010 and the ADC12020:

- +5.0V at 500 mA (1A when connected to the Digital Interface Board).

There is no need for a -5V supply unless the amplifier circuit of U12 is installed.

5.0 Installing the ADC12L080 Evaluation Board

The evaluation board requires power supplies as described in Section 4.5. An appropriate signal source should be connected to the Signal Input SMA connector J7. When evaluating dynamic performance, an appropriate signal generator (such as the HP8644B, HP8662A or the R&S SME-03) with 50 Ohm source impedance should be connected to the Analog Input BNC J7 through an appropriate bandpass filter as even the best signal generator available can not produce a signal pure enough to evaluate the dynamic performance of an ADC.

If this board is used in conjunction with the the WaveVision™ 4.0 Digital Interface Board and WaveVision™ software, a USB must be connected between the Digital Interface Board and the host. See the the WaveVision™ 4.0 Digital Interface Board manual for details.

6.0 Obtaining Best Results

Obtaining the best results with any ADC requires both good circuit techniques and a good PC board layout. The layout is taken care of with the design of this evaluation board.

6.1 Clock Jitter

When any circuitry is added after a signal source, some jitter is almost always added to that signal. Jitter in a clock signal, depending upon how bad it is, can degrade

dynamic performance. We can see the effects of jitter in the frequency domain (FFT) as "leakage" or "spreading" around the input frequency, as seen in Figure 2a. Compare this with the more desirable plot of Figure 2b. Note that all dynamic performance parameters (shown to the right of the FFT) are improved by eliminating clock jitter.

Because the divided signal from the Digital Interface Board and the oscillator at Y1 are not synchronized, bad data will sometimes be taken because we are latching data when the outputs are in transition. This data might be as you see in Figure 3 or Figure 4.

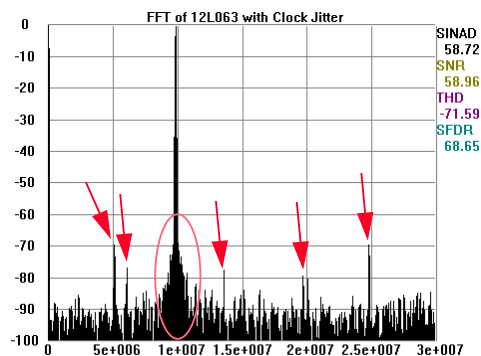


Figure 2a. Jitter causes a spreading around the input signal, as well as undesirable signal spurs.

The problem of Figure 3 is obvious, but it is not as easy to see the problem in Figure 4, where the only thing we see is small excursions beyond the normal envelope. Compare Figure 3 and Figure 4 with Figure 5.

If your data capture results in something similar to what is shown here in Figure 3 or in Figure 4, take another sample. It may take a few trials to get good data.

The use of WAVEVSN BRD 4.0 Digital Interface Board eliminates this problem, so that board is recommended.

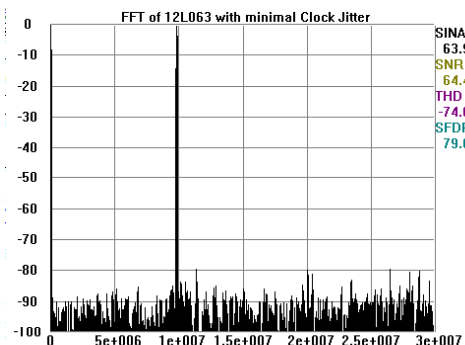


Figure 2b. Eliminating or minimizing clock jitter results in a more desirable FFT that is more representative of how the ADC actually performs.

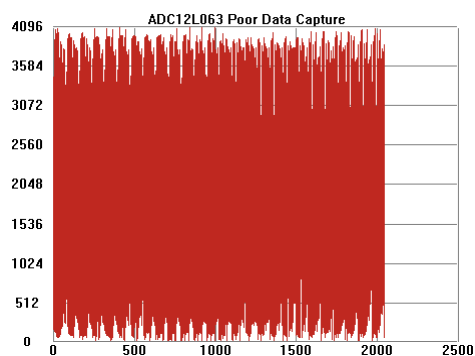


Figure 3. Poor data capture resulting from trying to capture data while the ADC outputs are in transition

6.2 Coherent Sampling

Artifacts can result when we perform an FFT on a digitized waveform, producing inconsistent results when testing repeatedly. The presence of these artifacts means that the ADC under test may perform better than the measurements would indicate.

We can eliminate the need for windowing and get more consistent results if we observe the proper ratios between the input and sampling frequencies. We call this *coherent sampling*. Coherent sampling greatly increases the spectral resolution of the FFT, allowing us to more accurately evaluate the spectral response of the A/D converter. When we do this, however, we must be sure that the input signal has high spectral purity and stability and that the sampling clock signal is extremely stable with minimal jitter.

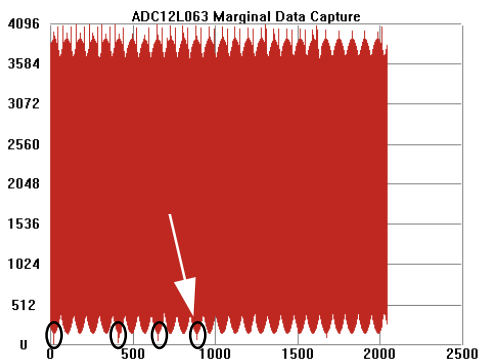


Figure 4 Marginal data capture that results from trying to capture data that is near but not right at the point where the ADC outputs are in transition.

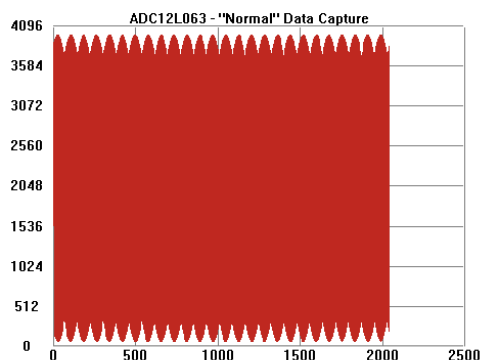


Figure 5. Normal data capture.

Coherent sampling of a periodic waveform occurs when a prime integer number of cycles exists in the sample window. The relationship between the number of cycles sampled (CY), the number of samples taken (SS), the signal input frequency (f_{in}) and the sample rate (f_s), for coherent sampling, is

$$\frac{CY}{SS} = \frac{f_{in}}{f_s}$$

CY, the number of cycles in the data record, must be a prime integer number and SS, the number of samples in the data record, must be a factor of 2 integer.

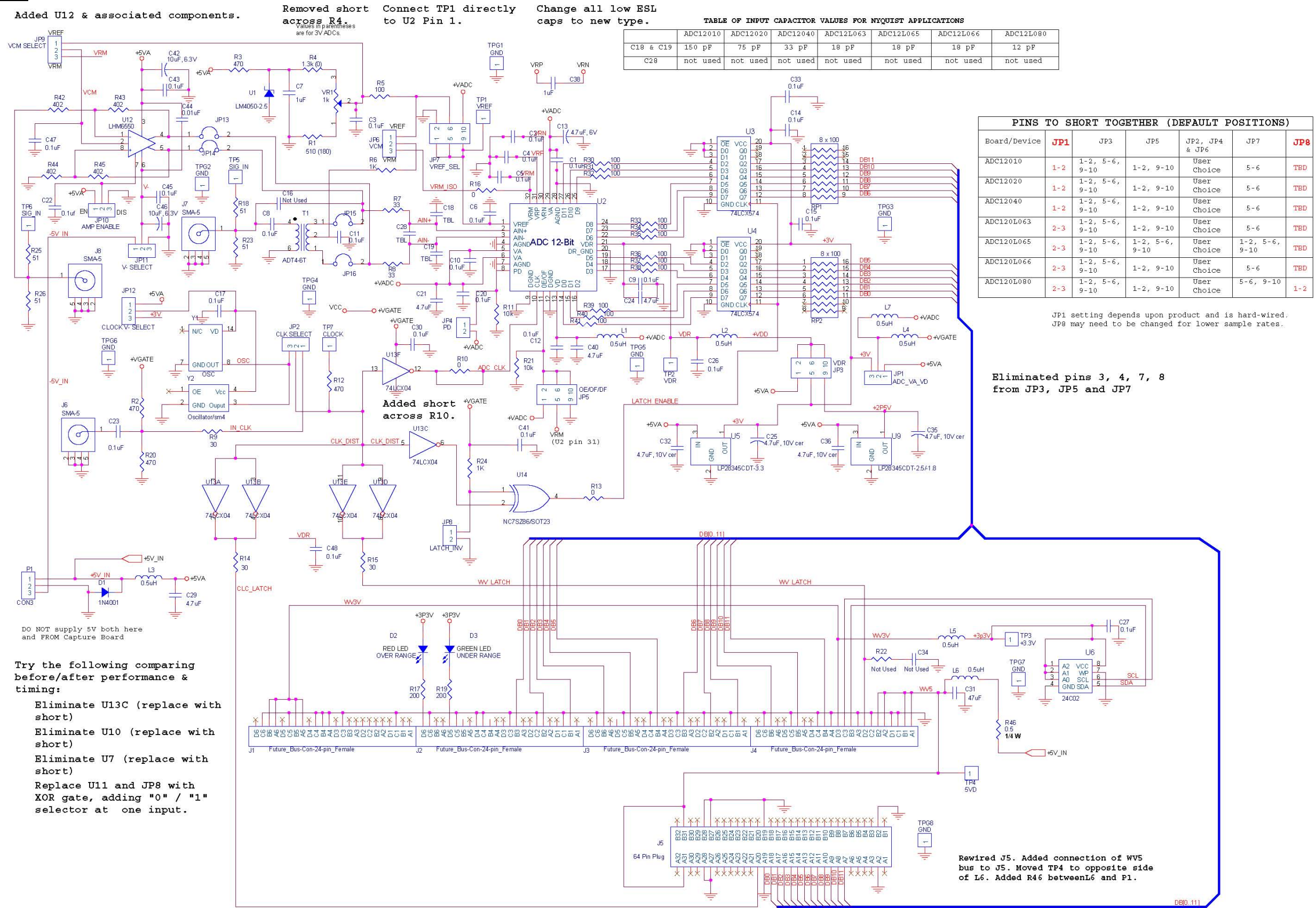
Further, f_{in} (signal input frequency) and f_s (sampling rate) should be locked to each other so that the relationship between the two frequencies is exact. Locking the two signal sources to each other also causes whatever sample-to-sample clock edge timing variation (jitter) that is present in the two signals to cancel each other.

Windowing (an FFT Option under WaveVision™) should be turned off for coherent sampling.

7.0 Evaluation Board Specifications

Board Size:	6" x 4.63" (15.25 cm x 11.75 cm)
Power Requirements:	+5.0V, 1 A (ADC12L080 and WaveVision™ 4.0 Board)
Clock Frequency Range:	20 MHz to 80 MHz
Analog Input	
Nominal Voltage:	1.4V _{p-p}
Impedance:	50 Ohms

8.0 Hardware Schematic



9.0 Evaluation Board Bill of Materials

Item	Qty	Reference	Part	Source
1	8	C1, C2, C4, C5, C6, C10, C12, C20	0.1μF, 6.3V or 10V	0805, LOW ESL, 10V; muRata Type LLL2191X1A104MA01B
2	2	C8, C11	0.1μF, 6.3V or 10V	0805, LOW ESL, 10V; muRata Type LLL2191X1A104MA01B
3	12	C3, C9, C14, C15, C17, C23, C26, C27, C30, C33, C41, C48	0.1μF, 6.3V or 10V	Type 0805
4	-	C43, C45, C47	not used	n/a
5	1	C7	1μF, 6.3V or 10V	Type 0805
6	1	C13	4.7μF, 6V	Type 0805
7	2	C18, C19	12 pF, 6.3V or 10V	Type 0603
8	4	C21, C24, C29, C40	4.7μF, 6.3V or 10V	Type 0805
9	-	C22	not used	n/a
10	4	C25, C32, C35, C36	4.7μF, 6.3V or 10V cer	Type 1206
11	1	C31	47μF, 6.3V or 10V	Type 3528
12	1	C38	1μF, 6.3V or 10V	0805, LOW ESL, 10V; muRata Type LLL2191X1A105MA01B
13	-	C42, C46	not used	n/a
14	-	C44	not used	n/a
15	-	C16, C34	Not Used	n/a
16	-	C28	not used	n/a
17	1	D1	1N4001 - DO-41 Pkg	Various
18	1	D2	RED LED	Various; 0.1" Spacing
19	1	D3	GREEN LED	Various; 0.1" Spacing
20	2	JP2, JP12	3-Pin Post Header	DigiKey # WM6503-ND
21	-	JP9, JP10, JP11,	not used	n/a
22	1	JP6,	3-Pin Post Header	DigiKey # WM6503-ND
23	3	JP3, JP5, JP7	5 x 2 Post Header	DigiKey # 22-28-4105-ND
24	2	JP4, JP8	2-Pin Post Header	DigiKey # A19350-ND
25	4	JP13, JP14, JP15, JP16	Selected Solder Short	n/a
26	-	JP1	Not Used (hard-wired)	n/a
27	4	J1, J2, J3, J4	FUTUREBUS Connector	AMP/Tyco 536501-1
28	-	J5	64 Pin Plug - not used	N/A
29	1	J6	SMA Connector	DigiKey # A25691-ND
30	1	J7	SMA Connector	DigiKey # A25691-ND
31	-	J8	not used	DigiKey # A25691-ND
32	7	L1, L2, L3, L4, L5, L6, L7	100 uH	DigiKey # 445-1155-1-ND or TDK # NLC322522T-331K
33	1	P1	2-Pin Terminal Block	DigiKey # ED1609-ND
34	2	RP1, RP2	8 x 100	DigiKey # 766-163-R101-ND or DigiKey # 768-163-R101-ND
35	1	R1	180 Ohms, 5%, 1/10 Watt	Type 0805
36	4	R2, R3, R12, R20	470 Ohms, 5%, 1/10 Watt	Type 0805
37	1	R4	0 Ohms	Type 0805
38	1	R5	100 Ohms, 5%, 1/10 Watt	Type 0805
39	2	R6, R24	1K Ohms, 5%, 1/10 Watt	Type 0805
40	2	R8, R7	33 Ohms, 5%, 1/10 Watt	Type 0603
41	3	R9, R14, R15	30 Ohms, 5%, 1/10 Watt	Type 0805
42	2	R10, R13	0 Ohms	Type 0805
43	2	R11, R21	10k Ohms, 5%, 1/10 Watt	Type 0805
44	1	R16	0 Ohms	Type 0603
45	2	R17, R19	200 Ohms, 5%, 1/10 Watt	Type 0805
46	1	R18	100 Ohms, 5%, 1/10 Watt	Type 0805
47	1	R23	51 Ohms, 5%, 1/10 Watt	Type 0805
48	-	R25, R26 [used with U12 amp]	not used	n/a

ADC12L080 Evaluation Board Bill of Materials (cont'd)

<u>Item</u>	<u>Qty</u>	<u>Reference</u>	<u>Part</u>	<u>Source</u>
49	12	R30, R31, R32, R33, R34, R35, R36, R37,R38, R39, R40, R41	100 Ohms, 5%, 1/10 Watt	Type 0603
50	4	R42, R43, R44, R45	402 Ohms, 1%, 1/10 Watt	Type 0603
51	1	R46	0.5 Ohms, 5 %, 1/10 Watt	Type 0805
52	-	R22	Not Used	Type 0805
53	1	TP1, TP2, ,TP3, TP4, TP5, TP6, TP7, TPG1, TPG2, TPG3, TPG4, TPG5, TPG6, TPG7, TPG8	Breakable Header	DigiKey # S1012-36-ND
54	1	T1	Signal Transformer	MiniCircuits #ADT4-6T
55	1	U1	LM4050AIM3-2.5	National Semiconductor
56	1	U2	ADC12L080CIVY	National Semiconductor
57	1	U3, U4	74AC574SC	Fairchild Semiconductor
58	2	U5	LP8345CDT-3.3	National Semiconductor
59	1	U6	24C02N	Various
60	1	U9	LP8345CDT-2.5	National Semiconductor
61	-	U12	not used	n/a
62	1	U13	74AC04SC	Fairchild Semiconductor
63	1	U14	NC7SZ86M5	Fairchild Semiconductor
64	1	VR1	1k Potentiometer	DigiKey # 3386F-103-ND
65	1	Y1	80 MHz Oscillator	Pletronics P1145-HCV/3SV-80.0M
66	1	Y2	Oscillator / SMD (not used)	n/a
67	1	--	4-Pin full-size oscillator socket	DigiKey # A462-ND
68	10	--	Shorting Jumpers	DigiKey #S9601-ND

APPENDIX

A1.0 Operating in the Computer Mode

The ADC12L080 Evaluation Board is compatible with the WaveVision™ 4.0 Digital Interface Board and WaveVision™ software. When connected to the Digital Interface Board, data capture is easily controlled from a personal computer operating in the Windows environment. The data samples that are captured can be observed on the PC video monitor in the time and frequency domains. The FFT analysis of the captured data yields insight into system noise and distortion sources and estimates of ADC dynamic performance such as SINAD, SNR and THD.

See the Digital Interface Board manual for more information.

A2.0 Summary Tables of Test Points, Connectors, and Jumper Settings

A2.1 Test Points

Test Points on the ADC12L080 Evaluation Board

TP 1	ADC Reference Voltage
TP 2	ADC output driver supply voltage
TP 3	+3.3V from the WaveVision™ 4.0 Digital Interface Board
TP 4	+5V supply
TP 5	Signal Input test point (Input Signal 1)
TP 6	Signal Input test point (Signal Input 2)
TP 7	ADC clock
TPG1 – TPG8	Ground

A2.2 Connectors

P1 Connector - Power Supply Connections

P1-1	+V	+5V Power Supply
P1-2	GND	Power Supply Ground
P1-3	-V	-5V Power Supply for Amplifier circuit (U12) – Not used with the ADC12L080

A2.3 Jumper settings

Note: Default settings are in **bold**

JP1 Jumper – ADC Analog/Digital power supply +VADC selection jumper settings

Connect 1-2	For +5V ADC's - DO NOT SELECT THIS FOR ADC12L080
Connect 2-3	For +3.3V ADC's (this is the correct setting for ADC12L080)

JP2 Jumper - ADC Clock selection jumper settings

Connect 1-2	Use external CLOCK IN from J6
Connect 2-3	Use crystal oscillator

JP3 Jumper - ADC driver power supply selection jumper settings

Connect 1-2	Vdr = 5V – DO NOT SELECT THIS FOR ADC12L080
Connect 5-6	Vdr = 3.3V
Connect 9-10	Vdr = 2.5V

JP4 Jumper – Power Down

Connect 1-2	Put ADC in Power Down mode
1-2 OPEN	ADC is in normal operation

JP5 Jumper – OE/OF/DF selection jumper settings

Connect 1-2	Select Output format of 2's complement
Connect 5-6	Not applicable for ADC12L080
Connect 9-10	Select Output format of Offset Binary

JP6 Jumper - Vcm selection jumper settings

Connect 1-2	Use voltage from VR1 as common mode voltage
Connect 2-3	Use common mode voltage from ADC

JP7 Jumper – VREF selection jumper settings

Connect 1-2	Not applicable for ADC12L080
Connect 5-6	Use voltage from VR1 as reference voltage
Connect 9-10	Use internal 1.0V reference

JP8 Jumper – Latch Invert

Connect 1-2	Invert clock for latches
1-2 OPEN	Do not invert clock

JP9, JP10, and JP11 are not used with the ADC12L080

JP12 Jumper – Crystal power supply selection jumper settings

Connect 1-2	For +5V Crystals
Connect 2-3	For +3.3V Crystals

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