LM10524 Triple Buck Power Management Unit

Check for Samples: LM10524

FEATURES

- **Three Highly Efficient Programmable Buck Regulators**
  - **Integrated FETs with Low R_{DSON}**
  - **Bucks Operate with Their Phases Shifted to Reduce the Input Current Ripple and Capacitor Size**
  - **Programmable Output Voltage via the SPI Interface**
  - **Over and Under-Voltage-Lockout**
  - **Automatic Internal Soft Start with Power-On-Reset**
  - **Current Overload and Thermal Shutdown Protection**
  - **PFM Mode for High Efficiency at Light Load Conditions**
- **Power-Down Data Protection Enhances Data Integrity**
- **Bypass Mode Available on Buck 1**
- **Sleep Mode to Save Power During Idle Times**
  - **DEVSLP Function**
- **SPI-Programmable Interrupt Comparator (2.0V to 4.0V)**
- **Factory Programmable Startup Sequencing for Varied Controllers**
- **Fast Startup for all Voltage Rails in about 3.5ms to PWR_OK**
- **Fast Turn-off / Active Discharge on Regulator Outputs**

APPLICATION

- **Solid-State Drives**

DESCRIPTION

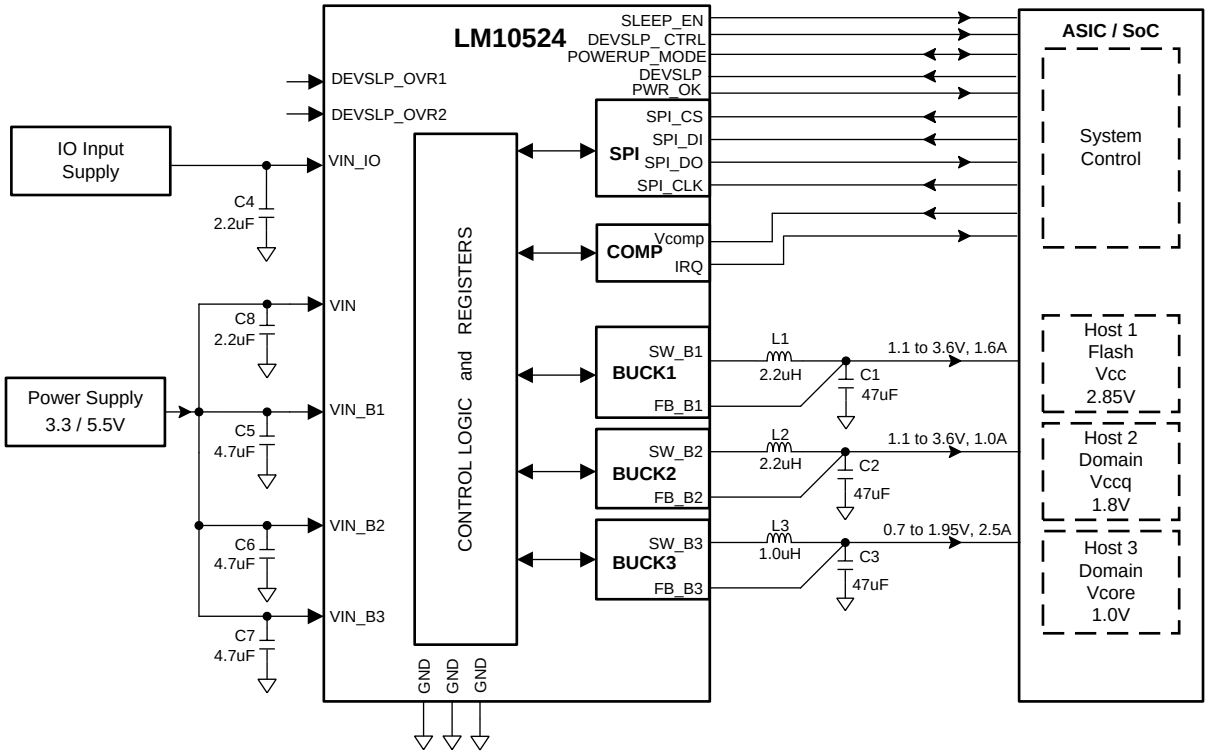
LM10524 is an advanced PMU containing three configurable, high-efficiency buck regulators for supplying variable voltages. The device is ideal for supporting ASIC and SOC designs for SSD and Flash drives.

The LM10524 can operate cooperatively with an ASIC to optimize the supply voltage for low-power conditions and to control power saving modes via the SPI interface.

KEY SPECIFICATIONS

- **Single input rail with wide range: 3.3 to 5.5V**
- **Programmable Buck Regulator Outputs:**
  - **Buck 1: 1.1V to 3.6V; 1.6A**
  - **Buck 2: 1.1V to 3.6V; 1A**
  - **Buck 3: 0.7V to 1.95V; 2.5A**
- **±3% feedback voltage accuracy**
- **Up to 95% efficient buck regulators**
- **2MHz switching frequency for smaller inductor size**
- **2.815mm, 3.215mm, 0.4mm pitch, 46 bump micro SMD package**

Typical Application Diagram



Overview

The LM10524 contains three buck converters. Supply Specification below lists the output characteristics of the power regulators.

Supply Specification

Regulator	Default V_{OUT} at Start-Up	V_{OUT} if DEVSLP=High (DEVSLP mode)	Output Voltage Range	Max Output Current
BUCK1(1)	2.85 V	OFF	1.1V to 3.6V; 50 mV steps	1.6A
BUCK2(1)	1.8 V	OFF	1.1V to 3.6V; 50 mV steps	1.0A
BUCK3(1)	1.0V	OFF	0.7V to 1.95V; 10mV steps	2.5A

(1) Default voltage values are determined when working in PWM mode. Voltage may be 0.8-1.6% higher when in PFM mode..

Connection Diagram And Package Marking

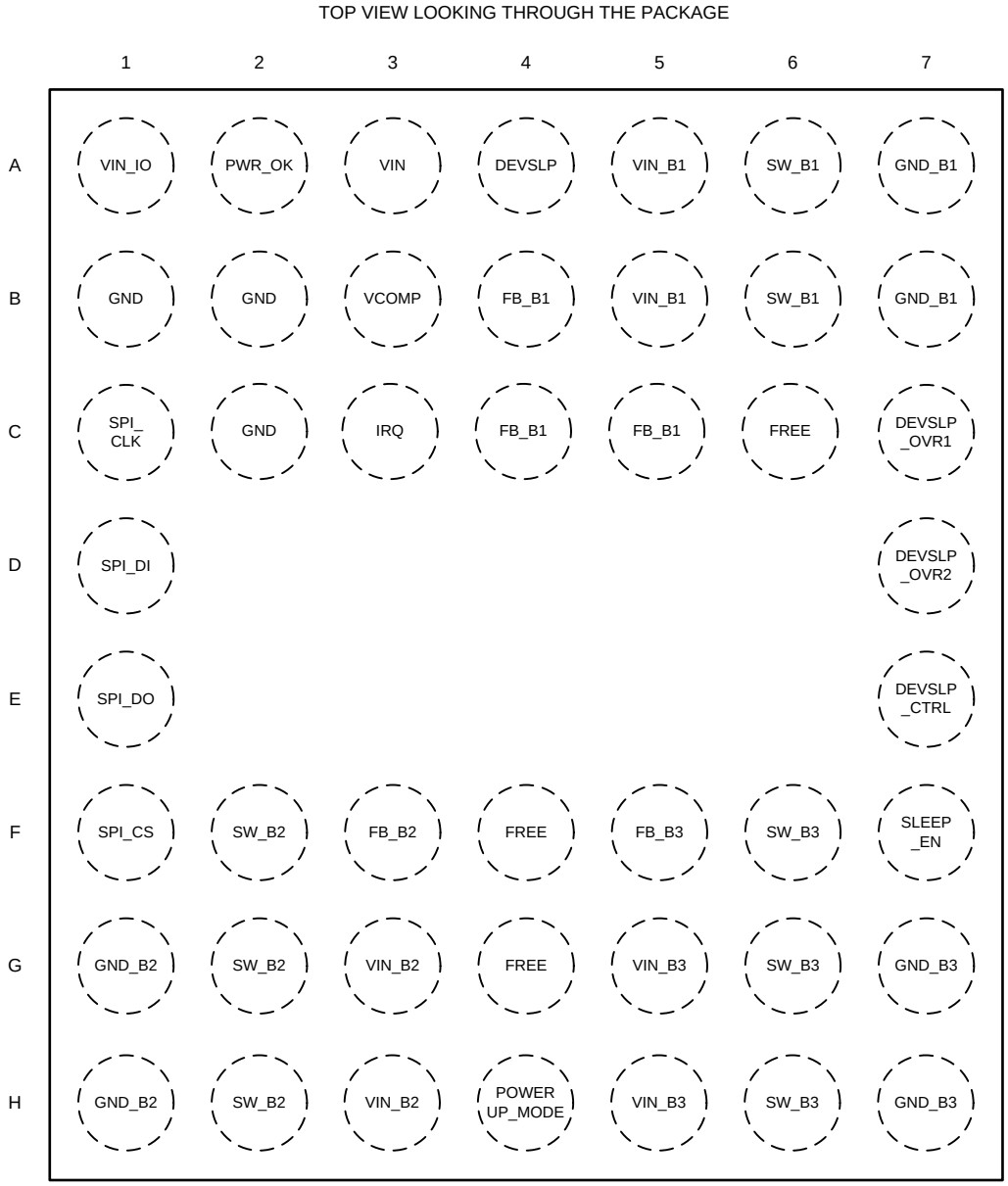


Figure 1. 46 Bump Micro SMD with 0.4mm Pitch

Table 1. 9.0 LM10524 Pin Description

Pin #	Pin Name	I/O(1)	Type(2)	Functional Description
A4	DEVSLP	I	D	Digital Input Control Signal for entering Device Sleep Mode. Input activates the device sleep function in conjunction with DEVSLP_OVR1, DEVSLP_OVR2, and PowerUp_mode. This is an active High pin with an option for an internal pullup resistor. Turns off all outputs and internal oscillator.
E7	DEVSLP_CTRL	O	D	Indicates DevSLP signal is active but drives low when device is in SLEEP mode.
C7	DEVSLP_OVR1	I	D	Used to gate activation of device sleep.
D7	DEVSLP_OVR2	I	D	Used to gate activation of device sleep.
C5	FB_B1	I/O	A	Buck Switcher Regulator 1 - Voltage output feedback plus Bypass Power.
B4	FB_B1	I/O	A	Buck Switcher Regulator 1 - Voltage output feedback plus Bypass Power.
C4	FB_B1	I/O	A	Buck Switcher Regulator 1 - Voltage output feedback plus Bypass Power.
F3	FB_B2	I	A	Buck Switcher Regulator 2 - Voltage output feedback.
F5	FB_B3	I	A	Buck Switcher Regulator 3 - Voltage output feedback.
C6	FREE			Not Used.
F4	FREE			Not Used.
G4	FREE			Not Used.
B1	GND	G	G	Ground. Connect to system Ground.
B2	GND	G	G	Ground. Connect to system Ground.
C2	GND	G	G	Ground. Connect to system Ground.
A7	GND_B1	G	P	Buck Switcher Regulator 1 - Power ground for Buck Regulator.
B7	GND_B1	G	P	Buck Switcher Regulator 1 - Power ground for Buck Regulator.
G1	GND_B2	G	P	Buck Switcher Regulator 2 - Power ground for Buck Regulator.
H1	GND_B2	G	P	Buck Switcher Regulator 2 - Power ground for Buck Regulator.
G7	GND_B3	G	P	Buck Switcher Regulator 3 - Power ground for Buck Regulator.
H7	GND_B3	G	P	Buck Switcher Regulator 3 - Power ground for Buck Regulator.
C3	IRQ	O	D	Interrupt. Digital Output of Comparator to signal interrupt condition.
A2	PWR_OK	O	D	PWR_OK Signal, Push Pull output.
H4	POWERUP _MODE	I/O	D	Used to indicate SSD initialization is complete. Once initialization is complete, this pin should be externally pulled low to allow Sleep mode activation via DEVSLP
F7	SLEEP_EN	O	D	Active high output indicates device is in Sleep Mode.
C1	SPI_CLK	I	D	SPI Interface - serial clock input.
F1	SPI_CS	I	D	SPI Interface - chip select.
D1	SPI_DI	I	D	SPI Interface - serial data input.
E1	SPI_DO	O	D	SPI Interface - serial data output.
A6	SW_B1	I/O	P	Buck Switcher Regulator 1 - Power Switching node, connect to inductor.
B6	SW_B1	I/O	P	Buck Switcher Regulator 1 - Power Switching node, connect to inductor.
F2	SW_B2	I/O	P	Buck Switcher Regulator 2 - Power Switching node, connect to inductor.
G2	SW_B2	I/O	P	Buck Switcher Regulator 2 - Power Switching node, connect to inductor.
H2	SW_B2	I/O	P	Buck Switcher Regulator 2 - Power Switching node, connect to inductor.
F6	SW_B3	I/O	P	Buck Switcher Regulator 3 - Power Switching node, connect to inductor.
G6	SW_B3	I/O	P	Buck Switcher Regulator 3 - Power Switching node, connect to inductor.
H6	SW_B3	I/O	P	Buck Switcher Regulator 3 - Power Switching node, connect to inductor.
B3	VCOMP	I	A	Analog Input for Comparator.
A3	VIN	I	P	Power supply Input Voltage — must be present for device to work; decouple closely to D7.
A5	VIN_B1	I	P	Buck Switcher Regulator 1 - Power supply voltage input for power stage PFET, if Buck 1 is not used, tie to ground to reduce leakage.
B5	VIN_B1	I	P	Buck Switcher Regulator 1 - Power supply voltage input for power stage PFET, if Buck 1 is not used, tie to ground to reduce leakage.

(1) I: Input Pin, O: Output Pin
(2) A: Analog Pin, D: Digital Pin, G: Ground, P: Power Connection

Table 1. 9.0 LM10524 Pin Description (continued)

Pin #	Pin Name	I/O(1)	Type(2)	Functional Description
G3	VIN_B2	I	P	Buck Switcher Regulator 2 - Power supply voltage input for power stage PFET, if Buck 2 is not used, tie to ground to reduce leakage.
H3	VIN_B2	I	P	Buck Switcher Regulator 2 - Power supply voltage input for power stage PFET, if Buck 2 is not used, tie to ground to reduce leakage.
G5	VIN_B3	I	P	Buck Switcher Regulator 3 - Power supply voltage input for power stage PFET.
H5	VIN_B3	I	P	Buck Switcher Regulator 3 - Power supply voltage input for power stage PFET..
A1	VIN_IO	I	A	Supply Voltage for Digital Interface.

Table 2. Device Information

Part Number	Buck 1 Bypass	FPWM Default	Package Type	Product Identification	Supplied as
LM10524TME	Disabled	All Bucks	micro SMD	V088	250 Tape & Reel
LM10524TMX					1000 Tape & Reel
LM10524TME-A	Disabled	Bucks 2 + 3	micro SMD	V089	250 Tape & Reel
LM10524TMX-A					1000 Tape & Reel

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Pins	Min	Max	Units
VIN, VCOMP	-0.3	6	V
VIN_IO, VIN_B1, VIN_B2, VIN_B3, SPI_CS, SPI_DI, SPI_CLK, SPI_DO, DEVSLP, DEVSLP_CTRL, SLEEP_EN, POWERUP MODE, SW_1, SW_2, SW_3, FB_1, FB_2, FB_3, PWR_OK, IRQ, DEVSLP_OVR1, DEVSLP_OVR2	-0.3	V_{VIN}	
Junction Temperature, T_{J-MAX}		150	°C
Storage Temperature	-65	150	
ESD Rating, HBM – Human Body Model		1	kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Operating Ratings(1)(2)(3)

Pins	Min	Max	Units
VIN_B1, VIN_B2, VIN_B3, VIN	3	5.5	V
VIN_IO	1.72	V_{VIN}	
All other Input Pins	0	V_{VIN}	
Junction Temperature, T_J	-30	125	°C
Ambient Temperature, T_A	-30	85	
Junction-to-Ambient Thermal resistance, θ_{JA}		40	°C/W
Maximum Continuous Power Dissipation, PD_{MAX}		1	W

(1) Internal thermal shutdown protects device from permanent damage. Thermal shutdown engages at TJ = +140°C and disengages at TJ = +120°C (typ.). Thermal shutdown is ensured by design.
(2) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junvction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(3) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage. (See General Electrical Characteristics).

General Electrical Characteristics (1) (2)

Unless otherwise noted, V_{VIN} = 5.0V where: V_{VIN}=V_{VIN_B1} = V_{VIN_B2} = V_{VIN_B3}. V_{VIN_I0} = 3.0V.
The application circuit used is the one shown in “Typical Application Circuit".
Limits in standard typeface are for T_J = 25°C.
Limits in **boldface** type apply over the full operating junction temperature range of -30°C ≤ T_A=T_J ≤ +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{Q(DEVSLP)}$	Quiescent supply current.	DevSLP=High No load.		50	**200**	µA
UNDER/OVER VOLTAGE LOCK OUT						
V_{UVLO_RISING}			**2.7**	2.9	**3.135**	V
$V_{UVLO\_FALLING}$			**2.45**	2.6	**2.75**	
V_{OVLO_RISING}				6.05		
$V_{OVLO\_FALLING}$				5.75		
DIGITAL INTERFACE						
V_{IL}	Logic Input Low	SPI_CS, SPI_DI, SPI_CLK, POWERUP_MODE (3)			**0.3*V_{VIN_IO}**	V
V_{IH}	Logic Input High		**0.7*V_{VIN_IO}**			
V_{IL}	Logic Input Low	DEVSLP_OVR1, DEVSLP_OVR2 (3)			**0.3*V_{VIN}**	
V_{IH}	Logic Input High		**0.7*V_{VIN}**			
V_{IL}	Logic Input Low	DEVSLP (3)			**0.3V**	
V_{IH}	Logic Input High		**1.2V**			
V_{OL}	Logic output Low	IRQ (at 2mA load), SPI_DO, DEVSLP_CTRL (3), SLEEP_EN (3),PWR_OK			**0.2*V_{VIN_IO}**	
V_{OH}	Logic output High		**0.8*V_{VIN_IO}**			
I_{IL}	Input Current, pin driven low	SPI_CS, SPI_DI, SPI_CLK	-2			µA
		DEVSLP	-5			
I_{IH}	Input Current, pin driven high	SPI_CS, SPI_DI, SPI_CLK,DEVSLP			2	
f_{SPI_MAX}	SPI max frequency				**10**	MHz

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.

Buck 1 Electrical Characteristics(1)(2)(3)

Unless otherwise noted, V_{VIN} = 5.0V where: V_{VIN}=V_{VIN_B1} = V_{VIN_B2} = V_{VIN_B3}.
The application circuit used is the one shown in "Typical Application Circuit".
Limits in standard typeface are for T_J = 25°C.
Limits in **boldface** type apply over the full operating junction temperature range of -30°C ≤ T_A=T_J ≤ +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_Q	DC Bias Current in VIN	No Load, PFM Mode		15	**50**	µA
$I_{OUT-MAX}$	Continuous maximum load current(4)(5)(6)	Buck 1 enabled, switching in PWM	**1.6**			A
I_{PEAK}	Peak switching current limit	Buck 1 enabled, switching in PWM	**1.9**	2.2	**2.8**	
η	Efficiency peak, Buck 1(4)	I_{OUT} = 0.3 A, V_{VIN} = 3.3V		90		%
F_{SW}	Switching Frequency		**1.75**	2	**2.3**	MHz
C_{IN}	Input Capacitor(4)	0mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		4.7		µF
C_{OUT}	Output Filter Capacitor(4)		22	47	100	
	Output Capacitor ESR(4)				20	mΩ
L	Output Filter Inductance(4)			2.2		µH
ΔV_{OUT}	DC Line regulation(4)	3.3V ≤ V_{VIN} ≤ 5V, I_{OUT} = $I_{OUT-MAX}$		0.5		%/V
	DC Load regulation, PWM(4)	V_{VIN}=3.3V, 0.1 * $I_{OUT-MAX}$ ≤ I_{OUT} ≤ $I_{OUT-MAX}$		0.3		%/A
I_{FB}	Feedback pin input bias current	V_{FB} = 2.85V		2.3	**5**	µA
V_{FB}	Feedback Accuracy	V_{FB} = 2.85V	**-3**		**3**	%
$R_{DS-ON-HS}$	High Side Switch On Resistance			115		mΩ
		V_{VIN} = 2.6V		190		
$R_{DS-ON-LS}$	Low Side Switch On Resistance			60	**110**	
$R_{DS-ON-BYPASS}$	Bypass FET on resistance	Used in parallel with the high side FET while in Bypass mode. Resistance (DCR) of inductor = 100 mΩ				
		V_{IN} = 3.1V		75		mΩ
		V_{IN} = 2.6V		120		
Startup						
Tstart_NoLoad	Internal soft-start (turn on time)(4)	Start up from shutdown, VOUT=0V, no load, LC = recommended circuit, using software enable, to VOUT = 95% of final value		0.1		ms
Tstart_FullLoad	Internal soft-start (turn on time)(4)	Start up from shutdown, VOUT =0V, Maximum Load, LC = recommended circuit, using software enable, to VOUT = 95% of final value		0.5		

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if V_{IN} ≥ V_{OUT}+1.0V.
(4) Specification ensured by design. Not tested during production.
(5) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(6) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage. (See General Electrical Characteristics.)

Buck 2 Electrical Characteristics[1][2][3]

Unless otherwise noted, V_{VIN} = 5.0V where: V_{VIN}=V_{VIN_B1} = V_{VIN_B2} = V_{VIN_B3}.
The application circuit used is the one shown in "Typical Application Circuit".
Limits in standard typeface are for T_J = 25°C.
Limits in **boldface** type apply over the full operating junction temperature range of -30°C ≤ T_A=T_J ≤ +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_Q	DC Bias Current in VIN	No Load, PFM Mode		15	**50**	µA
$I_{OUT-MAX}$	Continuous maximum load current[4][5][6]	Buck 2 enabled, switching in PWM	**1**			A
I_{PEAK}	Peak switching current limit	Buck 2 enabled, switching in PWM	**1.35**	1.55	**1.90**	
η	Efficiency peak, Buck2[4]	I_{OUT} = 0.3 A, V_{VIN} = 3.3V		90		%
F_{SW}	Switching Frequency		**1.75**	2	**2.3**	MHz
C_{IN}	Input Capacitor[4]	0mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		4.7		µF
C_{OUT}	Output Filter Capacitor[4]		22	47	100	
	Output Capacitor ESR[4]				20	mΩ
L	Output Filter Inductance[4]			2.2		µH
ΔV_{OUT}	DC Line regulation[4]	3.3V ≤ V_{VIN} ≤ 5V, I_{OUT} = $I_{OUT-MAX}$		0.5		%/V
	DC Load regulation, PWM[4]	V_{VIN}=3.3V, 100mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		0.3		%/A
I_{FB}	Feedback pin input bias current	V_{FB} = 1.8V		2.3	**5**	µA
V_{FB}	Feedback Accuracy	V_{FB} = 1.8V	**-3**		**3**	%
$R_{DS-ON-HS}$	High Side Switch On Resistance			125		mΩ
		V_{VIN} = 2.6V		200		
$R_{DS-ON-LS}$	Low Side Switch On Resistance			60	**110**	
Startup						
Tstart_NoLoad	Internal soft-start (turn on time)[4]	Start up from shutdown, VOUT=0V, no load, LC = recommended circuit, using software enable, to VOUT = 95% of final value		0.1		ms
Tstart_FullLoad	Internal soft-start (turn on time)[4]	Start up from shutdown, VOUT =0V, Maximum Load, LC = recommended circuit, using software enable, to VOUT = 95% of final value		0.5		

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if V_{IN} ≥ V_{OUT}+1.0V.
(4) Specification ensured by design. Not tested during production.
(5) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: T_{A-MAX} = $T_{J-MAX-OP}$ – (θ_{JA} × P_{D-MAX}).
(6) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: P = (T_J–T_A)/θ_{JA}, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage. (See General Electrical Characteristics.)

Buck 3 Electrical Characteristics(1)(2)(3)

Unless otherwise noted, V_{VIN} = 5.0V where: V_{VIN}=V_{VIN_B1} = V_{VIN_B2} = V_{VIN_B3}.
The application circuit used is the one shown in "Typical Application Circuit".
Limits in standard typeface are for T_J = 25°C.
Limits in **boldface** type apply over the full operating junction temperature range of -30°C ≤ T_A=T_J ≤ +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_Q	DC Bias Current in VIN	No Load, PFM Mode		15	**50**	µA
$I_{OUT-MAX}$	Continuous Peak load current (4)(5)(6)	Buck 3 enabled, switching in PWM	**2.5**			A
I_{PEAK}	Peak switching current limit	Buck 3 enabled, switching in PWM	**2.9**	3.5		
η	Efficiency peak, Buck3(4)	I_{OUT} = 0.3 A, V_{VIN} = 3.3V		90		%
F_{SW}	Switching Frequency		**1.75**	2	**2.3**	MHz
C_{IN}	Input Capacitor(4)	0mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		4.7		µF
C_{OUT}	Output Filter Capacitor(4)		47	47	100	
	Output Capacitor ESR(4)				20	mΩ
L	Output Filter Inductance(4)			1		µH
ΔV_{OUT}	DC Line regulation(4)	3.3V ≤ V_{VIN} ≤ 5V, I_{OUT} = $I_{OUT-MAX}$		0.5		%/V
	DC Load regulation, PWM(4)	V_{IN}=5V, 100mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		0.3		%/A
I_{FB}	Feedback pin input bias current	V_{FB} = 1.0V		3.0	**5**	µA
V_{FB}	Feedback Accuracy	V_{FB} = 1.0V	**-3**		**3**	%
$R_{DS-ON-HS}$	High Side Switch On Resistance			95		mΩ
		V_{VIN} = 2.6V		140		
$R_{DS-ON-LS}$	Low Side Switch On Resistance			45	**90**	
Startup						
Tstart_NoLoad	Internal soft-start (turn on time)(4)	Start up from shutdown, V_{OUT}=0V, no load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value		0.1		ms
Tstart_FullLoad	Internal soft-start (turn on time)(4)	Start up from shutdown, V_{OUT}=0V, Maximum Load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value		0.5		

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if V_{IN} ≥ V_{OUT}+1.0V.
(4) Specification ensured by design. Not tested during production.
(5) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(6) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage. (See General Electrical Characteristics.)

Comparators Electrical Characteristics(1)(2)

Unless otherwise noted, V_{VIN} = 5.0V where: V_{VIN}=V_{VIN_B1} = V_{VIN_B2} = V_{VIN_B3}.
The application circuit used is the one shown in “Typical Application Circuit".
Limits in standard typeface are for T_J = 25°C.
Limits in **boldface** type apply over the full operating junction temperature range of -30°C ≤ T_A=T_J ≤ +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{VCOMP}	VCOMP pin bias current	V_{COMP} = 0.0V		0.1	**2**	µA
		V_{COMP} = 5.0V		0.1	**2**	
V_{COMP_RISE}	Comparator rising edge trigger level			2.79		V
V_{COMP_FALL}	Comparator falling edge trigger level			2.73		
Hysteresis			**30**	60	**80**	mV
t_{COMP_IRQ}	Transition time of Interrupt output			6	**15**	µs

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.

Typical Performance Characteristics

(All plots are representative typical plots) Vin=5.0V

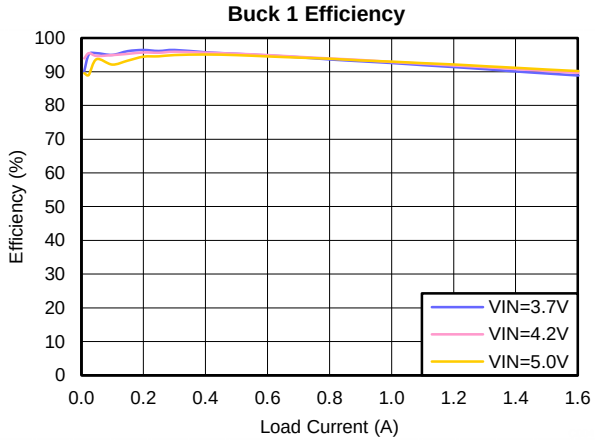


Figure 2.

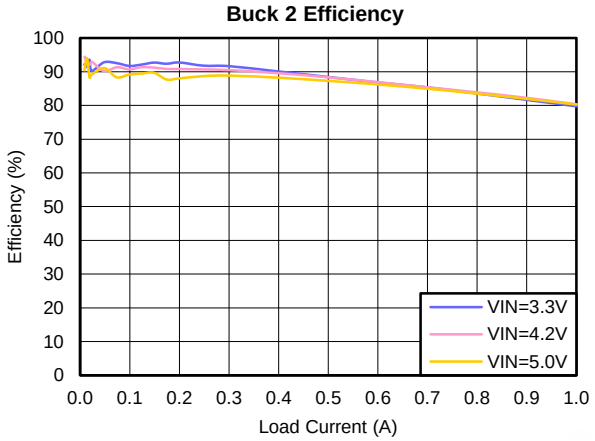


Figure 3.

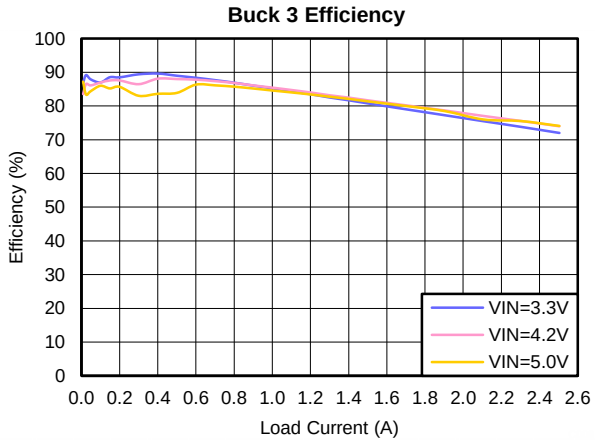


Figure 4.

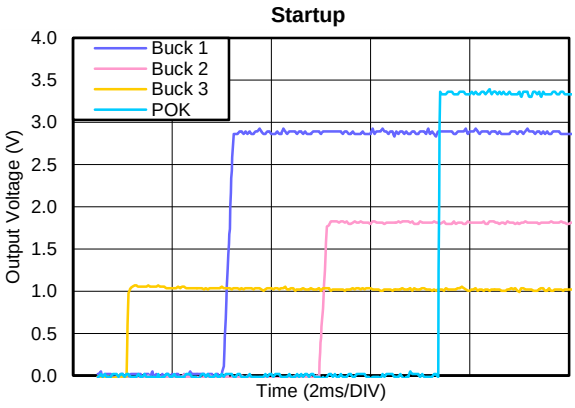


Figure 5.

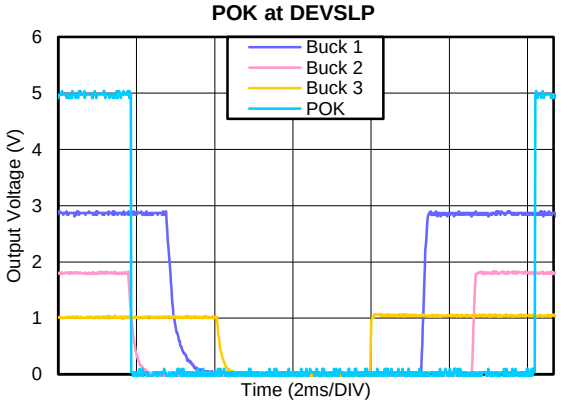


Figure 6.

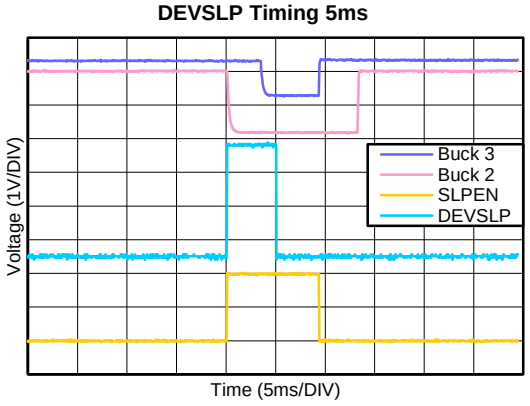


Figure 7.

Typical Performance Characteristics (continued)

DEVSLP Timing 10ms

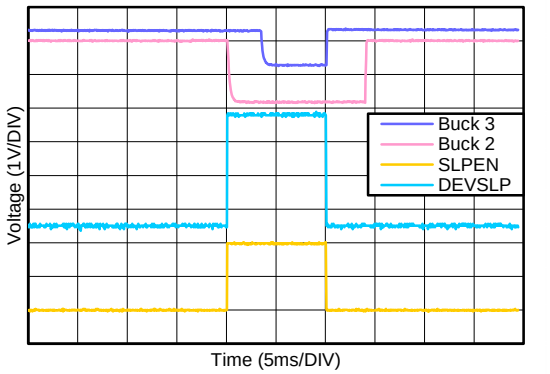


Figure 8.

Buck 1 - 0 to 750mA

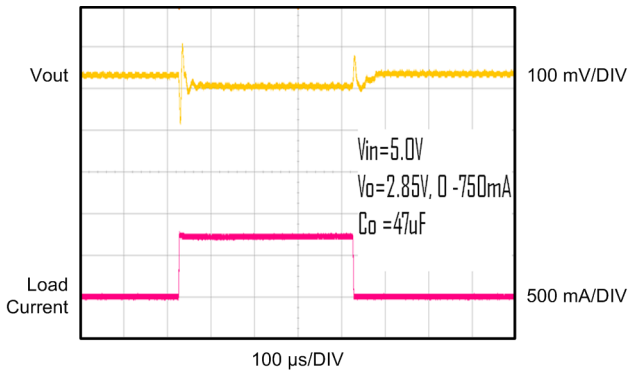


Figure 9.

Buck 1 - 750mA to 1.6A

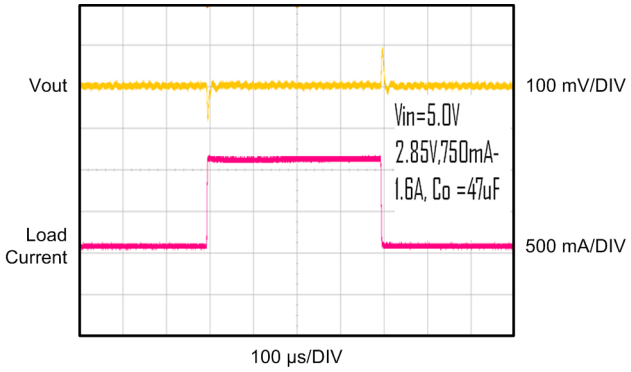


Figure 10.

Buck 2 - 0 to 500mA

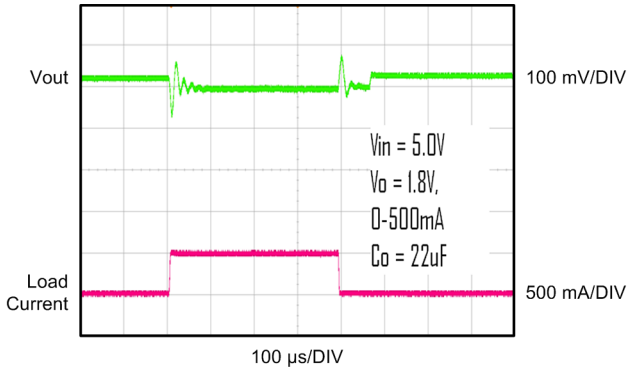


Figure 11.

Buck 2 - 500 to 1A

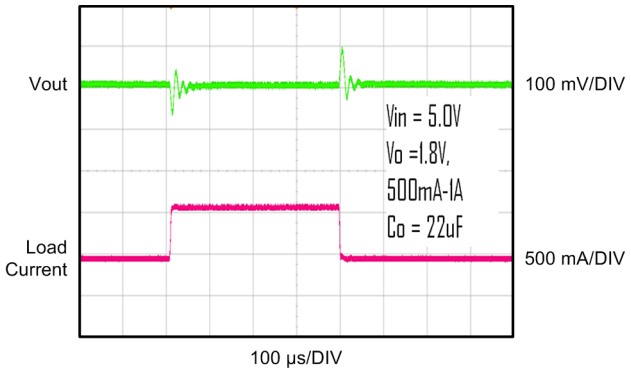


Figure 12.

Buck 3 - 0 to 1.25A

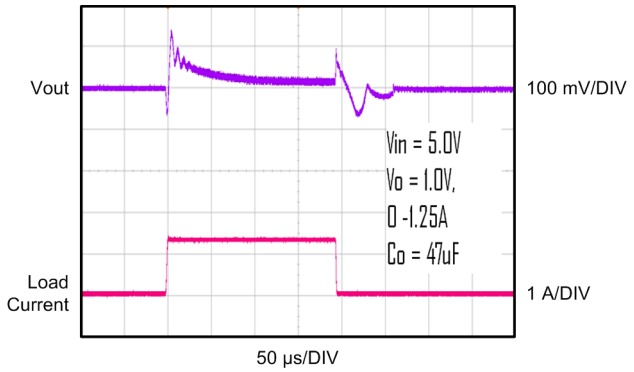


Figure 13.

Typical Performance Characteristics (continued)

Buck 3 - 1.25 to 2.5A

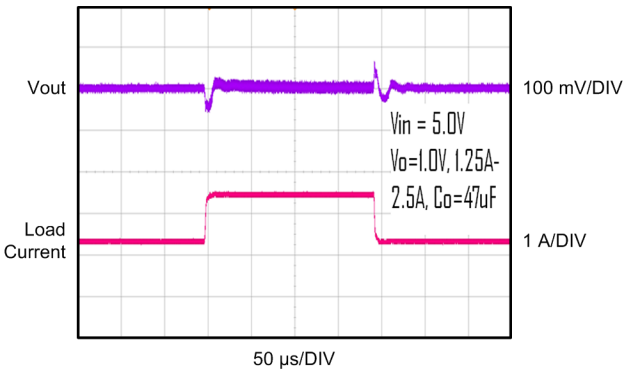


Figure 14.

APPLICATION INFORMATION

LM10524 is a highly efficient and integrated Power Management Unit for Systems-on-a-Chip (SoCs), ASICs, and processors. It operates cooperatively and communicates with processors over an SPI interface with output Voltage programmability.

The device incorporates three high-efficiency synchronous buck regulators that deliver three output voltages from a single power source.

The device also includes a SPI programmable Comparator Block that provides an interrupt output signal. The device has a separate logic supply input.

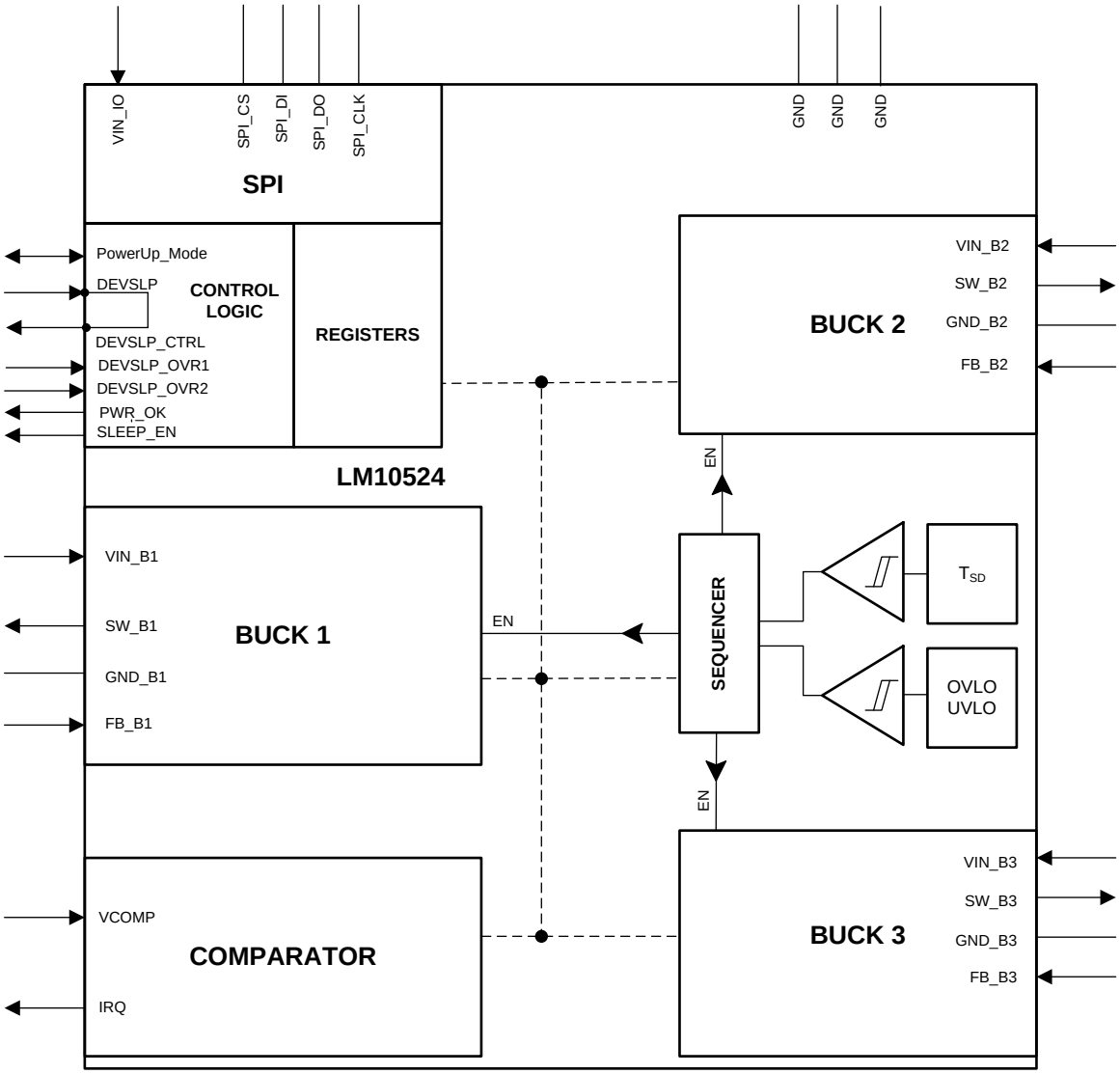


Figure 15. Internal Block Diagram of the LM10524 PMIC

SPI Data Interface

The device is programmable via 4-wire SPI Interface. The signals associated with this interface are CS, DI, DO and CLK. Through this interface, the user can enable/disable the device, program the output voltages of the individual Bucks and of course read the status of Flag registers.

By accessing the registers in the device through this interface, the user can get access and control the operation of the buck controllers and program the reference voltage of the comparator in the device.

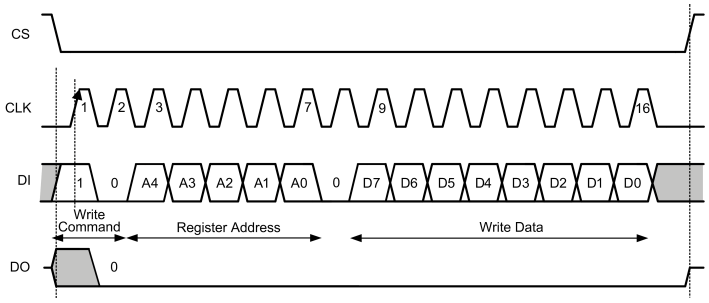


Figure 16. SPI Interface Write

- Data In (DI)
  - 1 to 0 Write Command
  - $A_4$to A_0 Register address to be written
  - D_7 to D_0 Data to be written
- Data Out (DO)
  - All Os

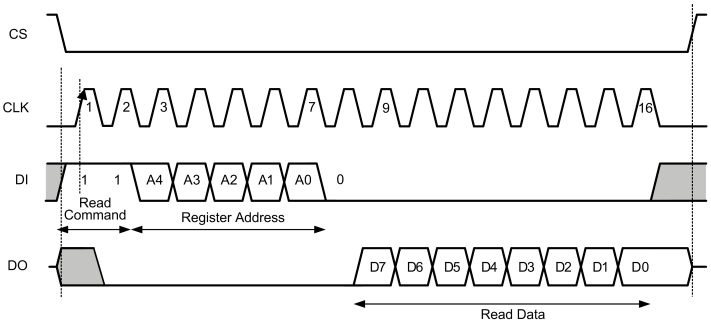


Figure 17. SPI Interface Read

- Data In (DI)
  - 1 to 1 Read Command
  - $A_4$to A_0 Register address to be read
  - Don’t care after A0
- Data Out (DO)
  - D_7 to D_0 Data Read

Registers Configurable Via The SPI Interface

Addr	Reg Name	Bit	R/W	Default	Description	Notes
0x00	Buck 3 Voltage	7	—	-		Reset default:
		6	R/W	0	Buck 3 Voltage Code[6]	0x1E (1.0V)
		5	R/W	0	Buck 3 Voltage Code[5]	
		4	R/W	1	Buck 3 Voltage Code[4]	Range: 0.7V to 1.95V
		3	R/W	1	Buck 3 Voltage Code[3]	
		2	R/W	1	Buck 3 Voltage Code[2]	
		1	R/W	1	Buck 3 Voltage Code[1]	
		0	R/W	0	Buck 3 Voltage Code[0]	
0x07	Buck 1 Voltage	7	—	-		Reset default:
		6	—	-		0x23 (2.85V)
		5	R/W	1	Buck 1 Voltage Code[5]	
		4	R/W	0	Buck 1 Voltage Code[4]	Range: 1.1V to 2.85V
		3	R/W	0	Buck 1 Voltage Code[3]	
		2	R/W	0	Buck 1 Voltage Code[2]	
		1	R/W	1	Buck 1 Voltage Code[1]	
		0	R/W	1	Buck 1 Voltage Code[0]	
0x08	Buck 2 Voltage	7	—	-		Reset default:
		6	—	-		0x0E (1.8V)
		5	R/W	0	Buck 2 Voltage Code[5]	
		4	R/W	0	Buck 2 Voltage Code[4]	Range: 1.1V to 3.6V
		3	R/W	1	Buck 2 Voltage Code[3]	
		2	R/W	1	Buck 2 Voltage Code[2]	
		1	R/W	1	Buck 2 Voltage Code[1]	
		0	R/W	0	Buck 2 Voltage Code[0]	
0x0A	Buck Control	7	R	1	BK3EN	Reads Buck 3 enable status
		6	—	-		
		5	—	-		
		4	R/W	(see notes)	BK1FPWM	Buck 1 forced PWM mode when high. Default = 1 (LM10524), Default = 0 (LM10524-A).
		3	R/W	1	BK2FPWM	Buck 2 forced PWM mode when high
		2	R/W	1	BK3FPWM	Buck 3 forced PWM mode when high
		1	R/W	1	BK1EN	Enables Buck 1 0-disabled, 1-enabled
		0	R/W	1	BK2EN	Enables Buck 2 0-disabled, 1-enabled
0x0B	Comparator Control	7	R/W	0	Comp_hyst[0]	Doubles Comparator hysteresis
		6	R/W	0	Comp_thres(5)	Programmable range of 2.0V to 4.0V, step size = 31.75 mV
		5	R/W	1	Comp_thres(4)	Comparator Threshold reset default: 6h'18.
		4	R/W	1	Comp_thres(3)	
		3	R/W	0	Comp_thres(2)	Comp_hyst=1 → min 80 mV hysteresis
		2	R/W	0	Comp_thres(1)	Comp_hyst=0 → min 40 mV hysteresis
		1	R/W	0	Comp_thres(0)	
		0	R/W	1	COMPEN	Comparator enable

Addr	Reg Name	Bit	R/W	Default	Description	Notes
0x0C	Interrupt Enable	7	—			
		6	—			
		5	—			
		4	—			
		3	R/W	0	Buck 3 OK	
		2	R/W	0	Buck 2 OK	
		1	R/W	0	Buck 1 OK	
		0	R/W	1	Comparator	Interrupt comp event
0x0D	Interrupt Status	7	—			
		6	—			
		5	—			
		4	R			
		3	R		Buck 3 OK	Buck 3 is greater than 90% of target
		2	R		Buck 2 OK	Buck 2 is greater than 90% of target
		1	R		Buck 1 OK	Buck 1 is greater than 90% of target
		0	R		Comparator	Comparator output is high
0x0E	MISC Control	7	—			
		6	—			
		5	—			
		4	—			
		3	—			
		2	—			
		1	—			
		0	R/W	0	Interrupt Polarity	Interrupt_polarity=0→Active low Interrupt Interrupt_polarity=1→Active high Interrupt

ADDR 0x07& 0x08: Buck 1 and Buck 2 Voltage Code and V_{OUT} Level Mapping

Voltage code	Voltage	Voltage code	Voltage
0x00	1.10	0x20	2.70
0x01	1.15	0x21	2.75
0x02	1.20	0x22	2.80
0x03	1.25	0x23	2.85
0x04	1.30	0x24	2.90
0x05	1.35	0x25	2.95
0x06	1.40	0x26	3.00
0x07	1.45	0x27	3.05
0x08	1.50	0x28	3.10
0x09	1.55	0x29	3.15
0x0A	1.60	0x2A	3.20
0x0B	1.65	0x2B	3.25
0x0C	1.70	0x2C	3.30
0x0D	1.75	0x2D	3.35
0x0E	1.80	0x2E	3.40
0x0F	1.85	0x2F	3.45
0x10	1.90	0x30	3.50
0x11	1.95	0x31	3.55
0x12	2.00	0x32	3.60
0x13	2.05	0x33	3.60
0x14	2.10	0x34	3.60
0x15	2.15	0x35	3.60
0x16	2.20	0x36	3.60
0x17	2.25	0x37	3.60
0x18	2.30	0x38	3.60
0x19	2.35	0x39	3.60
0x1A	2.40	0x3A	3.60
0x1B	2.45	0x3B	3.60
0x1C	2.50	0x3C	3.60
0x1D	2.55	0x3D	3.60
0x1E	2.60	0x3E	3.60
0x1F	2.65	0x3F	3.60

ADDR 0x00 & 0x09: Buck 3 Voltage Code and V_{OUT} Level Mapping

Voltage Code	Voltage	Voltage Code	Voltage	Voltage Code	Voltage	Voltage Code	Voltage
0x00	0.70	0x20	1.02	0x40	1.34	0x60	1.66
0x01	0.71	0x21	1.03	0x41	1.35	0x61	1.67
0x02	0.72	0x22	1.04	0x42	1.36	0x62	1.68
0x03	0.73	0x23	1.05	0x43	1.37	0x63	1.69
0x04	0.74	0x24	1.06	0x44	1.38	0x64	1.70
0x05	0.75	0x25	1.07	0x45	1.39	0x65	1.71
0x06	0.76	0x26	1.08	0x46	1.40	0x66	1.72
0x07	0.77	0x27	1.09	0x47	1.41	0x67	1.73
0x08	0.78	0x28	1.10	0x48	1.42	0x68	1.74
0x09	0.79	0x29	1.11	0x49	1.43	0x69	1.75
0x0A	0.80	0x2A	1.12	0x4A	1.44	0x6A	1.76
0x0B	0.81	0x2B	1.13	0x4B	1.45	0x6B	1.77
0x0C	0.82	0x2C	1.14	0x4C	1.46	0x6C	1.78
0x0D	0.83	0x2D	1.15	0x4D	1.47	0x6D	1.79
0x0E	0.84	0x2E	1.16	0x4E	1.48	0x6E	1.80
0x0F	0.85	0x2F	1.17	0x4F	1.49	0x6F	1.81
0x10	0.86	0x30	1.18	0x50	1.50	0x70	1.82
0x11	0.87	0x31	1.19	0x51	1.51	0x71	1.83
0x12	0.88	0x32	1.20	0x52	1.52	0x72	1.84
0x13	0.89	0x33	1.21	0x53	1.53	0x73	1.85
0x14	0.90	0x34	1.22	0x54	1.54	0x74	1.86
0x15	0.91	0x35	1.23	0x55	1.55	0x75	1.87
0x16	0.92	0x36	1.24	0x56	1.56	0x76	1.88
0x17	0.93	0x37	1.25	0x57	1.57	0x77	1.89
0x18	0.94	0x38	1.26	0x58	1.58	0x78	1.90
0x19	0.95	0x39	1.27	0x59	1.59	0x79	1.91
0x1A	0.96	0x3A	1.28	0x5A	1.60	0x7A	1.92
0x1B	0.97	0x3B	1.29	0x5B	1.61	0x7B	1.93
0x1C	0.98	0x3C	1.30	0x5C	1.62	0x7C	1.94
0x1D	0.99	0x3D	1.31	0x5D	1.63	0x7D	1.95
0x1E	1.00	0x3E	1.32	0x5E	1.64		
0x1F	1.01	0x3F	1.33	0x5F	1.65		

ADDR 0x0B: Comparator Threshold Mapping

Voltage code	Voltage	Voltage code	Voltage
6h'00	2.000	6h'20	3.016
6h'01	2.032	6h'21	3.048
6h'02	2.064	6h'22	3.080
6h'03	2.095	6h'23	3.111
6h'04	2.127	6h'24	3.143
6h'05	2.159	6h'25	3.175
6h'06	2.191	6h'26	3.207
6h'07	2.222	6h'27	3.238
6h'08	2.254	6h'28	3.270
6h'09	2.286	6h'29	3.302
6h'0A	2.318	6h'2A	3.334
6h'0B	2.349	6h'2B	3.365
6h'0C	2.381	6h'2C	3.397
6h'0D	2.413	6h'2D	3.429
6h'0E	2.445	6h'2E	3.461
6h'0F	2.476	6h'2F	3.492
6h'10	2.508	6h'30	3.524
6h'11	2.540	6h'31	3.556
6h'12	2.572	6h'32	3.588
6h'13	2.603	6h'33	3.619
6h'14	2.635	6h'34	3.651
6h'15	2.667	6h'35	3.683
6h'16	2.699	6h'36	3.715
6h'17	2.730	6h'37	3.746
6h'18	2.762	6h'38	3.778
6h'19	2.794	6h'39	3.810
6h'1A	2.826	6h'3A	3.842
6h'1B	2.857	6h'3B	3.873
6h'1C	2.889	6h'3C	3.905
6h'1D	2.921	6h'3D	3.937
6h'1E	2.953	6h'3E	3.969
6h'1F	2.984	6h'3F	4.000

Buck Regulators Operation

A buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground and a feedback path. The figure below shows the block diagram of each of the three buck regulators integrated in the device.

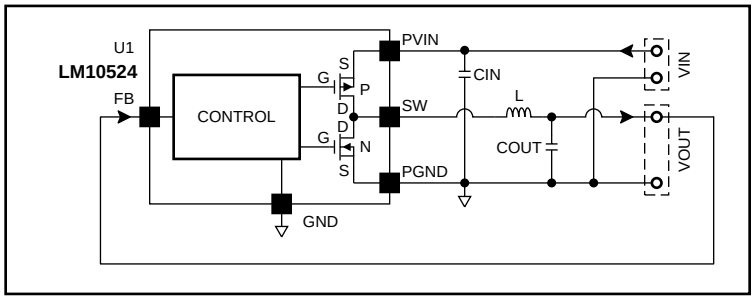


Figure 18. Buck Functional Diagram

During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{VIN\_Bx} - V_{OUT})/L$ by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $(-V_{OUT})/L$.

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

Buck Regulators Description

The LM10524 incorporates three high efficiency synchronous switching buck regulators that deliver various voltages from a single DC input voltage. They include many advanced features to achieve excellent voltage regulation, high efficiency and fast transient response time. The bucks feature voltage mode architecture with synchronous rectification.

Each of the switching regulators is specially designed for high efficiency operation throughout the load range. With a 2MHz typical switching frequency, the external L-C filter can be small and still provide very low output voltage ripple. The bucks are internally compensated to be stable with the recommended external inductors and capacitors as detailed in the application diagram. Synchronous rectification yields high efficiency for low voltage and high output currents.

All bucks can operate up to a 100% duty cycle allowing for the lowest possible input voltage that still maintains the regulation of the output. The lowest input to output dropout voltage is achieved by keeping the PMOS switch on.

Additional features include soft-start, under-voltage lock-out, and current and thermal overload protection. To reduce the input current ripple, the device employs a control circuit that operates the three bucks at 120° phase. These bucks are nearly identical in performance and mode of operation. They operate in FPWM (forced PWM) or automatic mode (PWM/PFM).

PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, a feed forward voltage inversely proportional to the input voltage is introduced.

In **Forced PWM Mode** the bucks always operate in PWM mode regardless of the output current.

In **Automatic Mode**, if the output current is less than 70 mA (typ.), the bucks automatically transition into PFM (Pulse Frequency Modulation) operation to reduce the current consumption. At higher than 100 mA (typ.) they operate in PWM mode. This increases the efficiency at lower output currents. The 30 mA (typ.) hysteresis is designed in for stable Mode transition.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. In this case the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

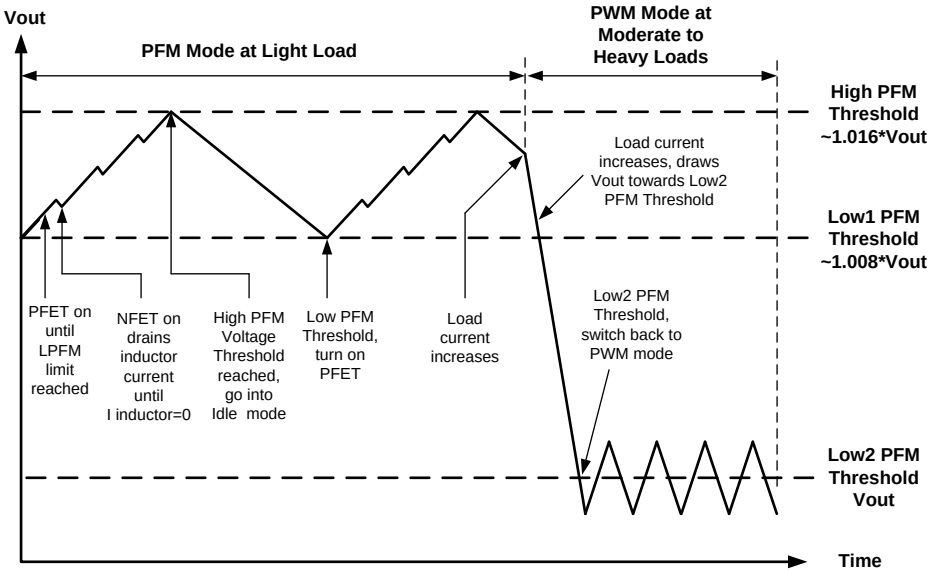


Figure 19. PFM vs PWM Operation

PFM Operation [BUCK 1, 2 & 3]

At very light loads, Buck 1, 2 and Buck 3 enter PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

Buck 1, 2 and 3 will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The inductor current becomes discontinuous, or
2. The peak PMOS switch current drops below the I_{MODE} level.

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{pfm} level set for PFM mode.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 19), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'idle' mode is less than 100uA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage to ~1.6% above the nominal PWM output voltage.

If the load current should increase during PFM mode causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

Soft Start

Each of the buck converters has an internal soft-start circuit that limits the in-rush current during start-up. This allows the converters to gradually reach the steady state operating point, thus reducing start-up stresses and surges. During start-up, the switch current limit is increased in steps.

For **Buck 1, 2 and 3** the soft start is implemented by increasing the switch current limit in steps that are gradually goes higher. The start-up time depends on the output capacitor size, load current and output voltage. Typical startup time with the recommended output capacitor of 10uF is 0.1-0.5ms. It is expected that in the final application the load current condition will be more likely in the lower load current range during the start up.

Current Limiting

A current limit feature protects the device and any external components during overload conditions. In PWM mode the current limiting is implemented by using an internal comparator that trips at current levels according to the buck capability. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

Internal Synchronous Rectification

While in PWM mode, the bucks use an internal NFET as a synchronous rectifier to reduce the rectifier forward voltage drop and the associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Bypass-FET Operation on Buck 1

This is a factory programmable option, this is disabled on the LM10524 and the LM10524-A.

There is an additional bypass FET used on Buck 1. The FET is connected in parallel to High Side FET and inductor. The bypass threshold will be 3.1V with an option of 3.5V (set by OTP). With standard setting if buck 1 input voltage is greater than 3.1V the bypass function is disabled. The determination of whether or not the Buck 1 is in bypass mode or standard switching regulation is constantly monitored while the regulator is enabled. If at any time the input voltage goes above 3.1V while in by-pass mode, the regulator will transition to normal operation.

When the bypass mode is enabled, the output voltage of the buck that is in bypass mode is not regulated, but instead, the output voltage follows the input voltage minus the voltage drop seen across the FET and DCR of the inductor. The voltage drop is a direct result of the current flowing across those resistive elements. When Buck 1 transitions into bypass mode, there is an extra FET used in parallel along with the high side FET for transmission of the current to the load. This added FET will help reduce the resistance seen by the load and decrease the voltage drop.

Equivalent Circuit of Bypass Operation of Buck 1

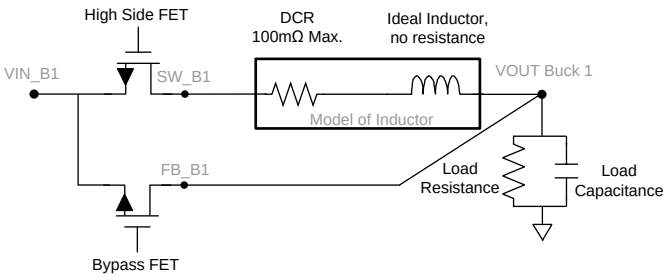


Figure 20. Bypass Operation - Equivalent Circuits

Low Dropout Operation

The device can operate nearly at 100% duty cycle (no switching; PMOS switch completely on) for low drop out support. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV.

The minimum input voltage needed to support the output voltage is:

$V_{IN\_MIN}=V_{OUT}+I_{LOAD}*(R_{DSON\_PFET}+R_{IND})$

Where:

- I_{LOAD} = Load Current

- R_{DSON_PFET} = Drain to source resistance of PFET (high side)
- R_{IND} = Inductor resistance (1)

Device Operating Modes

Startup Sequence

The startup mode of the LM10524 will depend on the input voltage. Once VIN reaches the UVLO threshold, there is a 15 msec delay before the LM10524 determines how to set up the buck regulators. If bypass mode is enabled and if V_{IN} is below 3.2V, then Buck 1 will be in bypass mode. See Bypass-FET Operation on Buck 1 for functionality description. If the V_{IN} voltage is greater than 3.2V buck 1 will start up as the standard regulators. The 3 buck regulators are staggered during startup to avoid large inrush currents. There is a fixed delay of 2 msec between the startup of each regulator.

The Startup Sequence will be:

1. 15 msec (±30%) delay after V_{IN} UVLO threshold
2. 2 ms delay
3. Buck 3 Startup
4. 2 ms delay
5. Buck 1 Startup
6. 2 ms delay
7. Buck 2 Startup

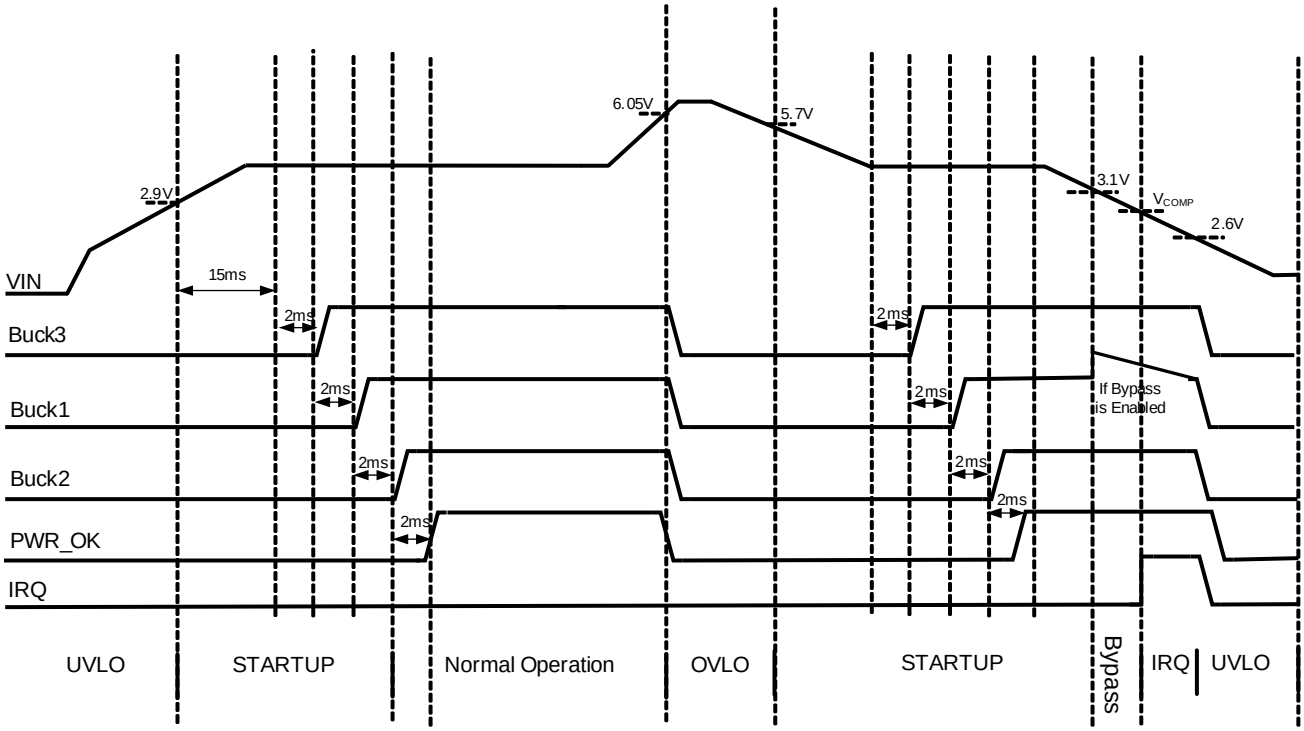


Figure 21. Normal Operating Modes

Power-On

The device is always enabled, unless outside of operating voltage range. There is no LM10524 Enable Pin. Once V_{IN} reaches a minimum required input Voltage, the power-up sequence will be started automatically and the startup sequence will be initiated. Once the device is started, the output voltage of the Bucks 1 and 2 can be individually disabled by accessing their corresponding BKEN register bits (BUCK CONTROL).

Sleep Function

The Device can be put into Sleep mode where all the outputs and the internal oscillator are switched off. Sleep mode is initiated by the DevSLP pin going high and the function is gated by the state of device pins DevSLP_OVR1, DevSLP_OVR2, and PowerUp_Enable. DevSLP_CTRL and SLEEP_EN pins are used to indicate the status of the device while DevSLP pin is high.

Device Power Up

During the device power up there is a 150ms period where all outputs will be low or tri-state. Following this the PowerUp_Mode output will be high and SLEEP_EN output will be low. The DEVSLP_CTRL output will mirror the state of the DEVSLP input. This initialization phase is complete when the PowerUp_Mode pin is externally pulled low and the device latches this low state on the pin.

Normal Operation

When Sleep mode is initiated by the DEVSLP pin being pulled high, this is mirrored to the DEVSLP_CTRL pin. The conditions for entry into Sleep mode are checked, DEVSLP_OVR1, DEVSLP_OVR2, and PowerUp_Mode pins must be low. If these conditions are met the Ouput shutdown is started and the DEVSLP_CTRL pin is driven low. The SLEEP_EN pin is driven high to indicate that Sleep mode is active. SLEEP_EN will remain high until all outputs have discharged to zero and DEVSLP goes low. In the case where the DEVSLP input goes low prior to full discharge, SLEEP_EN will remain high until all outputs have discharged. If any of the gating pins DEVSLP_OVR1, DEVSLP_OVR2, and PowerUp_Mode go high while in sleep mode SLEEP_EN will go low and DEVSLP_CTRL will go to the same state as DEVSLP pin.

19.2.3 DEVSLP Timing

Initialization phase:

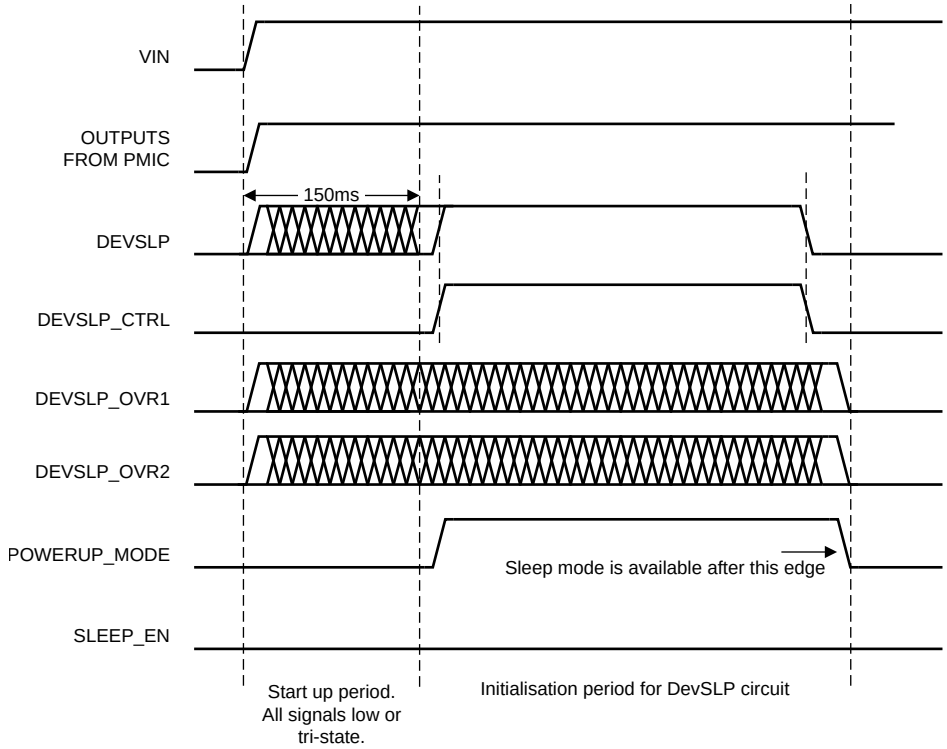


Figure 22. Initialization

After device power up the regulated outputs are on and at their specified outputs voltages indicated by the 'Outputs from PMIC' trace above. All DEVSLP signals are low or tri-state for a period of 150ms. Following this 150ms period the device will hold SLEEP_EN low and will allow the POWERUP_MODE pin to go high via a 1KΩ pullup resistor referenced to VIN supply. The DEVSLP function is ready when the POWERUP_MODE pin is pulled low externally, This negative edge on the POWERUP_MODE pin triggers the device to pulldown the POWERUP_MODE pin and this output remains low until a device reset. During this Initialization phase the DEVSLP_CTRL output mirrors the input at DEVSLP. The two signals DEVSLP_OVR1/2 are ignored by the device during this phase.

Normal Operation, DEVSLP high period > Outputs discharge time:

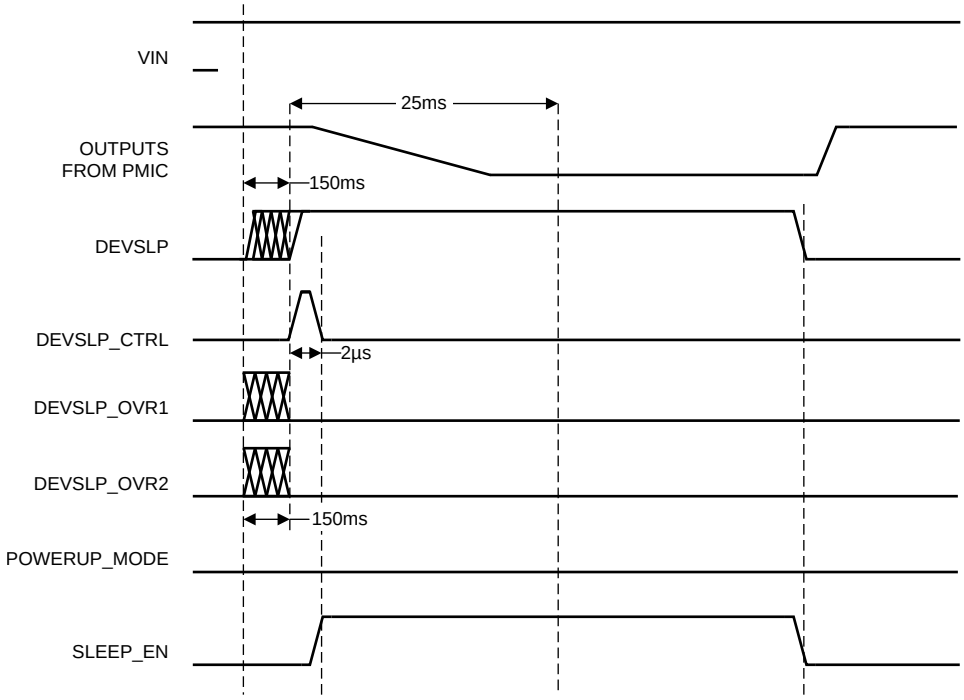


Figure 23. DEVSLP, Period Greater than Output Discharge Time

In normal operation when DEVSLP goes high, DEVSLP_CNTL will go high. The device checks the status of DEVSLP_OVR1 and DEVSLP_OVR2 as well as POWERUP_MODE to ensure they are low to allow entry into SLEEP mode. If these conditions are met then the device will power down all outputs in their time sequence and the DEVSLP_CTRL pin is forced low. SLEEP_EN is forced high. Following the outputs discharging to zero DEVSLP goes low, SLEEP_EN is driven low and the regulated outputs switch on in their determined time sequence.

Normal Operation, DEVSLP high period < Outputs discharge time

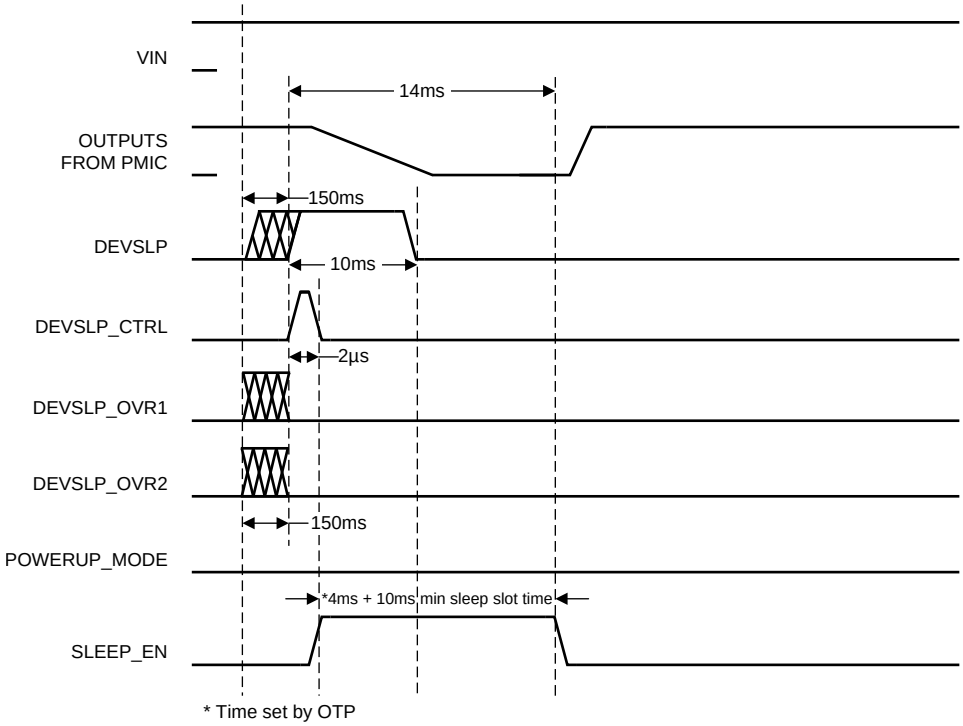


Figure 24. DEVSLP. Period less than Output Discharge Time

As above; in normal operation when DEVSLP goes high DEVSLP_CNTL will go high. The device checks the status of DEVSLP_OVR1 and DEVSLP_OVR2 as well as POWERUP_MODE to ensure they are low to allow entry into SLEEP mode. If these conditions are met then the device will power down all outputs in their time sequence (4ms) and the DEVSLP_CTRL pin is forced low. SLEEP_EN is forced high. In this case DEVSLP goes high prior to full output discharge to zero. SLEEP_EN will be forced low after a set time, (programmable) with default set to10ms (+4ms) to ensure the device outputs discharge fully. This timing is important to ensure proper discharge of the output capacitance (up to 100µF in a 7.5ms period. The device outputs will also be switched on after this time period. To ensure all buck outputs are discharged a minimum sleep time exists, this time is configured to 12ms (programmable set by OTP).In the case where DEVSLP is active for, <12ms, the SLEEP_EN and sleep cycle will be held for a minimum of 12ms.

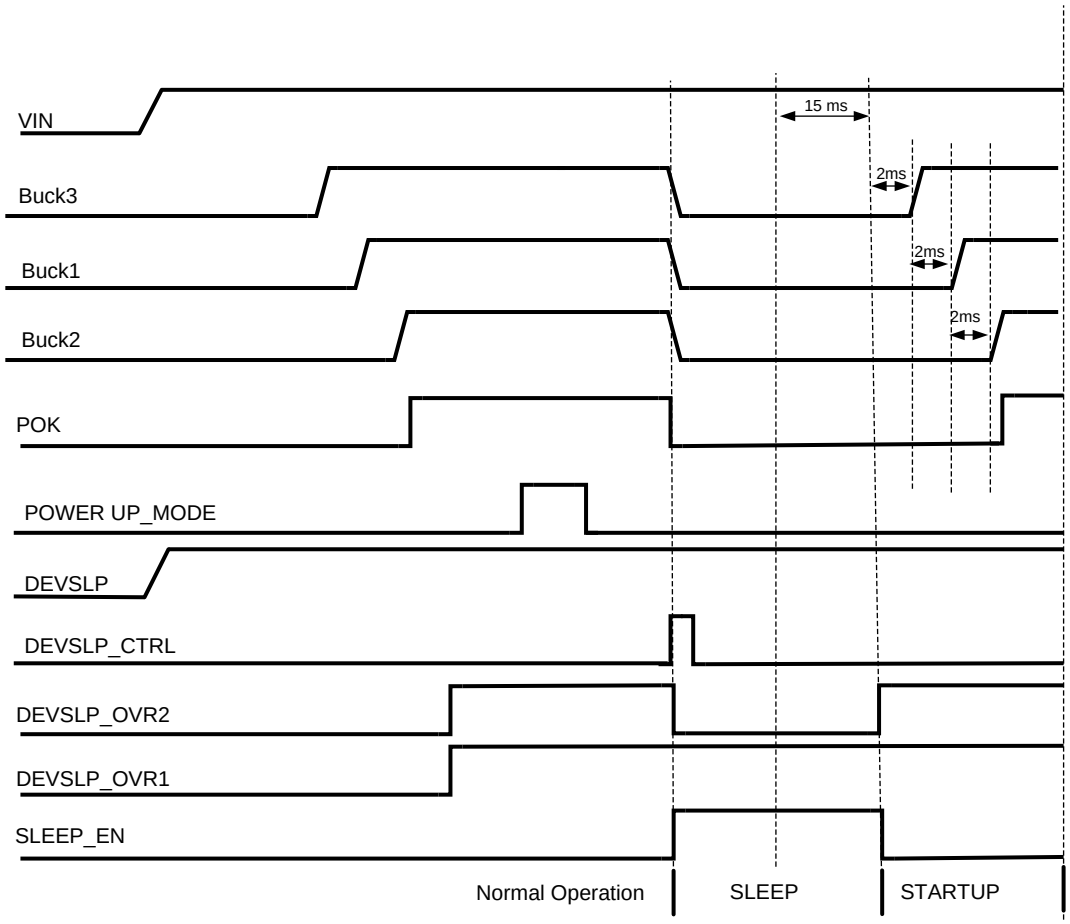


Figure 25. Sleep using DEVSLP_OVR1 or 2

Undervoltage Lockout (UVLO)

The V_{IN} voltage is monitored for a supply under voltage condition, for which the operation of the device cannot be ensured. The part will automatically disable Buck 3. To prevent unstable operation, the undervoltage lockout (UVLO) has a hysteresis window of about 300 mV. A UVLO event will force the device into the reset state, all internal registers are reset. Once the supply voltage is above the UVLO hysteresis, the device will initiate a power-up sequence and then enter the active state.

The Comparator will remain functional past the UVLO threshold until V_{IN} reaches approximately 2.25V.

Overvoltage Lockout (OVLO)

The V_{IN} voltage is monitored for a supply over voltage condition, for which the operation of the device cannot be ensured. The purpose of overvoltage lockout (OVLO) is to protect the part and all other consumers connected to the PMU outputs from any damage and malfunction. Once V_{IN} rises over 6.05V all the Bucks will be disabled automatically. To prevent unstable operation, the OVLO has a hysteresis window of about 100 mV. An OVLO event will force the device into the reset state; all internal registers are reset. Once the supply voltage is below the OVLO hysteresis, the device will initiate a power-up sequence, and then enter the active state. Operating maximum input voltage at which parameters are ensured is 5.5V. Absolute maximum of the device is 6.0V.

Device Status, Interrupt Enable

The LM10524 has 2 interrupt registers, INTERRUPT ENABLE and INTERRUPT STATUS. These registers can be read via the serial interface. The interrupts are not latched to the register and will always represent the current state and will not be cleared on a read.

If interrupt condition is detected, then corresponding bit in the INTERRUPT STATUS register (0x0D) is set to '1', and Interrupt output is asserted. There are 5 interrupt generating conditions:

- Buck 3 output is over flag level (90% when rising, 85% when falling)
- Buck 2 output is over flag level (90% when rising, 85% when falling)
- Buck 1 output is over flag level (90% when rising, 85% when falling)
- Comparator input voltage crosses over selected threshold

Reading the interrupt register will not release Interrupt output. Interrupt generation conditions can be individually enabled or disabled by writing respective bits in INTERRUPT ENABLE register (0x0C) to '1' or '0'.

Thermal Shutdown (TSD)

The temperature of the silicon die is monitored for an over-temperature condition, for which the operation of the device can not be ensured. The part will automatically be disabled if the temperature is too high (>140°C). The thermal shutdown (TSD) will force the device into the reset state. In reset, all circuitry is disabled. To prevent unstable operation, the TSD has a hysteresis window of about 20°C. Once the temperature has decreased below the TSD hysteresis, the device will initiate a powerup sequence and then enter the active state. In the active state, the part will start up as if for the first time, all registers will be in their default state.

Comparator

The comparator on the LM10524 takes its inputs from the V_{COMP} pin and an internal threshold level which is programmed by the user. The threshold level is programmable between 2.0 and 4.0V with a step of 31 mV and a default comp code of 6h'18. The output of the comparator is the Interrupt pin. Its polarity can be changed using Register 0x0E bit 0. If Interrupt polarity = 0 → Active low (default) is selected, then the output is low if V_{COMP} value is greater than the threshold level. The output is high if the V_{COMP} value is less than the threshold level. If Interrupt polarity = 1 → Active high is selected then the output is high if V_{COMP} value is greater than the threshold level. The output is low if the V_{COMP} value is less than the threshold level. There is some hysteresis when V_{COMP} transitions from high to low, typically 60 mV. There is a control bit in register 0x0B, comparator control, that can double the hysteresis value.

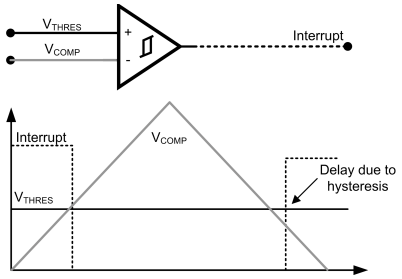


Figure 26. Comparator Thresholds

Thermal Shutdown (TSD)

The temperature of the silicon die is monitored for an over-temperature condition, for which the operation of the device cannot be ensured. The part will automatically be disabled if the temperature is too high. The thermal shutdown (TSD) will force the device into the reset state. In reset, all circuitry is disabled. To prevent unstable operation, the TSD has a hysteresis window of about 20°C. Once the temperature has decreased below the TSD hysteresis, the device will initiate a power-up sequence and then enter the active state. In the active state, the part will start up as if for the first time, all registers will be in their default state.

External Components Selection

All three switchers require an input capacitor and an output inductor-capacitor filter. These components are critical to the performance of the device. All three switchers are internally compensated and do not require external components to achieve stable operation. The output voltages of the bucks can be programmed through the SPI pins.

Output Inductors & Capacitors Selection

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Over current ruggedness

The device has been optimized for use with nominal LC values as shown in the Typical Application Circuit.

Inductor Selection

The recommended inductor values are shown in Typical Application Diagram. It is important to ensure the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current.

Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$\begin{aligned} I_{L(MAX)} &= I_{LOAD(MAX)} + \Delta I_{RIPPLE} \\ &= I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S} \\ &\approx I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times 2.2 \times 2.0} \ \text{(A typ.)}, \\ D = \frac{V_{OUT}}{V_{IN}}, \ F_S &= 2\,\text{MHz}, \ L = 2.2\,\mu\text{H} \end{aligned} \tag{2}$$

There are two methods to choose the inductor saturation current rating:

Recommended Method for Inductor Selection:

The best way to ensure the inductor does not saturate is to choose an inductor that has saturation current rating greater than the maximum device current limit, as specified in the Electrical Characteristics tables. In this case the device will prevent inductor saturation by going into current limit before the saturation level is reached.

Alternate Method for Inductor Selection:

If the recommended approach cannot be used care must be taken to ensure that the saturation current is greater than the peak inductor current:

$$I_{SAT} > IL_{PEAK}$$

$$IL_{PEAK} = I_{OUTMAX} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN} \times EFF}$$

Where:

- I_{SAT}: Inductor saturation current at operating temperature
- I_{LPEAK}: Peak inductor current during worst case conditions
- I_{OUTMAX}: Maximum average inductor current
- I_{RIPPLE}: Peak-to-Peak inductor current
- V_{OUT}: Output voltage

- V_{IN}: Input voltage
- L: Inductor value in Henries at I_{OUTMAX}
- F: Switching frequency, Hertz
- D: Estimated duty factor
- EFF: Estimated power supply efficiency (3)

I_{SAT} may not be exceeded during any operation, including transients, startup, high temperature, worst-case conditions, etc.

Suggested Inductors and Their Suppliers

The designer should choose the inductors that best match the system requirements. A very wide range of inductors are available as regarding physical size, height, maximum current (thermally limited, and inductance loss limited), series resistance, maximum operating frequency, losses, etc. In general, smaller physical size inductors will have higher series resistance (DCR) and implicitly lower overall efficiency is achieved. Very low-profile inductors may have even higher series resistance. The designer should try to find the best compromise between system performance and cost.

Value	Manufacturer	Part Number	DCR	Current	Package
1.0 µH	Murata	LQH44PN1R0NP0	30 mΩ	2.95A	1616
1.0 µH	Murata	LQH32PN1R0NNC	45mΩ	2.5A	3225(1210)
1.0 µH	Coilcraft	XFL3012-102MEC	35 mΩ	2.5A	3012
1.0 µH	Coilcraft	LPS4012-102NL	70mΩ	3.0A	4012
2.2 µH	Coilcraft	XFL3012-222MEC	81 mΩ	1.6A	3012
2.2 µH	Murata	LQH55PN2R2NR0L	31 mΩ	2.5A	2220

Output and Input Capacitors Characteristics

Special attention should be paid when selecting these components. As shown in the following figure, the DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g.0402) may not be suitable in the actual application.

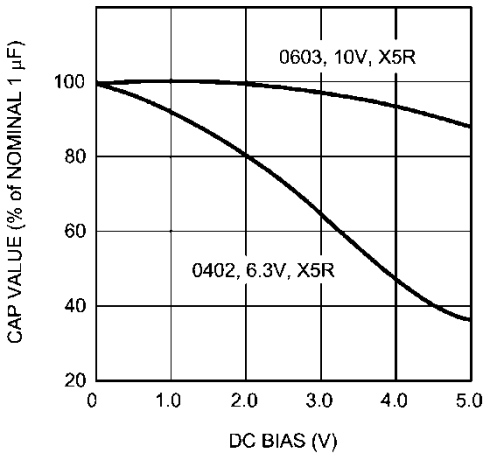


Figure 27. Typical Variation in Capacitance vs. DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47µF to 44µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −30°C, so some guard band must be allowed.

Output Capacitor Selection

The output capacitor of a switching converter absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can usually be neglected at the frequency ranges at which the switcher operates.

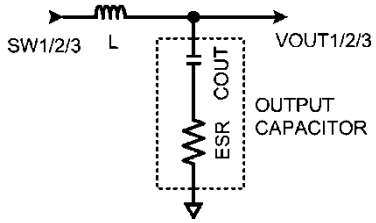


Figure 28. Output Capacitor Equivalent Circuit

The output-filter capacitor smooths out the current flow from the inductor to the load and helps maintain a steady output voltage during transient load changes. It also reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions.

Note that the output voltage ripple increases with the inductor current ripple and the Equivalent Series Resistance of the output capacitor (ESR_{COUT}). Also note that the actual value of the capacitor's ESR_{COUT} is frequency and temperature dependent, as specified by its manufacturer. The ESR should be calculated at the applicable switching frequency and ambient temperature.

$$V_{OUT-RIPPLE-PP} = \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \text{ where } \Delta I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S} \text{ and } D = \frac{V_{OUT}}{V_{IN}} \quad (4)$$

Output ripple can be estimated from the vector sum of the reactive (capacitance) voltage component and the real (ESR) voltage component of the output capacitor where:

$$V_{OUT-RIPPLE-PP} = \sqrt{V^2_{ROUT} + V^2_{COUT}} \quad (5)$$

where:

$$V_{ROUT} = I_{RIPPLE} \times ESR_{COUT} \text{ and } V_{COUT} = \frac{I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

Where:

- $V_{OUT\text{-}RIPPLE\text{-}PP}$: estimated output ripple,
- V_{ROUT}: estimated real output ripple,
- V_{COUT}: estimated reactive output ripple. (6)

The device is designed to be used with ceramic capacitors on the outputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The recommended value for the output capacitors is 22µF, 6.3V with an ESR of 2mΩ or less. The output capacitors need to be mounted as close as possible to the output/ground pins of the device.

Model	Vendor Type	Vendor	Voltage Rating	Case Size
GRM155B03J225KE95	Ceramic, X5R	Murata	6.3V	603
GRM155R60J475ME47	Ceramic, X5R	Murata	6.3V	603
GRM188B03J226MEA0	Ceramic, X5R	Murata	6.3V	603
GRM21BB30J476ME15	Ceramic, X5R	Murata	6.3V	805

Input Capacitor Selection

There are 3 buck regulators in the LM10524 device. Each of these buck regulators has its own input capacitor which should be located as close as possible to their corresponding SWx_VIN and SWx_GND pins, where x designates Buck 1, 2 or 3. The 3 buck regulators operate at 120° out of phase, which means that they switch on at equally spaced intervals, in order to reduce the input power rail ripple. It is recommended to connect all the supply/ground pins of the buck regulators, SWx_VIN to two solid internal planes located under the device. In this way, the 3 input capacitors work together and further reduce the input current ripple. A larger tantalum capacitor can also be located in the proximity of the device.

The input capacitor supplies the AC switching current drawn from the switching action of the internal power FETs. The in- put current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power.

The input capacitor must be rated to handle this current:

$$I_{RMS\_CIN} = I_{OUT} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \quad (7)$$

The power dissipated in the input capacitor is given by:

$$P_{D\_CIN} = I^2_{RMS\_CIN} \times R_{ESR\_CIN} \quad (8)$$

The device is designed to be used with ceramic capacitors on the inputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The minimum recommended value for the input capacitor is 10 µF with an ESR of 10mΩ or less. The input capacitors need to be mounted as close as possible to the power/ground input pins of the device.

The input power source supplies the average current continuously. During the PFET switch on-time, however, the demanded di/dt is higher than can be typically supplied by the input power source. This delta is supplied by the input capacitor.

A simplified “worst case” assumption is that all of the PFET current is supplied by the input capacitor. This will result in conservative estimates of input ripple voltage and capacitor RMS current.

Input ripple voltage is estimated as follows:

$$V_{PPIN} = \frac{I_{OUT} \times D}{C_{IN} \times F_S} + I_{OUT} \times ESR_{CIN} \quad (9)$$

where:

- V_{PPIN}: estimated peak-to-peak input ripple voltage,
- I_{OUT}: output Current
- C_{IN}: input capacitor value
- ESR_{CIN}: input capacitor ESR.

This capacitor is exposed to significant RMS current, so it is important to select a capacitor with an adequate RMS current rating. Capacitor RMS current estimated as follows:

$$I_{RMSCIN} = \sqrt{D \times \left(I^2_{OUT} + \frac{I^2_{RIPPLE}}{12} \right)}$$

- I_{RMSCIN}: estimated input capacitor RMS current. (10)

PCB Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC- DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

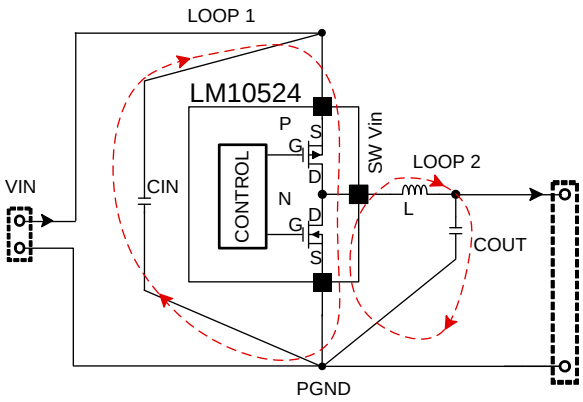


Figure 29. Buck Schematic Showing Layout Sensitive Nodes

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator Vin pin, through to PGND and back to the CIN input capacitor. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the inductor and then out to COUT and the load (see Figure 29). To minimize both loop areas the input capacitor should be placed as close as possible to the PVIN pin. Grounding for both the input and output capacitors should consist of a small localized top side plane that connects to PGND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW pins should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW pin. The inductors should be placed as close as possible to the SW pins to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB pin. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

PCB Layout Thermal Dissipation for Micro SMD Package

1. Position ground layer as close as possible to micro SMD package. Second PCB layer is usually good option.
2. Draw power traces as wide as possible. Bumps which carry high currents should be connected to wide traces. This helps the silicon to cool down.

REVISION HISTORY

Changes from Original (August 2013) to Revision A	Page
• Added Device Information Table	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10524TME-A/NOPB	NRND	DSBGA	YFR	46	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	0 to 0	V089	
LM10524TME/NOPB	ACTIVE	DSBGA	YFR	46	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	V088	Samples
LM10524TMX-A/NOPB	ACTIVE	DSBGA	YFR	46	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	V089	Samples
LM10524TMX/NOPB	NRND	DSBGA	YFR	46	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	0 to 0	V088	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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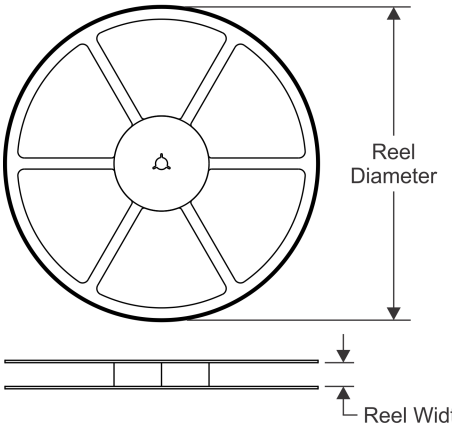
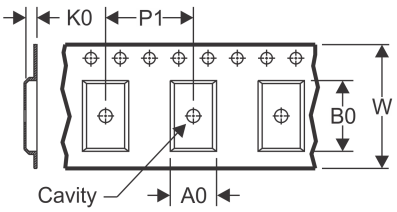
TAPE AND REEL INFORMATION

REEL DIMENSIONS

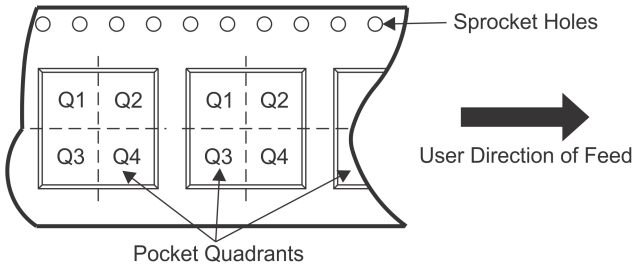


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

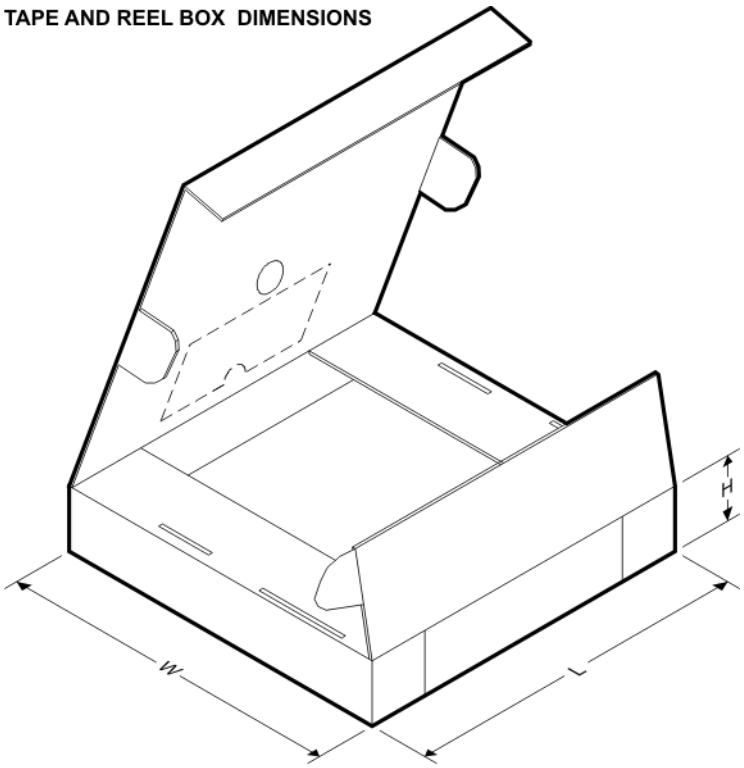
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

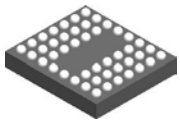
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10524TME-A/NOPB	DSBGA	YFR	46	250	178.0	12.4	3.02	3.42	0.76	8.0	12.0	Q1
LM10524TME/NOPB	DSBGA	YFR	46	250	178.0	12.4	3.02	3.42	0.76	8.0	12.0	Q1
LM10524TMX-A/NOPB	DSBGA	YFR	46	1000	178.0	12.4	3.02	3.42	0.76	8.0	12.0	Q1
LM10524TMX/NOPB	DSBGA	YFR	46	1000	178.0	12.4	3.02	3.42	0.76	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10524TME-A/NOPB	DSBGA	YFR	46	250	210.0	185.0	35.0
LM10524TME/NOPB	DSBGA	YFR	46	250	210.0	185.0	35.0
LM10524TMX-A/NOPB	DSBGA	YFR	46	1000	210.0	185.0	35.0
LM10524TMX/NOPB	DSBGA	YFR	46	1000	210.0	185.0	35.0

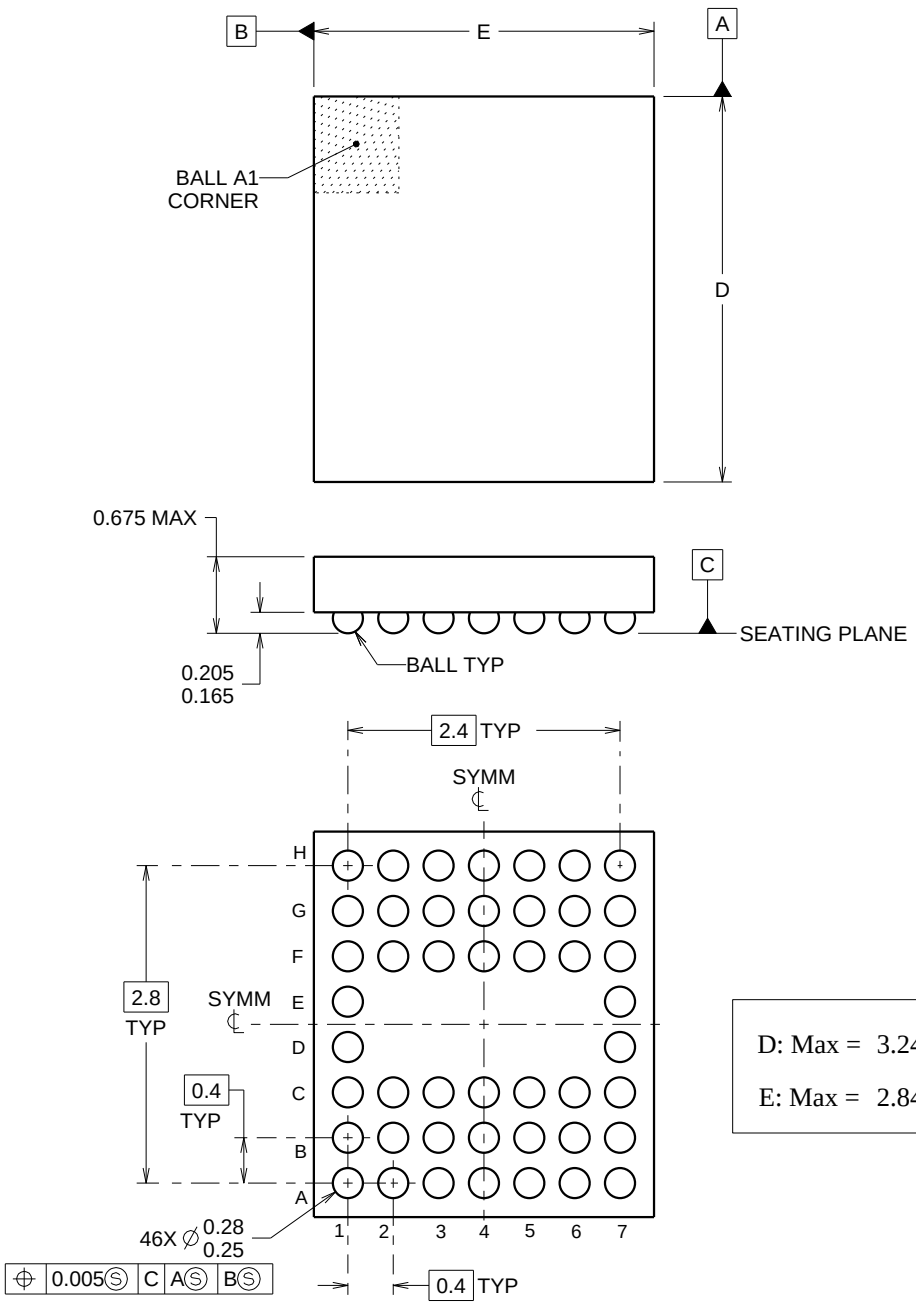


PACKAGE OUTLINE

YFR0046

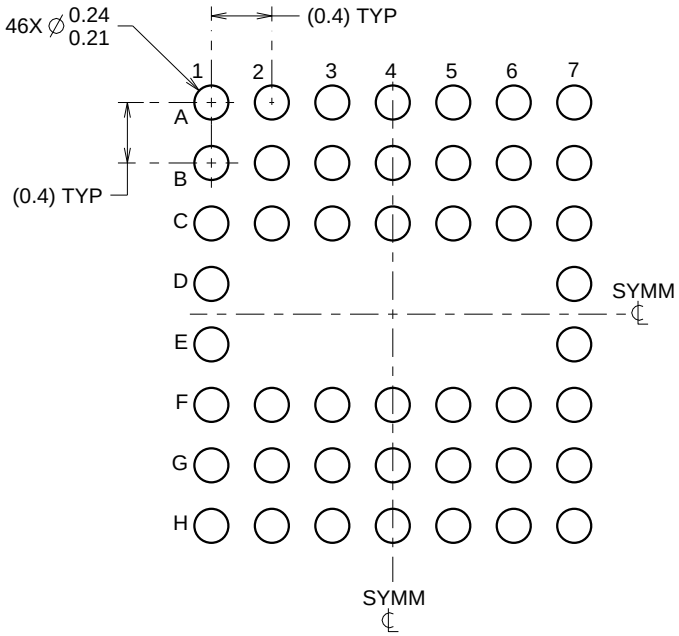
DSBGA - 0.675 mm max height

DIE SIZE BALL GRID ARRAY

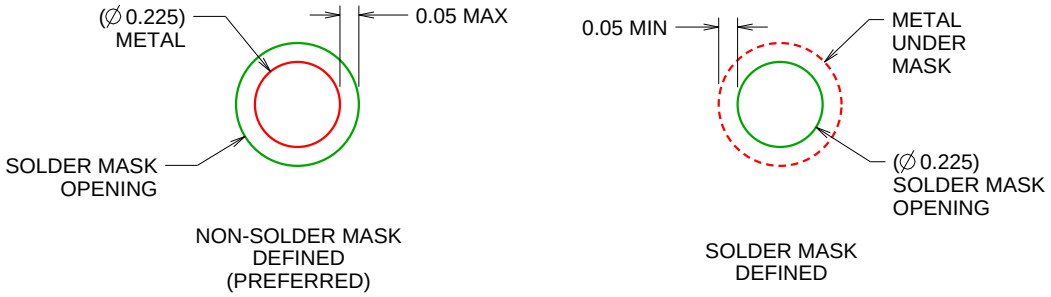


NOTES:

1. All linear dimensions are in millimeters. Any Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

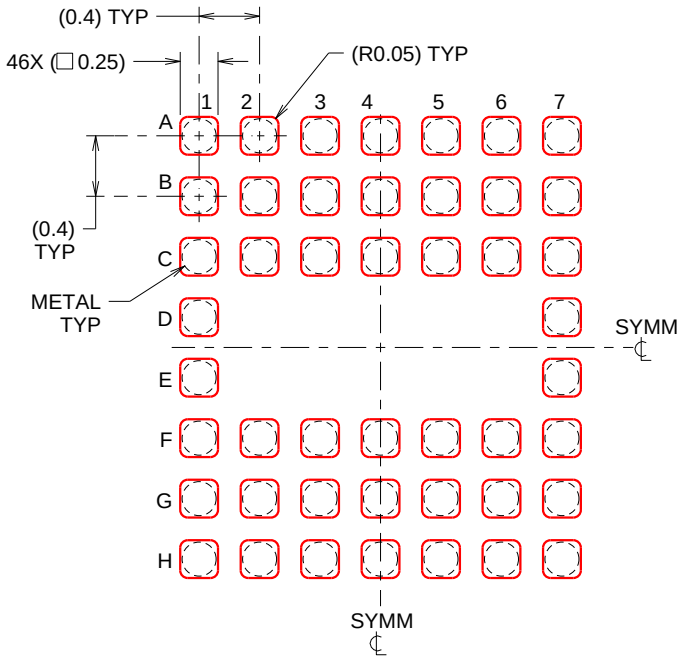
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YFR0046

DSBGA - 0.675 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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