# NTMFS4925N

## MOSFET – Power, Single, N-Channel, SO-8 FL
### 30 V, 48 A

**ON Semiconductor®**

**http://onsemi.com**

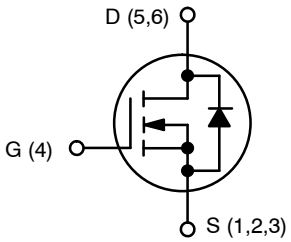
| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 30 V | 5.6 mΩ @ 10 V | 48 A |
| | 8.5 mΩ @ 4.5 V | |

### Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Optimized for 5 V, 12 V Gate Drives
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

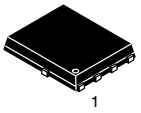
- CPU Power Delivery
- DC−DC Converters




**N−CHANNEL MOSFET**

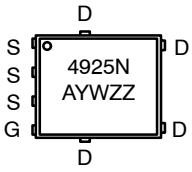
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 30 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JA}$ (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | 16.7 | A |
| | | $T_A$ = 100°C | | 10.5 | |
| Power Dissipation $R_{\theta JA}$ (Note 1) | | $T_A$ = 25°C | $P_D$ | 2.70 | W |
| Continuous Drain Current $R_{\theta JA} \le 10$ s (Note 1) | | $T_A$ = 25°C | $I_D$ | 25.2 | A |
| | | $T_A$ = 100°C | | 15.9 | |
| Power Dissipation $R_{\theta JA} \le 10$ s (Note 1) | | $T_A$ = 25°C | $P_D$ | 6.16 | W |
| Continuous Drain Current $R_{\theta JA}$ (Note 2) | | $T_A$ = 25°C | $I_D$ | 9.7 | A |
| | | $T_A$ = 100°C | | 6.2 | |
| Power Dissipation $R_{\theta JA}$ (Note 2) | | $T_A$ = 25°C | $P_D$ | 0.92 | W |
| Continuous Drain Current $R_{\theta JC}$ (Note 1) | | $T_C$ = 25°C | $I_D$ | 48 | A |
| | | $T_C$ =100°C | | 30 | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | | $T_C$ = 25°C | $P_D$ | 23.2 | W |
| Pulsed Drain Current | $T_A$ = 25°C, $t_p$ = 10 μs, $V_{GS}$ = 10 V | | $I_{DM}$ | 210 | A |
| Current Limited by Package | | $T_A$ = 25°C | $I_{Dmax}$ | 100 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to +150 | °C |
| Source Current (Body Diode) | | | $I_S$ | 21 | A |
| Drain to Source DV/DT | | | $dV/d_t$ | 6.0 | V/ns |




**SO−8 FLAT LEAD**
**CASE 488AA**
**STYLE 1**

**MARKING DIAGRAM**




A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTMFS4925NT1G | SO−8 FL (Pb−Free) | 1500 / Tape & Reel |
| NTMFS4925NT3G | SO−8 FL (Pb−Free) | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2012

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Drain−to−Source Avalanche Energy ($T_J$ = 25°C, $V_{DD}$ = 24 V, $V_{GS}$ = 20 V, $I_L$ = 26 $A_{pk}$, L = 0.1 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 34 | mJ |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

**THERMAL RESISTANCE MAXIMUM RATINGS**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case (Drain) | $R_{\theta JC}$ | 5.4 | °C/W |
| Junction−to−Ambient − Steady State (Note 3) | $R_{\theta JA}$ | 46.3 | |
| Junction−to−Ambient − Steady State (Note 4) | $R_{\theta JA}$ | 136.2 | |
| Junction−to−Ambient − (t ≤ 10 s) (Note 3) | $R_{\theta JA}$ | 20.3 | |

3. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
4. Surface−mounted on FR4 board using the minimum recommended pad size.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 30 | | | V |
| Drain−to−Source Breakdown Voltage (transient) | $V_{(BR)DSSt}$ | $V_{GS}$ = 0 V, $I_{D(aval)}$ = 11.0 A, $T_{case}$ = 25°C, $t_{transient}$ = 100 ns | | 34 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}$/$T_J$ | | | | 21 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 125°C | | | 10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 5) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 1.32 | 1.7 | 2.2 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}$/$T_J$ | $V_{GS}$ = 0 V, $V_{DS}$ = 15 V | | | 3.9 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 30 A | | 4.5 | 5.6 | mΩ |
| | | | $I_D$ = 15 A | | 4.5 | | |
| | | $V_{GS}$ = 4.5 V | $I_D$ = 30 A | | 6.8 | 8.5 | |
| | | | $I_D$ = 15 A | | 6.7 | | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 1.5 V, $I_D$ = 15 A | | | 52 | | S |
| **CHARGES, CAPACITANCES & GATE RESISTANCE** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 15 V | | | 1264 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 483 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 143 | | |
| Capacitance Ratio | $C_{RSS}$ / $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 15 V | | | 0.113 | 0.226 | |

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **CHARGES, CAPACITANCES & GATE RESISTANCE** | | | | | | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V; $I_D$ = 30 A | | | 10.8 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 2.0 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 3.8 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 4.2 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V; $I_D$ = 30 A | | | 21.5 | | nC |
| **SWITCHING CHARACTERISTICS** (Note 6) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 9.5 | | ns |
| Rise Time | $t_r$ | | | | 32.7 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 16.4 | | |
| Fall Time | $t_f$ | | | | 6.2 | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V, $I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 7.4 | | ns |
| Rise Time | $t_r$ | | | | 27.5 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 20.3 | | |
| Fall Time | $t_f$ | | | | 4.1 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 30 A | $T_J$ = 25°C | | 0.86 | 1.1 | V |
| | | | $T_J$ = 125°C | | 0.75 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, dIS/dt = 100 A/μs, $I_S$ = 30 A | | | 25.8 | | ns |
| Charge Time | $t_a$ | | | | 12.4 | | |
| Discharge Time | $t_b$ | | | | 13.4 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 13.6 | | nC |
| **PACKAGE PARASITIC VALUES** | | | | | | | |
| Source Inductance | $L_S$ | $T_A$ = 25°C | | | 1.00 | | nH |
| Drain Inductance | $L_D$ | | | | 0.005 | | nH |
| Gate Inductance | $L_G$ | | | | 1.84 | | nH |
| Gate Resistance | $R_G$ | | | | 0.8 | 2.2 | Ω |

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

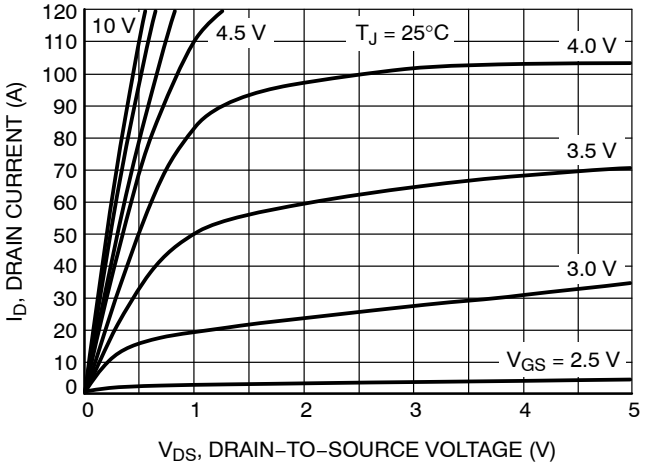



**Figure 1. On−Region Characteristics**

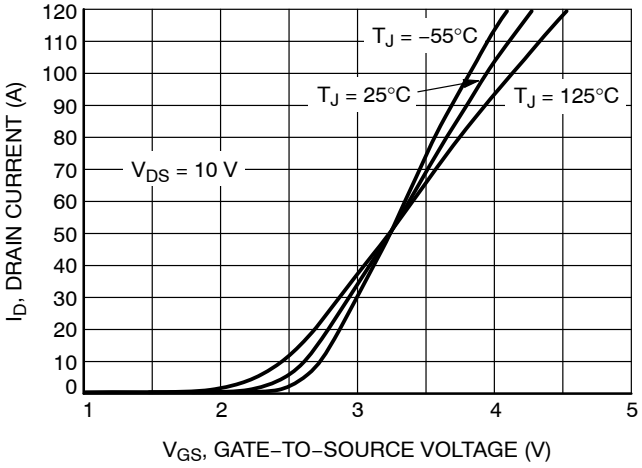



**Figure 2. Transfer Characteristics**

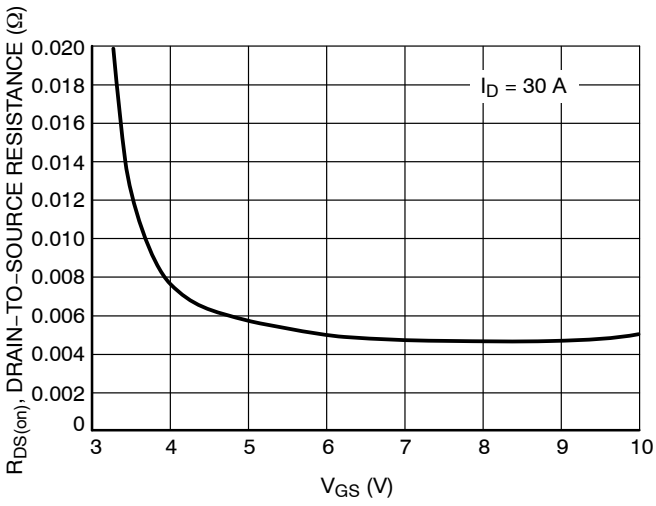



**Figure 3. On−Resistance vs. $V_{GS}$**

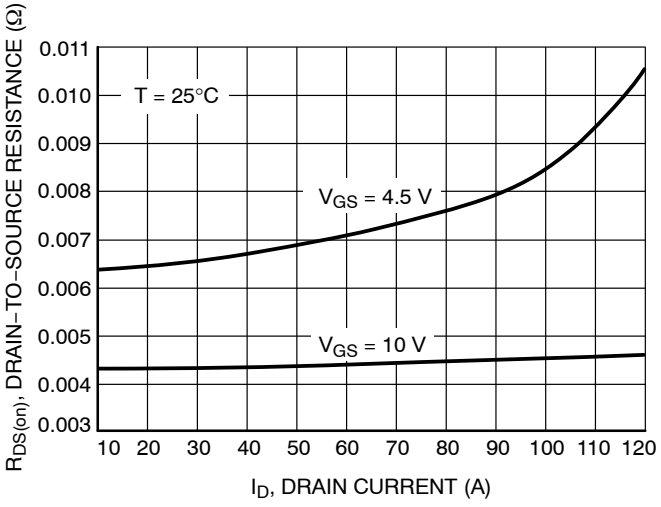



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

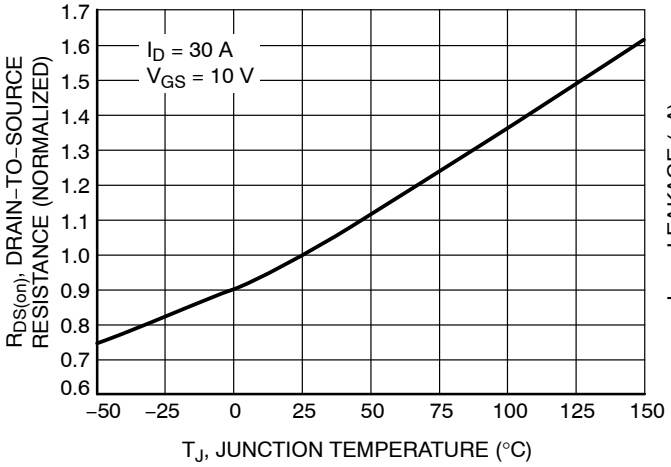



**Figure 5. On−Resistance Variation with Temperature**

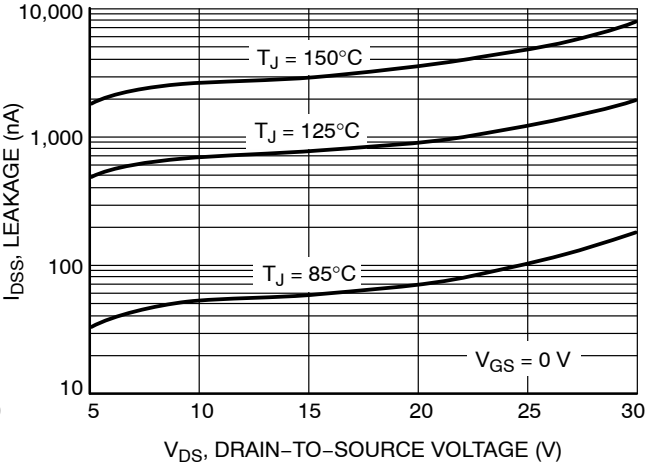



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS

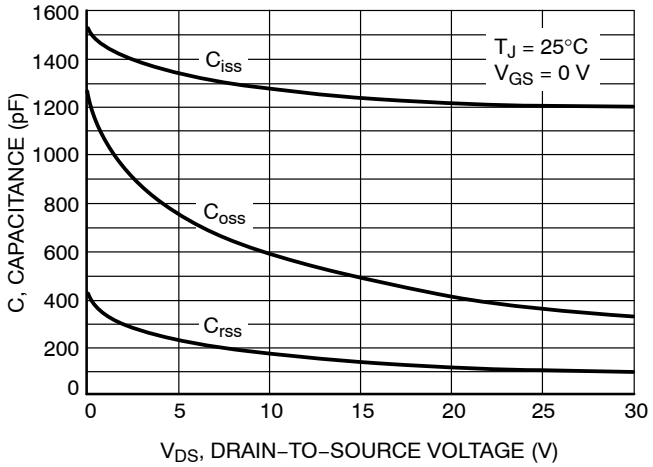



**Figure 7. Capacitance Variation**

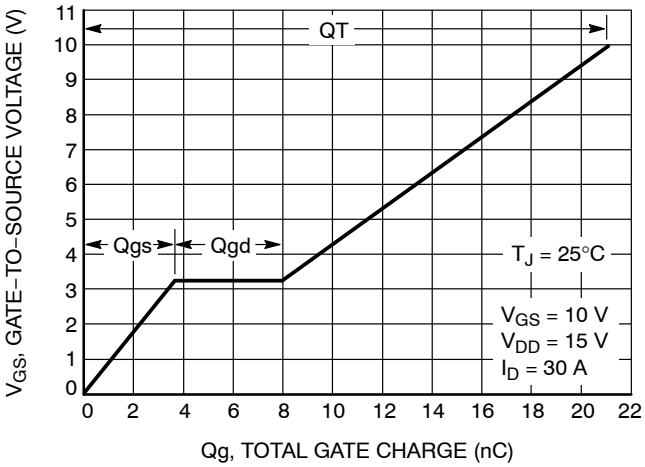



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

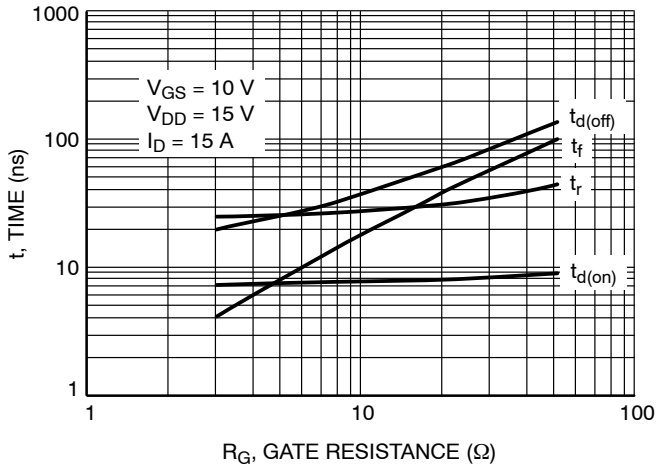



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

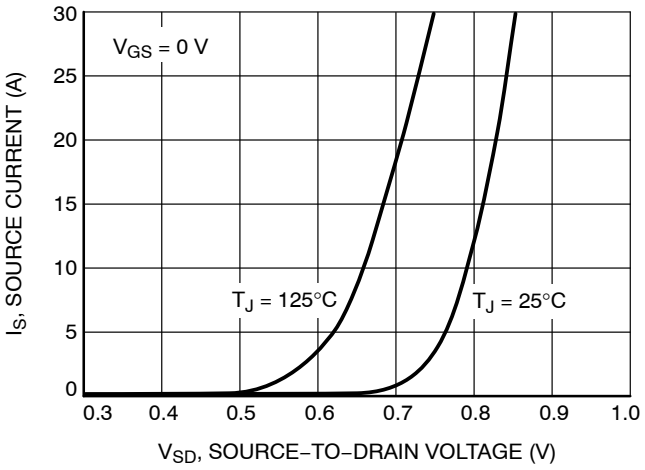



**Figure 10. Diode Forward Voltage vs. Current**

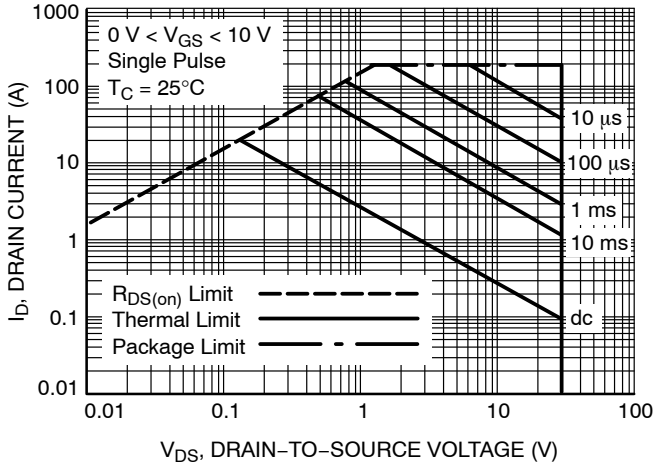



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

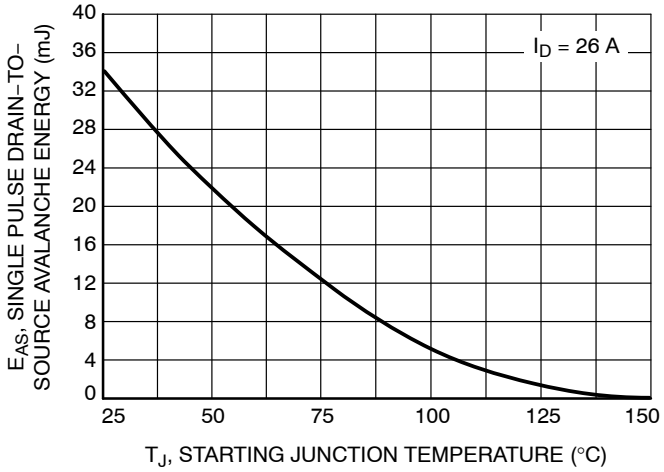



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

## TYPICAL CHARACTERISTICS

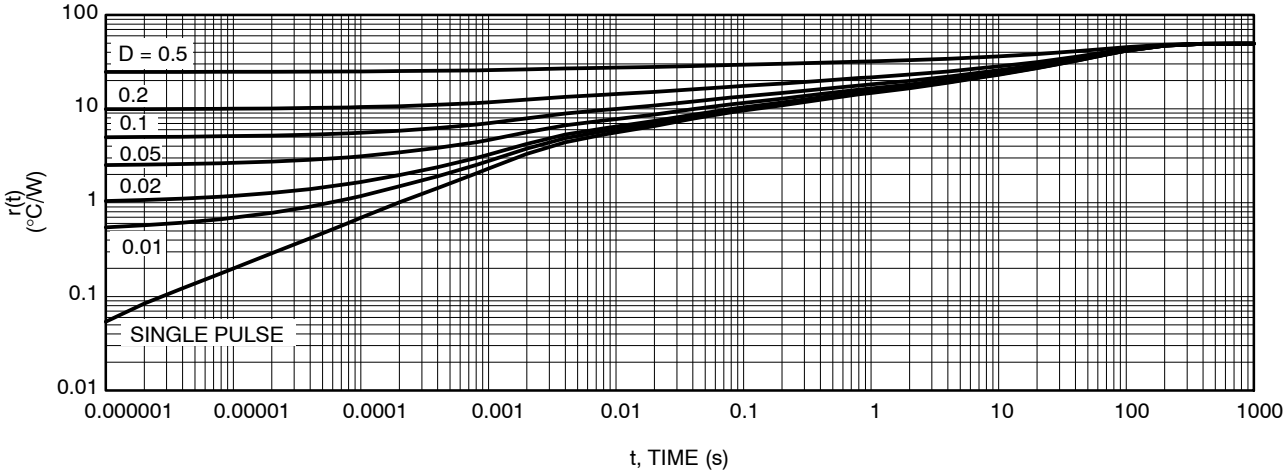
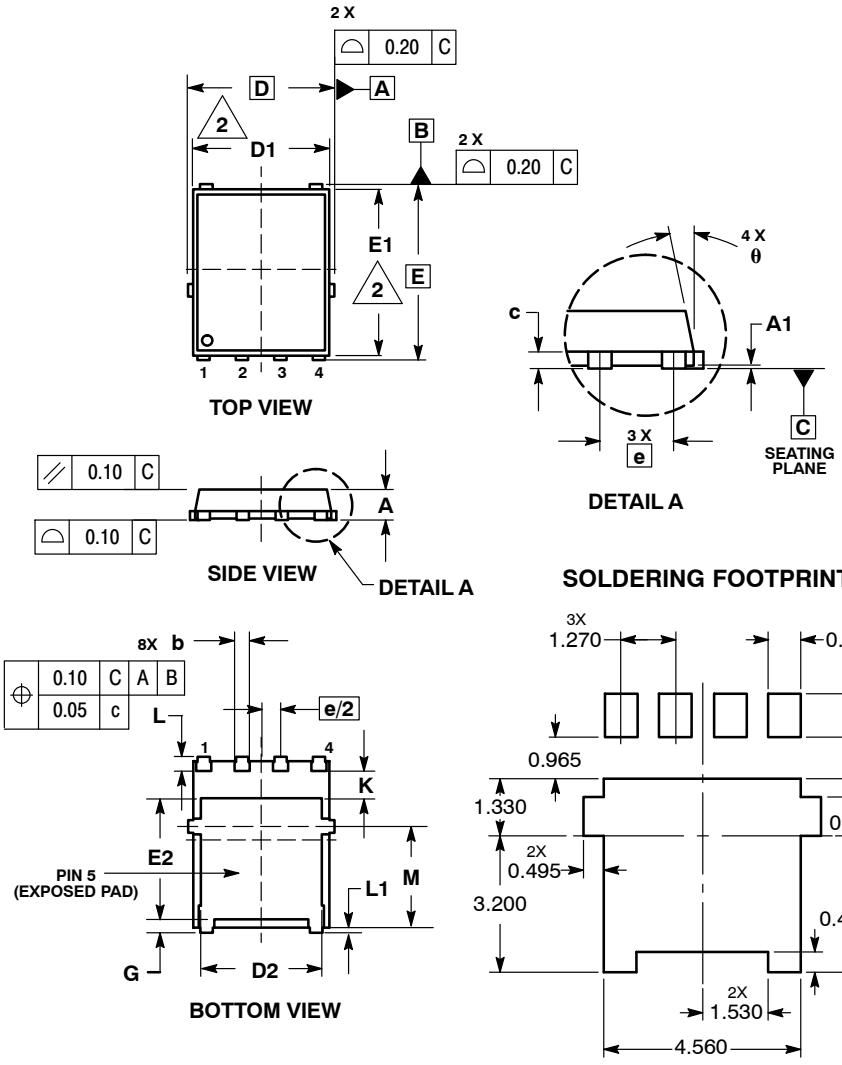



**Figure 13. Thermal Response**

## PACKAGE DIMENSIONS

**DFN5 5x6, 1.27P**
**(SO−8FL)**
CASE 488AA
ISSUE G




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | ––– | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.23 | 0.28 | 0.33 |
| D | | 5.15 BSC | |
| D1 | 4.50 | 4.90 | 5.10 |
| D2 | 3.50 | ––– | 4.22 |
| E | | 6.15 BSC | |
| E1 | 5.50 | 5.80 | 6.10 |
| E2 | 3.45 | ––– | 4.30 |
| e | | 1.27 BSC | |
| G | 0.51 | 0.61 | 0.71 |
| K | 1.20 | 1.35 | 1.50 |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.05 | 0.17 | 0.20 |
| M | 3.00 | 3.40 | 3.80 |
| θ | 0 ° | ––– | 12 ° |

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**ON Semiconductor** and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
**Japan Customer Focus Center**
Phone: 81−3−5817−1050

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative