

# ***THS6042 EVM***

## *User's Guide*

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Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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## Preface

# Read This First

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### ***About This Manual***

This manual provides information about the evaluation module of the amplifier under test. Additionally, this document provides a good example of PCB design for high-speed applications. The user should keep in mind the following points.

It is recommended that the user initially review the data sheet of the device under test.

- ☐ It is helpful to review the schematic and layout of the THS6042 EVM to determine the design techniques used in the evaluation board.
- ☐ The design of the high-speed amplifier PCB is a sensitive process. The user must approach high-speed PCB design with care and awareness.

### ***How to Use This Manual***

This document contains the following chapters:

- ☐ Chapter 1—Introduction and Description
- ☐ Chapter 2—Using the THS6042 EVM
- ☐ Chapter 3—THS6042 EVM Applications
- ☐ Chapter 4—High-Speed Amplifier PCB Layout Tips
- ☐ Chapter 5—EVM Hardware Description

### ***Information About Cautions and Warnings***

This book may contain cautions and warnings.

**This is an example of a caution statement.**

**A caution statement describes a situation that could potentially damage your software or equipment.**

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**A warning statement describes a situation that could potentially cause harm to you.**

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

### **Related Documentation From Texas Instruments**

The URL's below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- ☐ THS6042 data sheet (literature number SLOS264)
- ☐ Application report (literature number SLMA002), *Power Pad Thermally Enhanced Package*,  
<http://www-s.ti.com/sc/psheets/slma004/slma002.pdf>
- ☐ Application report (literature number SLMA004), *Power Pad Made Easy*,  
<http://www-s.ti.com/sc/psheets/slma004/slma004.pdf>
- ☐ Application report (literature number SSYA008), *Electrostatic Discharge (ESD)*, <http://www-s.ti.com/sc/psheets/ssya008/ssya008.pdf>
- ☐ Application report (literature number SLOA100), *Active Output Impedance for ADSL Line Drivers*,  
<http://www-s.ti.com/sc/psheets/sloa100/sloa100.pdf>

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### **Electrostatic Sensitive Components**



**This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.**

### **Trademarks**

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# Introduction and Description

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The Texas Instruments THS6042 evaluation module (EVM) helps designers evaluate the performance of the THS6042 operational amplifier. This EVM is a good example of high-speed PCB design.

This document details the THS6042 EVM. It includes a list of EVM features, a brief description of the module illustrated with a series of schematic diagrams, EVM specifications, details on connecting and using the EVM, and a discussion of high-speed amplifier design considerations.

The EVM enables the user to implement various circuits to clarify the available configurations presented by the EVM schematic. The user is not limited to the circuit configurations presented. The EVM provides enough hardware hooks that the only limitation is the creativity of the user.

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## 1.1 Description

The THS6042 EVM provides a platform for developing high-speed op amp application circuits. It contains the THS6042 high-speed dual op amp, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations. The PC board measures 4.095 by 2.855 inches.

## 1.2 Evaluation Module Features

THS6042 high-speed operational amplifier EVM features include:

- ☐ Active termination capability (R6 and R11)
- ☐ Snubber circuit (R19 and C5), for use with active termination
- ☐ Hooks for a receive path signal (TP1 through TP4)
- ☐ Noninverting gain configuration for DSL
- ☐ Virtual ground capability (JP1, R20, R21)
- ☐ HPF function for ADSL (C3 and R7)
- ☐ Single amp gain stage capability (R9, R10, R22, and C2)
- ☐ Short-loop length for the power supply differential high-frequency path (C8)

## 1.3 THS6042 Operating Conditions

Supply voltage range,  $\pm V_{CC}$       $\pm 5$  to  $\pm 15$  Vdc (see the device data sheet)

Supply current,  $I_{CC}$      (see the device data sheet)

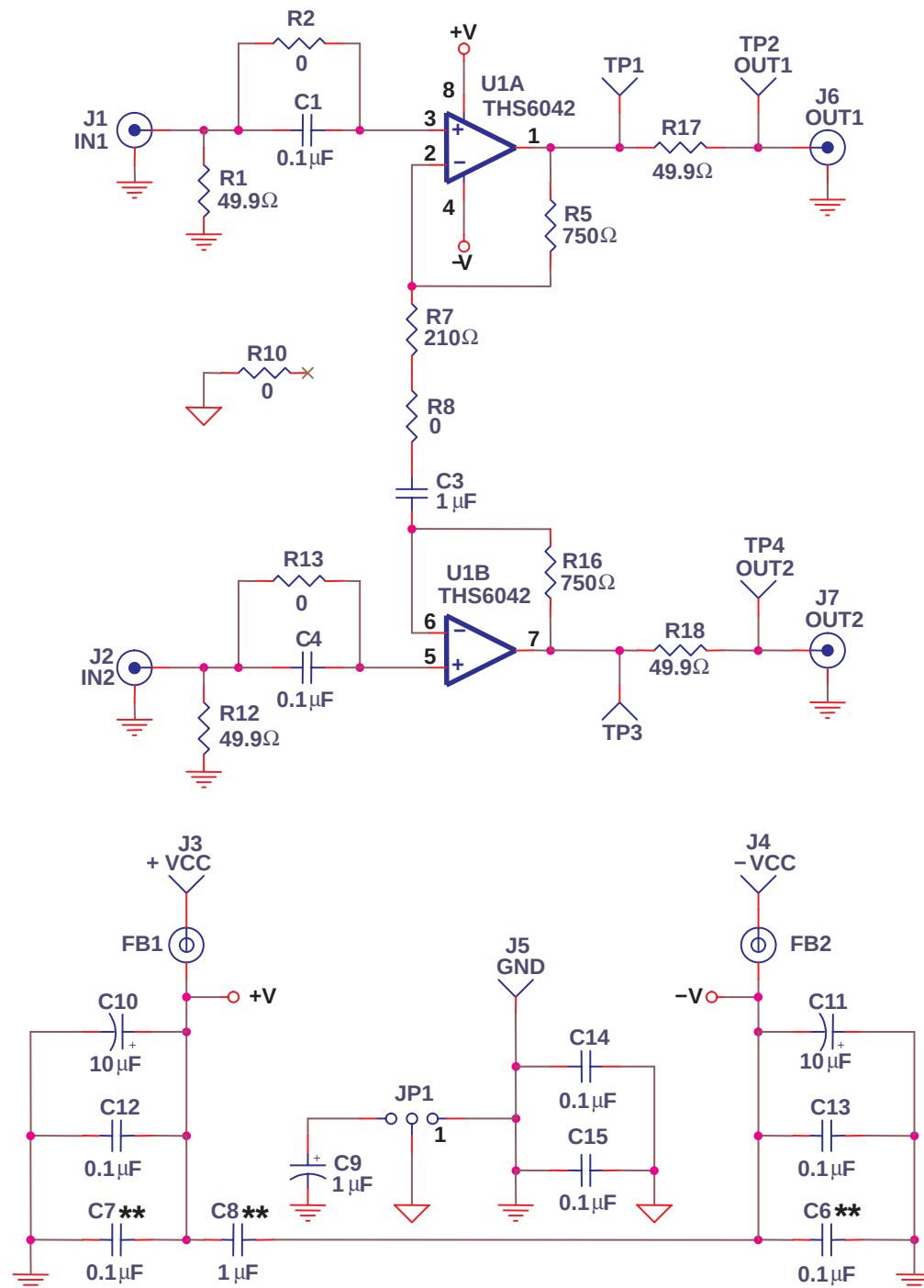
For complete THS6042 amplifier IC specifications, parameter measurement information, and additional application information, see the THS6042 data sheet, TI literature number SLOS264.

## 1.4 EVM Default Configuration

As delivered, the EVM has a fully functional example circuit; just add power supplies, a signal source, and monitoring instrument. See Figure 1–1 for the default schematic diagram. The complete EVM schematic—showing all component locations—is shown in Chapter 5.

The default configuration assumes a differential gain of 4, as determined by R5, R16, and R7 in combination with series matching resistors R17 and R18, and assuming a 50  $\Omega$  load on the outputs at J6 and J7.

Some components such as R10, C6–C15, FB1, FB2, JP1, J3, J4, and J5 are omitted on the application schematics of Chapter 3 for clarity.



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# Using the THS6042 EVM

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This section describes how to connect the THS6042 EVM to test equipment. It is recommended that the user connect the EVM as described in this section to avoid damage to the EVM or the THS6042 installed on the board.

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## 2.1 Required Equipment

- ☐ Dual dc output power supply ( $\pm 15$  V, 200-mA output minimum).
- ☐ Two dc current meters with resolution to 1 mA and capable of a maximum current which the dc power supply can supply. If available, set the current limit on the dc power supply to 200 mA.

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**Note:** Some power supplies incorporate current meters which may be applicable to this test..

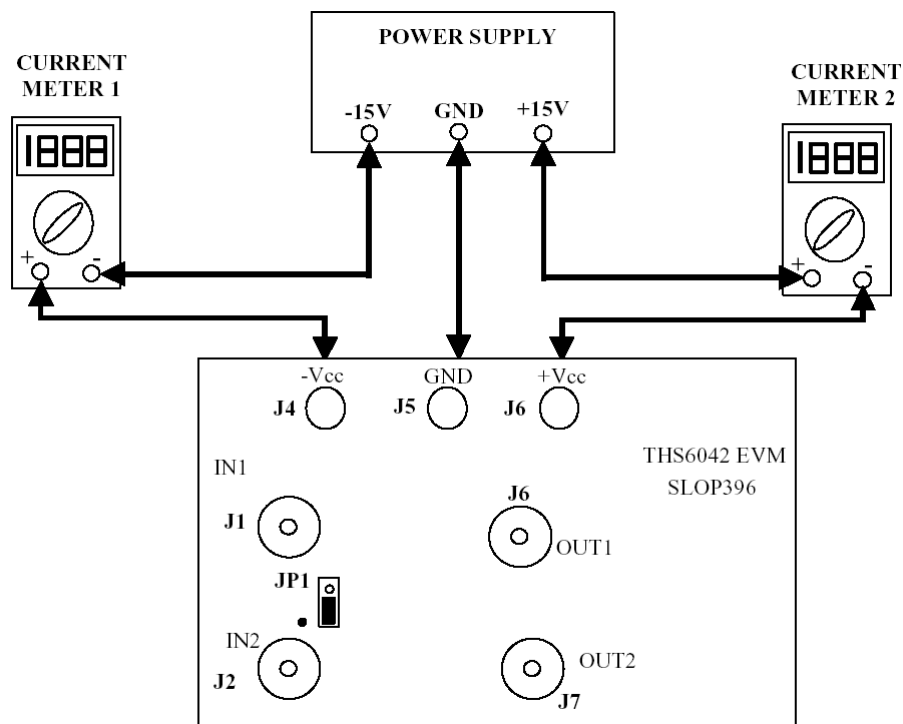
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- ☐ 50- $\Omega$  source impedance function generator (1 MHz, 10 V<sub>PP</sub> sine wave).
- ☐ Oscilloscope (50-MHz bandwidth minimum, 50- $\Omega$  terminated BNC input).

## 2.2 Power Supply Setup (Reference Figure 2–1)

- ☐ Set the dc power supply to  $\pm 15$  V.
- ☐ Make sure the dc power supply is turned off before proceeding to the next step.
- ☐ Connect the +15 V supply to the + input on current meter 2 (if applicable).
- ☐ Connect the – input on current meter 2 to J6 (+V<sub>CC</sub>) on the EVM.
- ☐ Connect the –15 V supply to the + input on current meter 1 (if applicable).
- ☐ Connect the + input on current meter 1 to J4 (–V<sub>CC</sub>) on the EVM.
- ☐ Make sure both dc current meters are set to at least 1-mA resolution and can withstand the maximum output current of the power supplies.
- ☐ Connect the ground(s) of the +15 V and –15 V power supply to J5 (GND) on the EVM.
- ☐ Verify JP1 is connected to the 1–2 position (lower posts).

Figure 2–1. Power Supply Connection

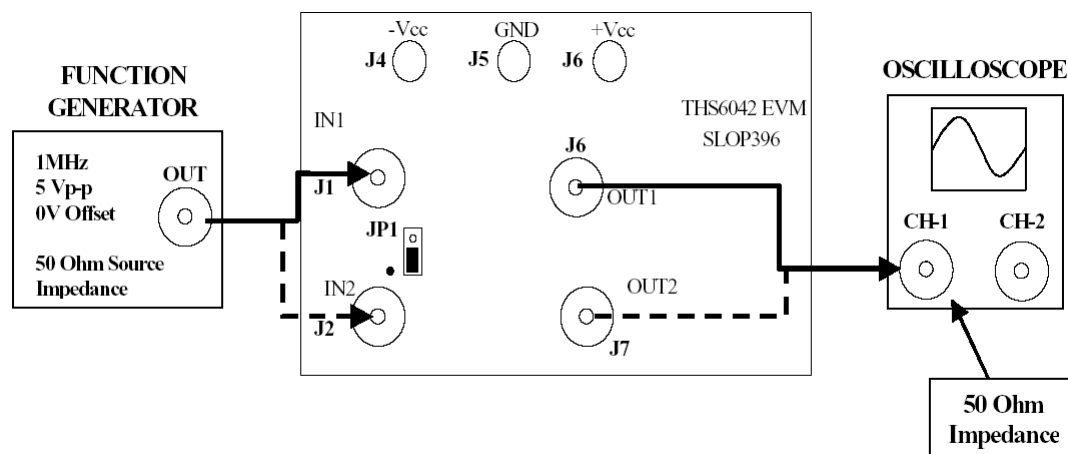


## 2.3 Input and Output Test Setup (Reference Figure 2–2)

- ☐ Set the function generator to a 1 MHz,  $\pm 2.5$  V (5 V<sub>PP</sub>) sine wave with no dc offset.
- ☐ Turn off the function generator before proceeding to the next step.
- ☐ Using a BNC cable, connect the function generator to J1 (IN1 BNC) on the EVM.
- ☐ Using a BNC cable, connect the oscilloscope to J6 (OUT1 BNC) on the EVM. Set the oscilloscope to 2 V/Division and a time-base of 0.2  $\mu$ Sec/Division.

**Note:** The Oscilloscope must be set in a 50- $\Omega$  termination for proper operation..

Figure 2–2. Signal Connections





# THS6042 EVM Applications

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Example applications are presented in this chapter. These applications demonstrate the most popular circuits to the user, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques. That is the function of an evaluation board.

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### 3.1 Standard Gain Configuration

The THS6042 EVM default configuration is a fully differential input, fully differential output gain of 4 (at the output connectors) as shown in Figure 3–1. This gain is calculated according an equation that is similar to the one that describes an instrumentation amplifier:

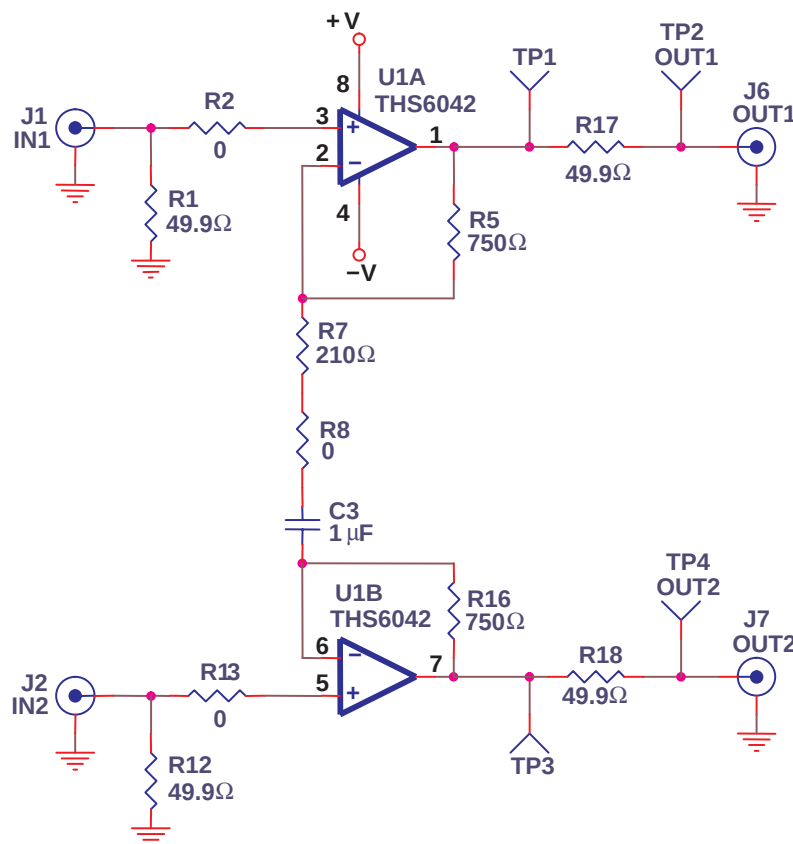
$$\text{Differential gain} = \frac{V_O(\text{diff})}{V_I(\text{diff})} = 1 + \frac{2 \times R5}{R7} \quad (1)$$

Where:

$$R5 = R16$$

Series resistors R17 and R18 affect output voltage at J6 and J7. The designer needs to take the voltage divider law into account for their load impedance and R17/R18. When a designer monitors the output at TP1 and TP3 using a high-impedance differential probe, the default gain is 8.

Figure 3–1. Default Configuration Operation



### 3.2 Single Supply Operation

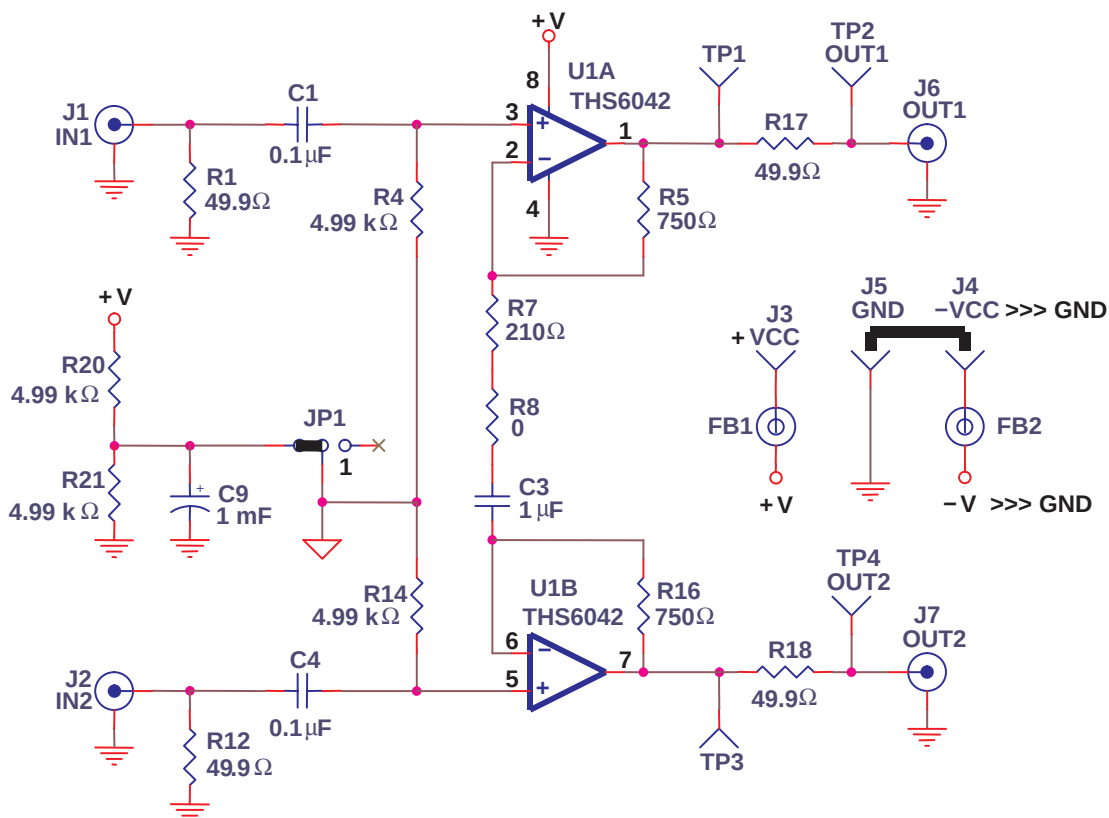
About half of designs use single supply, and the THS6042 EVM allows single supply operation. The THS6042 EVM can be reconfigured for single supply operation as shown in Figure 3–2. To convert to single supply operation:

- ☐ Connect ground from the power supply to both J5 (GND) and J4 ( $-V_{CC}$ ).
- ☐ Jumper pins 2 and 3 of JP1 together with a jumper plug. This enables connection to a *half supply* voltage divider.
- ☐ Populate R4, R14, R20, and R21, with 4.99 k $\Omega$  1% resistors. R20 and R21 create the *half supply* potential (virtual ground for the stage). R4 and R14 sum this potential into the noninverting inputs of the op amps.

The *half-supply* virtual ground potential is also present on the output of the op amps. No provision has been made on the EVM for output dc blocking capacitors. When the outputs are monitored with equipment that has 50  $\Omega$  inputs, 75 mW is dissipated through R17, R18, and the input resistors of the measuring equipment.

- ☐ Remove R2 and R13. C1 and C4 are then used as dc blocking capacitors.

Figure 3–2. Single-Supply Operation



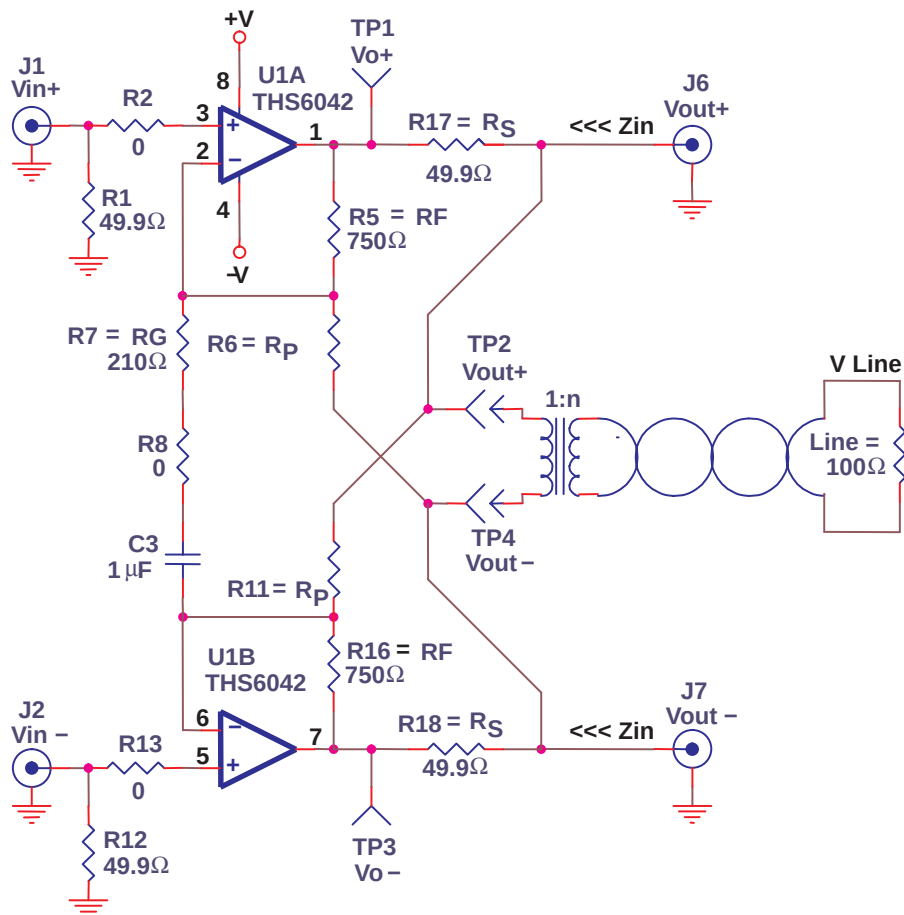
### 3.3 Active Termination

Active termination is a technique that allows the designer to use a small value resistor for the series resistance (R17 or R18). The circuit then utilizes positive feedback to make the impedance of this resistor, when looking from the line-side, appear much larger. This accomplishes two things:

- ❑ A very small resistance when the line-driver amplifier transmits signals to the line. This lowers the output voltage swing range required from the driver stage.
- ❑ Proper matching impedance when looking from the line to the amplifier.

Figure 3–3 shows the basic circuit for differential positive feedback.

Figure 3–3. Differential Positive Feedback



Active feedback creates larger impedance ( $Z$ ) than what is actually placed there by series resistors  $R_S$ :

$$Z(\Omega) = \frac{R_S}{1 - \frac{R_F}{R_P}} \quad (2)$$

The important thing to consider is that regardless of the forward gain from  $V_I$  to  $V_O$ , the active impedance ( $Z$ ) value remains constant.

Now that the return impedance is corrected, forward voltage gain from input to output is calculated. Equation 3 shows the simplified forward gain from  $V_I$  to  $V_O$ .

$$A_V = \frac{V_O}{V_{in}} = \frac{1 + \left( \frac{R_F}{R_G \parallel R_P} \right)}{1 - \left( \frac{R_F}{R_P} \right) \left( \frac{R_L}{R_L + R_S} \right)} \text{ iff } R_L \ll R_P \quad (3)$$

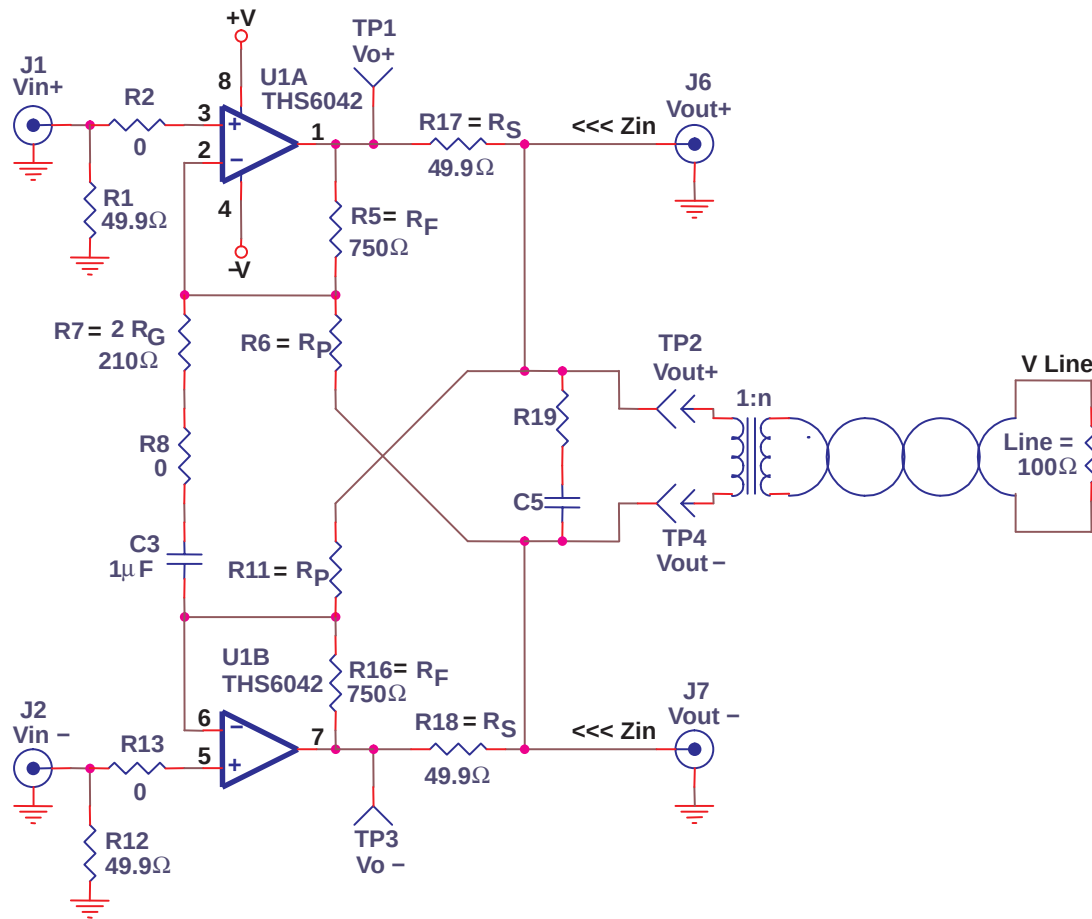
Where:

$$R_L = \frac{R_{LINE}}{2 n^2} \quad (4)$$

The reader is cautioned that active termination is a very complex topic, with many considerations. Carefully read the Texas Instruments Application Report, *Active Output Impedance for ADSL Line Drivers*, SLOA100 to gain a more complete understanding of the topic and all of the subtle implications of active termination.

### 3.4 Snubber Circuit

Figure 3–4. Addition of Snubber Circuit to Active Termination



R19 and C5 are located on the EVM so that a snubber circuit may be implemented. Some transformers have a high resonance frequency (as low as 25 MHz but as high as 150 MHz). When using traditional termination (just R17 and R18—no active termination), there is typically no reason to use these components. But, when active termination is used, the effective impedance of these two resistor values drop substantially. Thus, there can be very small resistor isolation between the amplifier and a resonance problem. Couple this with the feedback path of R6 and R11, and this can cause the amplifier to oscillate. The snubber is utilized to eliminate this oscillation. As a rule, to select the proper snubber values, select:

$$R19 = 2 \times \frac{R_{\text{LINE}}}{n^2} \quad (5)$$

Then select C5:

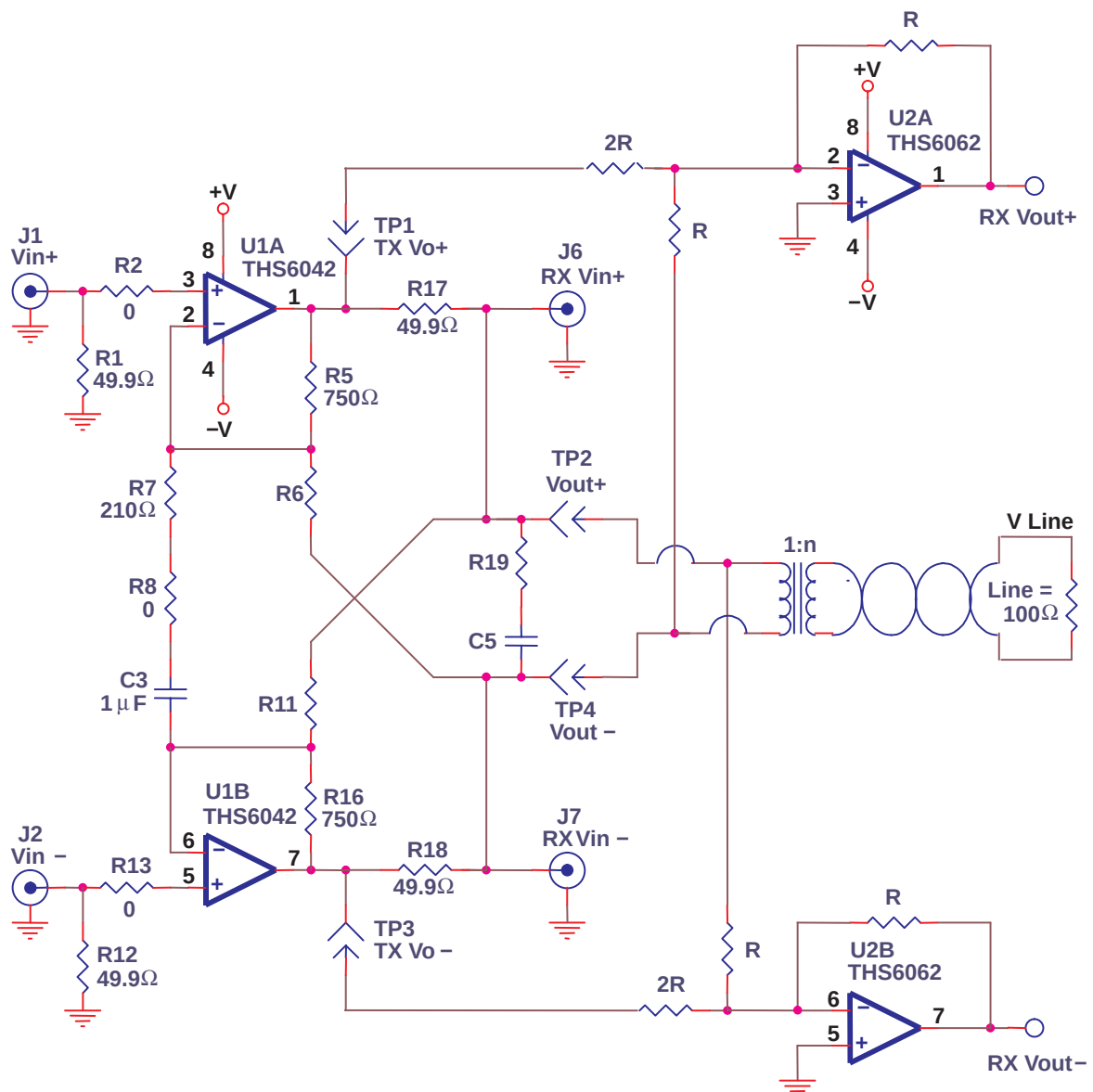
$$C5 = \frac{1}{2 \times \pi \times R19 \times F_C} \quad (6)$$

where  $F_C$  = at least 10X the highest operating frequency (1.104 MHz is the highest ADSL operating frequency). 20X or even larger may be preferable.

### 3.5 Receive Path Implementation

Test points TP1 through TP4 are located on the EVM to facilitate the addition of the receive signal path to the signal chain as shown in Figure 3-5. When implementing the receive path, a *hybrid* must be used, as ADSL is full duplex. The hybrid cancels out the TX signal and allows the RX signal from the line to come through. The THS6042 EVM does not have *hybrid* circuitry included. Texas Instruments assumes that the customer has a proprietary hybrid design they would prefer to implement. Each customer should know their nominal line impedance characteristics and thus should be able to match them better. Texas Instruments does have an EVM that contains a THS6062 ADSL receiver. The EVM can be purchased separately to facilitate construction of a complete ADSL transmit/receive interface.

Figure 3-5. Implementation of the Receive Signal Path

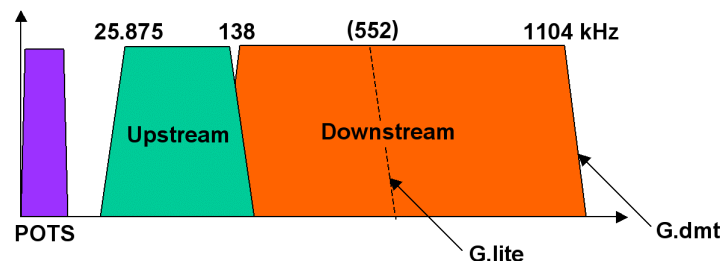


### 3.6 High-Pass Filter

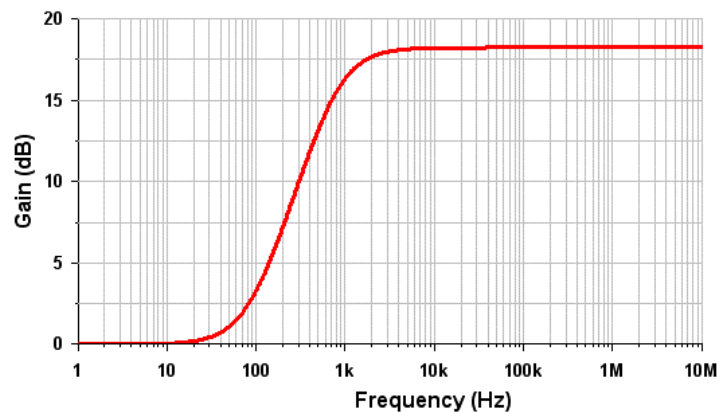
Because ADSL CPE is designed to transmit from 25.875 kHz to 138 kHz, C3 and R7 can be used to implement a HPF function. These are selected to be 20X lower than 25 kHz (1.25 kHz). Some designs use a capacitor—some do not. This path allows for a common gain setting between the two channels. This helps (but does not assure) that the signals are truly differential.

Figure 3–6 compares the frequency spectrum of ADSL to a simulation of the high-pass filter on the THS6042 EVM.

Figure 3–6. ADSL Spectrum and High-Pass Filter Response



(Above not on a logarithmic scale)



**Note:** The high-pass filter function is not a true high-pass filter. C3 in series with R7 creates a zero at about 10 Hz. As the frequency decreases from about 3 kHz to 10 Hz, the circuit changes from a gain stage into two unity gain buffers.



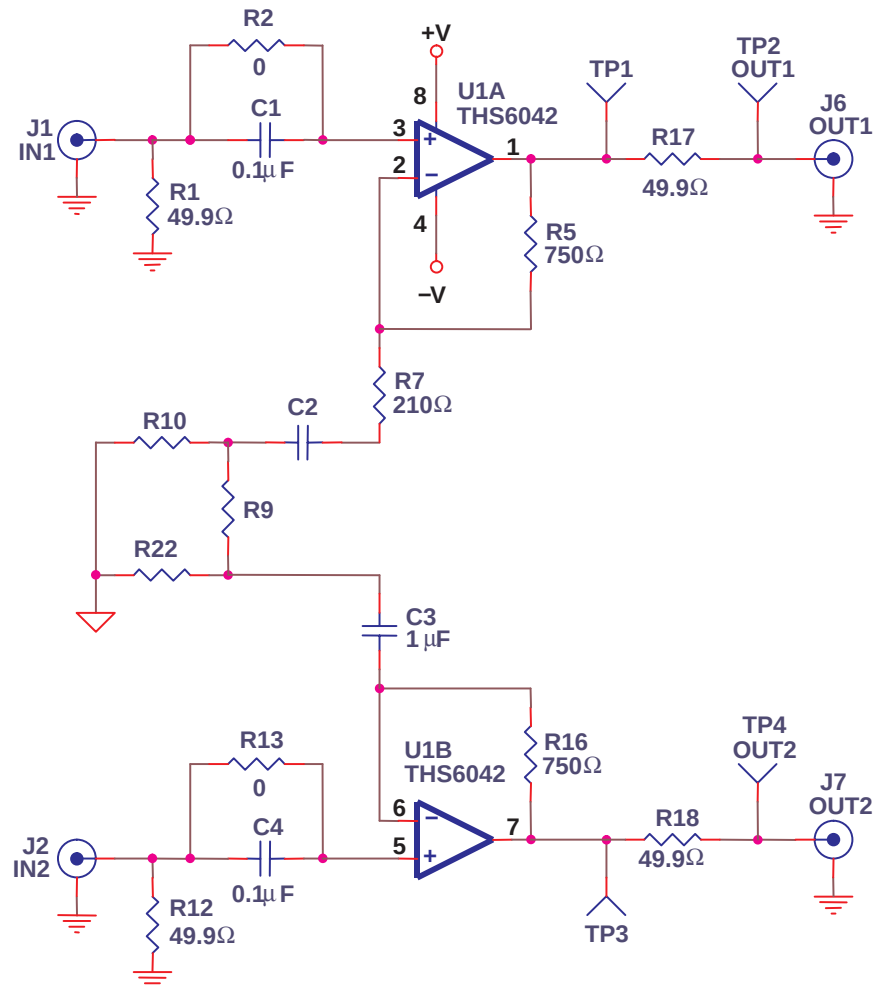
### 3.7 Single-Ended Gain Stages

Although ADSL is the obvious application for the THS6042 EVM, it can also be configured for other applications. If the common gain resistor R8 is removed, there is an array of components that allow various dc-coupled and ac-coupled gain stages to be constructed.

Referring to Figure 3–7, for example, two dc coupled gain stages could be formed by removing R9, making R10 0- $\Omega$ , shorting C2 and C3 with 0- $\Omega$  jumpers, and making R7 and R22 gain resistors for the two individual stages. There are many possibilities.

If for some reason the user does not want to use common gain resistor R7, they can remove R8 and utilize R9 and C2 (through R10) or utilize just R22 and C2/R10. This redundancy was done because layout would make these nodes too far away from the amplifier channels. This allows for a shorter connection path—needed for good high frequency performance.

Figure 3–7. Single-Ended Amplifier Configuration



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# High-Speed Amplifier PCB Layout Tips

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The THS6042 EVM layout, designed for use with high-speed signals, can be used as an example when designing PCBs incorporating the THS6042. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Disregarding these basic design considerations could result in less than optimum performance of the THS6042 high-speed operational amplifier. Surface-mount components were selected because of the extremely low lead inductance associated with this technology. This helps minimize both stray inductance and capacitance. Also, because surface-mount components are physically small, the layout can be very compact.

Tantalum power supply bypass capacitors at the power input pads help filter switching transients from the laboratory power supply. Power supply bypass capacitors are placed as close as possible to the IC power input pins to minimize the return path impedance. This improves high-frequency bypassing and reduces harmonic distortion. The GND side of these capacitors should be located close to each other, minimizing the differential current loops associated with differential output currents. If poor high frequency performance is observed, replace the 0.1- $\mu$ F capacitors with microwave capacitors with a self-resonance at the frequency that produces trouble. A proper ground plane on both sides of the PCB should be used with high-speed circuit design. This provides low-inductive ground connections for return current paths.

In the area of the amplifier input pins, the ground plane has been removed to minimize stray capacitance and to reduce ground plane noise coupling into these pins. This is especially important for the inverting input pin. A capacitance as low as 1-pF at the inverting input can significantly affect the response of the amplifier or even cause oscillation.

In general, it is best to keep signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50  $\Omega$  or 75  $\Omega$ , as required by the application. Such a signal line must also be properly terminated with an appropriate resistor.

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The printed-circuit board that is used with PowerPAD packages must have features included in the design to remove the heat from the package efficiently. As a minimum, there must be an area of solder-tinned-copper underneath the PowerPAD package. This area is called the thermal land. The thermal land varies in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat to be removed. In addition, this thermal land may or may not contain thermal vias depending on PCB construction. The requirements for thermal lands and thermal vias are detailed in <http://www-s.ti.com/sc/techlit/slma002> and <http://www-s.ti.com/sc/techlit/slma004>.

Finally, all inputs and outputs must be properly terminated, either in the layout or in the load instrumentation. Unterminated lines, such as coaxial cable, can appear to be a reactive load to the amplifier. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears to be purely resistive, and reflections are absorbed at each end of the line. Another advantage of using an output termination resistor is that capacitive loads are isolated from the amplifier output. This isolation helps minimize the reduction in the amplifier's phase-margin and improves the amplifier stability, resulting in reduced peaking and settling times.

On boards operated from dual power supplies, it is helpful to place a capacitor directly across the positive and negative power supplies. This helps the fully differential drive.

# EVM Hardware Description

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This chapter describes the EVM hardware. It includes the EVM parts list, and printed-circuit board layout.

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## 5.1 Bill of Materials

Table 5-1. THS6042 EVM Bill of Materials

| ITEM | DESCRIPTION                                          | REF DESIGNATOR                               | PCB QTY | MANUFACTURER'S PART NUMBER                                  | DISTRIBUTOR'S PART NUMBER                                |
|------|------------------------------------------------------|----------------------------------------------|---------|-------------------------------------------------------------|----------------------------------------------------------|
| 1    | Bead, ferrite, 3 A, 80 $\Omega$ , SMD size 1206      | FB1, FB2                                     | 2       | (Steward)<br>HI1206N800R-00<br>(Panasonic)<br>EXC-ML32A680U | (Digi-Key)<br>240-1010-1-ND<br>(Digi-Key)<br>P10437CT-ND |
| 2    | Open, size 0805                                      | C2                                           | 1       |                                                             |                                                          |
| 3    | Open, size 1206                                      | C5, R19                                      | 2       |                                                             |                                                          |
| 4    | Cap, 1.0 $\mu$ F, tantalum, 35 V, SMT size B         | C9                                           | 1       | (Panasonic)<br>ECS-T1VX105R                                 | (Digi-Key)<br>PCS6105CT-ND                               |
| 5    | Cap, 10 $\mu$ F, tantalum, 35 V, SMT, size D         | C10, C11                                     | 2       | (Panasonic)<br>ECS-T1VD106R<br>(AVX) TAJD106K035R           | (Digi-Key)<br>PCS6106CT-ND<br>(Allied) 213-1154          |
| 6    | Cap, 1.0 $\mu$ F, ceramic, Y5 V, 50 V, SMD size 1210 | C8                                           | 1       | (Murata)<br>GRM42-2Y5V105Z50D<br>500                        |                                                          |
| 7    | Cap, 1.0 $\mu$ F, ceramic, X7R, 25 V, SMD size 1206  | C3                                           | 1       | (Panasonic)<br>ECJ-3YB1E105K                                | (Digi-Key)<br>PCC1893CT-ND                               |
| 8    | Cap, 0.1 $\mu$ F, ceramic, X7R, 25 V, SMD size 1206  | C1, C4                                       | 2       | (Panasonic)<br>ECJ-3VB1E104K                                | (Digi-Key)<br>PCC1883CT-ND                               |
| 9    | Cap, 0.1 $\mu$ F, ceramic, 20%, 50 V, SMD size 0805  | C6, C7, C12, C13, C14, C15                   | 6       | (Murata)<br>GRM40Z5U104M050AD                               | (Allied) 231-0182                                        |
| 10   | Resistor, 0 $\Omega$ , SMD size 0805                 | R8, R10                                      | 2       | (KOA) RM73Z2A000                                            | (Garrett) RM73Z2A000                                     |
| 11   | Resistor, 210 $\Omega$ , 1/8 W, 1%, SMD size 0805    | R7                                           | 1       | (Phycomp)<br>9C08052A2100FKHFT                              | (Garrett)<br>9C08052A2100FKHFT                           |
| 12   | Resistor, 750 $\Omega$ , 1/8 W, 1%, SMD size 0805    | R5, R6                                       | 2       | (Phycomp)<br>9C08052A7500FKHFT                              | (Garrett)<br>9C08052A7500FKHFT                           |
| 13   | Open, size 0805                                      | R3, R4, R6, R9, R11, R14, R15, R20, R21, R22 | 10      |                                                             |                                                          |
| 14   | Resistor, 0 $\Omega$ , size 1206                     | R2, R13                                      | 2       | (KOA) RM73Z2B000                                            | (Garrett) RM73Z2B000                                     |
| 15   | Resistor, 49.9 $\Omega$ , 1/4 W, 1% SMD size 1206    | R1, R12, R17, R18                            | 4       | (Phycomp)<br>9C12063A49R9FKRFT                              | (Garrett)<br>9C12063A49R9FKRFT                           |
| 16   | Header, 0.1" CTRS, 0.025" SQ. pins                   | JP1                                          | 1       | (Sullins) PZC36SAAN                                         | (Digi-Key)<br>S1011-36-ND                                |
| 17   | Shunts                                               |                                              | 1       | (Sullins) SSC02SYAN                                         | (Digi-Key) S9002-ND                                      |
| 18   | Test points (black)                                  | TP2, TP4                                     | 2       | (Keystone) 5001                                             | (Allied) 839-3601                                        |
| 19   | Test points (red)                                    | TP1, TP3                                     | 2       | (Keystone) 5000                                             | (Allied) 839-3600                                        |
| 20   | Jack, banana receptance, 0.25" diameter hole         | J3, J4, J5                                   | 3       | (HH Smith) 101                                              | (Newark) 35F865                                          |
| 21   | Connector, BNC, vertical, PCB                        | J1, J2, J6, J7                               | 4       | (Amphenol) 31-5329                                          | (Allied) 713-7160<br>(Newark) 89F2885                    |
| 22   | Standoff, 4-40 hex, 0.625" length                    |                                              | 4       | (Keystone) 1804                                             | (Allied) 839-2089                                        |
| 23   | Screw, Phillips, 4-40, .250"                         |                                              | 4       |                                                             |                                                          |
| 24   | IC, THS6042                                          | U1                                           | 1       | (TI) THS6042DDA                                             |                                                          |
| 25   | PCB, THS SO8 PWP EVM, SLOP396                        | PCB1                                         | 1       |                                                             |                                                          |

## 5.2 Circuit Board Layout

Figure 5–1. Top Layer (Signals for THS6042 EVM)

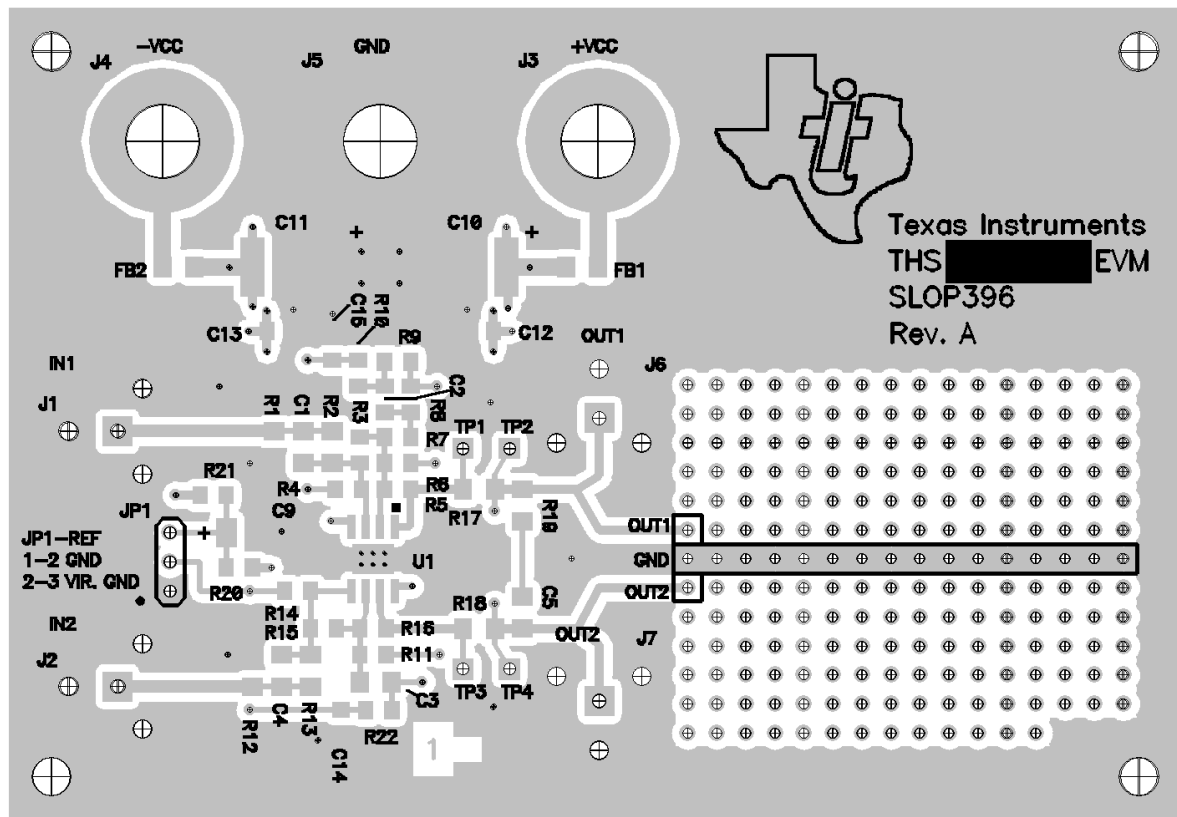
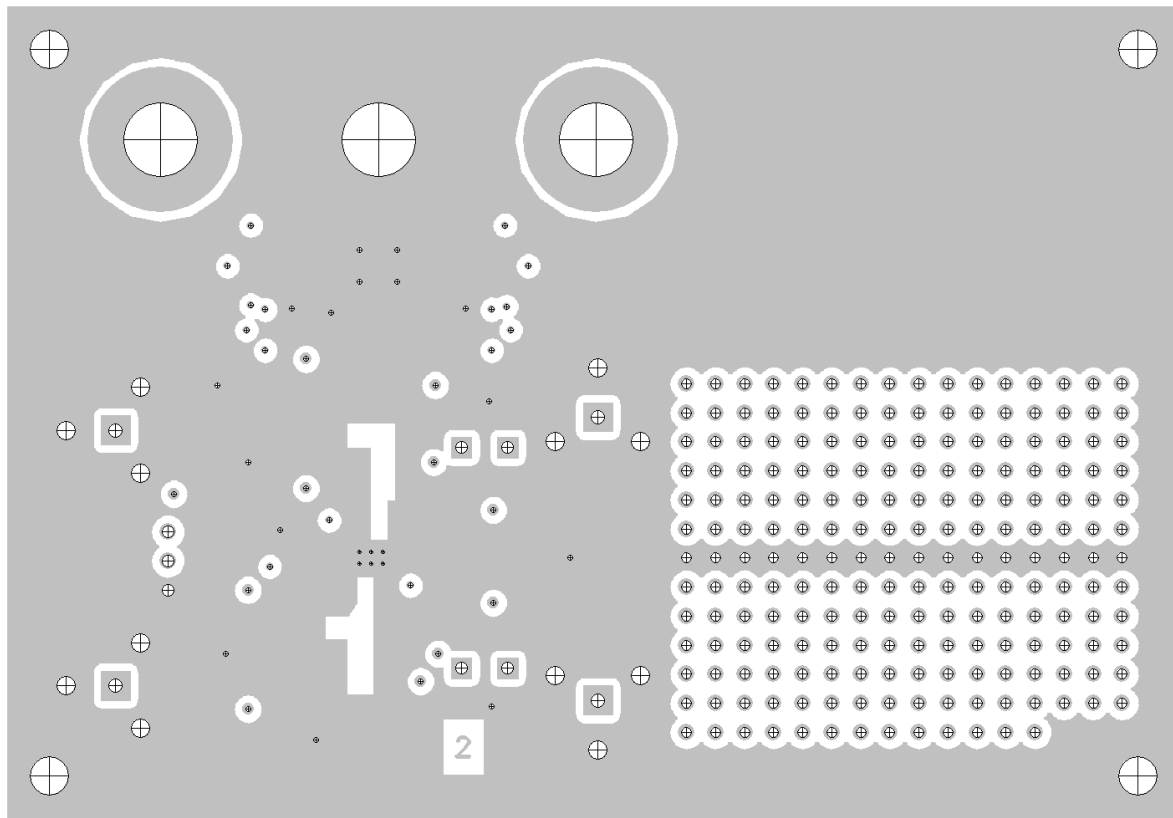


Figure 5–2. Internal Plane (Layer 2) (Ground 1 Plane)





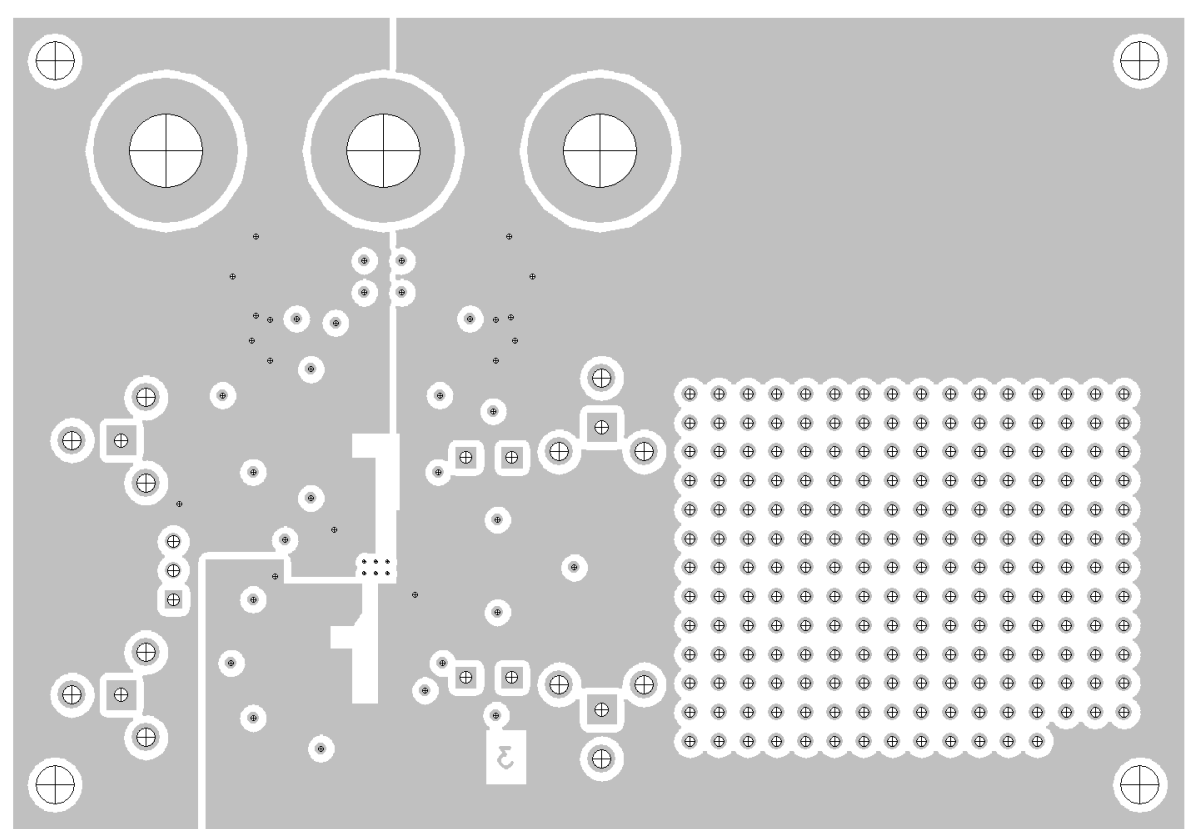
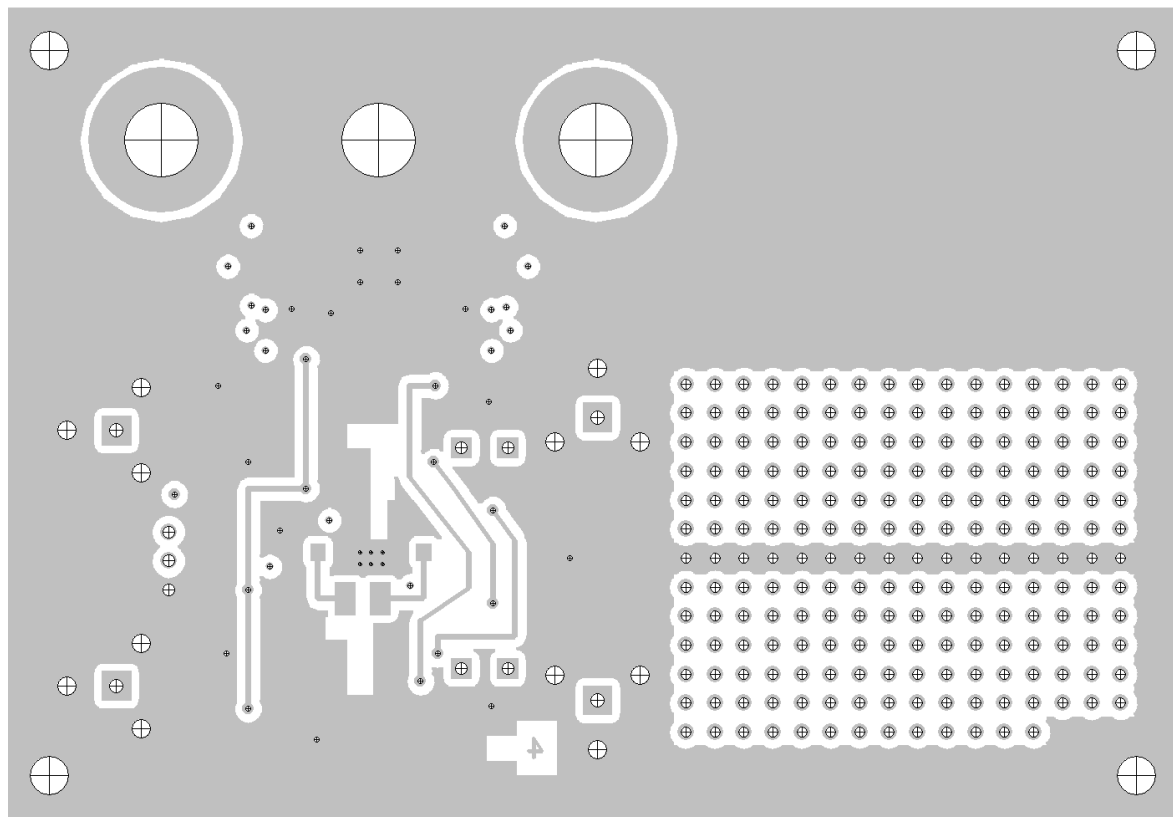
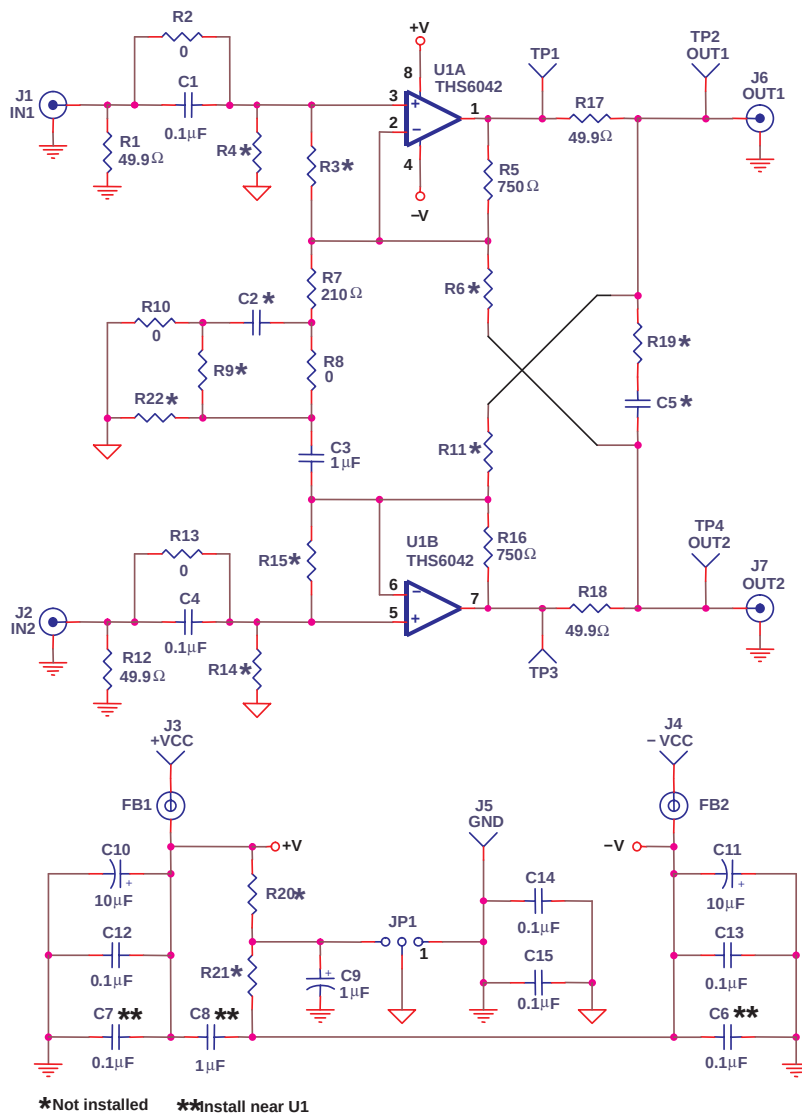


Figure 5–4. Bottom (Layer 4) (Ground and Signal)



### 5.3 Schematic

Figure 5–5. Full Schematic of the THS6042 EVM



Note: Devices designated with an \* are not installed on the EVM. The user must supply these components.