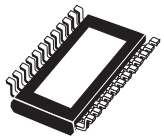
PM8801

High-efficiency, IEEE 802.3at compliant, integrated PoE-PD interface and PWM controller

Datasheet - production data



HTSSOP24

Features

- IEEE 802.3at compliant PD interface
- Works with power supplied from Ethernet LAN cables or from local auxiliary sources
- Successful IEEE802.3at Layer1 classification indicator
- Integrated 100 V, 0.45 Ω, 1 A hot-swap MOSFET
- Accurate 140 mA typ. inrush current level
- Programmable classification current
- Sleep mode with LED indicator and Maintain Power Signature (MPS)
- Precise DC current limit set at 640 mA typ.
- Integrated high-voltage startup bias regulator
- Thermal shutdown protection
- Current mode pulse width modulator
- Programmable oscillator frequency
- 80% maximum duty cycle with internal slope compensation
- Support for flyback, forward, forward active clamp, flyback with synchronous rectification

Applications

- VoIP phones, WLAN AP
- WiMAX CPEs
- Security cameras
- PoE/PoE+ Powered device appliances

Description

The PM8801 integrates a standard compliant Power over Ethernet (PoE) interface and a current mode PWM controller to simplify the design of the power supply sections of all powered devices.

The PoE/PoE+ interface incorporates all the functions required by the IEEE 802.3at including detection, classification, undervoltage lockout (UVLO) and inrush current limitation.

The PM8801 specifically performs IEEE802.3at Layer1 hardware classification, providing an indication of type 2 PSE successful detection to the rest of the system.

The PM8801 has been designed to work with power either from the Ethernet cable connection or from an external power source such as a wall adapter, ensuring prevalence of the auxiliary source with respect to the PoE interface.

The DC/DC section of the PM8801 features a programmable oscillator frequency, an adjustable slope compensation, dual complementary low-side drivers with programmable delay time and internal temperature sensor.

The PM8801 targets high-efficiency conversion at all load conditions supporting flyback, forward, forward active clamp and synchronous rectification.

Table 1. Device summary

Part number	Package	Packing
PM8801	HTSSOP24	Tube
PM8801TR		Tape and reel

This is information on a product in full production. www.st.com

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1 Typical application circuit and block diagram

1.1 Application circuits

Figure 1. Simplified application schematic for powered devices using PM8801 in forward active clamp configuration

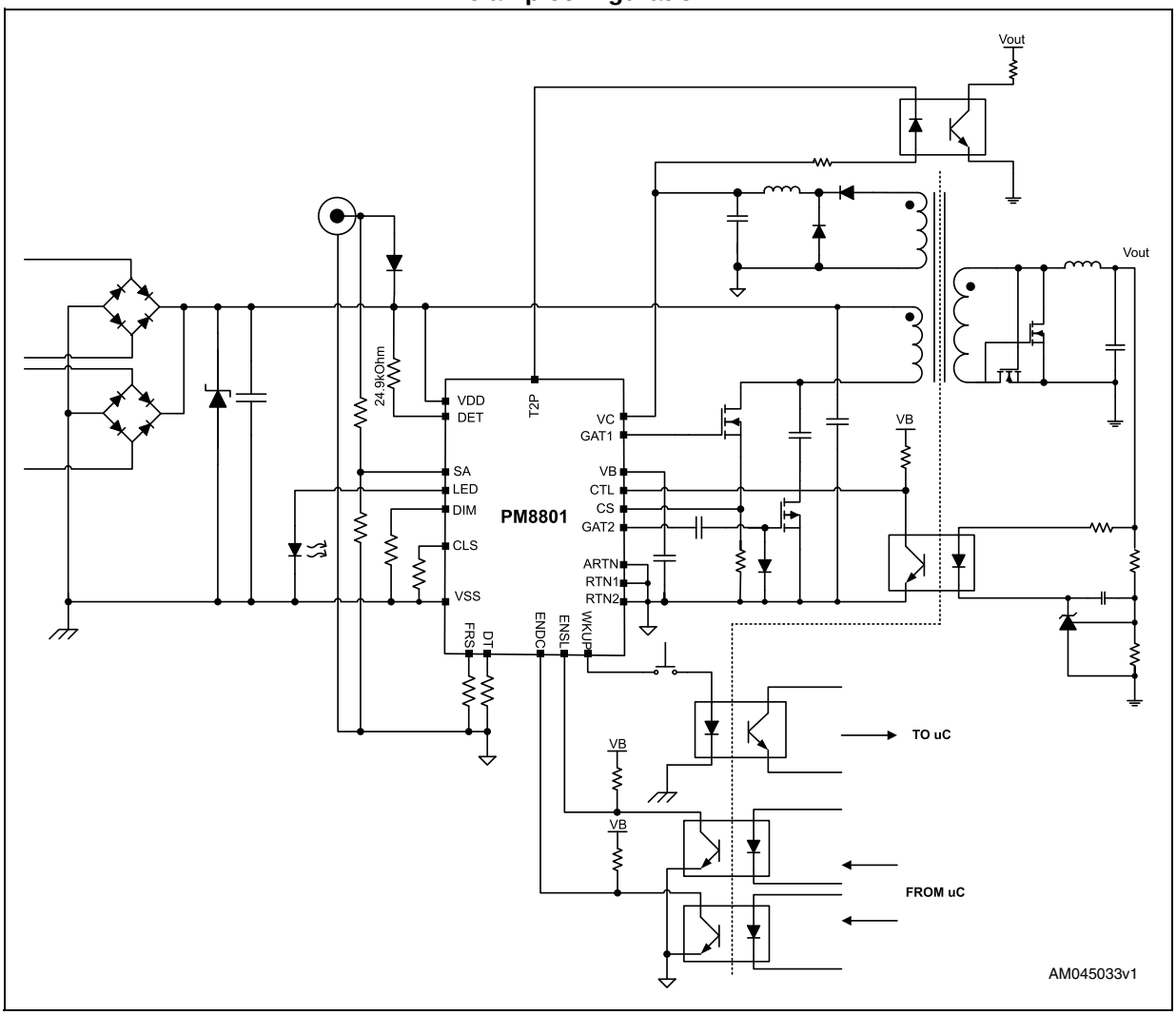
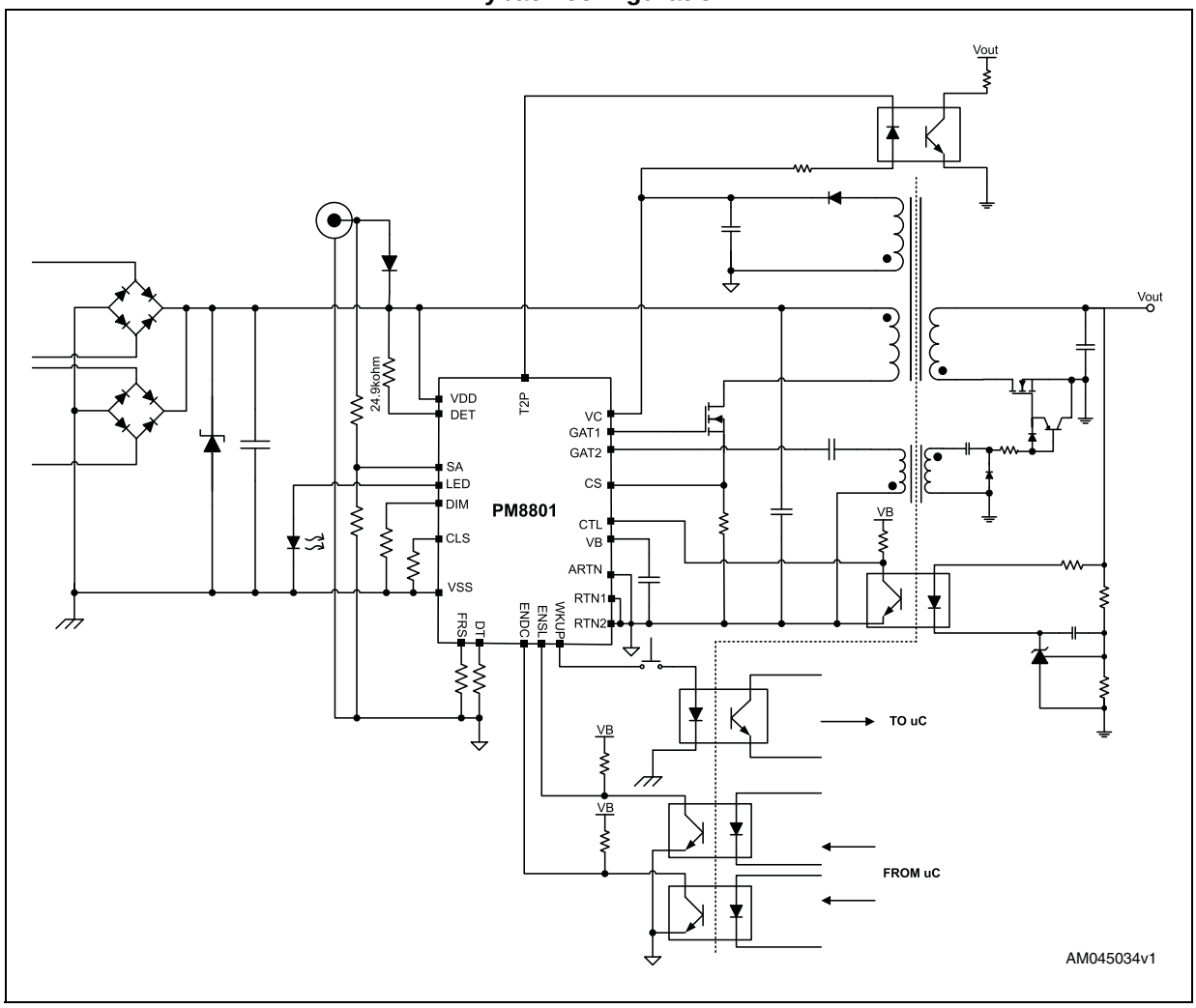


Figure 2. Simplified application schematic for powered devices using PM8801 in synchronous flyback configuration



1.2 Block diagrams

Figure 3. PM8801 internal block diagram

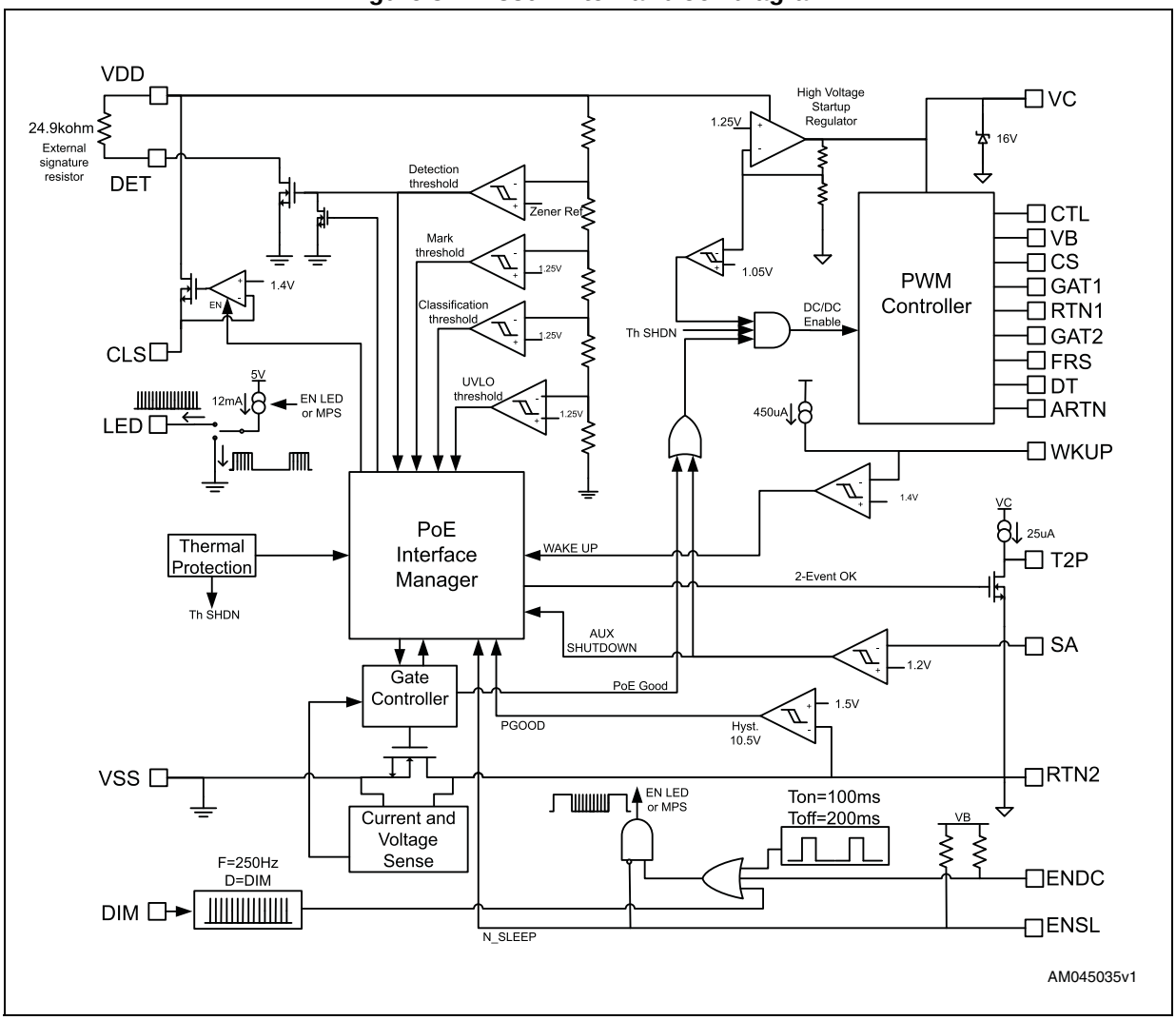
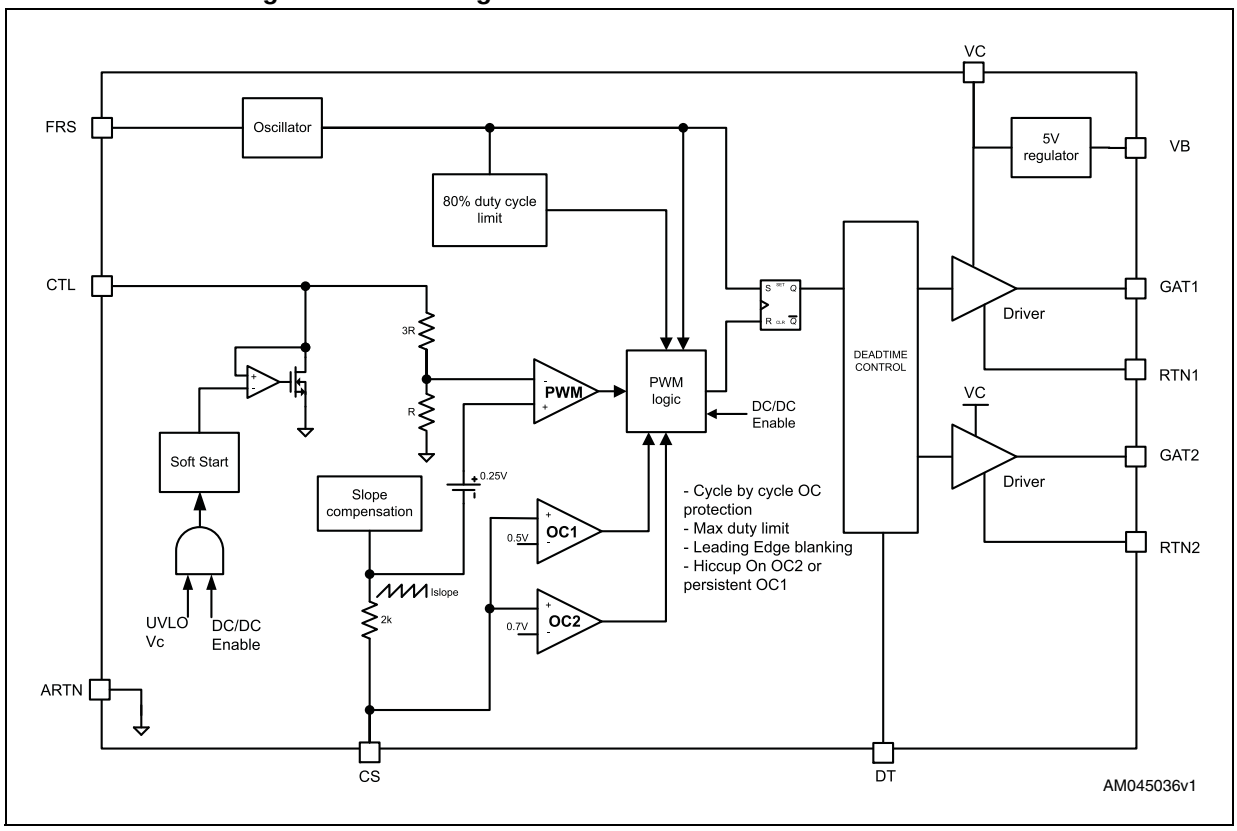


Figure 4. Block diagram of the DC/DC section of the PM8801



2 Pin descriptions and connection diagram

Figure 5. Pin connections (top view)

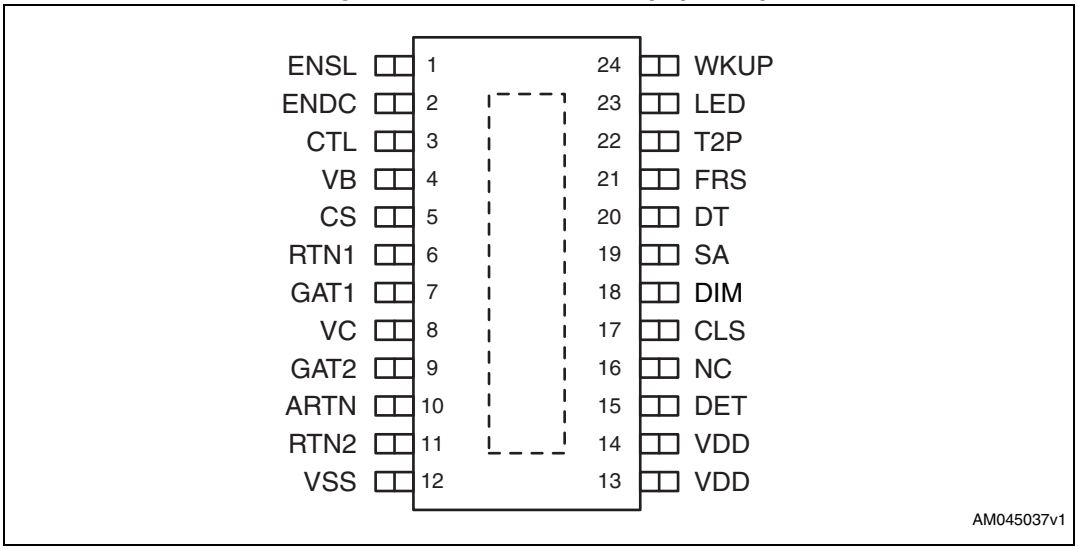


Table 2. Pin descriptions

Pin#	Name	Function
1	ENSL	Sleep mode input: active-low signal. An optocoupler may be used to force the PM8801 to enter into sleep mode, shutting down its internal DC/DC controller.
2	ENDC	MPS duty cycle / LED enable: active-low signal. Drive this pin low to disable the LED driver during normal operations. Entering sleep mode the host of the PoE-PD may drive this pin through an optocoupler to set the MPS current profile. The signal value is sampled on the ENSL pin during transition to sleep mode. If low the MPS current is pulsed, if high the MPS current is constant.
3	CTL	Input of the pulse width modulator. CTL pull-up to VB is provided by an external resistor which may be used to bias an opto-coupler transistor.
4	VB	5 V, up to 10 mA bias regulator. This reference voltage can be used to bias an opto-coupler transistor. In sleep mode VB regulator is switched off.
5	CS	Current sense input for current mode control and overcurrent protection. Current sensing is accomplished using a dedicated current sense comparator. If the CS pin voltage exceeds 0.5 V, the GAT1 pin switches low for cycle-by-cycle current limiting. CS is internally held low for 60 ns after GAT1 switches high to blank leading edge current spikes.
6	RTN1	Power ground for the GAT1 driver. This pin must be connected to RTN2 and ARTN.

Table 2. Pin descriptions (continued)

Pin#	Name	Function
7	GAT1	Main gate driver output of the PWM controller. DC-DC converter gate driver output with 1A peak sink-source current capability. (5 Ω typ MOSFETs).
8	VC	Output of the internal high-voltage regulator. When the auxiliary transformer winding (if used) raises the voltage on this pin above the 8 V typ. regulation set point, the internal regulator will shut down, reducing the internal power dissipation. Filter this pin with a 1 µF typ connected to ground.
9	GAT2	Secondary gate driver output. AUX gate driver output for active clamp or synchronous rectification designs. 1 A peak sink-source current capability (5 Ω typ MOSFETs).
10	ARTN	Analog PWM supply ground. RTN for sensitive analog circuitry including the SMPS current limit amplifier.
11	RTN2	Power ground for the secondary gate driver. This pin is also connected to the drain of the internal current-limiting power MOSFET which closes VSS to the return path of the DC-DC converter. This pin must be connected to RTN1 and ARTN.
12	VSS	System low potential input. Diode "OR'd" to the RJ45 connector and PSE's –48 V supply, it is the more negative input potential.
13	VDD	System high potential input. The diode "OR" of several lines entering the PD, it is the most positive input potential.
14	VDD	System high potential input. The diode "OR" of several lines entering the PD, it is the most positive input potential.
15	DET	Detection resistor. Connect the signature resistance between DET pin and VDD. Current will flow through the resistor only during the detection phase. This pin is 100 V rated with negligible resistance with respect to the external 24.9 kΩ.
16	NC	Not Connected.
17	CLS	Classification resistor. Connect the classification programming resistor from this pin to VSS.
18	DIM	LED dimming set. A resistor between this pin and VSS will set the duty cycle of the PWM current driving the LED connected to pin 23.
19	SA	Auxiliary input startup pin. Pulling up this pin will give high priority to an auxiliary power source like an external wall adapter. Use a resistor voltage divider from the auxiliary voltage to ARTN to connect this low voltage rating pin. Connect this pin to ARTN if not used.

Table 2. Pin descriptions (continued)

Pin#	Name	Function
20	DT	Delay time set. A resistor connected from this pin to ARTN sets the delay time between GAT1 and GAT2. This pin cannot be left open.
21	FRS	Switching frequency set. An external resistor connected from FRS to ARTN sets the oscillator frequency.
22	T2P	Successful 2-event classification indicator. T2P open-drain signal assertion happens when powered by a PSE performing a 2-event classification. T2P is an active-low signal.
23	LED	Sleep mode LED indicator. An LED connected to VSS is driven by a 250 Hz, 12 mA PWM current. The LED brightness can be set through the DIM pin.
24	WKUP	Wake-up signal. Closing the switch from WKUP to VSS, the PM8801 wakes up from sleep mode, enabling the DC/DC controller with a soft-start. The WKUP is an active-low input.
	EP	Exposed Pad. Connect this pad to a pcb copper plane to improve heat dissipation; must be electrically connected to VSS.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3.Absolute maximum ratings

Parameter	Value	Unit
VDD, DET, ARTN to VSS	-0.3 to 100	V
LED to VSS	-0.3 to 5.5	V
CLS, DIM, WKUP to VSS	-0.3 to 3.6	V
VC to ARTN	-0.3 to 16	V
GAT1, GAT2, T2P to ARTN	-0.3 to VC+0.3	V
CTL, VB, DT, ENDC, ENSL to ARTN	-0.3 to 5.5	V
FRS, SA, CS to ARTN	-0.3 to 3.6	V
RTN1, RTN2 to ARTN	-0.3 to 0.3	V
ESD HBM	2	kV
ESD CDM	500	V
Operating junction temperature(1)	-40 to 150	°C
Storage temperature	-40 to 150	°C

1. Internally limited to 160 °C typ. with internal overtemperature protection circuit.

Note: Absolute maximum ratings are limits beyond which damage to the device may occur.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Max thermal resistance junction to ambient(1)	40	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Operative junction temperature range	-40 to 125	°C
T_A	Operative ambient temperature range	-40 to 85	°C

1. Package mounted on a 4-layer board (2 signals + 2 powers), CU thickness 35 micron, with 6-8 vias on the exposed pad copper area connected to an inner power plane

3.3 Electrical characteristics

VDD = 48 V, VC = not loaded, Cvc = 1 µF, VB = not loaded, Cvb =1 µF,

GAT1 and GAT2 = not loaded, T_A = 25 °C unless otherwise specified.

Values in Bolded type apply over the full operating ambient temperature range.

Table 5. Electrical characteristics - interface section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Detection and Classification						
	Signature enable	VDD rising			**1.5**	V
	Signature pull down resistance	within signature range		150	**350**	Ω
	Signature disable	VDD rising	**10.3**	10.8	**11.3**	V
	Classification enable	VDD rising	**11.3**	12	12.7	V
	Classification turn-off	VDD rising	**21.5**	23.0	**24.5**	V
	Mark event threshold / Classification turn-off	VDD falling	**9**	10	**11**	V
	Classification reset threshold	VDD falling	**3**	4	**5**	V
	CLS voltage	within classification range with 44 mA load	**1.3**	1.4	**1.5**	V
	CLS max current capability	within classification range with CLS pin grounded	**50**	65	**80**	mA
Bias current						
Idd	VDD supply current during detection	VDD = 8 V			10	µA
	VDD supply current during classification			900	**1200**	µA
	VDD supply current during mark event		**500**	800	**1100**	µA
Undervoltage lockout						
V_{UVLO_R}	UVLO release	VIN rising	**34**	35	**36.5**	V
V_{UVLO_F}	UVLO lockout	VIN falling	**30**	31	**32.5**	V
	UVLO hysteresis		**3.5**	4	**4.5**	V
Hot-swap MOSFET						
R_{DSON}	MOSFET resistance			0.45	**1**	Ω
	Default inrush current limit		**125**	140	**155**	mA
	Default DC current limit		**590**	640	**690**	mA

Table 5. Electrical characteristics - interface section (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Inrush to DC current switchover						
	V_{DS} required for inrush to DC switchover	V_{DS} falling - hot-swap MOSFET closing	**1.35**	1.50	**1.75**	V
	V_{GS} required for inrush to DC Switchover	V_{DS} falling - hot-swap MOSFET closing. Guaranteed by design.		2		V
	V_{DS} required for inrush to DC Switchover	V_{DS} rising - hot-swap MOSFET opening	**11**	12	**13**	V
LED						
I_{LED}	LED PWM current amplitude	Sourced from LED pin	**9**	12	**14**	mA
Vf_{LED_MAX}	LED maximum forward voltage		**4.5**			V
f_{LED}	LED PWM current frequency			250		Hz
Maintain Power Signature						
Idd_{MPS}	MPS current	including VDD quiescent current		13		mA
T_{MPS}	MPS current draw duration	ENDC = 0 V	**75**	100		ms
T_{MPDO}	MPS current dropout duration	ENDC = 0 V		200	**250**	ms
Wakeup from sleep mode						
	WKUP threshold	WKUP falling	**1.3**	1.4	**1.5**	V
	WKUP pull-up current			450		µA

Table 6. Electrical characteristics - SMPS section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Oscillator						
F_{osc}	Frequency accuracy	In the range 100 to 500 kHz		+/-10		%
	Frequency programmability	R_{FRS} = 100 kΩ	**220**	245	**270**	kHz
		R_{FRS} = 47.5 kΩ	**445**	495	**545**	kHz
	Frequency range		100		1000	kHz
	FRS voltage		**1.20**	1.25	**1.30**	V
Delay time						
	GAT1 to GAT2 delay time	R_{DT} = 20 kΩ, GAT1and GAT2 open		32		ns
		R_{DT} = 200 kΩ, GAT1and GAT2 open		320		ns
	DT voltage		**1.20**	1.25	**1.30**	V

Table 6. Electrical characteristics - SMPS section (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Soft-start						
T_{SS}	Soft-start time	Over CTL full range (0 to 3V), at F_{osc} = 250 kHz		12.3		ms
Current limit						
	Delay to output	Guaranteed by design		20		ns
	Cycle-by-cycle current limit threshold voltage		**0.44**	0.50	**0.56**	V
	Leading edge blanking time		**45**	60	**75**	ns
	Slope compensation current	Sourced by CS pin		45		µA
PWM comparator						
	Delay to output	Guaranteed by design		25		ns
	Minimum duty cycle	CTL = 0, CS = 0			0	%
	Maximum duty cycle	CTL = 2 V, CS = 0, F_{osc} = 250 kHz	**75**	80	**85**	%
	CTL to PWM gain	Guaranteed by design		1: 4		
	CTL operative range		1		3	V
Output driver GAT1						
	Output high	I_{GD} = 100 mA		VC-0.25	**VC-0.5**	V
	Output low	I_{GD} = –100 mA		0.25	**0.5**	V
	Fall time	C_{LOAD} = 3.3 nF, VC = 10 V Guaranteed by design		40		ns
	Rise time	C_{LOAD} = 3.3 nF, VC = 10 V Guaranteed by design		45		ns
	Peak source current	C_{LOAD} = 3.3 nF, VC = 10 V Guaranteed by design		800		mA
	Peak sink current	C_{LOAD} = 3.3 nF, VC = 10 V Guaranteed by design		1		A
Output driver GAT2						
	Output high	I_{GD} = 100 mA		VC-0.25	VC-0.5	V
	Output low	I_{GD} = –100 mA		0.25	0.5	V
	Fall time	C_{LOAD} = 3.3 nF, VC = 10 V Guaranteed by design		40		ns
	Rise time	C_{LOAD} = 3.3 nF, VC = 10 V Guaranteed by design		45		ns

Table 6. Electrical characteristics - SMPS section (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
	Peak source current	C_{LOAD} = 3.3 nF, VC = 10 V Guaranteed by design		800		mA
	Peak sink current	C_{LOAD} = 3.3 nF, VC = 10 V Guaranteed by design		1		A
Thermal shutdown						
	Shutdown temp.	Always active; Guaranteed by design		160		°C
	Shutdown hyst.			30		°C
Sleep mode						
	ENSL threshold	ENSL falling	**1.7**	1.85	**1.95**	V
	ENSL hysteresis	Guaranteed by design		0.1		V
	ENDC threshold	ENDC falling	**1.7**	1.85	**1.95**	V
	ENDC hysteresis			0.1		V
VC regulation						
VC	Internal default		**7.7**	8.0	**8.3**	V
	VC current limit	IB = 0; GAT1, GAT2 = open	**14**	20		mA
VC_{UVLO}	Internal default UVLO, release	VC rising		VC-0.3		V
	Internal default; UVLO, lockout	VC falling	5.7	6.0	**6.3**	V
	VC regulator dropout	IC = 10 mA; GAT1, GAT2 = open		2		V
VB regulation						
VB	Internal default		**4.85**	5.0	**5.15**	V
	VB current capability	IC = 0; GAT1, GAT2 = open	5		10	mA
	VB sink current capability				**1**	mA
Auxiliary source detection						
	SA threshold		**1.1**	1.2	**1.3**	V
	SA hysteresis			180		mV
	Minimum VDD voltage for aux. operations		13	15		V
T2P flag						
	T2P pull-up current		**20**	25	**30**	µA
	T2P pull-down resistance			45	**75**	Ω

Table 6. Electrical characteristics - SMPS section (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Device current consumption						
Iddq	VDD quiescent current	VD > $V_{UVLO_R,}$ VC = 12 V, CTL = 0		1.25	**1.5**	mA
	VC quiescent current	VD > $V_{UVLO_R,}$ VC = 12 V, CTL = 0		2	**2.5**	mA

Note: 1) Minimum and maximum limits are guaranteed by test, design, or statistical correlation.Typical values represent the most likely parametric norm at T_A = 25 °C, and are provided for reference only.

2) Device thermal limitations could limit useful operating range.

3) he VC regulator is intended for internal use only as the startup supply of the PM8801; any additional external VC current, including the VB regulator current and external MOSFET driving current, has to be limited within the specified max current limit.

4 PD interface

4.1 Detection

In Power over Ethernet systems, the Power Sourcing Equipment (PSE) senses the Ethernet connection to detect whether the Powered Device (PD) is plugged to the cable termination by applying a small voltage (2.7 to 10 V) on the Ethernet cable and measuring the equivalent resistance in at least two successive steps. During this phase, the PD must present a resistance between 23.75 kΩ and 26.25 kΩ.

The signature resistor must be connected between the DET and VDD pins. This resistor is in-series to a pass transistor (see *Figure 3*) enabled only during the detection phase. No current is flowing through the signature resistor for the rest of the operative phases (classification and turn-on).

The value of the detection resistance has to be selected also taking into account the typical drop in voltage of the diode bridges. The typical value that can be used in most cases is 24.9 kΩ.

During detection, most of the circuits inside the PM8801 are disabled to minimize the offset current.

4.2 Classification

The classification phase in a PoE network is the feature that allows PSE to plan and allocate the available power to the appliances connected to various Ethernet ports.

PM8801 complies with both IEEE802.3at 1-event and 2-event classification schemes.1-event classification in IEEE802.3at is the same as specified in the IEEE 802.3af standard, which divides the power levels below 12.95 W into 5 classes (Class 0 to Class 4).

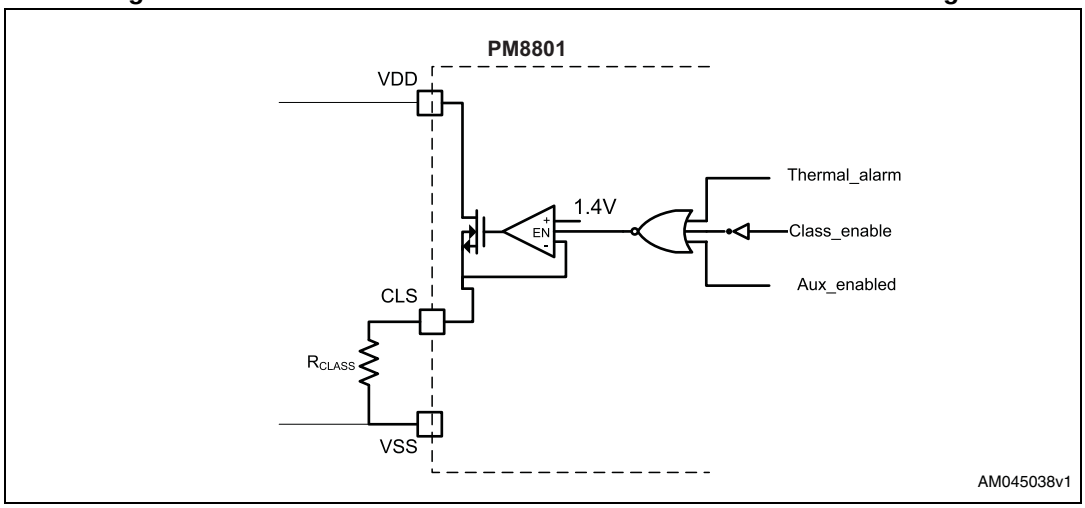
While Class 4 was reserved in IEEE802.3af, in IEEE802.3at Class 4 identifies Type2 PDs requiring up to 25.5 W.

A Type2 PD is a PD that provides a Class 4 signature during Physical Layer classification, understands 2-event classification and is capable of Data Link Layer classification.

Figure 8 represents the voltage at the input of the PD when connected to a PSE performing 2-event classification. A Type2 PD will present in both classification events a Class 4 current, while during the so called “mark-event”, between the 2 classification fingers, the PD will present an invalid signature resistance.

To support the classification function, an equivalent programmable constant current generator has been implemented. *Figure 6* depicts the primary schematic of the classification circuit. Following the successful completion of the detection phase, the voltage of the CLS pin is set to the 1.4 V voltage reference and a pass transistor connects the VIN pin to the CLS pin.

Figure 6. PM8801: reference schematic of the PoE classification logic



The classification resistor can be disconnected for the following reasons:

– the classification has been successfully completed
– an auxiliary power source has been connected
– the device is in thermal protection.

Designers can set the current by changing the value of the external resistor according to the following table.

Table 7. Value of the external classification resistor for the different PD classes of power

Class	PD max average power (W)	R_{CLS} (Ω)
0	13	2 k
1	3.84	150
2	6.49	80.6
3	13	51.1
4	25.5	35.6

4.3 Indication of successful 2-event classification

PM8801 is capable of recognizing whether it is connected to a PSE performing physical layer classification by asserting the T2P signal.

T2P is an open-drain, active-low signal which is pulled down in case a successful 2-event classification event is completed.

T2P will be asserted as soon as the high-voltage startup regulator output is stable (see *Figure 7* and *Figure 8* for timing sequences). If PM8801 sees a 1-event classification or no classification, T2P is pulled up and the main circuit in the PD can try to establish an LLDP connection to negotiate the power. No LLDP response from the PSE means that the PD is connected to a Type1 PSE, and only 13 W input power will be available.

A low T2P signal after the turn-on phase of the PD means that the device is connected to a Type2, 2-event physical layer classification PSE which may allocate power either through further LLDP negotiation or directly feeding the PD with the required power.

In isolated applications, the main circuits and the PM8801 are at both sides of the galvanic isolation. The T2P signal is normally connected to an optocoupler to pass the Type 2, 2-event PSE detection information to the main circuit in the PD system.

Figure 7. T2P signal when connected to PSE supporting 1-event classification

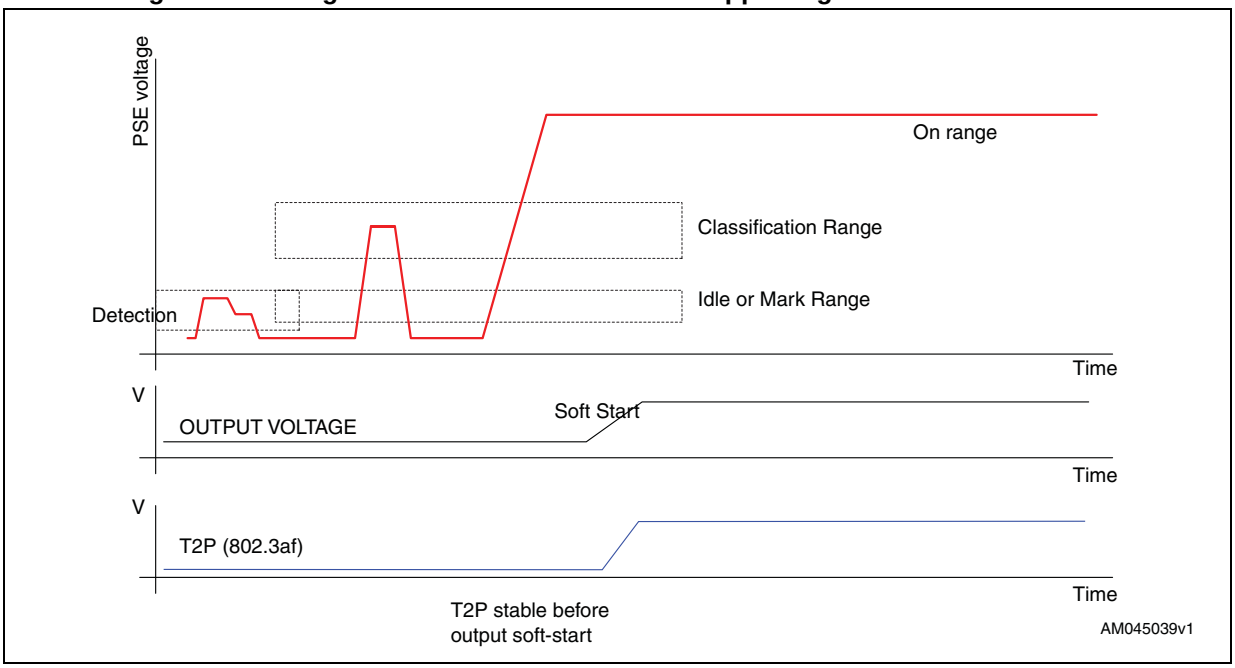
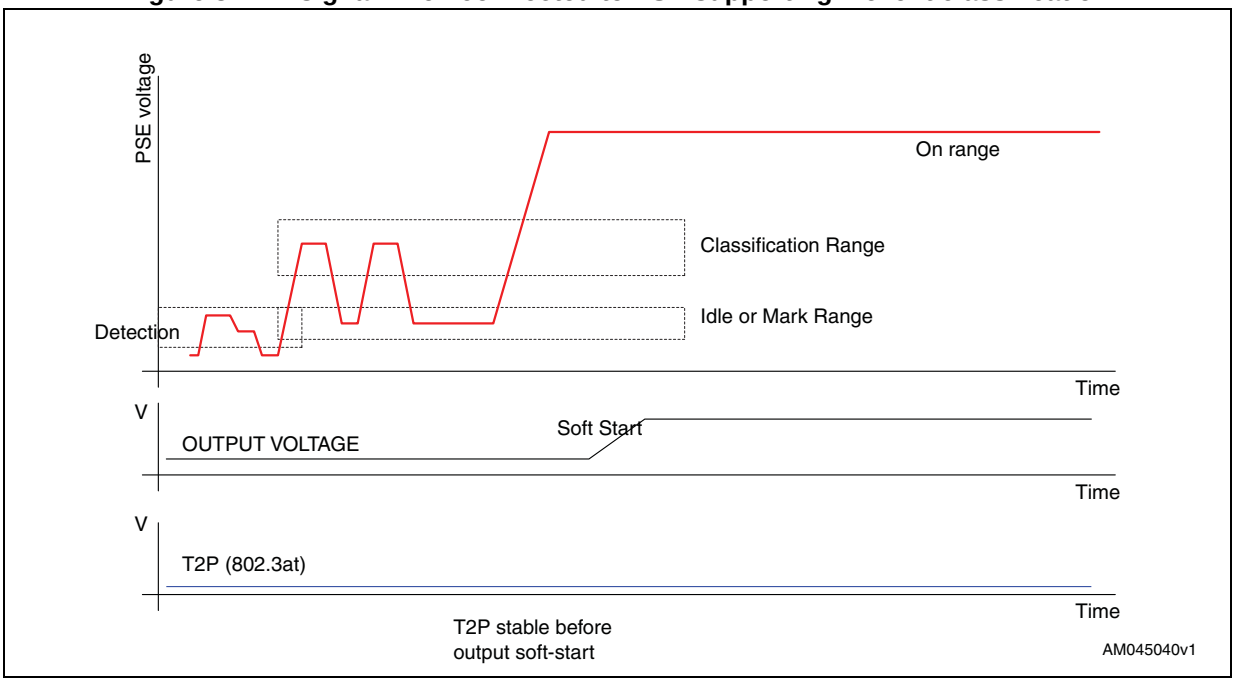


Figure 8. T2P signal when connected to PSE supporting 2-event classification



4.4 Undervoltage lockout

After classification is completed, the PSE raises the voltage to provide the Powered Device with the negotiated power. During the transition from low to operating voltage, the internal UVLO is released and the hot-swap MOSFET is activated, initiating the inrush sequence.

PM8801 implements the UVLO mechanism by setting 2 internal thresholds on the voltage across the VDD-VSS pins. One is to activate the hot-swap (V_{UVLO_R}), while the other is to switch off the hot-swap MOSFET upon detection of a supply voltage drop (V_{UVLO_F}) from normal operating conditions.

No additional external components are required to comply with the IEEE requirements. The thermal protection alarm overrides the gate driving of the MOS, immediately switching off the MOS itself in case of device overheating. The hot-swap is bypassed also in auxiliary source topology, supplying directely the PWM section of the PM8801 and bypassing the hot-swap MOSFET.

4.5 Inrush and DC current limiting

Once the detection and classification phases have been succesfully completed, the PSE raises the voltage across the Ethernet cable. When the voltage difference between VIN and VSS is greater than the V_{UVLO_R} threshold, the internal hot-swap MOSFET is switched on and the DC/DC input capacitance is charged in a controlled manner.

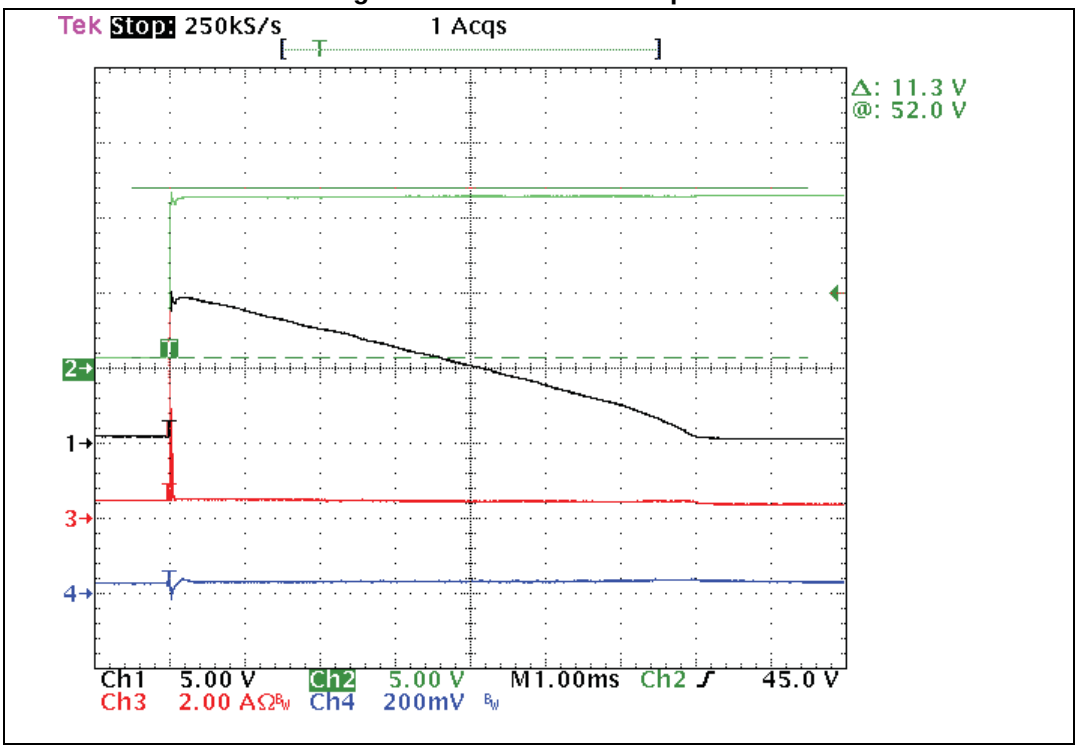
During the inrush phase the current is limited to 140 mA.

When the RTN voltage falls below 1.5 V, an internal signal (PGOOD in *Figure 3*) is asserted to activate the DC/DC section.

This feature is active only when working from an input voltage with a "frontal" connection, that must use the hot-swap MOSFET; this voltage could be from the PoE interface or from an external auxiliary adapter connected before the internal hot-swap MOSFET. If the auxiliary source is connected after the hot-swap MOSFET, it will be opened and this feature is disabled, allowing the converter to work with a low-voltage auxiliary source. The PGOOD comparator includes hysteresis to allow the PM8801 to operate near the current limit point without inadvertently disabling it. The MOSFET voltage must increase to 12 V before PGOOD is deasserted. This feature will also allow withstanding positive line transients of up to 12 V without stopping DC/DC normal operations as shown in *Figure 9*. The line transient is managed by the PWM section, adjusting its operating parameters accordingly without shutting down the output voltage. The input current during the transient is controlled by the hot-swap MOSFET at the DC current limit.

After PGOOD assertion, a comparator on the gate of the hot-swap MOSFET controls the transition between the 140 mA to the 640mA DC current limit, with a 2 V threshold. The comparator is needed to ensure that the charge of the DC/DC input capacitor is completed, avoiding current spikes on the last portion of the charge.

Figure 9. Line transient response



Ch1: RTN - VSS, Ch2: VDD - VSS, Ch3: I input, Ch4: 5Vout (with offset)

4.6 Sleep mode / MPS mode

It is possible to put the PM8801 in sleep mode for applications connected to either a PoE network or auxiliary sources. In both cases the DC/DC converter is turned off. The device draws a minimum current and the LED is activated (see *Section 4.7* for details).

The sleep mode is activated by pulling ENSL below its internal threshold. The ENSL pin is a logic level active-low input. The ENSL pin may be connected to a system microcontroller through an optocoupler.
When working from a PoE network or from a frontal auxiliary source, the internal hot-swap MOSFET is opened and the DC/DC section shuts down. In this condition the PD consumption is very low and for this reason it may be disconnected by the PSE.

To avoid this disconnection the PM8801 features a Maintain Power Signature (MPS) current control. The device will keep on drawing a current whose profile is determined by sampling the level of ENDC when entering sleep mode. The ENDC pin is designed to receive the signal from a system microcontroller connected through an optocoupler.

According to the IEEE802.3at standard, continuous or pulsed MPS profiles are available.

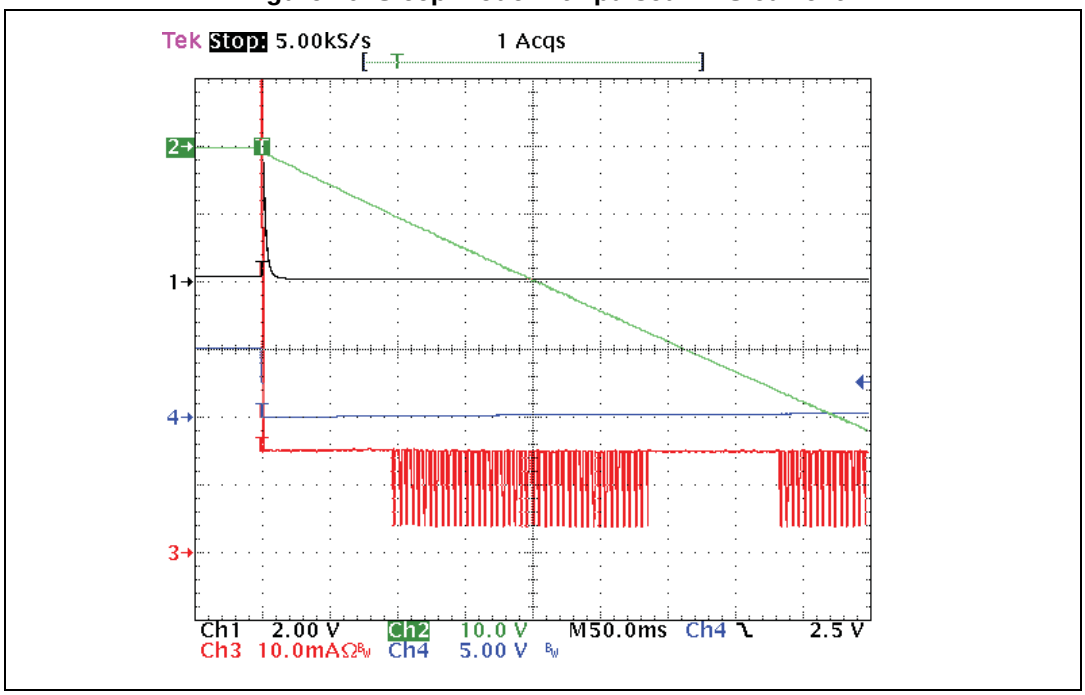
Pulsed MPS is obtained by 100 ms pulses of 12 mA current, followed by 200 ms of MPS dropout as shown in *Figure 10*. This profile is obtained with ENDC = low when entering sleep mode.

Constant current MPS is a 12 mA constant current drawn during the entire duration of the sleep mode. This profile is obtained with ENDC = high when entering sleep mode.

In case of thermal shutdown, MPS is released, making sure that current consumption is below the threshold and allowing the PSE to detach the PD.

When the PM8801 is powered by an auxiliary source (see *Section 6*), the MPS current is not activated.

Figure 10. Sleep mode with pulsed MPS current



Ch1: ENSL, Ch2: VSS-RTN. Ch3: Iinput, Ch4: 5Vout

4.7 LED driving

The PM8801 features a current-driven LED output. The LED is enabled when the ENDC pin is driven high, or automatically enabled in sleep mode.

The LED driver sources a PWM current at 250 Hz frequency and 12 mA typical amplitude.

The LED brightness is adjustable connecting a resistor R_{DC} at 1% accuracy between DIM and VSS. The correspondence between duty-cycle and resistor values are shown in the following *Table 8*.

Table 8. LED duty cycle selection

LED duty cycle D	R_D [Ω]
0	>1 M
15%	453 k
33%	243 k
47%	162 k
75%	110 k

To minimize current consumption during sleep mode, the MPS current is obtained by:

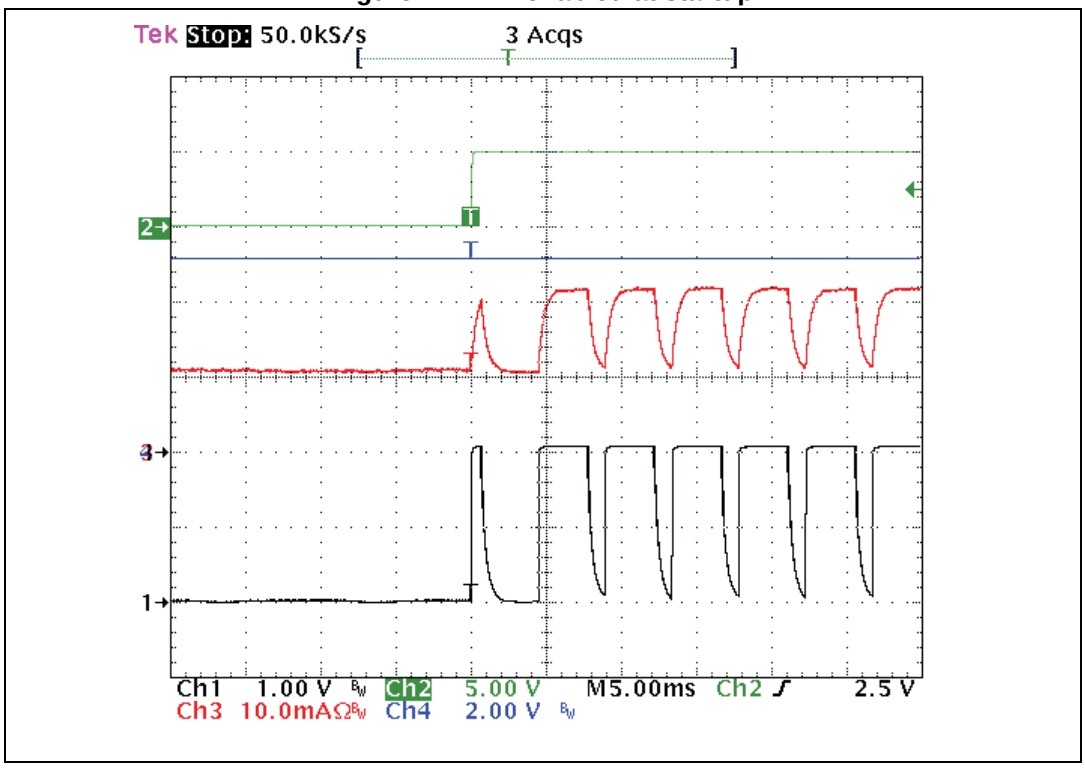
- the 12 mA driving LED current when the LED is on
- an internal 12 mA sink when the LED is off

This behavior ensures a 12 mA constant MPS current shape when the MPS is on.

During MPS dropout the consumption is due only to the quiescent current and the average LED driving current.

$$I_{MPDO} = Iddq + D*I_{LED}$$

Figure 11. LED enabled at startup



Ch1: LED, Ch2: ENDC, Ch3: Iinput, Ch4: 5Vout

LED signal will be present also in the case an auxiliary source is used in place of PoE.

If both PoE and auxiliary source are connected, the PoE interface is not providing power to the DC/DC section, but still provides current to the LED.

When working from an auxiliary source, if the system requires disconnection from the PSE, it is suggested to turn off the LED for at least 400 msec after insertion of the auxiliary power jack.

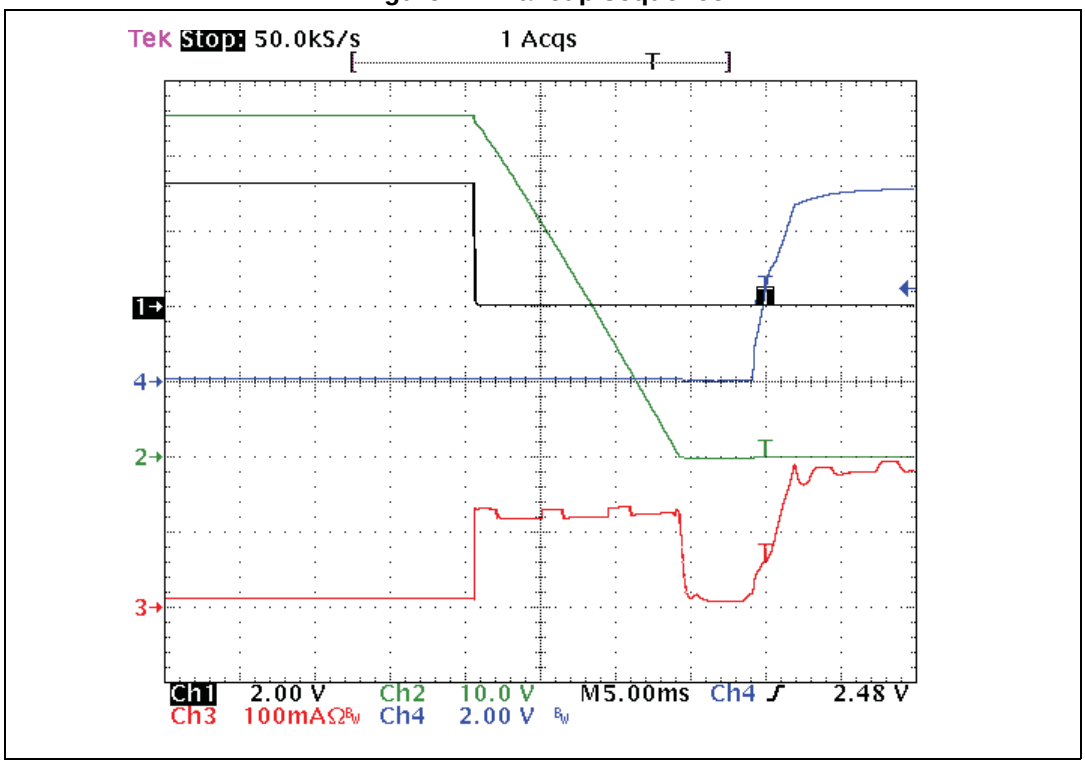
4.8 Wakeup from sleep mode

The PM8801 pin WKUP is a logic-level active-low input, internally pulled high. It can be connected to VSS ground through a switch. The closure of this switch wakes up the device from sleep mode, performing a soft-start of the DC/DC converter.

If the switch is closed during normal operations, no action is taken by the PM8801.

Other conditions to wake up the device are a voltage drop below UVLO threshold or the insertion of a wall adapter connected to the SA pin.

Figure 12. Wakeup sequence



Ch1: WKUP, Ch2: VSS-RTN, Ch3: Iinput, Ch4: 5 Vout

4.9 High-voltage startup regulator

The PM8801 embeds a high-voltage startup regulator to provide a controlled reference voltage of 8.0 V to the internal current mode PWM controller during its startup phase.

The regulator output is connected to the VC pin as well as to the DC/DC section.

In standard isolated topology, the VC pin is diode connected to the auxiliary winding of the transformer used for the flyback or forward configuration. When the voltage from the transformer exceeds the regulated voltage, the high-voltage regulator is shut off, reducing the amount of power dissipated inside the PM8801.

In more detail, when the voltage from the auxiliary winding exceeds 8.0 V, the regulator resets its intervention threshold to 7 V. In this way, a loosely regulated voltage from the auxiliary winding is allowed without current-sharing with the internal regulator.

In the meantime, if the auxiliary voltage fails, the internal regulator takes over without losing DC/DC control.

The UVLO threshold on VC is 6.0 V typically. At this voltage the DC/DC controller operations are stopped and the outputs frozen in low state.

While the external auxiliary voltage has to be chosen higher than 8.0 V to take advantage of the auxiliary winding, it must also be lower than 16 V for all operating conditions, to avoid the intervention of the internal protection clamp.

A capacitor in the range of 220 nF - 10 µF must be connected to DC/DC ground for stability. For applications with high current drawn from VC, large capacitance should be used, (e.g. 10 µF) in order to avoid converter switch-off during the startup phase.

A VC UVLO mechanism monitors the level of voltage on the VC pin. When VC voltage exceeds the VC_{UVLO_R}, the PWM controller is enabled and it remains enabled until the VC voltage drops below its VC_{UVLO_F} value.

When an auxiliary winding is not used, the internal HV regulator UVLO threshold is set at 6.6 V and the current limit is set at 20 mA typ. This value includes the current internally drawn to bias the DC/DC controller, the gate drivers, the VB bias regulator and the external components that may be connected to the VC and VB pins.

Notice that using the HV regulator without the auxiliary winding increases the internal power dissipation, and when operating at high ambient temperature may lead the device to go into thermal shutdown.

4.10 5 V bias regulator

The PM8801 features an accurate 5 V output regulator, which can be used to bias the DC/DC feedback network and the optocoupler connected to the microcontroller.

A capacitor in the range of 100 nF - 2.2 µF must be connected to ARTN for stability.

The regulator current is supplied from the VC pin, to take advantage of the more efficient bias from the auxiliary winding. This means that the current drawn from the VB pin must be taken into account to evaluate the maximum current drawn from the VC pin.

The current drawn from the VB pin must be limited to 10 mA maximum.

The VB regulator is also able to accept injected current up to 1 mA without losing voltage regulation.

5 PWM controller

5.1 Oscillator

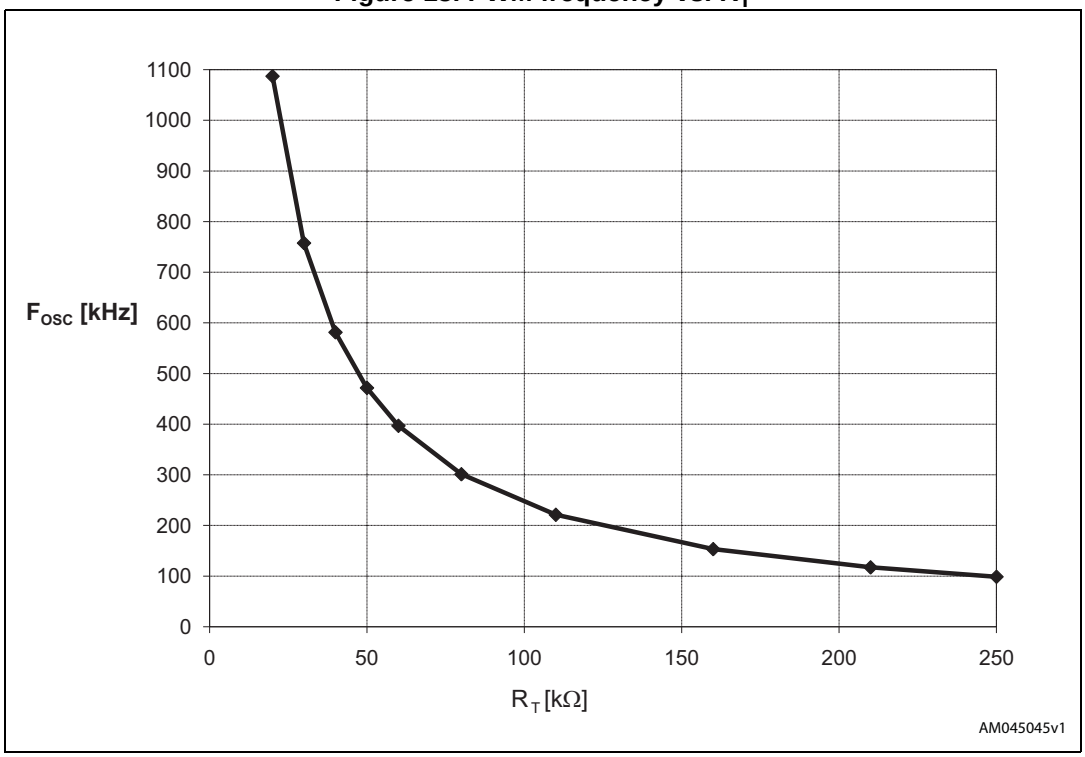
The internal oscillator frequency can be programmed by connecting an external resistor R_T between the FRS and ARTN pins. The relationship between the oscillator frequency F_{OSC} and the R_T resistor is:

$$F_{osc}(kHz) = \frac{25000}{3k\Omega + R_T(k\Omega)}$$

The PWM switching frequency is equal to the programmed oscillator frequency.

The useful range for R_T is from 25 k to 200 kΩ.

Figure 13. PWM frequency vs. R_T



5.2 Delay time control

The delay between the rising edge of GAT2 and GAT1 waveforms can be set by putting a programming resistor R_{DT} between DT and AGND or VB. The relationship between the delay time and the R_{DT} resistor is:

$$t_{del}(ns) = 1.6R_{DT}(k\Omega)$$

The same delay time is set between the GAT1 falling edge and the subsequent GAT2 falling edge.

The useful range for R_{DT} is between 5 k to 200 kΩ. A resistor should always be connected to this pin.

Figure 14. Delay time vs. R_{DT}

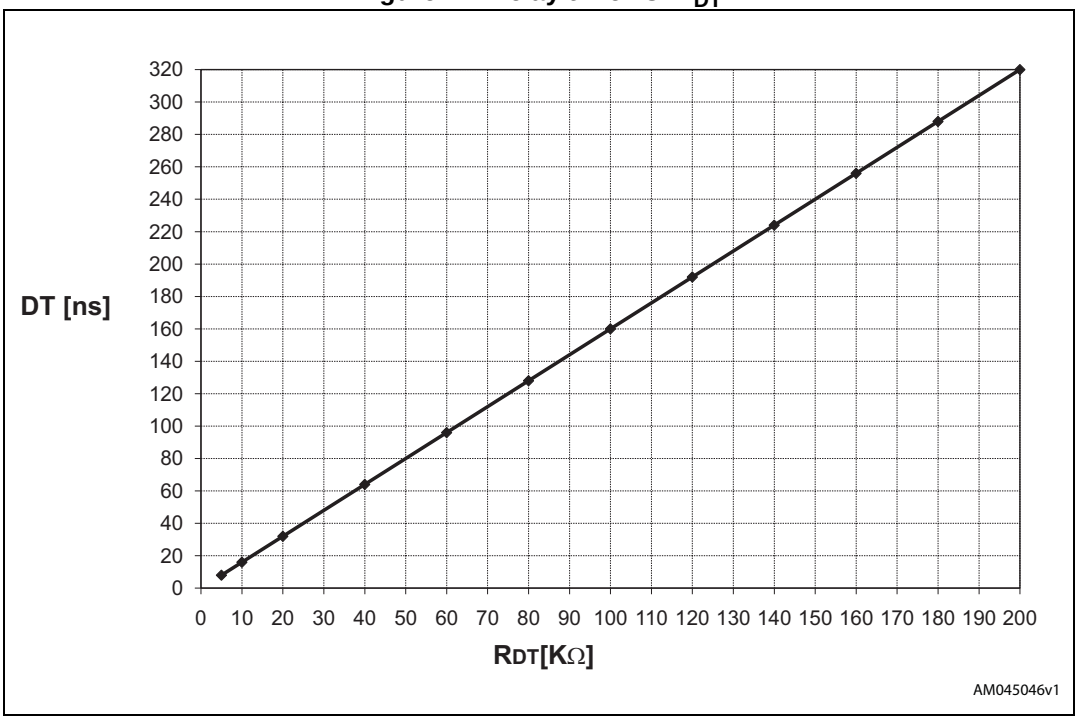
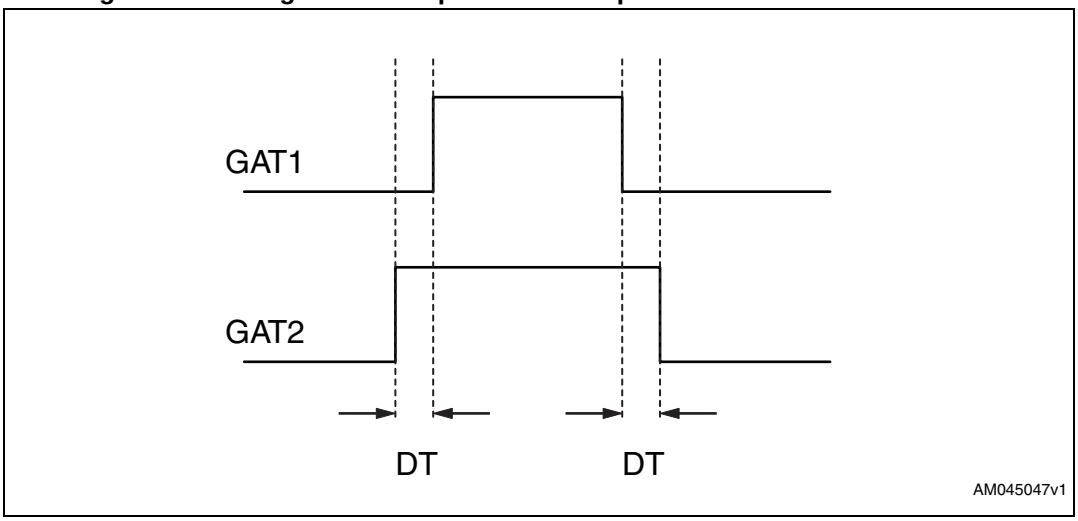


Figure 15. Timing relationship between output drivers as a function of DT



5.3 Soft-start

The DC/DC section of the PM8801 features an internal, digitally controlled, soft-start to make sure that output voltage ramps up in a safe and controlled manner.

At the startup of the converter, the input voltage of the PWM comparator (CTL pin) is clamped to a value which is increased cycle by cycle until it reaches the regulation voltage. This results in a converter duty-cycle increasing from zero to the operative value in 4096 switching periods maximum.

Taking into account that the output voltage will start to increase only when the CTL pin is higher than 1 V, effective duration of the output voltage soft-start ramp can be estimated with the following formula:

$$T_{SS}[ms] = \frac{4096}{F_{OSC}[kHz]} \cdot \frac{CTL[V] - 1V}{4V}$$

5.4 PWM comparator / slope compensation

In typical isolated operations, current is sensed on a sense resistor R_S put between the source of the primary side MOS and the RTN pin.

The PWM comparator produces the PWM duty cycle by comparing the R_S ramp signal on CS with an error voltage derived from the error amplifier output.

The error amplifier output voltage at the CTL pin is attenuated by a 4:1 resistor divider before it is presented to the PWM comparator input.

The PWM duty cycle increases with the voltage at the CTL pin. The controller output duty cycle reduces to zero when the CTL pin voltage drops below approximately 1 V.

For duty cycles greater than 50%, current mode control loops are subject to sub-harmonic oscillation. PM8801 fixes the maximum duty cycle at 80% and implements a slope compensation technique consisting of adding an additional fixed slope voltage ramp to the signal at the CS pin. This is achieved by injecting a 45 µA sawtooth current into the current sense signal path on an integrated 2 kΩ resistor.

Additional slope compensation may be added by increasing the source impedance of the current sense signal with an external resistor between the CS pin and the source of the current sense signal. The net effect in this case is to increase the slope of the voltage ramp at the PWM comparator terminals.

5.5 Current limit

The current sensed through the CS pin is compared to two fixed levels of 0.5 V and 0.7 V.

The lower level is used to perform a cycle-by-cycle current limit, terminating the PWM pulse. If the overload persists for a duration longer than 4096 switching periods, the PWM is shut down for the same duration before beginning a new soft-start.

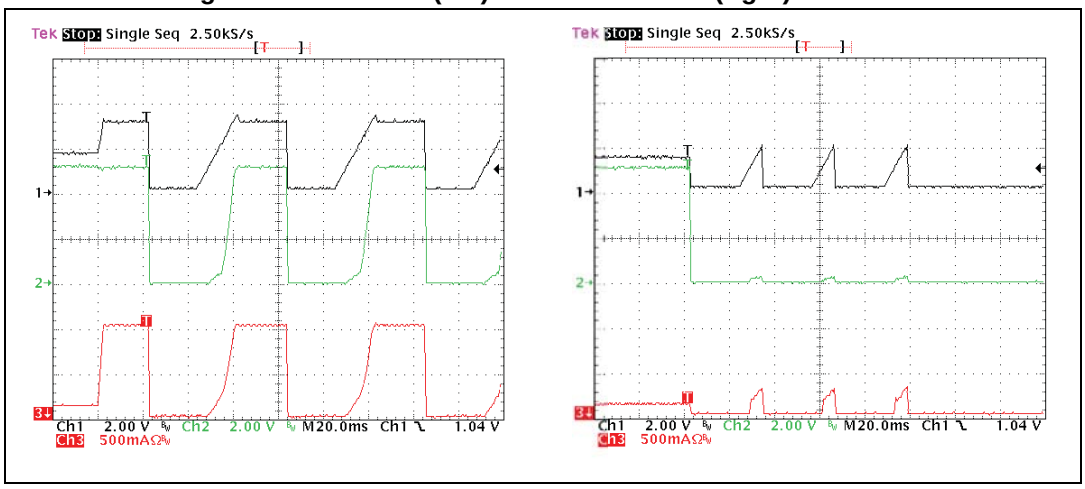
At 250 kHz the allowed overcurrent duration is about 16 ms.

When a severe overcurrent occurs, like a short-circuit of an internal power component, and 0.7 V level is reached on CS, the gate driver is instantaneously shut down and a new soft-start is performed after 4096 switching periods.

In case of persistent severe overcurrent, the control logic tries 4 cycles of fast hiccup before completely shutting down the PWM controller.

To restart the device, after removing the cause of the overcurrent, VDD must be reduced below the UVLO level.

Figure 16. Overload (left) and short-circuit (right) behavior



Ch1: CTL signal, Ch2: 5Vout, Ch3: I input

5.6 Thermal protection

The PM8801 thermal protection limit is set to 160 °C on the junction temperature and is always active. When this threshold is exceeded, the hot-swap MOSFET is opened and the PWM controller is switched off.

When the junction temperature goes below about 130 °C the converter will start automatically, without needing to recycle the input voltage.

6 Auxiliary sources

The majority of Powered Devices is designed to work with power from either a PoE network or auxiliary sources. Even though having both sources simultaneously connected is not the normal operating case, the presence of an auxiliary supply allows PDs to be used also when the PoE is not available or not sufficient.

Different alternatives are available for connecting auxiliary sources to the PoE section of a PD device. Auxiliary sources can be connected prior to the hot-swap MOSFET, after the hot-swap MOSFET or even at the output of the DC/DC converter.

All the above-mentioned methods are available with the PM8801.

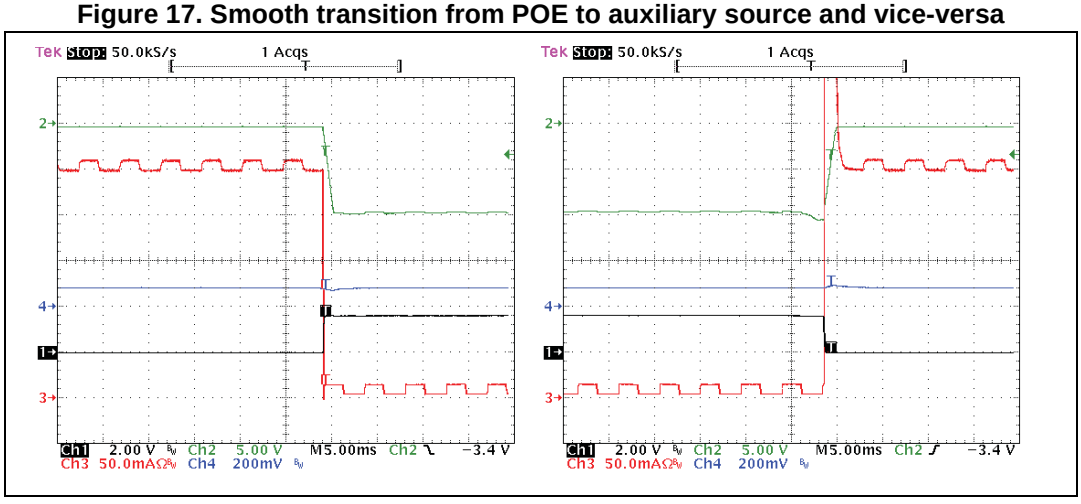
Connection of the wall adapter **prior** to the internal hot-swap MOSFET has a limitation on the voltage of the adapter itself, since it is seen as an alternative of the PoE line and the embedded DC/DC section is activated only when its value is above the UVLO_R threshold. Default inrush and DC current limitation are considered in this case.

Priority of one source over another cannot be guaranteed by design, since it depends on timings of insertion and the value of the PoE line with respect to the auxiliary source, for example, the PoE connection is already established, the auxiliary source cannot prevail unless its value is higher than the one from the PoE after the diode bridge.

Both *Figure 1* and *Figure 2* show simplified application schematics where auxiliary sources are connected **after** the internal hot-swap MOSFET (VDD and RTN). This connection together with the resistor divider on the SA pin allows priority of the external source with respect to the PoE. Indeed, if the voltage of this pin is above the value of 1.20 V typ., the PM8801 will disable its PD interface section and enable only the DC/DC section. The internal hot-swap MOSFET will be opened.

Depending on the value of the auxiliary source, the resistor divider must be dimensioned in order to have voltage on the SA pin above the threshold 1.20 V (see *Table 6*) but still below its maximum operative value of 3.3 V, as reported on *Table 3*.

Figure 17. Smooth transition from POE to auxiliary source and vice-versa



Ch1:SA, Ch2: VSS-RTN, Ch3: Iinput, Ch4: 5Vout

The minimum operative voltage for auxiliary sources connected on the SA pin is 13 V, thus allowing the use of a 15 V typ ±10% power adapter.

The internal logic will enable operations of the pwm controller only if the input voltage is over the signature disable threshold (10.8 V typ, 10.3 - 11.3 V range).

Note that inrush current in this case is not limited and an external solution must be found. The simplest solution is to put a low-value resistor in-series, but this lowers the converter's efficiency. A more efficient solution is the use of a MOSFET as the power switch, able to limit the current during the charging phase, and to add only a few mΩ in-series during normal operation.

No DC current limit is foreseen for rear connection, since the current will not be flowing through the hot-swap MOSFET. Cycle-by-cycle, overcurrent protection and thermal protection are instead always active, as well as when the voltage on SA pin is above the threshold 1.20 V.

The T2P signal will remain high (de-asserted) if a rear auxiliary source is connected.

If the T2P signal was asserted, when the the auxiliary source is connected, it will be turned off; its status is stored unless the input voltage drops. So if the PSE stays connected until the auxiliary source is removed, the T2P indication turns on again when the wall adapter is disconnected.

The removal of the external auxiliary source such as a wall adapter usually is followed by a system reboot because the PSE needs some time to re-detect the PD.

If a rear auxiliary connection (using SA pin) is foreseen in the converter design, it is suggested to move the 0.1 µF capacitor (required by the IEEEE802.3at standard) from the input (VDD to VSS) to the internal hot-swap MOSFET (VSS to GND). Alternatively, split the 0.1 uF in two capacitors of 47 nF: one placed at the input terminal, the second one across the hot-swap MOSFET.

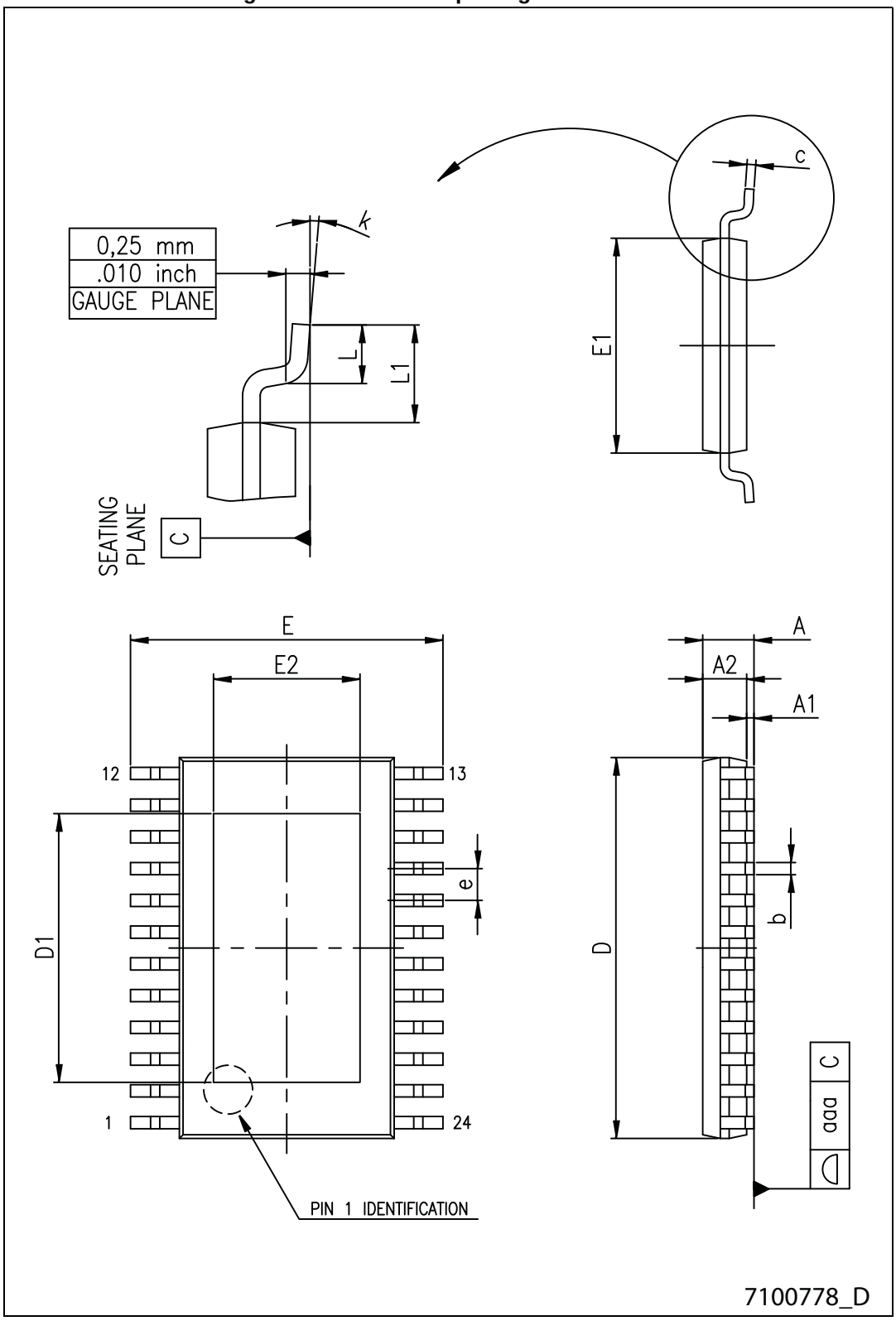
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. TSSOP24 mechanical data

Symbol	mm		
	Min	Typ	Max
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	2.70		
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	1.50		
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0		8
aaa			0.10

Figure 18. HTSSOP24 package dimensions



8 Revision history

Table 10. Document revision history

Date	Revision	Changes
10-Mar-2011	1	Initial release.
29-Jul-2013	2	Document status promoted from preliminary data to production data. Modified title. Updated *Table 4: Thermal data*, *Section 4: PD interface*, *Section 5: PWM controller*, *Section 6: Auxiliary sources* and *Section 7: Package mechanical data*. Minor text changes.

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