FAN9672

Two-Channel Interleaved CCM PFC Controller

Description

The FAN9672 is an interleaved two−channel Continuous Conduction Mode (CCM) Power Factor Correction (PFC) controller IC intended for PFC pre−regulators. Incorporating circuits for leading edge, average current, and “boost”−type power factor correction; the FAN9672 enables the design of a power supply that fully complies with the IEC1000−3−2 specification. Interleaved operation provides substantial reduction in the input and output ripple currents and the conducted EMI filtering becomes simpler and cost effective.

An innovative channel−management function allows slave channels to be loaded and unloaded smoothly in lower power−level conditions according to setting voltage on the CM pin, improving the PFC converter’s load transient response.

The FAN9672 also incorporates a variety of protection functions, including: peak current limiting, input voltage brownout protection, and TriFault Detect function.

Features

- Continuous Conduction Mode Control
- Two−Channel PFC Control (Maximum)
- Average Current−Mode Control
- PFC Slave Channel Management Function
- Programmable Operation Frequency Range: 18 kHz ~ 40 kHz or 55 kHz ~ 75 kHz
- Programmable PFC Output Voltage
- Dual Current Limit Functions
- TriFault Detect Protects Against Feedback Loop Failure
- Sag Protection
- Programmable Soft−Start
- Under−Voltage Lockout (UVLO)
- Differential Current Sensing
- Available in 32−Pin LQFP Package

Typical Applications

- High Power AC−DC Power Supply
- DC Motor Power Supply
- White Goods; e.g. Air Conditioner Power Supply
- Server and Telecom Power Supply
- UPS
- Industrial Welding and Power Supply

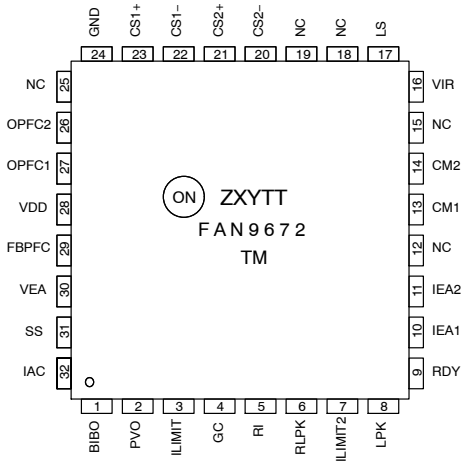
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LQFP−32
FT SUFFIX
CASE 561AB

MARKING DIAGRAM



Z	=	Assembly Plant Code
X	=	Year Code
Y	=	Work Code
TT	=	Die Run Code
T	=	Package Type (Q:LQFP)
M	=	Manufacture Flow Code

ORDERING INFORMATION

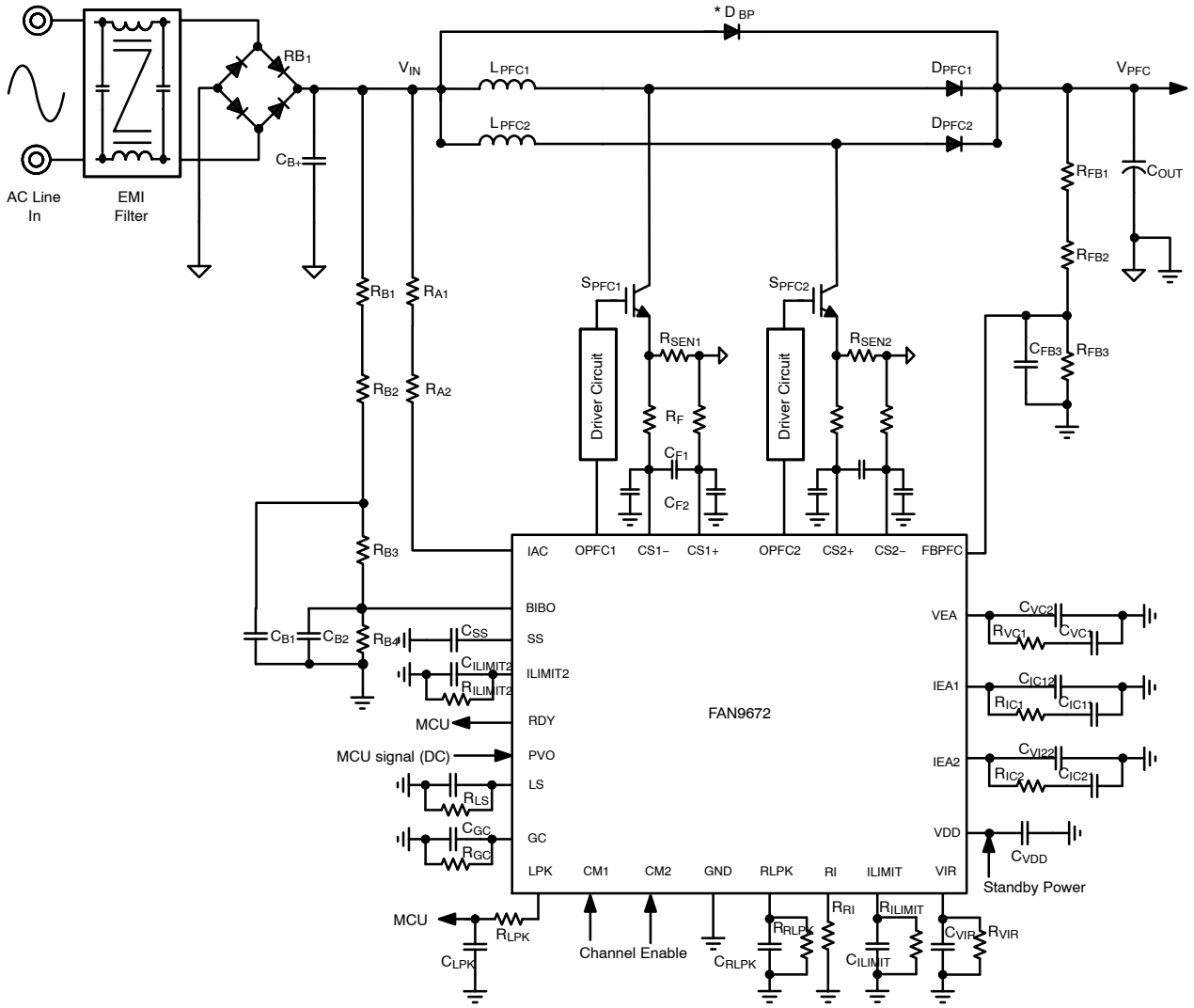
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method
FAN9672Q	−40°C to 105°C	32−Lead, Low Quad Flat Package (LQFP), JEDEC MS−026, Variation BBA, 7 mm Square	Tray

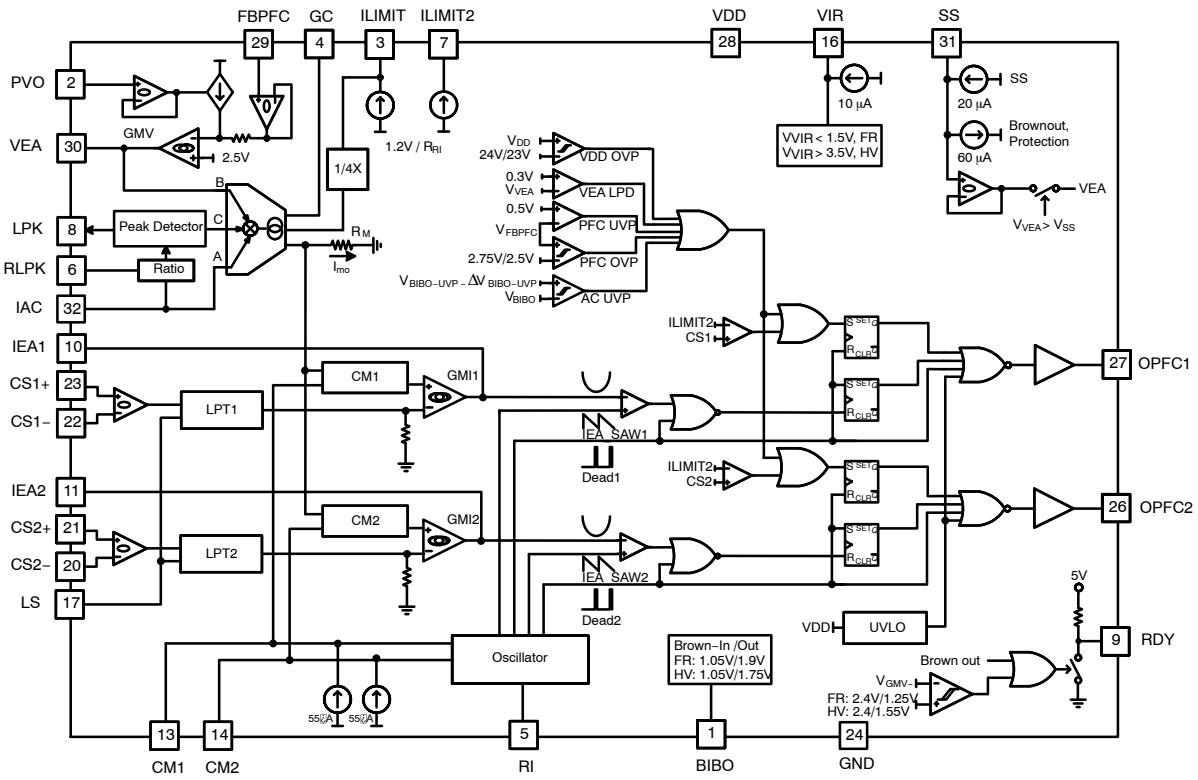
TYPICAL APPLICATION



* About D_{BP} please reference System Design Precautions

Figure 1. Typical Application Diagram for Two−Channel PFC Converter

BLOCK DIAGRAM



* FR: Full Range AC Input, AC85 V~264 V
HV: High Voltage Range AC Input, AC180 ~ 264 V

Figure 2. Functional Block Diagram

PIN CONFIGURATION

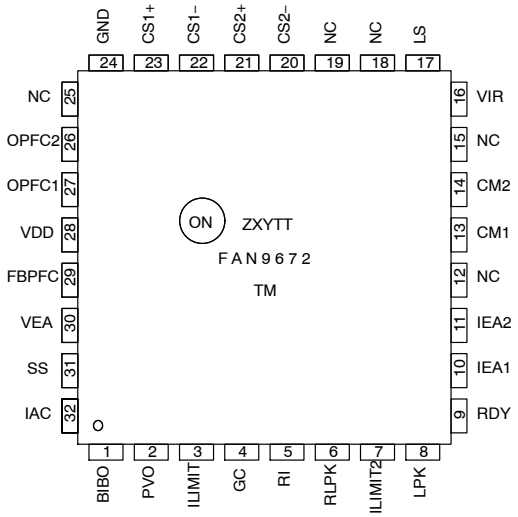


Figure 3. Pin Layout (Top View)

Table 1. PIN DEFINITIONS

Pin #	Name	Description
1	BIBO	Brown−In/Out Level Setting: This pin is used for brown in/out setting.
2	PVO	Programmable Output Voltage: DC voltage from a microcontroller (MCU) can be applied to this pin to program the output voltage level. The operation range is 3.5 V ~ 0.5 V. If V_{PO} < 0.5 V, the PVO function is disabled.
3	ILIMIT	Current Command Clamp Setting: Average current mode is to control the average value of inductor current by a current command. Connecting a resistor and a capacitor to this pin can determine a limit value of the current command.
4	GC	Input Voltage Gain Control: Connecting a resistor on this pin to set a gain on the input−voltage signal to match FBPFC. The signal here is used for the LPT function. A small capacitor connecting from GC to GND is recommended for noise filtering.
5	RI	Oscillator Setting: There are two oscillator frequency ranges: 18 ~ 40 kHz and 50 ~ 75 kHz. A resistor connected from RI to ground determines the switching frequency. A resistor value between 10.6 k ~44.4 kΩ is recommended.
6	RLPK	Ratio of V_{LPK} and V_{IN}: Connect a resistor and a capacitor to this pin to adjust the ratio of V_{IN} peak to V_{LPK}. Typical value is 12.4 kΩ (1:100 of V_{LPK} and V_{IN} peak). The accuracy of V_{LPK} is primarily determined by the tolerance of R_{RLPK} at this pin.
7	ILIMIT2	Peak Current Limit Setting: Connect a resistor and a capacitor to this pin to set the over−current limit threshold and to protect power devices from damage due to inductor saturation. This pin sets the over−current threshold for cycle−by−cycle current limit.
8	LPK	Peak of Line Voltage: This pin can be used to provide information about the peak amplitude od the line voltage to an MCU.
9	RDY	Output Ready Signal: When the feedback voltage on FBPFC teaches 2.4 V, the RDY pin outputs a high−state V_{RDY} signal to inform the MCU the downstream power stage can start normal operation. If AC brownout is detected, the V_{RDY} signal is LOW to signal the MCU the PFC is not ready.
10	IEA1	Output 1 of PFC Current Amplifier: The signal from this pin is compared with an internal sawtooth signal to determine the pulse width for PFC gate drive 1.
11	IEA2	Output 2 of PFC Current Amplifier: The signal from this pin is compared with an internal sawtooth signal to determine the pulse width for PFC gate drive 2.
12	NC	No connection.
13	CM1	Channel 1 Management Setting: This pin is used to configure the characteristics of PFC enable/disable. Pull voltage on this pin LOW (= 0 V) to enable and HIGH (> 4 V) to disable the whole PFC system.
14	CM2	Channel 2 Management Setting: There are two control methods for channel 2. The first uses an external signal to enable/disable channel 2 (V_{CM2} = 0 V/V_{CM2} > 4 V). The second is linear increase/decrease loading of channel 2 when V_{VEA}, proportional to power level, meets the setting level on V_{CM2}.
15	NC	No connection.
16	VIR	Input Voltage Range Setting: A capacitor and a resistor are connected in parallel from this pin to GND. When V_{VIR} > 3.5 V, the PFC controller only works for the high−voltage input range (180 V_{AC} ~264 V_{AC}) and R_{IAC} must be 12 MΩ. When V_{VIR} < 1.5 V, the PFC controller works for the Universal Input voltage range (90 V_{AC} ~264 V_{AC}) and R_{IAC} must be 6 MΩ. Voltage between 1.5 V and 3.5 V is not allowed.
17	LS	Setting for Current Predict Function: A resistor, connected from this pin to ground, is used to adjust the compensation of linear predict function (LPT). A small capacitor connected from this pin to GND is recommended for noise filtering.
18	NC	No connection.
19	NC	No connection.
20	CS2−	Channel 2 Negative PFC Current Sense Input
21	CS2+	Channel 2 Positive PFC Current Sense Input
22	CS1−	Channel 1 Negative PFC Current Sense Input
23	CS1+	Channel 1 Positive PFC Current Sense Input
24	GND	Ground Reference and Return
25	NC	No connection.
26	OPFC2	Channel 2 PFC Gate Drive: The totem−pole output drive for the MOSFET or IGBT. This pin has an internal 15 V clamp to protect the external power switch.

Table 1. PIN DEFINITIONS (continued)

Pin #	Name	Description
27	OPFC1	Channel 1 PFC Gate Drive: The totem−pole output drive for the MOSFET or IGBT. This pin has an internal 15 V clamp to protect the external power switch.
28	VDD	External Bias Supply for the IC: The typical turn−on and turn−off threshold voltages are 12.8 V and 10.8 V respectively.
29	FBPFC	Voltage Feedback Input for PFC: Inverting input of the PFC error amplifier. This pin is connected to the PFC output through a resistor−divider network.
30	VEA	Output of PFC Voltage−Loop Amplifier: An error−amplifier output for the PFC voltage feedback loop. A compensation network is connected between this pin and ground.
31	SS	Soft−Start: Connect a capacitor to this pin to set the soft−start time. Pulling this pin to ground can disable the gate drive outputs OPFC1 and OPFC2.
32	IAC	Input AC Current: During normal operation, this input provides a current reference for an internal gain modulator. The recommended maximum current on IAC is 65 μA.

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter		Min	Max	Unit
V_{DD}	DC Supply Voltage			30	V
V_{OPFC}	Voltage on OPFC1, OPFC2 Pins		−0.3	V_{DD} + 0.3 V	V
V_L	Voltage on IAC, BIBO, LPK RLPK, FBPFC, VEA, CS1+, CS2+, CS1−, CS2−, CM1, CM2, ILIMIT, ILIMIT2, RI, PVO, GC, LS, VIR Pins		−0.3	7.0	V
V_{IEA}	Voltage on IEA1, IEA2, SS Pins		0	8	V
I_{IAC}	Input AC Current			1	mA
$I_{PFC−OPFC}$	Peak PFC OPFC Current, Source or Sink			0.5	A
P_D	Power Dissipation, T_A < 50 °C			1640	mW
$R_{\theta J−A}$	Thermal Resistance (Junction−to−Air)			77	°C/W
T_J	Operating Junction Temperature		−40	150	°C
T_{STG}	Storage Temperature Range		−55	150	°C
T_L	Lead temperature (Soldering)			260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012		4	kV
		Charged Device Model, JESD22−C101		2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
$V_{DD−OP}$	Operating Voltage		15		V
$L_{MISMATCH}$	Boost Inductor Mismatch	−5		+5	%

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{DD} = 15 V and T_J = −40~105°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD SECTION						
$I_{DD\ ST}$	Startup Current	V_{DD} = V_{TH-ON} - 0.1 V		30	80	μA
I_{DD-OP}	Operating Current	V_{DD} = 14 V, Output Not Switching, R_{RI} = 25 kΩ	4	6	7	mA
V_{TH-ON}	Turn−On Threshold Voltage	V_{DD} Rising	11.7	12.8	13.9	V
ΔV_{TH}	UVLO Hysteresis		2		3	V
V_{DD-OVP}	V_{DD} OVP Threshold	OPFC1~2 Disabled, IEA1~2 and SS Pull Low	23	24	25	V
ΔV_{DD-OVP}	V_{DD} OVP Hysteresis			1		V
t_{D-OVP}	V_{DD} OVP Debounce Time				80	μs
OSCILLATOR (Note 3)						
V_{RI}	Sourcing Voltage on RI	R_{RI} = 25 kΩ	1.15	1.20	1.25	V
f_{OSC1}	PFC Frequency Test Case 1	R_{RI} = 25 kΩ	30	32	34	kHz
f_{OSC2}	PFC Frequency Test Case 2	R_{RI} = 12.5 kΩ	58	62	66	kHz
f_{DV}	Voltage Stability	13 V ≤ V_{DD} ≤ 22 V			2	%
f_{DT}	Temperature Stability				2	%
$\Delta V_{IEA-SAW32}$	$V_{IEA-SAW}$ of PFC Frequency 32 kHz	R_{RI} = 25 kΩ		5		V
$\Delta V_{IEA-SAW64}$	$V_{IEA-SAW}$ of PFC Frequency 64 kHz	R_{RI} = 12.5 kΩ		5.15		V
$D_{PFC-MAX}$	Maximum Duty Cycle	V_{IEA} > 7 V	94	97		%
$D_{PFC-MIN}$	Minimum Duty Cycle	V_{IEA} < 1 V			0	%
f_{RANGE1}	Frequency Range 1 (Notes 3, 4)		18		40	kHz
f_{RANGE2}	Frequency Range 2 (Notes 3, 4)		55		75	kHz
$t_{DEAD-MIN}$	Minimum Dead Time	R_{RI} = 10.7 kΩ		600		ns
INPUT−RANGE SETTING (VIR)						
V_{VIR-H}	HIGH Setting Level for High Voltage Input Range	R_{VIR} = 500 kΩ (V_{VIR} = 5 V)	3.5			V
V_{VIR-L}	LOW Setting Level for Low Voltage Input Range or Full Voltage Input Range	V_{VIR} = 0 V			1.5	V
I_{VIR}	Sourcing Current of VIR Pin		7	10	13	μA
PFC Soft−Start						
I_{SS}	Constant Current Output for Soft−Start	System Brown−in		22		μA
V_{SS}	Maximum Voltage on SS		6.8			V
$I_{SS-Discharge}$	Discharge Current of SS Pin	Brownout, SAG, V_{CM1}>4 V, R_{RI} Open / Short, OTP		60		μA
VOLTAGE ERROR AMPLIFIER						
V_{REF}	Reference Voltage	PVO = GND, T_J = 25°C	2.45	2.50	2.55	V
A_V	Open-Loop Gain (Note 3)		42	65		dB
G_{mv}	Transconductance	V_{NONINV} − V_{INV} = 0.5 V, T_J = 25°C		100		μS
$I_{FBPFC-L}$	Maximum Source Current	V_{FBPFC} = 2 V, V_{VEA} = 3 V	40	50		μA
$I_{FBPFC-H}$	Maximum Sink Current	V_{FBPFC} = 3 V, V_{VEA} = 3 V		−50	−40	μA
I_{BS}	Input Bias Current Range		−1		1	μA
$I_{FBPFC-FL}$	Pull High Current for FBPFC	FBPFC Floating		500		nA
V_{VEA-H}	Output High Voltage on V_{VEA}	V_{FBPFC} = 2 V	5.7	6.0		V
V_{VEA-L}	Output Low Voltage on V_{VEA}	V_{FBPFC} = 3 V		0	0.15	V

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{DD} = 15 V and T_J = −40~105°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOLTAGE ERROR AMPLIFIER						
$I_{VEA-DIS}$	Discharge Current	Brownout, R_{RI} Open /Short, OTP, SAG		10		μA
$V_{VEA-OFF}$	Threshold Voltage for Low−Power Detection	When $V_{VEA} < V_{VEA-OFF}$, $V_{OPFC1~2}$ are Off & $V_{IEA1~2}$ are Pulled Low		0.3		V
CURRENT ERROR AMPLIFIERS						
G_{mi}	Transconductance	$V_{NONINV} = V_{INV}$, V_{IEA} = 4 V, V_{ILIMIT} > 0.6 V, T_J = 25°C		88		μS
V_{OFFSET}	Input Offset Voltage	V_{VEA} = 0.45 V, R_{IAC}=12 MΩ, V_{IAC} = 311 V, V_{FBPFC} = 2 V, V_{VIR} = 5 V, T_J = 25°C		0		mV
V_{IEA-H}	Output High Voltage		6.8	7.0		V
V_{IEA-L}	Output Low Voltage			0	0.4	V
I_L	Sourcing Current	$V_{NONINV} - V_{INV}$, = +0.6 V, V_{IEA} = 1 V, V_{ILIMIT} >0.6 V	35	50		μA
I_H	Sinking Current	$V_{NONINV} - V_{INV}$, = -0.6 V, V_{IEA} = 6.5 V, V_{ILIMIT} > 0.6 V		−50	−35	μA
A_I	Open−Loop Gain (Note 3)		40	50		dB
$I_{IEA-LOW}$	IEA Pin Pull−Low Capability	$V_{IEA} \geq$ 5 V	500			μA
GAIN MODULATOR (Current Command Generator)						
I_{AC}	Input for AC Current (Notes 3, 5)	Multiplier Linear Range	0		65	μA
BW	Bandwidth (Notes 3, 5)	I_{AC} = 40 μA		2		kHz
V_{RM}	Gain Modulator Output (I_{MO}* R_M) Test Cases	V_{IAC} = 106.07 V, R_{IAC} = 6 MΩ, V_{FBPFC} = 2.25 V, V_{BIBO} = 2 V, V_{CM2} > 4.5 V, T_J = 25°C		0.490		V
		V_{IAC} = 120.21 V, R_{IAC} = 6 MΩ, V_{FBPFC} = 2.25 V, V_{BIBO} = 2 V, V_{CM2} > 4.5 V, T_J = 25°C		0.430		
		V_{IAC} = 155.56 V, R_{IAC} = 6 MΩ, V_{FBPFC} = 2.25 V, V_{BIBO} = 2 V, V_{CM2} > 4.5 V, T_J = 25°C		0.327		
		V_{IAC} = 311.13 V, R_{IAC} = 12 MΩ, V_{FBPFC} = 2.25 V, V_{BIBO} = 2 V, V_{CM2} > 4.5 V, V_{VIR} > 3.5 V, T_J = 25°C		0.320		
		V_{IAC} = 373.35 V, R_{IAC} = 12 MΩ, V_{FBPFC} = 2.25 V, V_{BIBO} = 2 V, V_{CM2} > 4.5 V, V_{VIR} > 3.5 V, T_J = 25°C		0.260		
R_M	Resistor of Gain Modulator Output	$R_M = V_{RM} / I_{MO}$		7.5		kΩ
ILIMIT (Current Command Limit)						
V_{RM-R}	Range of Peak Value in Current Command (V_{ILIMIT}/4)		0.2		0.8	V
$V_{RM-ILIMIT}$	Current Command Limit Test Case	R_{ILIMIT} = 42 kΩ, R_{RI} = 25 kΩ, $V_{RM-LIMIT} = R_{ILIMIT} * I_{ILIMIT}/4$		0.504		V
I_{ILIMIT}	Sourcing Current of ILIMIT Pin	R_{RI} = 25 kΩ		49		μA
ILIMIT2 (CS1/CS2, Pulse−by−Pulse Current Limit)						
$V_{ILIMIT2-CS1}$	Peak Current Limit Voltage Test Case	$R_{ILIMIT2}$ = 30 kΩ, R_{RI} = 25 kΩ, CS1~2 > $V_{ILIMIT2}$ OPFC1 Disables, $V_{IEA1~2}$ Pull Low		1.48		V
$V_{ILIMIT2-CS2}$				1.48		V
$I_{ILIMIT2}$	Sourcing Current for ILIMIT2 Pin	R_{RI} = 25 kΩ, T_J = 25°C		49.5		μA
$t_{PFC-BNK1}$	Leading−Edge Blanking Time of ILIMIT of Each Channel	V_{DD} = 15 V, OPFC Drops to 9 V		250		ns
$t_{PFC-BNK2}$				250		ns

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{DD} = 15 V and T_J = −40~105°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ILIMIT2 (CS1/CS2, Pulse−by−Pulse Current Limit)						
t_{PD1}	Propagation Delay to Output of Each Channel			200	400	ns
t_{PD2}				200	400	ns
$V_{ILIMIT2-OPEN}$	Threshold of ILIMIT2 Open−Circuit Protection	OPFC1~2 Disabled and $V_{IEA1\sim3}$ Pull Low	3.8	4.0	4.2	V
TriFault Detect™						
$V_{PFC-UVP}$	FBPFC Under−Voltage Protection		0.4	0.5	0.6	V
$V_{PFC-OVP}$	FBPFC Over−Voltage Protection (OVP)		2.70	2.75	2.80	V
$\Delta V_{PFC-OVP}$	FBPFC OVP		200	250	300	mV
$t_{FBPFC-OPEN}$	FBPFC Open Delay (Note 3)	V_{FBPFC} = $V_{PFC-UVP}$ to FBPFC Open, 470 pF from FBPFC to GND		2		ms
$t_{FBPFC-UVP}$	Under−Voltage Protection Debounce Time			50		μs
PVO						
V_{PVO}	Programmable Output Setting Range on PVO Pin		0.3		3.5	V
V_{PVO_DIS}	PVO Disable Voltage	PVO< V_{PVO_DIS}		0.2		V
$V_{PVO-CLAMPH}$	Low−clamp of FBPFC based on PVO	FBPFC Connected to VEA, V_{PVO} = 4 V		1.6		V
V_{FBPFC1}	FBPFC Voltage Test Cases	FBPFC Connected to VEA, V_{PVO} = 0.3 V		2.425		V
V_{FBPFC2}		FBPFC Connected to VEA, V_{PVO} = 3.5 V		1.625		V
$I_{PVO-Discharge}$	PVO Discharge Current	PVO Open		1		μA
GAIN COMPENSATION (GC) SECTION (Note 6)						
I_{GC-L1}	Test Cases of Mirror Current of I_{AC} on GC Pin	V_{VIR} = 0 V, V_{IAC} = 127.28 V, R_{IAC} = 6 MΩ,		20.71		μA
I_{GC-L2}		V_{VIR} = 0 V, V_{IAC} = 311.13 V, R_{IAC} = 6 MΩ,		51.86		μA
I_{GC-HV}		V_{VIR} = 5 V, V_{IAC} = 311.13 V, R_{IAC} = 12 MΩ.		51.86		μA
$I_{GC-OPEN}$	Pull High Current for GC−Pin Open			100		nA
$V_{GC-OPEN}$	GC−Pin Open Voltage	V_{GC} > $V_{GC-OPEN}$ V_{IEA}, OPFC1&2 Blanking	2.85	3.00	3.15	V
INDUCTANCE SETTING (LS) Section (Note 6)						
R_{LS}	Acceptable Range of Inductance Setting		12		87	kΩ
V_{LS-MIN}	Voltage Difference between V_{FBPFC} and V_{GC} on LS Pin	$V_{FBPFC} - V_{GC} \geq 0$ V		50		mV
BROWN IN /OUT						
$V_{BIBO-FL}$	Threshold of Brown−out at VIR = LOW Setting (Full AC−Input Range)	V_{VIR} < 1.5 V, R_{IAC} = 6 MΩ	1.00	1.05	1.10	V
ΔV_{BIBO-F}	Hysteresis	V_{BIBO} > $V_{BIBO-FL}$ + ΔV_{BIBO-F}, Brown−in, Start SS		850		mV
$V_{BIBO-HL}$	Threshold of BO at VIR=HIGH Setting (High AC−Input Range)	V_{VIR} > 3.5 V, R_{IAC} = 12 MΩ	1.00	1.05	1.10	V
ΔV_{BIBO-H}	Hysteresis	V_{BIBO} > $V_{BIBO-HL}$ + ΔV_{BIBO-H}, Brown−in, Start SS		700		mV
t_{UVP}	Under−Voltage Protection Delay Time			450		ms

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{DD} = 15 V and T_J = −40~105°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SAG PROTECTION SECTION						
V_{SAG}	SAG Voltage of BIBO	1. $V_{BIBO} < V_{SAG}$ & V_{RDY} High for 33 ms, or 2. $V_{BIBO} < V_{SAG}$ & V_{RDY} Low, Brownout,		0.85		V
t_{SAG-DT}	SAG Debounce Time	$V_{BIBO} < V_{SAG}$ & V_{RDY} High		33		ms
RLPK, VOLTAGE−SETTING RESISTANCE FOR PEAK DETECTOR						
$I_{RLPK-OPEN}$	Pull High Current for RLPK Open			100		nA
$V_{RLPK-OPEN}$	RLPK Open Voltage	RLPK Open	2.28	2.40	2.52	V
LPK, PEAK−DETECTOR OUTPUT (Note 7)						
V_{LPK-H1}	V_{LPK} Output Test Cases	V_{IAC} = 311 V, R_{IAC} = 1 2MΩ, V_{VIR} > 3.5 V, R_{LPK} = 12.4 kΩ, T_J = 25°C		3.168		V
V_{LPK-H2}		V_{IAC} = 373 V, R_{IAC} = 12 MΩ, V_{VIR} > 3.5 V, R_{LPK} = 12.4 kΩ, T_J = 25°C		3.80		V
V_{LPK-L1}		V_{IAC} = 127 V, R_{IAC} = 6 MΩ, V_{VIR} < 1.5 V, R_{LPK} = 12.4 kΩ, T_J = 25°C		1.29		V
V_{LPK-L2}		V_{IAC} = 373 V, R_{IAC} = 6 MΩ, V_{VIR} < 1.5 V, R_{LPK} = 12.4 kΩ, T_J = 25°C		3.80		V
V_{AC-OFF}	AC OFF Threshold Voltage Test Case	V_{IAC} = 373 V, R_{IAC} = 12 MΩ, V_{VIR} > 3.5V After t_{AC-OFF} V_{IEA} Pull Low		32		V
V_{AC-ON}	AC ON Threshold Voltage Test Case	V_{IAC} = 373 V, R_{IAC} = 12 MΩ, V_{VIR} > 3.5 V		V_{AC-OFF} +26		V
CM1 SECTION						
I_{CM1}	CM1 Sourcing Current			55		μA
$V_{CM1-disable}$	PFC Disable Voltage	$I_{CM1} * R_{CM1}$ > 4 V OPFC1~2 Disabled and IEA1~2 Pull Low and SS Pull Low		4		V
θ1	Phase of OPFC1	When $I_{CM1} * R_{CM1}$ < 4 V or Short		0		°
θ2	Phase of OPFC2 (Note 8)		170	180	190	°
CM2 SECTION						
I_{CM2}	CM2 Sourcing Current			55		μA
$V_{CM2-disable}$	Channel−2 Disable Voltage	$I_{CM2} * R_{CM2}$ > 4 V or CM2 Floating OPFC2 Disables and IEA2 Pulls Low		4		V
$V_{CM2-range}$	Set VEA Unload Voltage		0		3.8	V
RDY SECTION						
V_{FB-RD}	Level of V_{FBPFC} to Pull RDY High	V_{PVO} = 0 V, Brown−in, $V_{FBPFC} > V_{FB-RD}$	2.3	2.4	2.5	V
$\Delta V_{FB-RD-L}$	Hysteresis	V_{PVO} = 0 V, V_{IR} < 1.5 V		1.15		V
$\Delta V_{FB-RD-H}$	Hysteresis	V_{PVO} = 0 V, V_{IR} > 3.5 V		0.85		V
Z_{RDY}	Pull High Input Impedance	T_J = 25°C		100		kΩ
$V_{RDY-High}$	High Voltage of RDY		4.8	5.0		V
$V_{RDY-Low}$	Low Voltage of RDY	Pull High Current = 1 mA			0.5	V
PFC OUTPUT DRIVER 1~2						
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD} = 22 V	13	15	17	V

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{DD} = 15 V and T_J = −40~105°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PFC OUTPUT DRIVER 1~2						
V_{GATE-L}	Gate Low Voltage	V_{DD} = 15 V, I_O = 100 mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD} = 13 V, I_O = 100 mA	8			V
t_r	Gate Rising Time	V_{DD} = 15 V, C_L = 4.7 nF, V_{OPFC} from 2 V to 9 V		70		ns
t_f	Gate Falling Time	V_{DD} = 15 V, C_L = 4.7 nF, V_{OPFC} from 9 V to 2 V		60		ns
OTP						
T_{OTP-ON}	Over−Temperature Protection (Note 3)			140		°C
ΔT_{OTP}	Hysteresis (Note 3)			30		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. This parameter, although guaranteed by design, is not 100% production tested.
4. The setting range of resistance at the RI pin is between 53.3 kΩ and 10.7 kΩ.
5. Frequency of AC input should be <75 Hz.
6. The R_{LS} and R_{GC} setting suggestion follows the calculation result from application notes AN−4164 and AN−4165.
7. LPK specification is guaranteed at state of PFC working.
8. Pull the CM pin low to ground, ensuring VCM < 0.2 V, to enable an individual channel.

THEORY OF OPERATION

Continuous Conduction Mode (CCM)

The boost converter, shown in Figure 4, is the most popular topology for power factor correction (PFC) in AC−DC power supplies. This can be attributed to the continuous input current waveform provided by the boost inductor and the boost converter's input voltage range low down to 0 V. These fundamental properties make close−to−unity power factor easier to achieve.

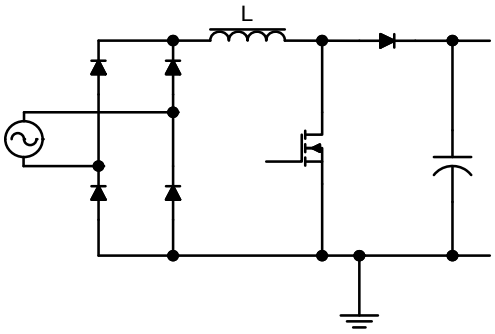
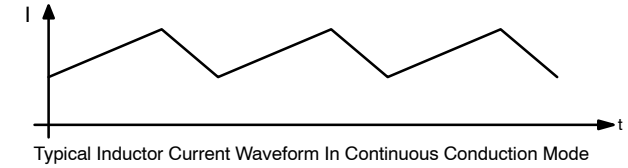
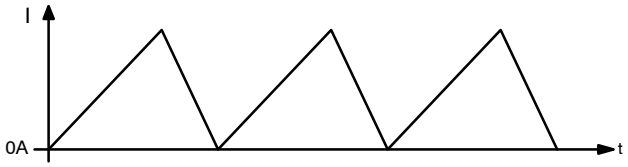


Figure 4. Basic PFC Boost Converter

The boost converter can operate in Continuous Conduction Mode (CCM) or in Boundary Conduction Mode (BCM). These two descriptive names refer to the current flowing in the energy storage inductor of the boost power stage.



Typical Inductor Current Waveform In Continuous Conduction Mode



Typical Inductor Current Waveform In Boundary Conduction Mode

Figure 5. Basic PFC Boost Converter

As the names indicate, the inductor current in CCM is continuous and always above zero. In BCM, the new switching period is initiated when the inductor current returns to zero. There are many fundamental differences in CCM and BCM operation and the respective designs of the boost converter. The FAN9672 is designed for CCM control, as Figure 5 shows. This method reduces inductor current ripple because the start current of each cycle is typically not 0 A. The ripple is controlled by the operation frequency and inductance design. This characteristic makes the maximum peak current in the power semiconductor devices lower.

Gain Modulator (IA, LPK, VEA)

The FAN9672 employs two control loops for power factor correction: a current control loop and a voltage control loop. The current control loop shapes inductor current, as shown in Figure 6, through a current command, IMO, from the gain modulator.

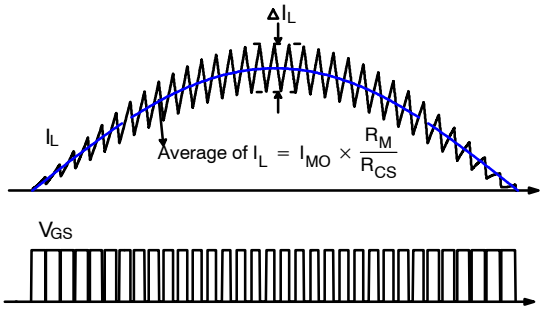


Figure 6. CCM PFC Operation Waveforms

The gain modulator is the block that provides the reference to control PFC input current. The output signal of the gain modulator, IMO, is a function of VVEA, IIAC, and VLPK; as shown in the Figure 7.

There are three inputs to the gain modulator:

- I_{IAC}: A current representing the instantaneous input voltage (amplitude and wave shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is fed into the gain modulator. Sampling mechanism on I_{IAC} minimizes ground noise, important in high−power, switching−power conversion environment. The gain modulator responds linearly to I_{AC}.
- V_{LPK}: Voltage proportional to the peak-voltage output of the bridge rectifier when the PFC is working. The signal is the output of peak−detect circuit detecting from I_{AC}. This factor of the gain modulator is input−voltage feed−forward control. This voltage information is not valid when the PFC is not working.
- V_{VEA}: The output of the voltage error amplifier. The gain modulator responds linearly to variations of this voltage.

The output of the gain modulator is a current signal, I_{MO}, as eq. 1:

$$I_{MO} = K \times \frac{I_{AC} \times V_{VEA}}{V_{LPK}^2} \qquad \text{(eq. 1)}$$

where the K term is about 0.8 for V_{IR} < 1.5 V and 3.2 for V_{IR} > 3.5V respectively.

The current signal, I_{MO}, is in the form of a full−wave rectified sinusoid at twice of the line frequency. The gain modulator forms the reference for the current loop and ultimately controls the instantaneous current drawn from the power line.

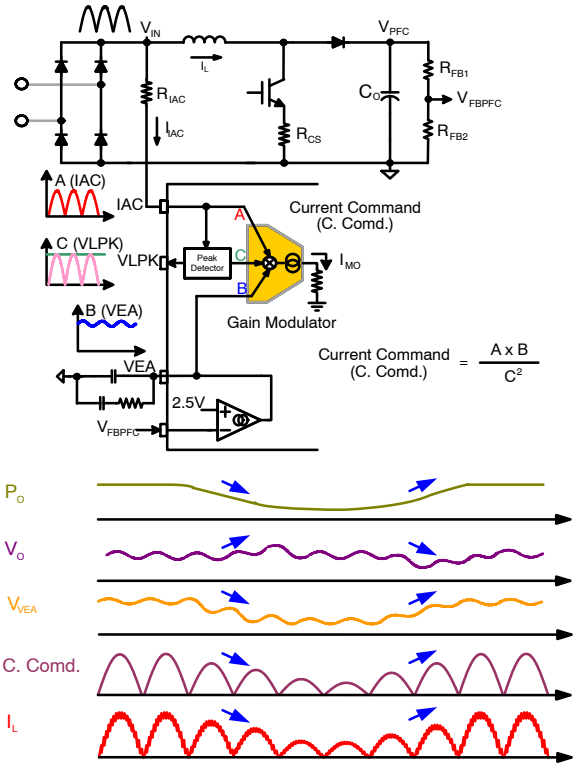


Figure 7. Input of Gain Modulation

Current Balance

Current matching of different channel is an important topic of multi−channel control. In FAN9672, control of current in each channel is based on sensed signal V_{CS} to track the current command from the gain modulator, as shown in Figure 8.

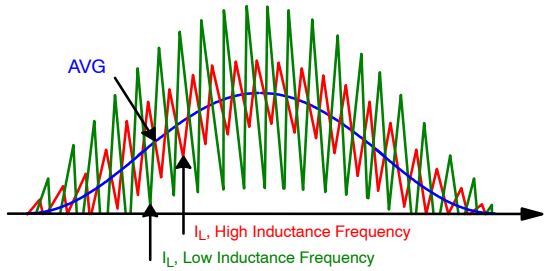


Figure 8. Average Current Mode Control

The main factors to balance current in each channel are layout and device tolerance. The tolerance of the shunt resistor for the current sense is especially important. If the feedback signal, V_{CS}, has large deviation due to the tolerance of the sense resistor, the current of the channels tends to be unbalanced. High precision resistors are recommended.

High−power applications implies current values are high, so the distance of layout trace between the current sense resistors and the controller or power ground (negative of output capacitor) to IC ground is important, as shown in Figure 9. The longer trace and large current make the offset voltage and ground bounce differ significantly for different channels. Decreasing the deviation help balancing different channels. Please check the layout guidance in application notes AN−4164 or AN−4165.

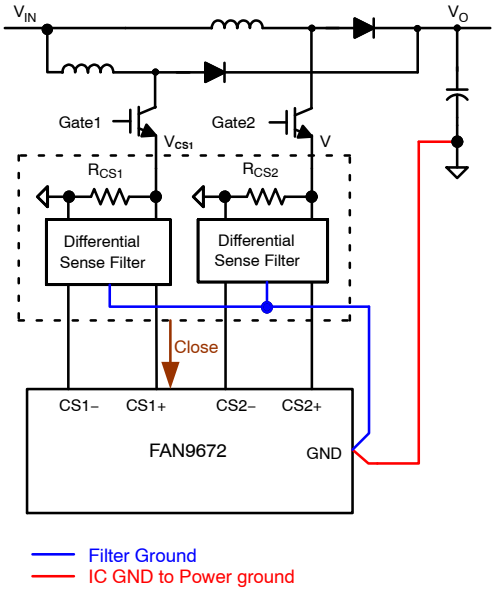


Figure 9. Current Balance Factors

acting as changing relative weighting, for the current command. The relationship of CM and the gain of the slave channel is shown in Figure 10. The level of CM set the threshold of power level, representing by V_{VEA}, for reducing the current command for the slave PFC. The FAN9672 starts to reduce the current command ($I_{MO} \times R_M$) for channel 2 by G_{ain2} from one to zero when the V_{VEA} level is lower than its CM level, as Figure 11 and Figure 12 show. The output power of the slave channel is reduced in response to reduction in current command. For example, when CM2 is set at 3 V and V_{VEA} is less than the CM2 voltage, the channel management block reduces the command for channel 2 as:

$$V_{gmi2+} = I_{MO} \times R_M \times G_{ain2} \quad \text{(eq. 2)}$$

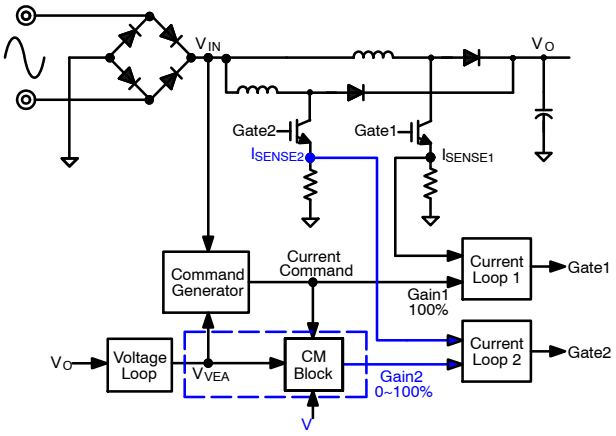


Figure 10. Current Balance Factors

Interleaving

The FAN9672 controller is used to control two−channel boost converters connected in parallel. The controller operates in average−current mode and supports Continuous Conduction Mode (CCM). Each channel affords one−second the power when the system operates close to full load or when channel management is disabled.

Parallel power processing increases the number of power components, but the current rating of independent channels is reduced, allowing power semiconductors with lower current ratings to be applied.

The switches of the two boost converters are operated at a 180° out−of−phase. The interleaving controller can reduce the total ripple current of input. Simultaneously, the output current ripple of each channel is evenly distributed and sequentially rippled on the output capacitor, which can extend the life of the capacitor.

Channel Management/CM Control

The CM pin is used for controlling channel management. The channel management is realized by changing a gain,

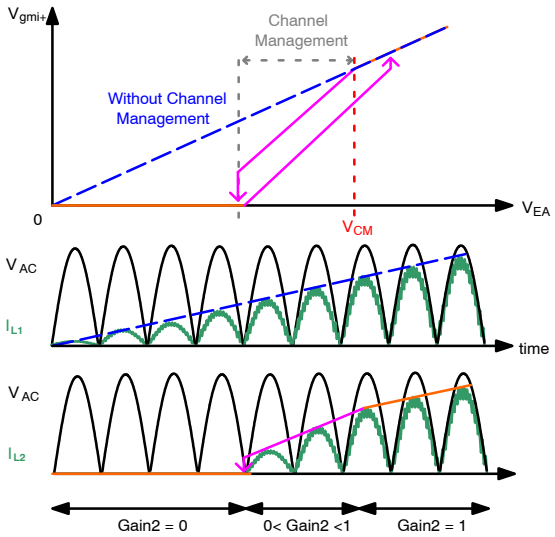


Figure 11. V_{VEA} and CM Relationship

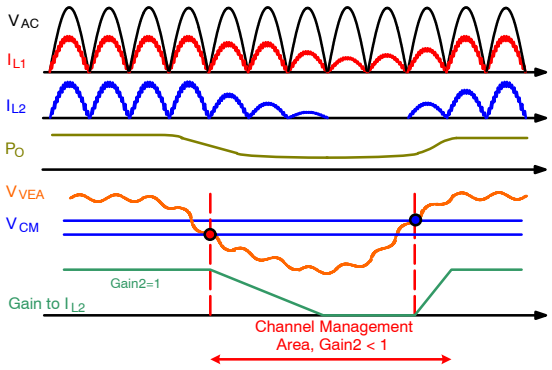


Figure 12. V_{VEA} and V_{CM} Relationship in Channel Management Operation

Table 2 describes the gain change of the slave channel when the PFC operates at various loads. The loading decreases the gain to the slave until it is disabled.

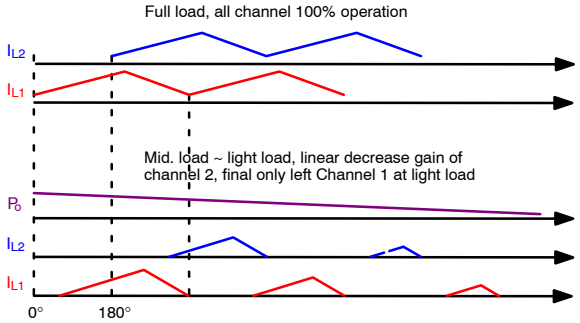


Figure 13. Phase and Gain Change of CM Control

Table 2. PHASE AND GAIN CHANGE OF CM CONTROL

CM (Channel Management)	Phase and Gain	
	Channel 1	Channel 2
Heavy Load (Two Channel 100% Works)	0° (Gain1 = 1)	180° (Gain2 = 1)
Mid. Load	0° (Gain1 = 1)	180° (0 < Gain2 < 1)
Light Load (Only Channel1 Left)	0° (Gain1 = 1)	Disable (Gain2 = 0)

Channel Management 2: External Control

Channel Management (CM) function can also be accessed by an MCU through the connection shown in Figure 14. CM pins have internal pull−up current source. If V_{CM} > 4 V, the channel is disabled. To enable the channel, make V_{CM} = 0 V, as shown in Figure 15.

The CM pin of the slave should be connected with a switch S_2 to ground. One pin of MCU must read the V_{VEA} signal to determine when to turn on/off the slave channel. For example, as shown in Figure 16, two thresholds, $V_{P2-OFF-L}$ and $V_{P2-OFF-H}$, are set in MCU program. When $V_{VEA} < V_{P2-OFF-L}$, the slave PFC turns off. If $V_{VEA} > V_{P2-OFF-H}$, the slave PFC turns on.

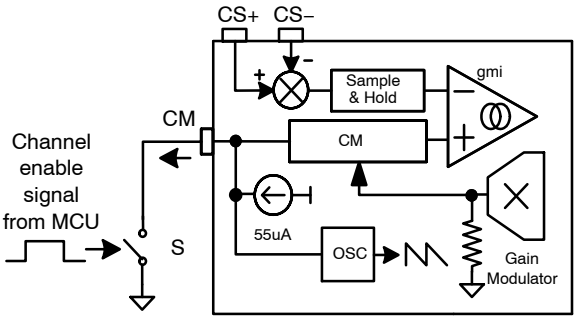


Figure 14. Channel Management by MCU

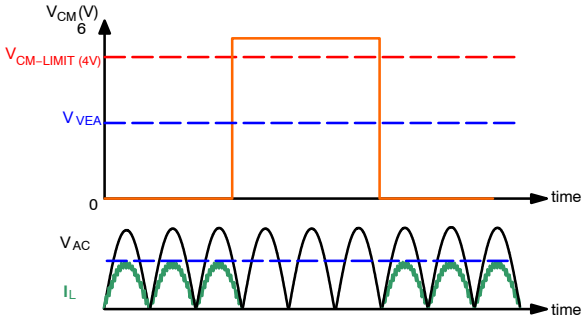


Figure 15. Channel Management by MCU

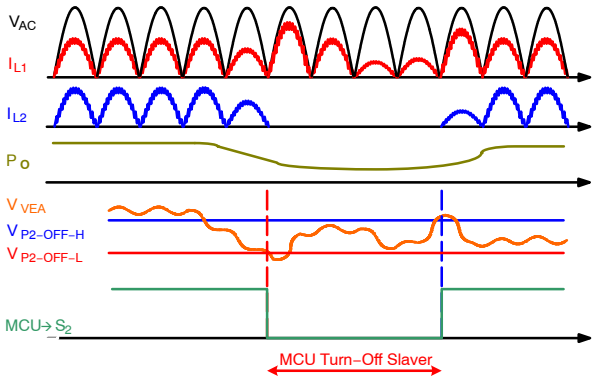


Figure 16. Channel Management by External Signal from MCU

When CM is accessed this way, behavior of each phase will be as illustrated in Table 3 and Figure 17. When the MCU disables channel 2 at mid−load ~ light load, only channel 1 will be operated. G_{ain2} under this control method switches between 100% and 0%.

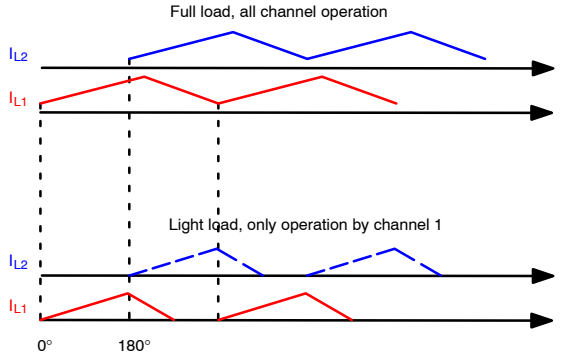


Figure 17. Phase Change under External Signal Control

Table 3. PHASE CHANGE OF EXTERNAL SIGNAL CONTROL

External Signal Control	Phase (Disable Channel: V_{CM} > 4 V, Enable Channel: V_{CM} = 0 V)	
	Channel 1	Channel 2
Heavy Load (All Channels Enabled)	0°	180°
Light Load (Channel 2)	0°	Disable (V_{CM2} > 4 V)
Disable All System	V_{CM1} > 4 V, All Channels Disabled	

FUNCTIONAL DESCRIPTION

Internal Oscillator (RI)

The Frequency of an internal oscillator is determined by an external resistor, R_{RI}, on the RI pin. The frequency of the oscillator is given by eq. 3. The frequency can be freely set in two ranges, 18 kHz ~ 40 kHz and 55 kHz~75 kHz. Setting frequency between 40 kHz and 55 kHz is not allowed in FAN9672.

$$f_{osc} = \frac{8 \times 10^8}{R_{RI}} \qquad \text{(eq. 3)}$$

Current−Control Loop of Boost Stage

As shown in Figure 18, the two control loops for power factor correction are a current−control loop and a voltage−control loop. Based on the reference signal obtained at the IAC pin, the error amplifier in current−control loop regulates current signal as:

$$I_L \times R_{CS} = I_{MO} \times R_M \times G_{ain2} = K \times \frac{I_{AC} \times V_{EA}}{V_{LPK}^2} \times R_M \times G_{ain2} \qquad \text{(eq. 4)}$$

Average value of sensed current, $I_L \times R_{CS}$, is regulated to the current command, $I_{MO} \times R_M$. G_{ain2} is a gain between 0 ~ 1 when the channel management block is engaged for the slave channels. G_{ain2} term is equal to one for channel 1.

Voltage−Control Loop of Boost Stage

The voltage−control loop regulates PFC output voltage by using the internal error amplifier, G_{mv}, making voltage on FBPFC same as the internal reference voltage, 2.5 V. It stabilizes PFC output voltage and decreases 120−Hz ripple on PFC output voltage.

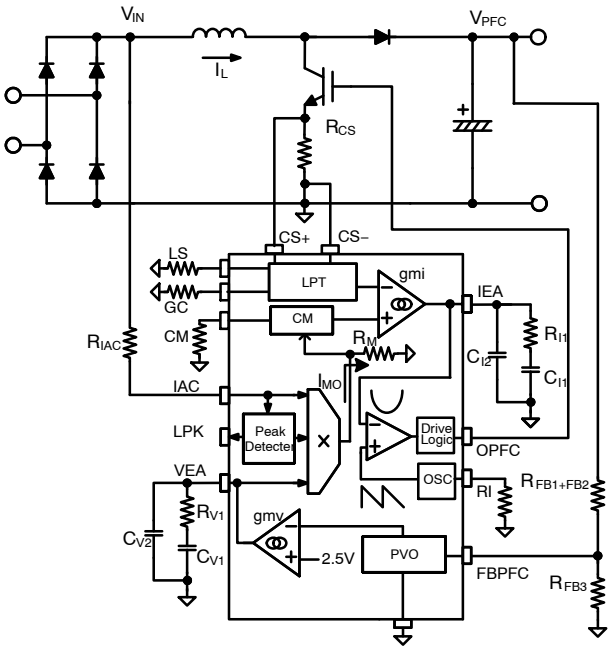


Figure 18. Gain Modulation Block

TriFault Detect

To improve power supply reliability, reduce system component count, and simplify compliance to UL 1950 safety standards, the FAN9672 brings TriFault Detect technology. This feature monitors FBPFC for certain PFC fault conditions.

In the case of a feedback path failure, the output of the PFC can exceed operating limits. Should FBPFC go too low, too

high, or open, the TriFault Detect senses the fault and terminates the PFC output drive.

TriFault Detect is an entirely internal circuit. It requires no external components to perform its function.

PFC Over−Voltage Protection (OVP)

FAN9672 has an auto−restart OVP function. When the feedback level, V_{FBPFC}, reaches 2.75 V (reference level is 2.5 V), the PFC gate signal stops. The PFC gate signal resumes when V_{FBPFC} returns to 2.5 V.

PFC Brown In/Out (BIBO)

An internal AC Under−Voltage Protection (UVP) comparator monitors the AC input information from V_{IN}, as shown in Figure 19. The OPFC is disabled when the V_{BIBO} is less than 1.05 V for 410 ms. If V_{BIBO} is larger than 1.9 V (V_{VIR} < 1.5 V) or 1.75 V (V_{VIR} > 3.5 V), the PFC stage is enabled. The VIR pin is used to set the AC input range according to Table 4.

Table 4. BIBO SETTING OF VARIOUS AC INPUT

Input Range	AC (V)	R_{VIR} Setting (kΩ)	R_{IAC} Setting (MΩ)	BIBO Level (V)
Full−Range	85 ~ 264	10	6	85/75
HV−Single	180 ~ 264	470	12	170/160

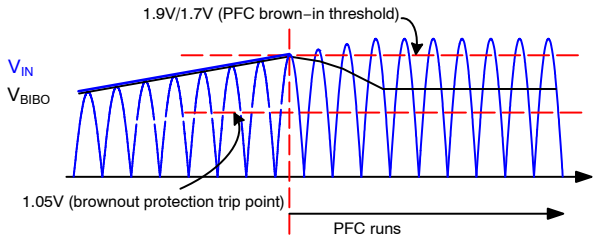


Figure 19. V_{BIBO} According to the PFC Operation

PFC Gate Driver

For high−power applications, the switch device of the system requires high driving current. The totem−pole circuit shown in Figure 20 is recommended.

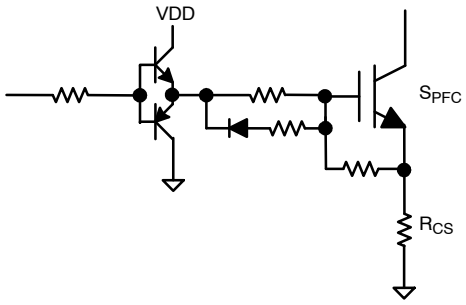


Figure 20. Gate Drive Circuit

Differential Current Sensing (CS+, CS−)

Switching noise problems in interleaved PFC control is more critical than on a single channel, especially for current sensing. The FAN9672 uses a differential amplifier to eliminate switching noise from other channels. The FAN9672 has two groups of differential current−sensing pins. The CSn+ and CSn− are the inputs of the internal differential amplifiers. This makes the PFC more stable in higher−power applications and eliminates switching noise from other channels. As Figure 21 shows, ground bounce can be decreased by a differential sense function.

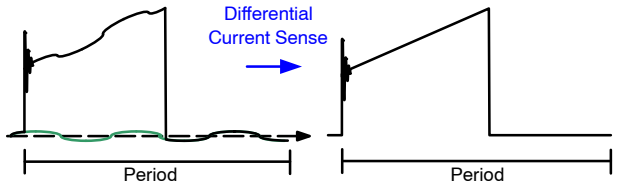


Figure 21. Gate Drive Circuit

Linear Predict Function (GC & LC)

Current sense signal reflects inductor current only when OPFC is on. The linear predict function is used to emulate the behavior of inductor current when the OPFC is off. Resistor on the LS pin is used to set equivalent inductance value for the internal emulator. Resistor on the GC pin is used to align sensed input voltage (IAC) and output voltage (FBPFC) signals. Values of those resistors can be determined by:

$$R_{LS} = \frac{L_{PFC}}{1.5 \times 10^{-9} \times R_{CS} \times \frac{(R_{FB1}+R_{FB2}+R_{FB3})}{R_{FB3}}} \quad \text{(eq. 5)}$$

$$R_{GC} = \frac{6 \times 10^{6}}{\left(\frac{R_{FB1}+R_{FB2}+R_{FB3}}{R_{FB3}}\right)} \quad \text{(eq. 6)}$$

Care must be taken that RLS value need to be within 12~87 kΩ.

Current−Limit Protection

The FAN9672 includes three factors that limits current to manage OCP and inductor saturation: V_{VEA} limit, V_{ILIMIT}, and $V_{ILIMIT2}$. The current-limit thresholds, $V_{ILIMIT1}$ and $V_{ILIMIT2}$, are configurable through ILIMIT and ILIMIT2 pins.

Power (Normal State)

In the normal case, average input power is controlled by the command V_{VEA}. When V_{VEA} rises to 5.6 V, it is internally clamped. Input power can't increase further.

Current Limit 1 (Abnormal State)

The current command from the gain modulator is $K \times I_{AC} \times V_{VEA}/V_{LPK}^2$. In abnormal state, such as AC cycle miss and recover in a short period, the V_{LPK} has a delay before returning to the original level. This delay makes the current command increased. If the command is greater than the limit clamp level, V_{ILIMIT}, current command will be clamped, as shown in Figure 22 and Figure 23. The peak current of this state can be used as the maximum current for inductor design, assuring inductor is not saturated.

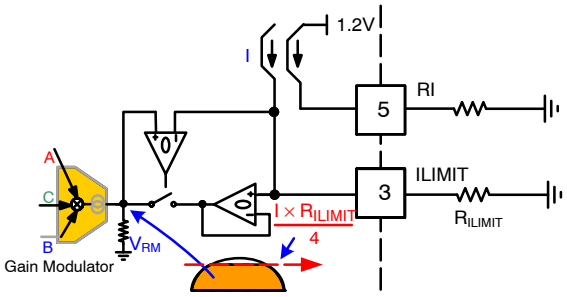


Figure 22. Current Command Limit by ILIMIT

Current Limit 2 (Saturation State)

Use 80% ~ 90% of the maximum current of the switch device to serve as the saturation protection. V_{LIMIT2} is a cycle−by−cycle limit.

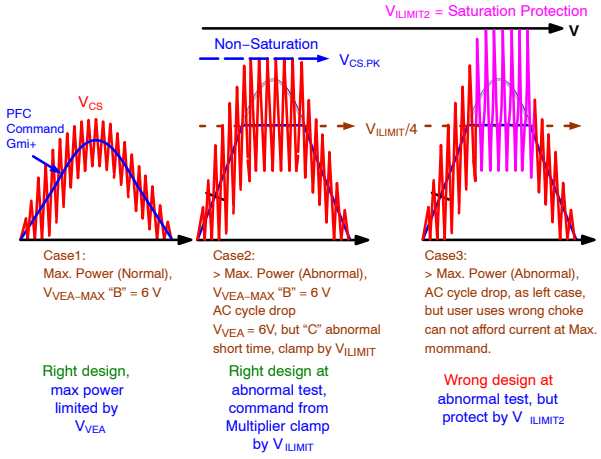


Figure 23. I_{LIMIT} and I_{LIMIT2} Setting

Programmable PFC Output Voltage (PVO)

In some cases, decreasing the PFC output voltage can improve efficiency of the PFC stage. The PVO pin is used to program output voltage, as shown in Figure 24. This function is controlled by an external voltage signal on PVO pin from MCU or other source.

V_{PVO} should be over 0.5 V and the relationship for V_{PVO} and V_{FBPFC} is given by:

$$V_{FBPFC} = 2.5\ V - \left[\frac{V_{PVO}}{4}\right] \qquad \text{(eq. 7)}$$

For instance, if PVO input is 1 V, $R_{FB1}+R_{FB2}$ = 3.7 MΩ, and R_{FB3} = 23.7 kΩ, V_{FBPFB} will be regulated to 2.25 V, making PFC V_O = 354 V.

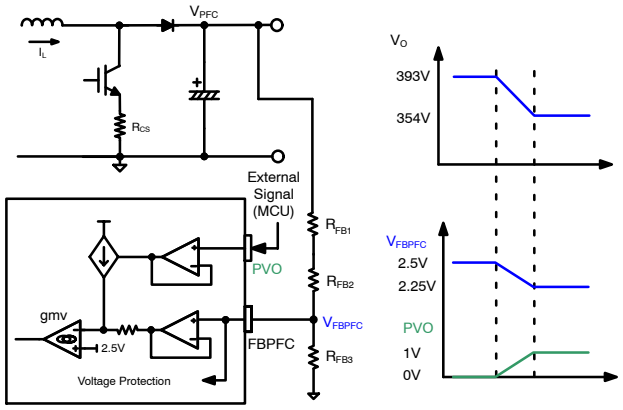


Figure 24. Programmable PFC Output Voltage

RDY Function and AC Line Off/AC "SAG"

The ready (RDY) function is used to signal the MCU that the PFC stage is ready and the downstream power stage can start to operate. When the feedback voltage on FBPFC rises above 2.4 V, V_{RDY} signal pulls HIGH as shown in Figure 25.

If the AC line is OFF (or AC signal drops for a long time), the FAN9672 enters brown−out and V_{RDY} pulls LOW to indicate to the MCU that the power stage should stop, as shown in Figure 26.

When the AC signal drops for only a short time (i.e. 1~1.5 AC cycles), brown−out is not triggered and V_{FBPFC} may not drop too much. In this case, RDY will not go LOW as shown in Figure 27.

AC "sag" means the AC drops to a low level, such as 110 V / 220 V → 40 V. AC "missing" means the AC drops to 0 V. If AC drops, the PFC attempts to transfer energy to V_O before V_O drops to the 50% level. If AC is 0 V, the PFC cannot transfer energy. If the level reaches 50%, the PFC stops, and FAN9672 resets and waits for AC to return.

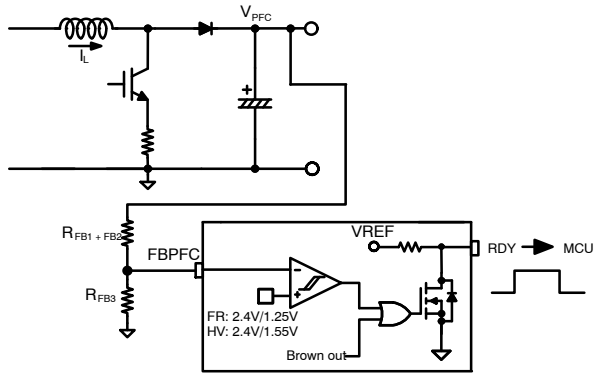


Figure 25. RDY Function to MCU

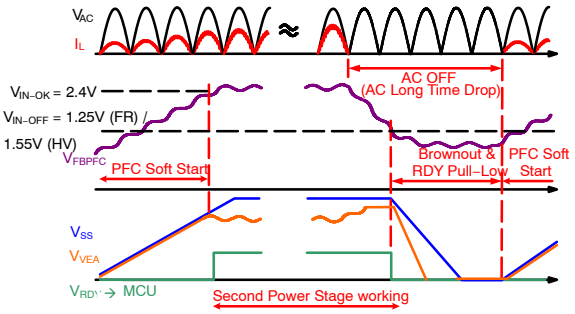


Figure 26. When AC Drops for a Long Time

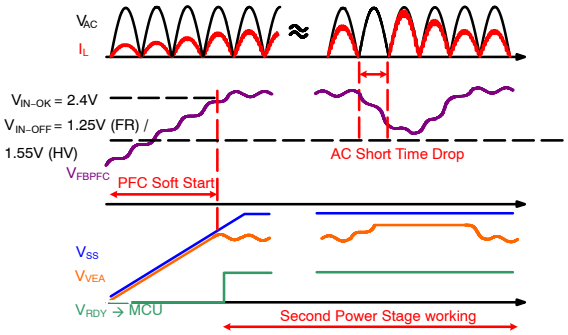


Figure 27. When AC Drops Only Briefly

Soft−Start

Soft−start is combined with RDY pin operation, as Figure 26 and Figure 27 show. During startup, the RDY pin remains LOW until the PFC output voltage reaches 96% of its nominal value. When the supply voltage of the downstream converter is controlled by the RDY pin, the PFC stage always starts with no load because the downstream converter does not operate until the PFC output voltage reaches the required level for the design.

Usually, the error amplifier output, V_{VEA}, is saturated to HIGH during startup because the actual output voltage is less than the target value. V_{VEA} remains saturated to HIGH until the PFC output voltage reaches its target value. Once the PFC output reaches its target value, the error amplifier comes out of saturation. However, it takes several line cycles for V_{VEA} to drop to its proper value for output regulation, which delivers more power to the load than required and causes output voltage overshoot. To prevent output voltage overshoot during startup caused by the saturation of error amplifier, the FAN9672 clamps the error amplifier output voltage (V_{EA}) by the V_{SS} value until PFC output reaches 96% of its nominal value.

Input Voltage Peak Detection

The input AC peak voltage is sensed at the IAC pin. Ideally, RMS value of the input voltage should be used for feed−forward control in the gain modulator circuit. Since the RMS value of the AC input voltage is directly proportional to its peak, it is sufficient to find the peak instead of the more−complicated and slower method of integrating the input voltage over a half line cycle. The internal circuit of the IAC pin works with peak detection on the input AC waveform and output to the LPK pin for MCU use, as shown in Figure 28.

One of the important benefits of this approach is that the peak indicates the correct RMS value even at no load. At no load, the HF filter capacitor at the input side of the boost converter is not discharged around the zero−crossing of the line waveform. Another notable benefit is that, during line transients, when the peak exceeds the previously measured value, the input−voltage feed−forward circuit can react immediately without waiting for a valid integral value at the end of the half−line period.

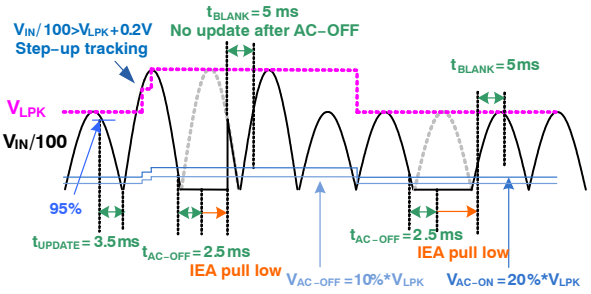


Figure 28. Waveform of LPK Function

The relationship of $V_{IN.PK}$ to V_{LPK} is shown in Figure 29. The peak detection circuits recognizes the V_{IN} information from I_{AC}. When recommended design values in Table 4 are followed, RLPK pin sets the ratio of V_{IN} to V_{LPK} via a resistor R_{RLPK} as described in eq. 8. The target value of V_{LPK} is usually set as one percent (1%) of V_{IN_pk}. The maximum V_{LPK} should not exceed 3.8 V when system operation is at maximum AC input.

As in the below design example, assume the maximum $V_{IN.PK}$ at 373 V (264 V_{AC}), the relationship of $V_{IN.PK}$/ V_{LPK} is 100, and V_{LPK} = 3.73 V < 3.8 V.

$$V_{LPK} = \frac{V_{IN.PK}}{100} \times \frac{R_{RLPK}}{12.4k} \qquad \text{(eq. 8)}$$

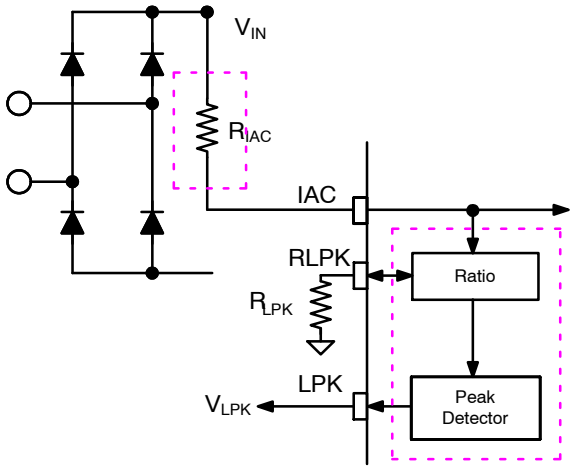


Figure 29. Relationship of $V_{IN.PK}$ to V_{LPK}

Typical Performance Characteristics

Typical characteristics are provided at V_{DD} = 15 V unless otherwise noted.

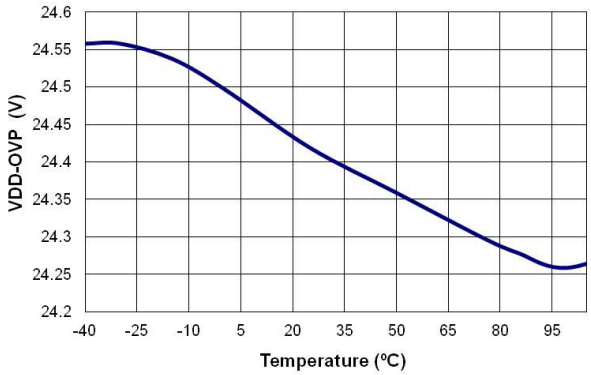


Figure 30. I_{DD-OP} vs. Temperature

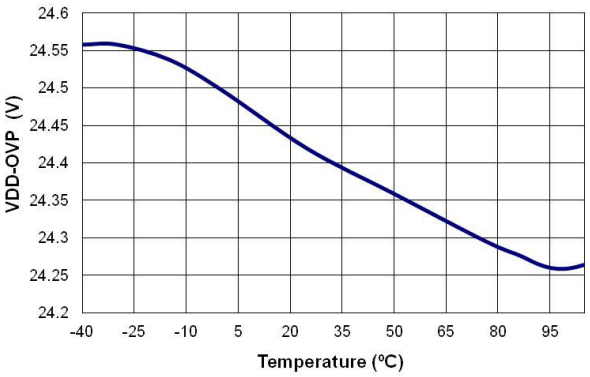


Figure 31. V_{DD-OVP} vs. Temperature

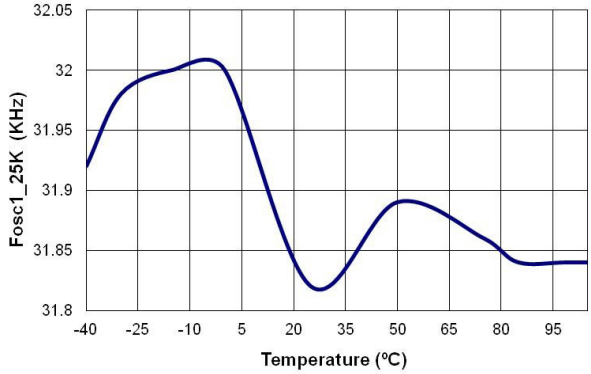


Figure 32. f_{osc} vs. Temperature

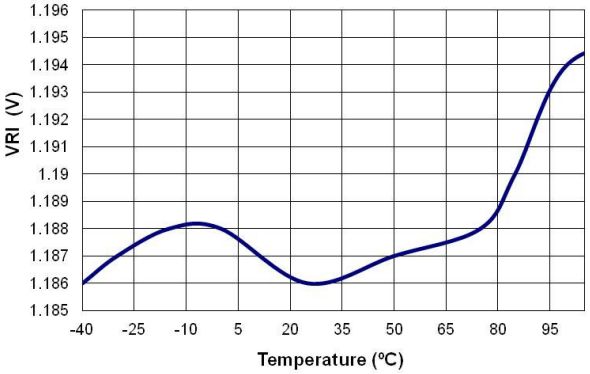


Figure 33. V_{RI} vs. Temperature

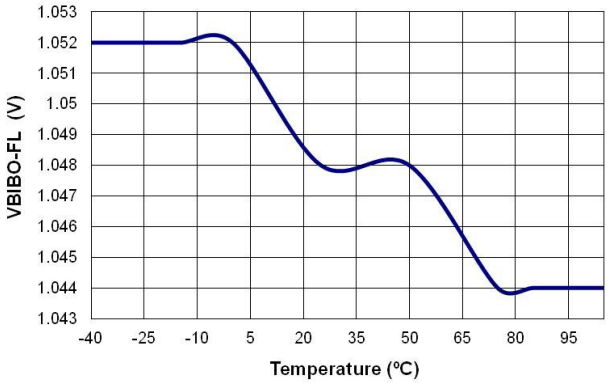


Figure 34. $V_{BIBO-FL}$ vs. Temperature

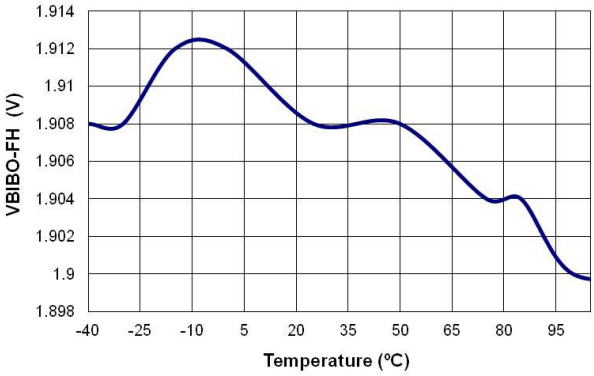


Figure 35. $V_{BIBO-FH}$ vs. Temperature

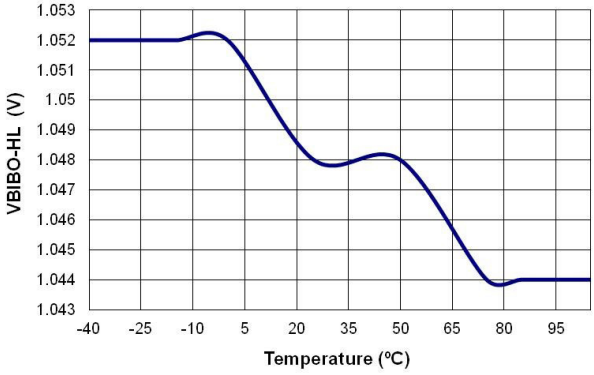


Figure 36. $V_{BIBO-HL}$ vs. Temperature

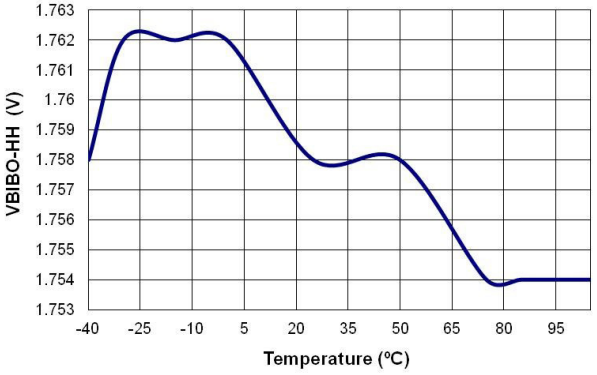


Figure 37. $V_{BIBO-HH}$ vs. Temperature

Typical Performance Characteristics (continued)
Typical characteristics are provided at V_{DD} = 15 V unless otherwise noted.

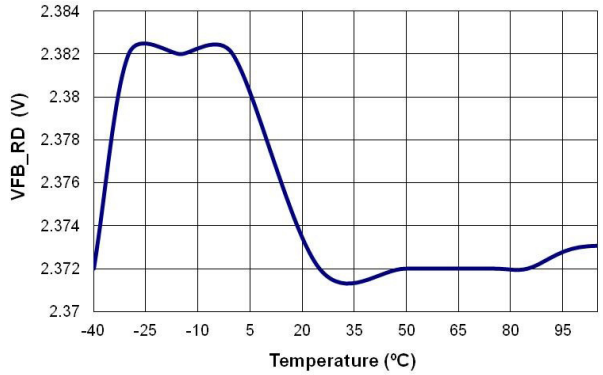


Figure 38. $V_{FBPFC-RD}$ vs. Temperature

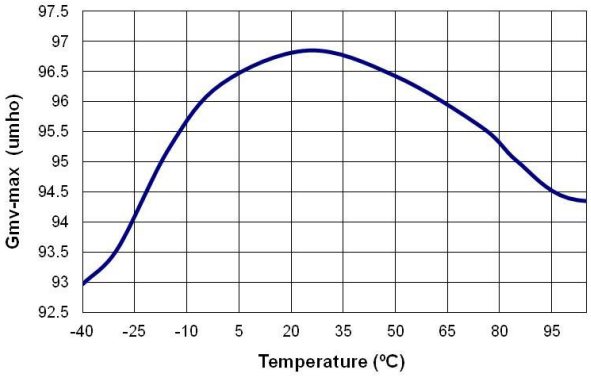


Figure 39. Gm_{V-MAX} vs. Temperature

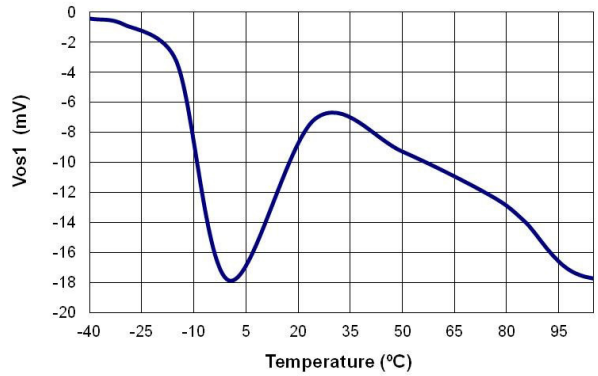


Figure 40. V_{OFFSET} vs. Temperature

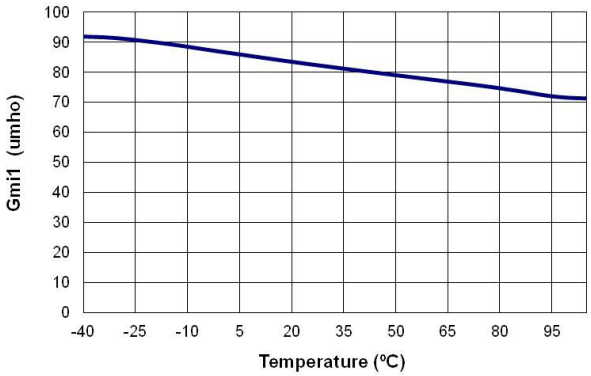


Figure 41. GM_I vs. Temperature

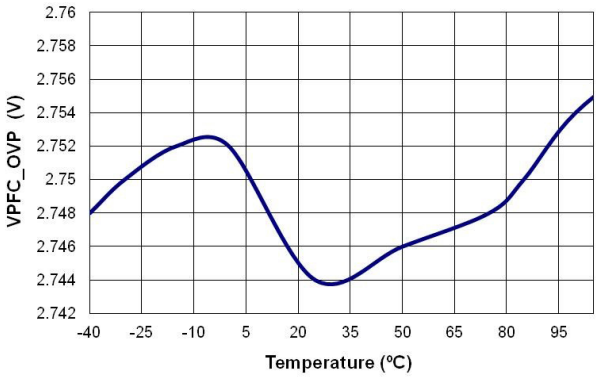


Figure 42. $V_{PFC-OVP}$ vs. Temperature

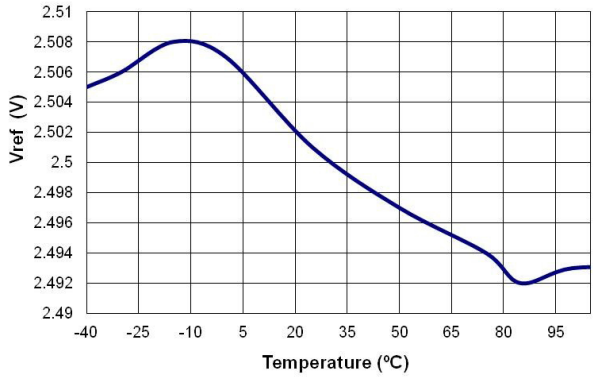


Figure 43. V_{REF} vs. Temperature

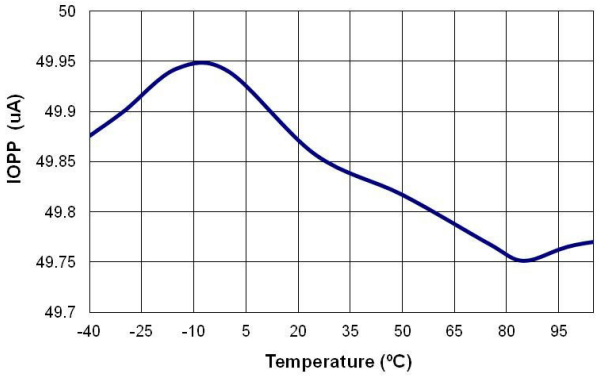


Figure 44. I_{LIMIT} vs. Temperature

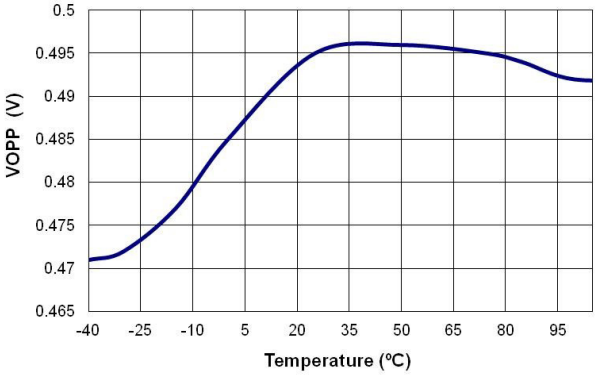


Figure 45. V_{LIMIT} vs. Temperature

Typical Performance Characteristics (continued)

Typical characteristics are provided at V_{DD} = 15 V unless otherwise noted.

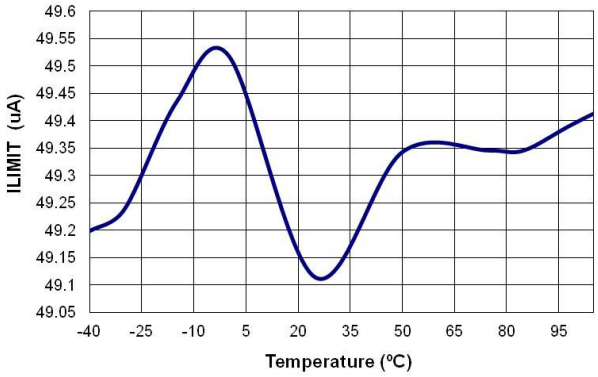


Figure 46. $I_{I\ IMIT2}$ vs. Temperature

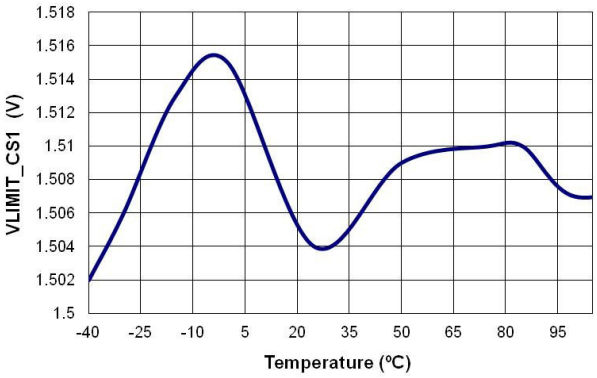


Figure 47. $V_{ILIMIT2-CS1}$ vs. Temperature

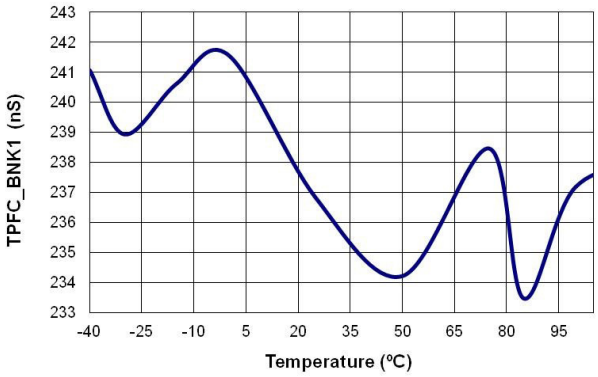


Figure 48. $t_{PFC-BNK}$ vs. Temperature

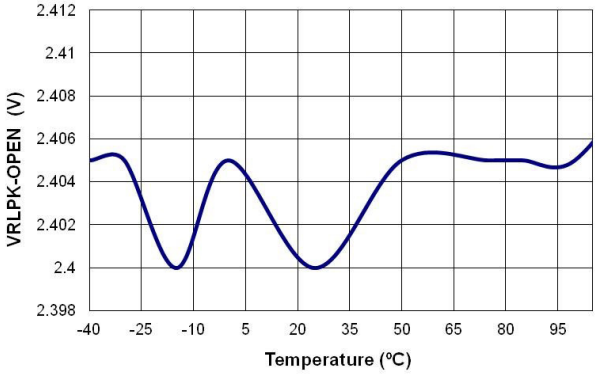


Figure 49. $V_{RLPK-OPEN}$ vs. Temperature

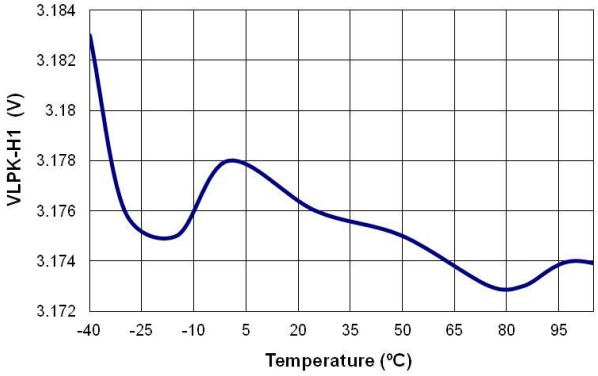


Figure 50. V_{LPK-H1} vs. Temperature

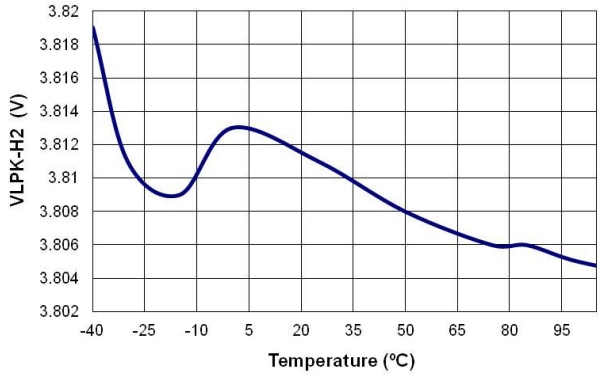


Figure 51. V_{LPK-H2} vs. Temperature

Table 5. TYPICAL APPLICATION CIRCUIT

Application	Output Power	Input Voltage	Output Voltage/Output Current
Single−Stage, Two−Channel PFC	3400 W	180 ~ 264 V_{AC}	393 V/8.48 A

Features

- 180 V_{AC} ~264 V, Two−Channel PFC Using FAN9672
- Switch−Charge Technique of Gain Modulator for Better PF and Lower THD
- 40 kHz Low Switching Frequency Operation with IGBT
- Over−Voltage Protection (OVP), Under−Voltage Protection (UVP), Over−Current Protection (I_{LIMIT}), Inductor Saturation Protection (I_{LIMIT2})

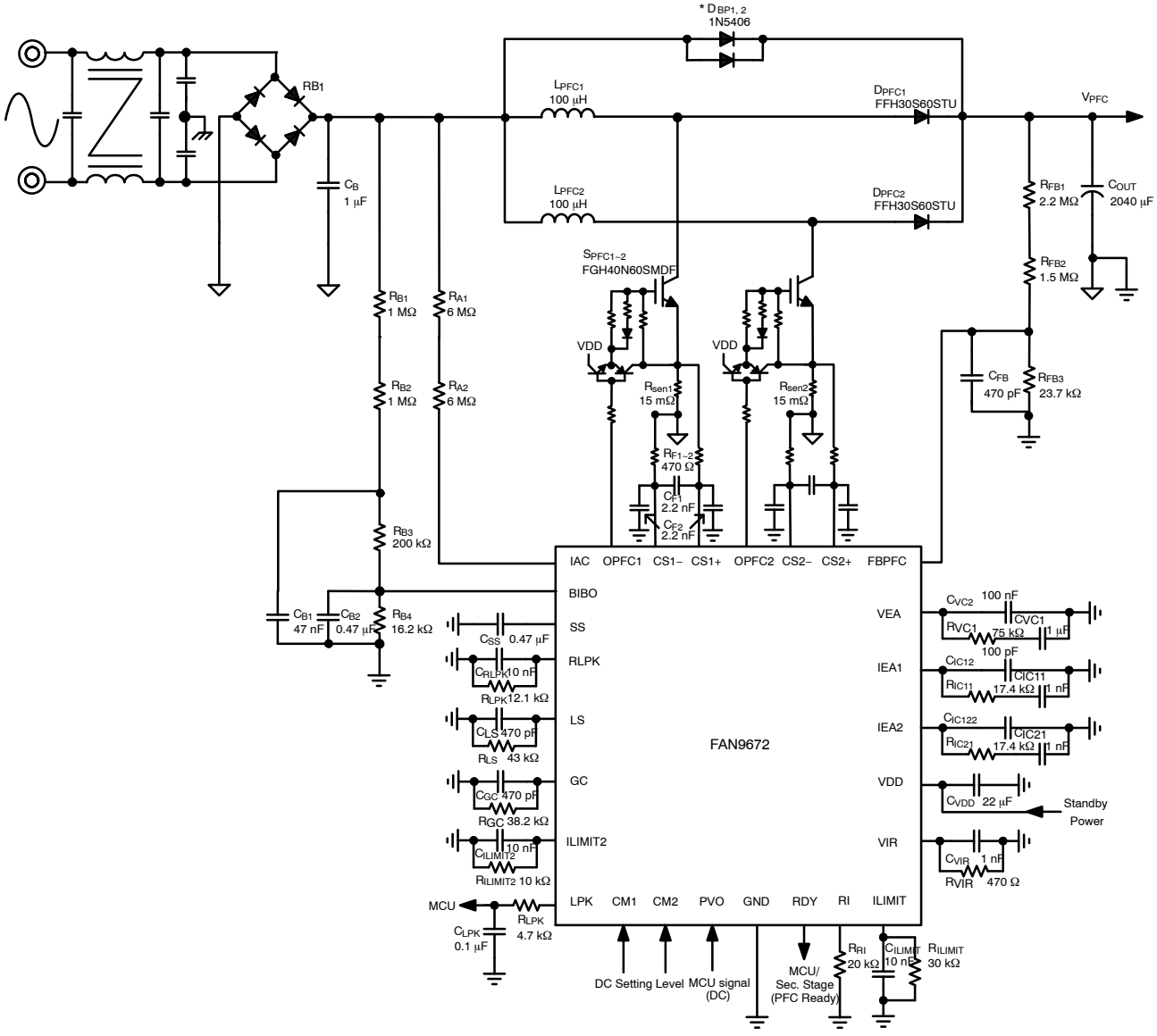


Figure 52. Schematic of Design Example

Specification

- V_{DD} Maximum Rating: 20 V
- V_{DD} OVP: 24 V
- V_{CC} UVLO: 10.3 V/12.8 V
- PVO: 0 V ~ 1 V
- PFC Soft−Start: C_{SS} = 0.47 μF
- Brown−In/Out: 170 V/160 V
- Switching Frequency: 40 kHz
- V_{FBPFC} for RDY: 2.4 V/1.55 V (96% / 62%)
- R_{IAC}: 12 MΩ

Inductor Schematic Diagram

- Switching Frequency: 40 kHz
- Bobbin: 7 Pins

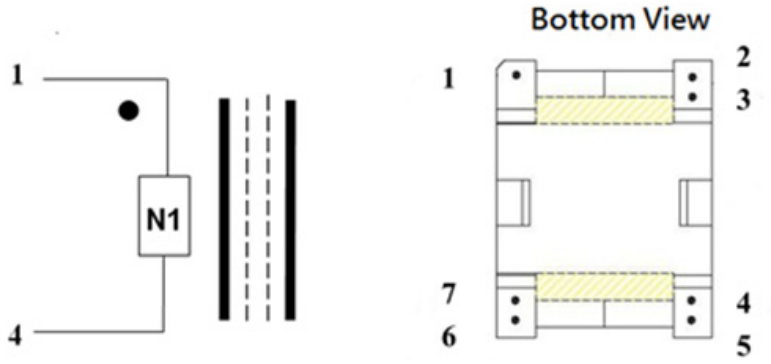


Figure 53. Inductor Schematic Diagram

Table 6. WINDING SPECIFICATION

No.	Winding	Pin (S → F)	Wire	Turns	Winding Method
1	N1	1 → 6, 7	0.2ϕ × 35 *1	25	Solenoid Winding
2	Insulation: Polyester Tape t = 0.025 mm, 2 Layer				
3	Copper−Foil 1.2T to PIN4, 5				

Table 7. MOSFET AND DIODE REFERENCE SPECIFICATION

IGBT's	
Voltage Rating	
600 V (IGBT)	FGH40N60SMDF
Boost Diodes	
600 V	FFH30S60STU

Typical Performance

Table 8. EFFICIENCY

	25% Load	50% Load	75% Load	100% Load
180 V/50 Hz	96.31	96.93	96.60	96.41
220 V/50 Hz	97.01	97.34	97.33	97.17
264 V/50 Hz	97.76	97.92	97.92	97.77

Table 9. POWER FACTOR

	25% Load	50% Load	75% Load	100% Load
180 V/50 Hz	0.9546	0.9856	0.9917	0.9955
220 V/50 Hz	0.9397	0.9694	0.9780	0.9879
264 V/50 Hz	0.8402	0.9158	0.9337	0.9500

Table 10. TOTAL HARMONIC DISTORTION

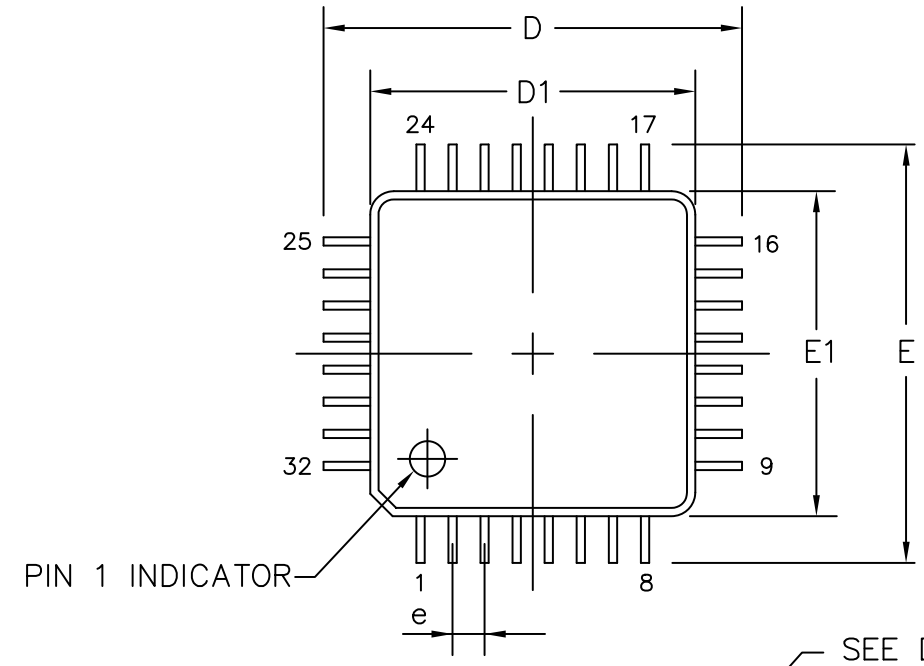
	25% Load	50% Load	75% Load	100% Load
180 V/50 Hz	14.51	10.98	8.87	6.96
220 V/50 Hz	20.12	17.24	15.30	11.87
264 V/50 Hz	50.52	36.86	33.11	29.26

System Design Precautions

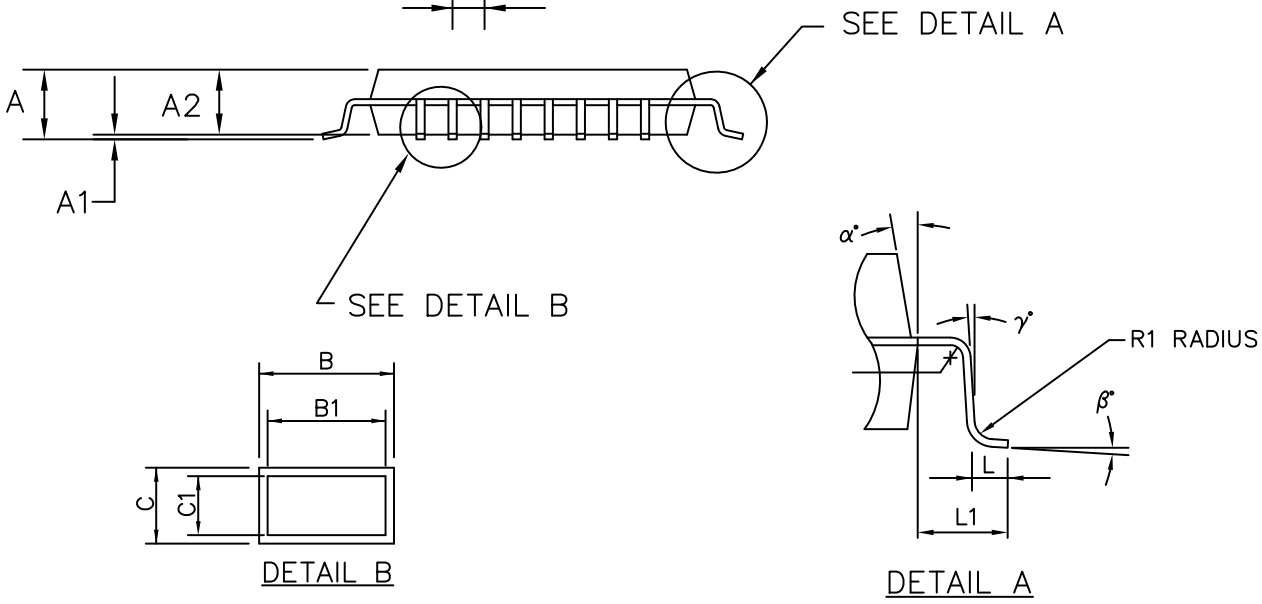
- Pay attention to the inrush current when AC input is first connected to the boost PFC convertor. It is recommended to use NTC and a parallel connected relay circuit to reduce inrush current.
- Add bypass diode to provide a path for inrush current when PFC start up.
- The PFC stage is normally used to provide power to a downstream DC−DC or inverter. It's recommend that downstream power stage is enabled to operate at full load once the PFC output voltage has reaches a level close to the specified steady−state value.
- The PVO function is used to change the output voltage of PFC, V_{PFC}. The V_{PFC} should be kept at least 25 V higher than V_{IN}.

LQFP−32, 7x7
CASE 561AB−01
ISSUE O

DATE 19 JUN 2008



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
B	0.30	0.37	0.45
B1	0.30	0.35	0.40
C	0.09	–	0.20
C1	0.09	–	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00		
R1	0.08	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–



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