









DRV8889-Q1

SLVSEE9B - JANUARY 2020 - REVISED JANUARY 2020

DRV8889-Q1 Automotive Stepper Driver with Integrated Current Sense, 1/256 Micro-Stepping, and Stall Detection

Technical

1 Features

- AEC-Q100 Qualified for Automotive
- Up to 1/256 microstepping
- Integrated current sense functionality No sense resistors required
- Smart tune decay technology, Fixed slow, and mixed decay options
- 4.5 to 45-V Operating supply voltage range
- Low R_{DS(ON)}: 900 mΩ HS + LS at 13.5 V, 25°C
- High current capacity per bridge
 - 2.4-A peak, 1.5-A full-scale, 1.1-A rms
- TRQ DAC bits to scale full-scale current
- Configurable off-time PWM chopping
 - 7-μs, 16-μs, 24-μs, or 32-μs.
- Simple STEP/DIR interface
- SPI with daisy chain support
- Low-current sleep mode (2 μ A)
- Programmable output slew rate
- Spread spectrum clocking to minimize EMI
- Protection features
 - VM undervoltage lockout
 - Overcurrent protection
 - Stall detection
 - _ Open load detection
 - Overtemperature warning and shutdown
 - Undertemperature warning
 - Fault condition indication pin (nFAULT) _

2 Applications

- Automotive bipolar stepper motors
- Headlight position adjustment
- Head-up display (HUD)
- **HVAC** stepper motors
- Electronic fuel injection (EFI)

3 Description

The DRV8889-Q1 is a fully integrated stepper motor driver, supporting up to 1.5 A full scale current with an internal microstepping indexer, smart tune decay technology, advanced stall detection algorithm, and integrated current sensing.

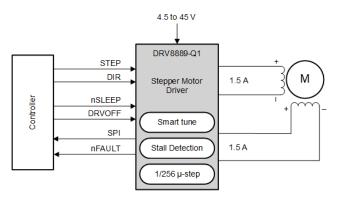
With a simple step/dir interface to manage the direction and step rate, DRV8889-Q1 supports up to 1/256 levels of microstepping to enable a smooth motion profile. Integrated current sensing eliminates the need for two external resistors, saving board space and cost. With advanced stall detection algorithm, designers can detect if the motor stopped and take action as needed which can improve efficiency and reduce noise. DRV8889-Q1 provides 8 decay mode options including: smart tune, slow, and mixed decay options. Smart tune automatically adjusts for optimal current regulation performance and compensates for any motor variation and aging effects. The device also includes an integrated torque DAC which allows for the controller to scale the output current through SPI without needing to scale the VREF voltage reference. A low-power sleep mode is provided for very low standby current using an nSLEEP pin. The device features full duplex, 4-wire synchronous SPI communication, with daisy chain support for up to 63 devices connected in series, for configurability and detailed fault reporting.

View our full portfolio of stepper motor drivers on ti.com

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8889QPWPRQ1	HTSSOP (24)	7.80 mm × 4.40 mm
DRV8889QWRGERQ1	VQFN (24) (Wettable Flank)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



Copyright © 2020, Texas Instruments Incorporated

Table of Contents

1	Feat	tures 1
2	Арр	lications 1
3	Des	cription1
4	Rev	ision History2
5	Pin	Configuration and Functions 3
6	Spe	cifications
	6.1	Absolute Maximum Ratings 5
	6.2	ESD Ratings 5
	6.3	Recommended Operating Conditions 6
	6.4	Thermal Information 6
	6.5	Electrical Characteristics7
	6.6	SPI Timing Requirements 9
	6.7	Indexer Timing Requirements 10
	6.8	Typical Characteristics 11
7	Deta	ailed Description 13
	7.1	Overview 13
	7.2	Functional Block Diagram 14
	7.3	Feature Description 15
	7.4	Device Functional Modes

	7.5	Programming	38
	7.6	Register Maps	13
8	App	lication and Implementation5	51
	8.1	Application Information	51
	8.2	Typical Application	51
9	Pow	er Supply Recommendations6	33
		Bulk Capacitance	
10		out	
	10.1	Layout Guidelines6	34
	10.2	Layout Example6	35
11	Dev	ice and Documentation Support6	57
	11.1		
	11.2	Receiving Notification of Documentation Updates	37
	11.3	Community Resources	37
	11.4	Trademarks6	37
	11.5	Electrostatic Discharge Caution	37
	11.6	Glossary6	37
12	Mec	hanical, Packaging, and Orderable	
	Info	rmation6	38

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision A (December 2019) to Revision B	Page
•	Changed R-C time constant for low-pass filter in Controlling VREF with an MCU DAC	19
•	Added table to Disable Mode (nSLEEP = 1, DRVOFF = 1)	37
•	Added new scope shot to Application Curves	54
•	Added data on thermal parameters in Thermal Parameters for HTSSOP Package	58

Changes from Original (November 2019) to Revision A

•	Changed Device status to Production Data		1
---	------------------------------------------	--	---

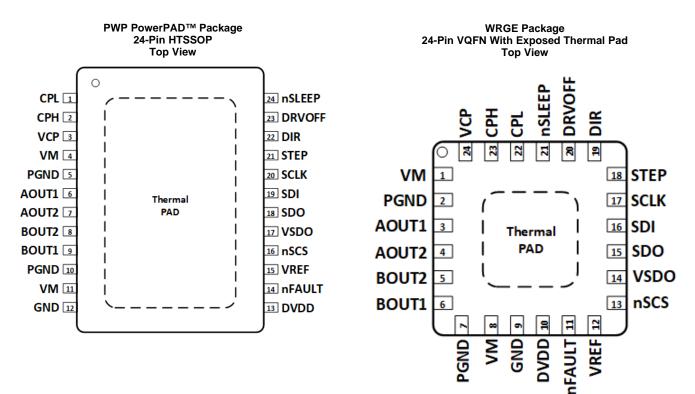
TEXAS INSTRUMENTS

www.ti.com

Page



5 Pin Configuration and Functions



Pin Functions

PIN						
NAME	N	10.	I/O	TYPE	DESCRIPTION	
NAME	HTSSOP	VQFN				
AOUT1	6	3	0	Output	Winding A output. Connect to stepper motor winding.	
AOUT2	7	4	0	Output	Winding A output. Connect to stepper motor winding.	
PGND	5, 10	2, 7	_	Power	Power ground. Both PGND pins are shorted internally. Connect to system ground on PCB.	
BOUT1	9	6	0	Output	Winding B output. Connect to stepper motor winding	
BOUT2	8	5	0	Output	Winding B output. Connect to stepper motor winding	
CPH	2	23		Power	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic	
CPL	1	22		Fower	capacitor from CPH to CPL.	
DIR	22	19	I	Input	Direction input. Logic level sets the direction of stepping; internal pulldown resistor.	
DRVOFF	23	20	I	Input	Logic high to disable device outputs; logic low to enable; internal pullup to DVDD.	
DVDD	13	10		Power	Logic supply voltage. Connect a X7R, 0.47-µF, 6.3-V or 10-V rated ceramic capacitor to GND.	
GND	12	9		Power	Device ground. Connect to system ground.	
VREF	15	12	I	Input	Current set reference input. Maximum value 3.3 V. DVDD can be used to provide VREF through a resistor divider.	
SCLK	20	17	I	Input	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.	
SDI	19	16	I	Input	Serial data input. Data is captured on the falling edge of the SCLK pin	
SDO	18	15	0	Push Pull	Serial data output. Data is shifted out on the rising edge of the SCLK pin.	
STEP	21	18	I	Input	Step input. A rising edge causes the indexer to advance one step; internal pulldown resistor.	

Copyright © 2020, Texas Instruments Incorporated

DRV8889-Q1 SLVSEE9B – JANUARY 2020 – REVISED JANUARY 2020

www.ti.com

NSTRUMENTS

Texas

Pin Functions (continued)

PIN						
	NO.		I/O	TYPE	DESCRIPTION	
NAME	HTSSOP	VQFN				
VCP	3	24		Power	Charge pump output. Connect a X7R, 0.22- μ F, 16-V ceramic capacitor to VM.	
VM	4, 11	1, 8	_	Power	Power supply. Connect to motor supply voltage and bypass to GND with two 0.01 - μ F ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.	
VSDO	VSDO 17 14			Power	Supply pin for SDO output. Connect to 5-V or 3.3-V depending on the desired logic level.	
nFAULT	14	11	0	Open Drain	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.	
nSCS	16	13	I	Input	Serial chip select. An active low on this pin enables the serial interface communications. Internal pullup to DVDD.	
nSLEEP	24	21	I	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.	
PAD		-	-	Thermal pad. Connect to system ground.		



DRV8889-Q1 SLVSEE9B – JANUARY 2020 – REVISED JANUARY 2020

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Power supply voltage (VM)	-0.3	50	V
Charge pump voltage (VCP, CPH)	-0.3	VM + 7	V
Charge pump negative switching pin (CPL)	-0.3	VM	V
Charge pump negative switching pin (nSLEEP)	-0.3	VM	V
Internal regulator voltage (DVDD)	-0.3	5.75	V
SDO output reference voltage (VSDO)	-0.3	5.75	V
Control pin voltage (STEP, DIR, DRVOFF, nFAULT, SDI, SDO, SCLK, nSCS)	-0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	-0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	-1.0	VM + 1.0	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	-3.0	VM + 3.0	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internal	ly Limited	А
Operating ambient temperature, T _A	-40	125	°C
Operating junction temperature, T _J	-40	150	°C
Storage temperature, T _{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
V(FOD)		Human body model (HBM), per AEC Q100–002 ⁽¹⁾		±2000	
	Electrostatic discharge		Corner pins for PWP (1, 12, 13, and 24)	±750	V
			Other pins	±500	

(1) AECQ100–002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS–001specification.

SLVSEE9B-JANUARY 2020-REVISED JANUARY 2020

www.ti.com

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	45	V
VI	Logic level input voltage	0	5.5	V
V _{SDO}	SDO buffer supply voltage	2.9	5.5	V
V _{VREF}	VREF voltage	0.05	3.3	V
f_{STEP}	Applied STEP signal (STEP)	0	100 ⁽¹⁾	kHz
I _{FS}	Motor full-scale current (xOUTx)	0	1.5 ⁽²⁾	А
I _{rms}	Motor RMS current (xOUTx)	0	1.1 ⁽²⁾	А
T _A	Operating ambient temperature	-40	125	°C
TJ	Operating junction temperature	-40	150	°C

STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load Power dissipation and thermal limits must be observed (1)

(2)

6.4 Thermal Information

		DRV88	DRV8889-Q1			
	THERMAL METRIC ⁽¹⁾	PWP (HTSSOP)	RGE (VQFN)	UNIT		
		24 PINS	24 PINS			
R_{\thetaJA}	Junction-to-ambient thermal resistance	30.9	40.7	°C/W		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	25.2	31.1	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	17.9	°C/W		
ΨJT	Junction-to-top characterization parameter	0.4	0.6	°C/W		
ΨJB	Junction-to-board characterization parameter	11.3	17.8	°C/W		
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	3.1	4.3	°C/W		

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
POWER S	UPPLIES (VM, DVDD, VSDO)	· · ·				
I _{VM}	VM operating supply current	DRVOFF = 0, nSLEEP = 1, No output		5	7	mA
I _{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	μA
t _{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	75			μs
t _{RESET}	nSLEEP reset pulse	nSLEEP low to only clear fault registers	18		35	μS
t _{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.6	0.9	ms
t _{ON}	Turn-on time	VM > UVLO to output transition		0.6	0.9	ms
V _{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 45 V	4.5	5	5.5	V
	PUMP (VCP, CPH, CPL)					
V _{VCP}	VCP operating voltage			VM + 5		V
f _(VCP)	Charge pump switching frequency	V _{VM} > UVLO; nSLEEP = 1		400		kHz
LOGIC-LE	VEL INPUTS (STEP, DIR, nSLEEI	P, nSCS, SCLK, SDI, DRVOFF)				
V _{IL}	Input logic-low voltage		0		0.6	V
V _{IH}	Input logic-high voltage		1.5		5.5	V
V _{HYS}	Input logic hysteresis			150		mV
I _{IL1}	Input logic-low current	VIN = 0 V (nSCS, DRVOFF)	8		12	μA
I _{IL2}	Input logic-low current	VIN = 0 V	-1		1	μA
I _{IH1}	Input logic-high current	VIN = DVDD (nSCS, DRVOFF)			500	nA
I _{IH2}	Input logic-high current	VIN = 5 V			50	μA
PUSH-PUL	L OUTPUT (SDO)					
R _{PD,SDO}	Internal pull-down resistance	5mA load, with respect to GND		40	75	Ω
R _{PU,SDO}	Internal pull-up resistance	5mA load, with respect to VSDO		30	60	Ω
I _{SDO}	SDO Leakage Current	SDO = VSDO and 0V	-1		1	μA
CONTROL	OUTPUTS (nFAULT)					
V _{OL}	Output logic-low voltage	I _O = 5 mA			0.4	V
I _{OH}	Output logic-high leakage	V _{VM} = 13.5 V	-1		1	μA

SLVSEE9B – JANUARY 2020 – REVISED JANUARY 2020

NSTRUMENTS

Texas

www.ti.com

Electrical Characteristics (continued)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DR	RIVER OUTPUTS (AOUT1, AOUT	2, BOUT1, BOUT2)				
		VM = 13.5 V, T _J = 25°C, I _O = -1 A		450	550	mΩ
R _{DS(ONH)}	High-side FET on resistance	VM = 13.5 V, T _J = 125°C, I _O = -1 A		700	850	mΩ
· · /		VM = 13.5 V, T _J = 150°C, I _O = -1 A	C, I _O = -1 A 780		950	mΩ
		VM = 13.5 V, T _J = 25°C, I _O = 1 A		450	550	mΩ
R _{DS(ONL)}	Low-side FET on resistance	VM = 13.5 V, T _J = 125°C, I _O = 1 A		700	850	mΩ
. ,		VM = 13.5 V, T _J = 150°C, I _O = 1 A	780 950		950	mΩ
		SR = 00b, VM = 13.5 V, I _O = 0.5 A		10		
		SR = 01b, VM = 13.5 V, I _O = 0.5 A		35		
t _{SR}	Output slew rate	SR = 10b, VM = 13.5 V, I _O = 0.5 A		50		V/µs
		SR = 11b, VM = 13.5 V, I _O = 0.5 A		105		
	RENT CONTROL (VREF)				I	
K _V	Transimpedance gain			2.2		V/A
<u>.</u>		TOFF = 00b		7		
		TOFF = 01b		16		
t _{OFF}	PWM off-time	TOFF = 10b		24		μS
		TOFF = 11b		32		
		I _O = 1.5 A, 10% to 20% current setting	-13		10	%
ΔI_{TRIP}	Current trip accuracy $I_0 = 1.5 \text{ A}, 20\%$	I _O = 1.5 A, 20% to 67% current setting	-8		8	
		$L_{0} = 1.5 \text{ A} 67\% \text{ to } 100\% \text{ current}$	-7.5		7.5	
I _{O,CH}	AOUT and BOUT current matching	I _O = 1.5 A	-2.5		2.5	%
PROTECTI	ON CIRCUITS	1				
		VM falling, UVLO falling	4.15	4.25	4.35	
V _{UVLO}	VM UVLO lockout	VM rising, UVLO rising	4.25	4.35	4.45	V
V _{UVLO,HYS}	Undervoltage hysteresis	Rising to falling threshold		100		mV
V _{RST}	VM UVLO reset	VM falling, device reset, no SPI communications			3.9	V
V _{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		VM + 2		V
OCP	Overcurrent protection	Current through any FET	2.4			А
	·	V _{VM} < 37 V		3		
t _{OCP}	Overcurrent deglitch time	V _{VM} ≥ 37 V		0.5		μS
t _{RETRY}	Overcurrent retry time	OCP_MODE = 1b		4		ms
t _{OL}	Open load detection time	EN_OL = 1b			200	ms
	Open load current threshold			30		mA
T _{OTW}	Overtemperature warning	Die temperature T _J	135	150	165	°C
T _{UTW}	Undertemperature warning	Die temperature T ₁	-25	-10	5	°C
T _{OTSD}	Thermal shutdown	Die temperature T_1	150	165	180	°C
T _{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_{ij}		20		°C
T _{HYS_OTW}	Overtemperature warning hysteresis	Die temperature T _J		20		°C
T _{HYS_UTW}	Undertemperature warning hysteresis	Die temperature T _J		10		°C

6.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t _(READY)	SPI ready, VM > V _{RST}		1		ms
t _(CLK)	SCLK minimum period	100			ns
t _(CLKH)	SCLK minimum high time	50			ns
t _(CLKL)	SCLK minimum low time	50			ns
t _{su(SDI)}	SDI input setup time	20			ns
t _{h(SDI)}	SDI input hold time	30			ns
t _{d(SDO)}	SDO output delay time, SCLK high to SDO valid, $C_L = 20 \text{ pF}$			30	ns
t _{su(nSCS)}	nSCS input setup time	50			ns
t _{h(nSCS)}	nSCS input hold time	50			ns
t _(HI_nSCS)	nSCS minimum high time before active low			2	μs
t _{dis(nSCS)}	nSCS disable time, nSCS high to SDO high impedance		10		ns

SLVSEE9B-JANUARY 2020-REVISED JANUARY 2020

www.ti.com

ISTRUMENTS

ÈXAS

6.7 Indexer Timing Requirements

NO.			MIN	MAX	UNIT
1	f _{step}	Step frequency		500 ⁽¹⁾	kHz
2	t _{WH(STEP)}	Pulse duration, STEP high	970		ns
3	t _{WL(STEP)}	Pulse duration, STEP low	970		ns
4	t _{SU(DIR, Mx)}	Setup time, DIR to STEP rising	200		ns
5	t _{H(DIR, Mx)}	Hold time, DIR to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth islimited by the motor load.

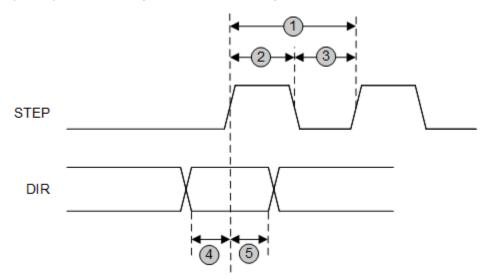


Figure 1. STEP and DIR Timing Diagram

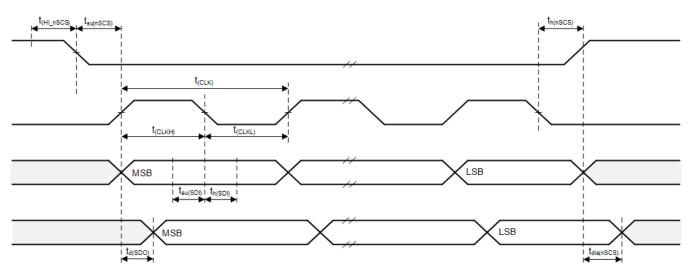
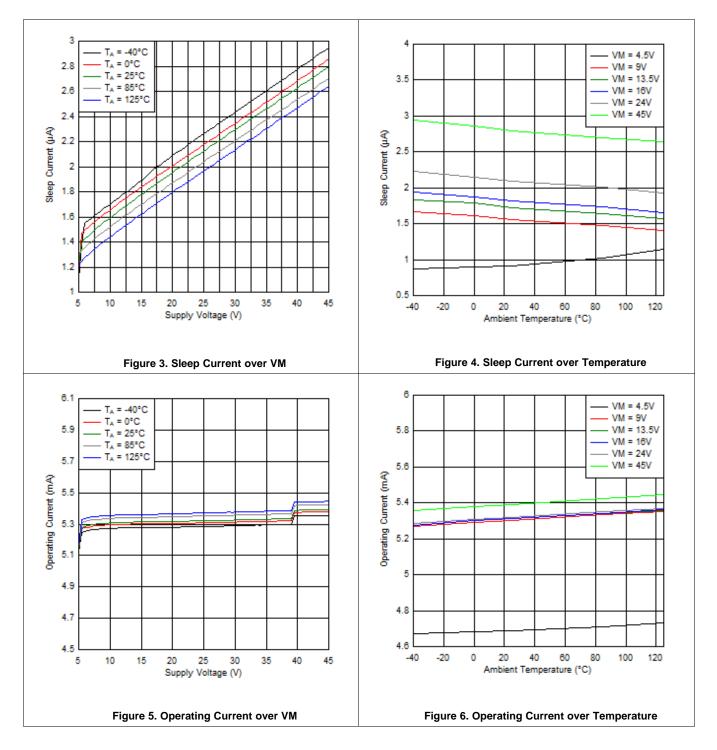


Figure 2. SPI Slave-Mode Timing Definition



6.8 Typical Characteristics

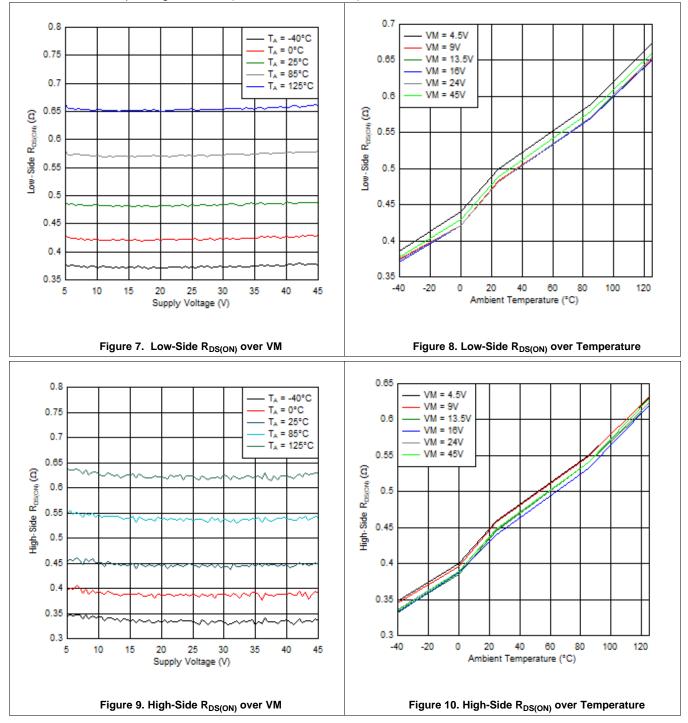
Over recommended operating conditions (unless otherwise noted)





Typical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted)





7 Detailed Description

7.1 Overview

The DRV8889-Q1 device is an integrated motor-driver solution for bipolar stepper motors. The device integrates two N-channel power MOSFET H-bridges, integrated current sense and regulation circuitry, and a microstepping indexer. The DRV8889-Q1 device can be powered with a supply voltage from 4.5 to 45 V and is capable of providing an output current up to 2.4-A peak, 1.5-A full-scale, or 1.1-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The device uses an integrated current-sense architecture which eliminates the need for two external power sense resistors. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREF pin. These features reduces external component cost, board PCB size, and system power consumption.

A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal indexer can execute high-accuracy microstepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128 and 1/256 microstepping. In addition to a standard half stepping mode, a noncircular half stepping mode is available for increased torque output at higher motor RPM.

The current regulation is configurable between several decay modes. The decay mode can be selected as a slow-mixed, mixed decay, smart tune Ripple Control, or smart tune Dynamic Decay current regulation scheme. The slow-mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps. The smart tune decay modes automatically adjust for optimal current regulation performance and compensate for motor variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic decay percentage scheme to minimize distortion of the motor winding current. In smart tune Ripple Control mode, the device can detect a motor overload stall condition or an end-of-line travel, by detecting back-emf phase shift between rising and falling current quadrants of the motor current.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature combined with output slew rate control minimizes the radiated emissions from the device.

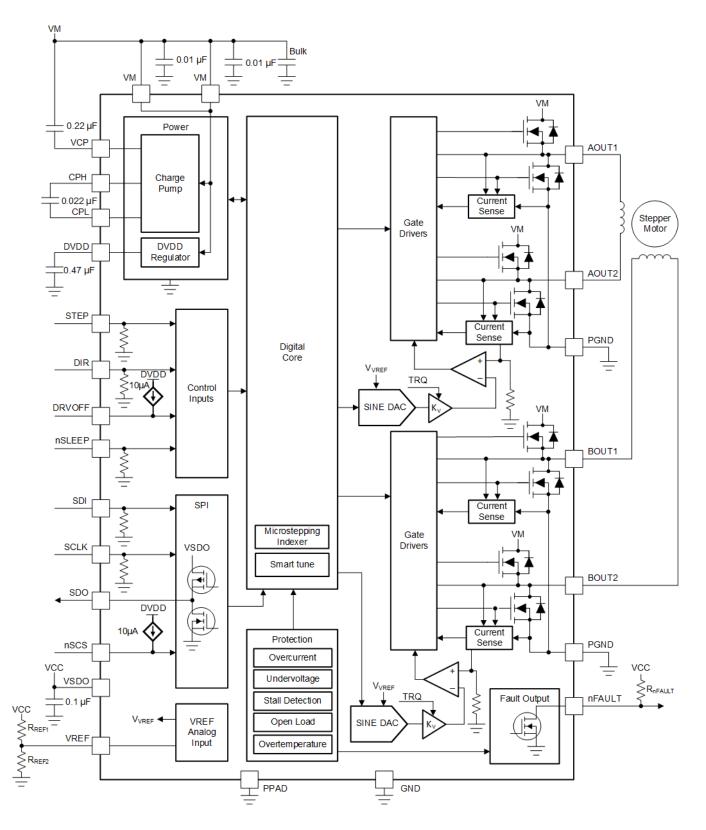
A torque DAC feature allows the controller to scale the output current without needing to scale the VREF voltage reference. The torque DAC is accessed using a digital input pin which allows the controller to save system power by decreasing the motor current consumption when high output torque is not required.

A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

TEXAS INSTRUMENTS

www.ti.com

7.2 Functional Block Diagram





7.3 Feature Description

Table 1 lists the recommended external components for the DRV8889-Q1 device.

COMPONENT	PIN 1	PIN 2	RECOMMENDED		
C _{VM1}	VM	GND	Two X7R, 0.01-µF, VM-rated ceramic capacitors		
C _{VM2}	VM	GND	Bulk, VM-rated capacitor		
C _{VCP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor		
C _{SW}	СРН	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor		
C _{DVDD}	DVDD	GND	X7R, 0.47-μF to 1-μF, 6.3-V ceramic capacitor		
R _{nFAULT}	VCC ⁽¹⁾	nFAULT	>4.7-kΩ resistor		
R _{REF1}	VREF	VCC	Resistor to limit chopping current. It is recommended that the value of parallel		
R _{REF2} (Optional)	VREF	GND	combination of R_{REF1} and R_{REF2} should be less than 50-k Ω .		

Table 1. DRV8889-Q1 External Components

(1) VCC is not a pin on the DRV8889-Q1 device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD

7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, rms, and full-scale.

7.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP} . The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver.

For the DRV8889-Q1 device, the peak current rating is 2.4 A per bridge.

7.3.1.2 rms Current Rating

The rms (average) current is determined by the thermal considerations of the IC. The rms current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating rms current may be higher or lower depending on heatsinking and ambient temperature.

For the DRV8889-Q1 device, the rms current rating is 1.1 A per bridge.

7.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the rms current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$.

For the DRV8889-Q1 device, the full-scale current rating is 1.5 A per bridge.

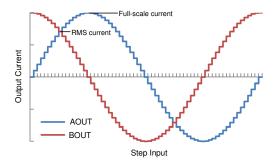


Figure 11. Full-Scale and RMS Current

SLVSEE9B - JANUARY 2020 - REVISED JANUARY 2020

7.3.2 PWM Motor Drivers

The device has drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 12 shows a block diagram of the circuitry.

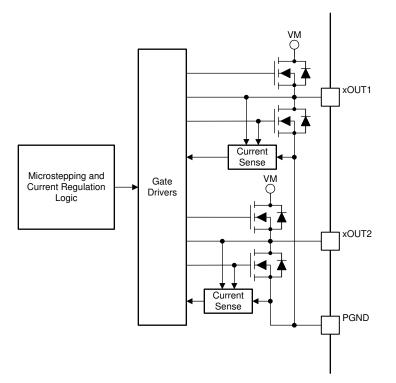


Figure 12. PWM Motor Driver Block Diagram

7.3.3 Microstepping Indexer

Built-in indexer logic in the device allows a number of different step modes. The MICROSTEP_MODE bits in the SPI register are used to configure the step mode as shown in Table 2.

MICROSTEP_MODE	STEP MODE					
0000b	Full step (2-phase excitation) with 100% current					
0001b Full step (2-phase excitation) with 71% cur						
0010b	Non-circular 1/2 step					
0011b	1/2 step					
0100b	1/4 step					
0101b	1/8 step					
0110b	1/16 step					
0111b	1/32 step					
1000b	1/64 step					
1001b	1/128 step					
1010b	1/256 step					



Table 3 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table. The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

NOTE

If the step mode is changed on the fly while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP.

NOTE

While DIR = 0 and the electrical angle is at a full step angle (45, 135, 225, or 315 degrees), two rising edge pulses on the STEP pin are required in order to advance the indexer after changing from any microstep mode to the full step mode. The first pulse will induce no change in the electrical angle, the second pulse will move the indexer to the next full step angle.

The home state is an electrical angle of 45°. This state is entered after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0	100	0
2				20	98	11
3	2			38	92	23
4				56	83	34
5	3	2	1	71	71	45
6				83	56	56
7	4			92	38	68
8				98	20	79
9	5	3		100	0	90
10				98	-20	101
11	6			92	-38	113
12				83	-56	124
13	7	4	2	71	-71	135
14				56	-83	146
15	8			38	-92	158
16				20	-98	169
17	9	5		0	-100	180
18				-20	-98	191
19	10			-38	-92	203
20				-56	-83	214
21	11	6	3	-71	-71	225
22				-83	-56	236
23	12			-92	-38	248
24				-98	-20	259
25	13	7		-100	0	270
26				-98	20	281

Table 3. Relative Current and Step Directions

Table 3. Relative Current and Step Directions (co	ontinued)
---------------------------------------------------	-----------

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
27	14			-92	38	293
28				-83	56	304
29	15	8	4	-71	71	315
30				-56	83	326
31	16			-38	92	338
32				-20	98	349

Table 4 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

Table 4. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)	
1	100	100	45	
2	-100	100	135	
3	-100	-100	225	
4	100	-100	315	

Table 5 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)			
0	100	0			
100	100	45			
100	0	90			
100	-100	135			
0 –100		180			
-100	-100	225			
-100 0		270			
-100	100	315			
	(% FULL-SCALE) 0 100 100 100 0 -100 -100	(% FULL-SCALE) (% FULL-SCALE) 0 100 100 100 100 0 100 0 100 -100 0 -100 -100 -100 -100 0			

7.3.4 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC should not rise above 3.3 V.



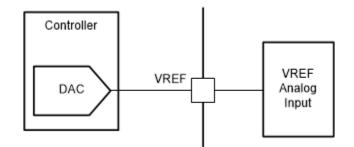


Figure 13. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter. The R-C time constant for the low-pass filter should be longer than 10 times the period of the PWM signal.

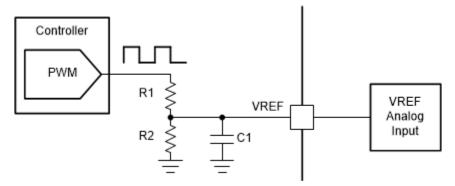


Figure 14. Controlling VREF With a PWM Resource



7.3.5 Current Regulation

The current through the motor windings is regulated by a PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the TOFF register setting and the selected decay mode to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

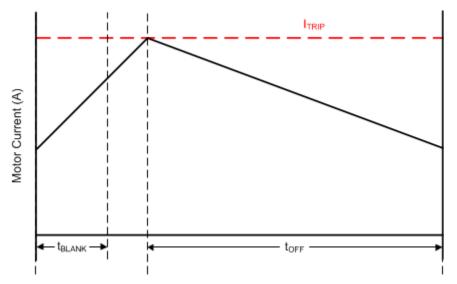


Figure 15. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin. In addition, the TRQ_DAC register can further scale the reference current.

Use Equation 1 to calculate the full-scale regulation current.

$$I_{FS}(A) = \frac{V_{REF}(V)}{K_{V}(V/A)} \times TRQ_{DAC}(\%) = \frac{V_{REF}(V) \times TRQ_{DAC}(\%)}{2.2(V/A)}$$
(1)

The TRQ_DAC is adjusted via the SPI register. Table 6 lists the current scalar value for different inputs.

TRQ_DAC	CURRENT SCALAR (TRQ)			
0000b	100%			
0001b	93.75%			
0010b	87.5%			
0011b	81.25%			
0100b	75%			
0101b	68.75%			
0110b	62.5			
0111b	56.25%			
1000b	50%			
1001b	43.75%			
1010b	37.5%			
1011b	31.25%			

Table 6. Torque DAC Settings



TRQ_DAC	CURRENT SCALAR (TRQ)		
1100b	25%		
1101b	18.75%		
1110b	12.5%		
1111b	6.25%		

Table 6. Torque DAC Settings (continued)



7.3.6 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 16, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. The opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 16, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 16, Item 3.

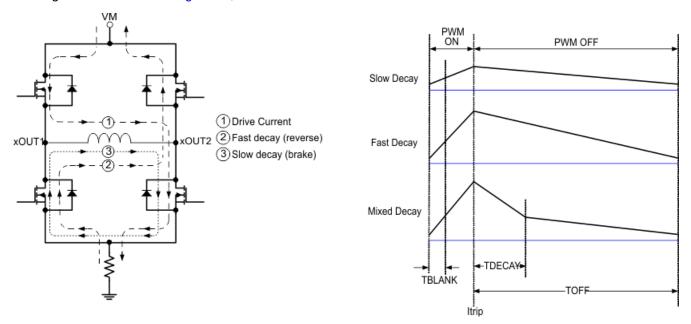


Figure 16. Decay Modes

The decay mode is selected by the DECAY register as shown in Table 7.

DECAY	INCREASING STEPS	DECREASING STEPS				
000b	Slow decay	Slow decay				
001b	Slow decay	Mixed decay: 30% fast				
010b	Slow decay	Mixed decay: 60% fast				
011b	Slow decay	Fast decay				
100b	Mixed decay: 30% fast	Mixed decay: 30% fast				
101b	Mixed decay: 60% fast	Mixed decay: 60% fast				
110b	Smart tune Dynamic Decay	Smart tune Dynamic Decay				
111b (default)	Smart tune Ripple Control	Smart tune Ripple Control				

Table	7.	Decav	Mode	Settings
I GANIG		Doouy	mouo	ooungo



Figure 17 defines increasing and decreasing current. For the slow-mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full step and noncircular 1/2-step operation, the decay mode corresponding to decreasing steps is always used.

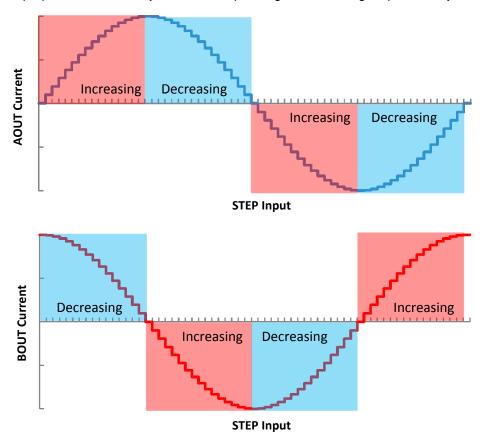


Figure 17. Definition of Increasing and Decreasing Steps



7.3.6.1 Slow Decay for Increasing and Decreasing Current

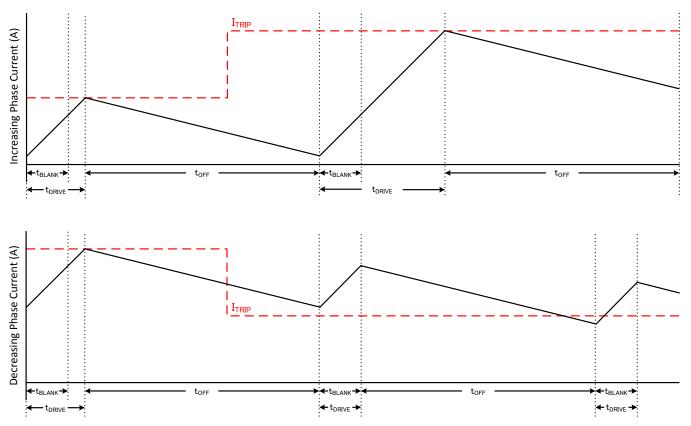


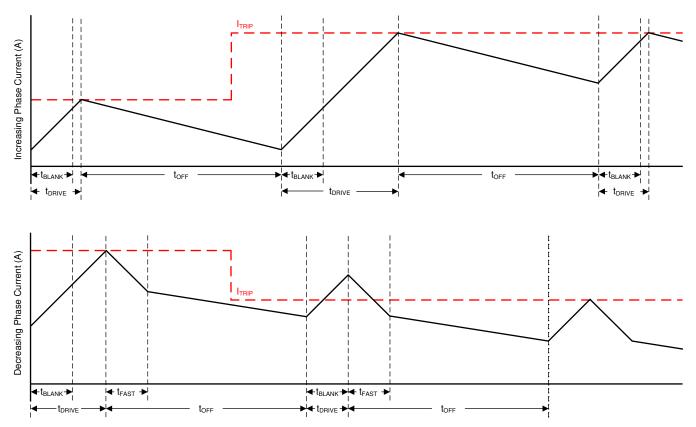
Figure 18. Slow/Slow Decay Mode

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF} . However on decreasing current steps, slow decay will take a long time to settle to the new I_{TRIP} level because the current decreases very slowly. If the current at the end of the off time is above the ITRIP level, slow decay will be extended for another off time duration and so on, till the current at the end of the off time is below ITRIP level.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and may require a large off-time. In some cases this may cause a loss of current regulation, and a more aggressive decay mode is recommended.





7.3.6.2 Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

Figure 19. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of the t_{OFF} time. In this mode, mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This mode exhibits the same current ripple as slow decay for increasing current, because for increasing current, only slow decay is used. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

t_{BLANK}→

26

t_{DRIVE}

 $t_{\cap F}$



Please note that these graphs are not the same scale; t_{OFF} is the same

7.3.6.3 Mode 4: Slow Decay for Increasing Current, Fast Decay for Decreasing current

Figure 20. Slow/Fast Decay Mode

tore

. ←t_{BLANK}

← t_{DRIVE} →

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction. In this mode, fast decay only occurs during decreasing current. Slow decay is used for increasing current.

Fast decay exhibits the highest current ripple of the decay modes for a given t_{OFF}. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

Product Folder Links: DRV8889-Q1

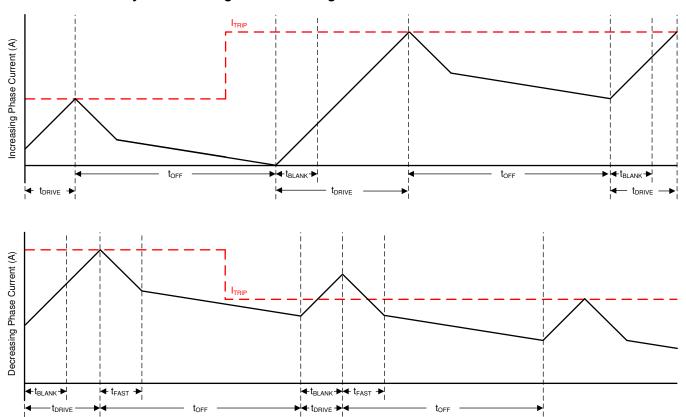


t_{bl ank}

← t_{DRIVE} →

www.ti.com





7.3.6.4 Mixed Decay for Increasing and Decreasing Current

Figure 21. Mixed-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF}. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing or decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

SLVSEE9B - JANUARY 2020 - REVISED JANUARY 2020



7.3.6.5 Smart tune Dynamic Decay

The smart tune current regulation schemes are advanced current-regulation control methods compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dl/dt

The device provides two different smart tune current regulation modes, named smart tune Dynamic Decay and smart tune Ripple Control.

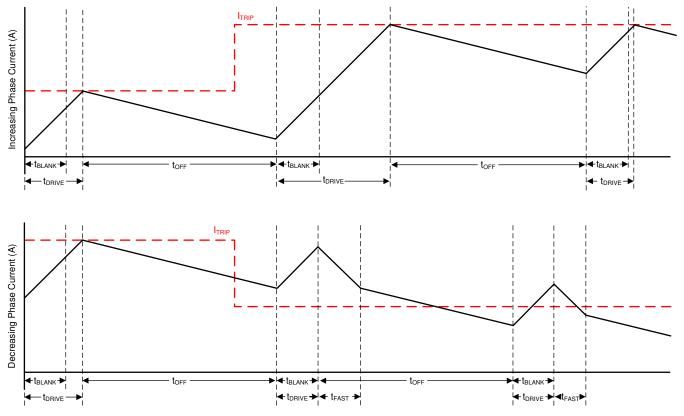


Figure 22. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.



7.3.6.6 Smart tune Ripple Control

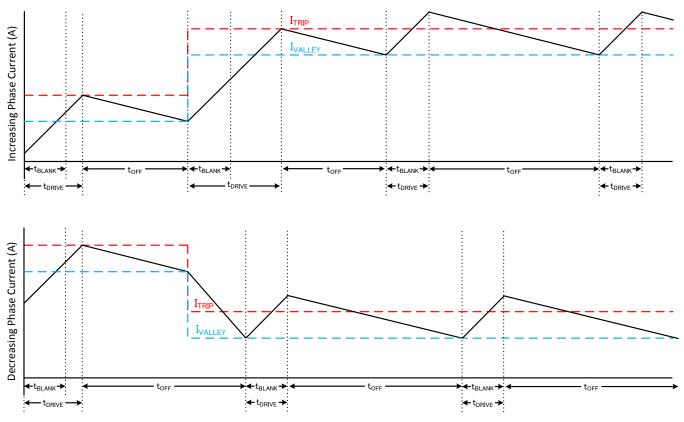


Figure 23. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP} , instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

This method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation.



7.3.7 Blanking Time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. When the device goes into a drive phase at the end of a slow-decay phase, the blanking time is roughly 500 ns. If the device goes into drive phase at the end of a fast-decay phase, the approximate blanking time is as shown in the following table -

SLEW_RATE	Blanking Time (t _{BLANK})		
00b	5.6 µs		
01b	2 µs		
10b	1.5 µs		
11b	860 ns		

Table 8. Blanking Time

7.3.8 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

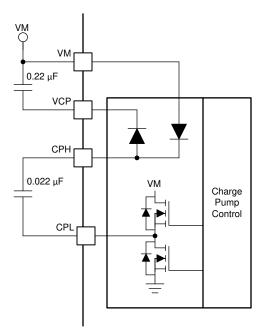


Figure 24. Charge Pump Block Diagram



7.3.9 Linear Voltage Regulators

A linear voltage regulator is integrated into the device. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2 mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2 mA, the output voltage drops significantly.

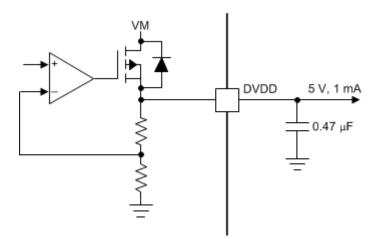


Figure 25. Linear Voltage Regulator Block Diagram

If logic level inputs must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 k Ω .

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.3.10 Logic Level Pin Diagrams

Figure 26 shows the input structure for the logic-level pins STEP, DIR, nSLEEP, SDI, and SCLK.

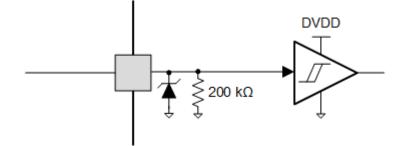


Figure 26. Logic-Level Input Pin Diagram

Figure 27 shows the input structure for the logic-level pins DRVOFF, and nSCS.



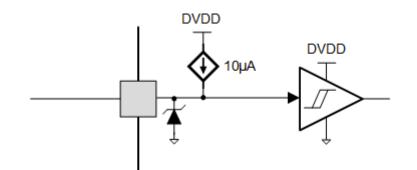


Figure 27. Logic-Level with Internal Pull-up Input Pin Diagram

7.3.10.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V or 3.3-V supply. When a fault is detected, the nFAULT pin is logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V pullup, an external 3.3-V supply must be used.

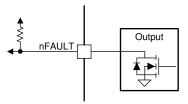


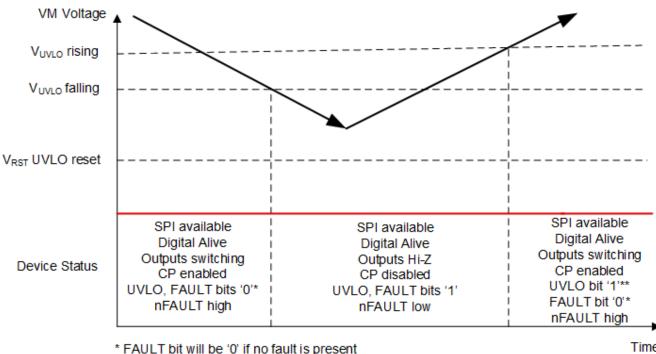
Figure 28. nFAULT Pin

7.3.11 Protection Circuits

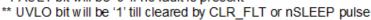
The device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, device overtemperature, and open load events.

It provides additional diagnostics in the form of stall detection.

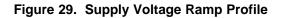


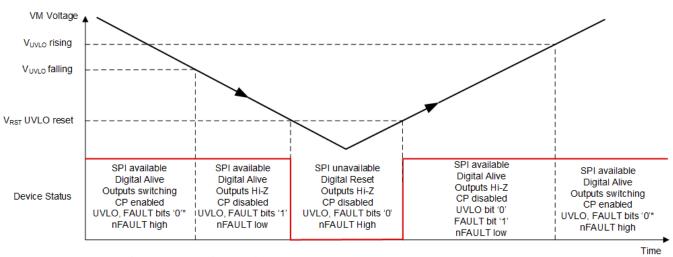


7.3.11.1 VM Undervoltage Lockout (UVLO)



Time





* FAULT bit will be '0' if no fault is present

Figure 30. Supply Voltage Ramp Profile

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage, all the outputs are disabled (High-Z) and the charge pump (CP) is disabled. Normal operation resumes (motor driver and charge pump) when the VM voltage recovers above the UVLO rising threshold voltage.



When the voltage on the VM pin falls below the UVLO falling threshold voltage (4.25 V typical), but is above the VM UVLO reset voltage (V_{RST} , 3.9 V maximum), SPI communication is available, the digital core of the device is alive, the FAULT and UVLO bits are made high in the SPI registers and the nFAULT pin is driven low, as shown in Figure 29. From this condition, if the VM voltage recovers above the UVLO rising threshold voltage (4.35 V typical), nFAULT pin is released (is pulled-up to the external voltage), and the FAULT bit is reset, but the UVLO bit remains latched high until cleared through the CLR_FLT bit or an nSLEEP reset pulse.

When the voltage on the VM pin falls below the VM UVLO reset voltage (V_{RST} , 3.9 V maximum), SPI communication is unavailable, the digital core is shutdown, the FAULT and UVLO bits are low and the nFAULT pin is high. During the subsequent power-up, when the VM voltage exceeds the V_{RST} voltage, the digital core comes alive, UVLO bit stays low but the FAULT bit is made high; and the nFAULT pin is pulled low, as shown in Figure 30. When the VM voltage exceeds the VM UVLO rising threshold, FAULT bit is reset, UVLO bit stays low and the nFAULT pin is pulled high.

7.3.11.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. The FAULT and CPUV bits are made high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed. The CPUV bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.

7.3.11.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in that particular H-bridge are disabled and the nFAULT pin is driven low. The FAULT and OCP bits are latched high in the SPI registers. For xOUTx to VM short, corresponding OCP_LSx_x bit goes high in the DIAG Status 1 register. Similarly, for xOUTx to ground short, corresponding OCP_HSx_x bit goes high. For example, for AOUT1 to VM short, OCP_LS1_A bit goes high; and for BOUT2 to ground short, the OCP_HS2_B bit goes high. The charge pump remains active during this condition. The overcurrent protection can operate in two different modes: latched shutdown and automatic retry.

7.3.11.3.1 Latched Shutdown (OCP_MODE = 0b)

In this mode, after an OCP event, the relevant outputs are disabled and the nFAULT pin is driven low. Normal operation resumes after nSLEEP cycling or a power cycling. This is the default mode for an OCP event for the device.

7.3.11.3.2 Automatic Retry (OCP_MODE = 1b)

In this mode, after an OCP event, the relevant outputs are disabled and the nFAULT pin is driven low. Normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.3.11.4 Open-Load Detection (OL)

If the winding current in any coil drops below the open load current threshold (I_{OL}) and the I_{TRIP} level set by the indexer, and if this condition persists for more than the open load detection time (t_{OL}) , an open-load condition is detected. The EN_OL bit must be '1' to enable open load detection. When an open load fault is detected, the OL and FAULT bits are latched high in the SPI register and the nFAULT pin is driven low. If the OL_A bit is high, it indicates an open load fault in winding A, between AOUT1 and AOUT2. Similarly, an open load fault between BOUT1 and BOUT2 causes the OL_B bit to go high. Normal operation resumes and the nFAULT line is released when the open load condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse. The fault also clears when the device is power cycled or comes out of sleep mode.

If the motor is held at a position corresponding to 0°, 90°, 180° or 270° electrical angles, for more than the open load detection time, open load fault will be flagged, as one of the coil current is zero. This situation does not arise in full-step mode, because the coil currents are never zero.



7.3.11.5 Stall Detection

Stepper motors have a distinct relation between the winding current, back-EMF, and mechanical torque load of the motor, as shown in Figure 31. As motor load approaches the torque capability of the motor at a given winding current, the back-EMF will move in phase with the winding current. By detecting back-emf phase shift between rising and falling current quadrants of the motor current, the DRV8889-Q1 can detect a motor overload stall condition or an end-of-line travel.

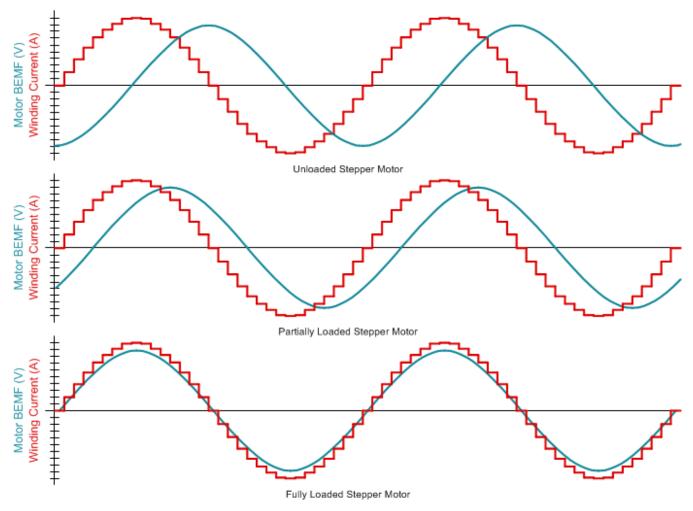


Figure 31. Stall Detection by Monitoring Motor Back-EMF

The Stall Detection algorithm works only when the device is programmed to operate in the smart tune Ripple Control decay mode. The EN_STL bit in CTRL5 register has to be '1' to enable stall detection. The algorithm compares the back-EMF between the rising and falling current quadrants by monitoring PWM off time and generates a value represented by the 8-bit register TRQ_COUNT. The comparison is done in such a way that the TRQ_COUNT value is practically independent of motor current, motor winding resistance, ambient temperature and supply voltage. Full step mode of operation is supported by this algorithm.

For a lightly loaded motor, the TRQ_COUNT will be a non-zero value. As the motor approaches stall condition, TRQ_COUNT will approach zero and can be used to detect stall condition. If anytime TRQ_COUNT falls below the stall threshold (represented by the 8-bit STALL_TH register), device will detect stall and the STALL, STL and FAULT bits are latched high in the SPI register. To indicate stall detection fault on the nFAULT pin, the STL_REP bit in CTRL5 register has to be '1'. When the STL_REP bit is '1', the nFAULT pin will be driven low when stall is detected. In stalled condition, the motor shaft does not spin. The motor starts to spin again when the stall condition is removed and the motor is ramped from zero speed to its target speed. The nFAULT line is released and the fault registers are cleared when a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.

Copyright © 2020, Texas Instruments Incorporated

DRV8889-Q1 SLVSEE9B – JANUARY 2020 – REVISED JANUARY 2020



TRQ_CNT gets calculated as an average from the latest four electrical half-cycles. Once calculated, it gets updated in the SPI register within 100 ns. After the latest TRQ_CNT is updated, it retains the value in the SPI register for the next electrical half-cycle, after which the TRQ_CNT is updated with a new value. The duration of the electrical half-cycle is dependent on microstepping and step-frequency. At the most, it takes two electrical cycles to detect stall.

Stall threshold can be set in two ways – either user can write the STALL_TH bits, or let the algorithm learn the stall threshold value itself through the stall learning process. The stall learning process requires that the STL_LRN bit in CTRL5 register is '1' and the motor is deliberately stalled for some time to allow the algorithm to learn the ideal stall threshold. The process takes 16 electrical cycles and at the end of a successful learning, loads the STALL_TH register with the proper stall threshold bits. Also, the STL_LRN_OK bit goes high at the end of successful learning. It is recommended that users set the stall threshold using the stall learning process for proper stall threshold at one speed may not work well for another speed - therefore it is recommended to re-learn the stall threshold when the motor speed changes.

7.3.11.6 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. In addition, the FAULT, TF and OTS bits are latched high. This protection feature cannot be disabled. The overtemperature protection can operate in two different modes: latched shutdown and automatic recovery.

7.3.11.6.1 Latched Shutdown (OTSD_MODE = 0b)

In this mode, after a OTSD event all the outputs are disabled and the nFAULT pin is driven low. The FAULT, TF and OTS bits are latched high in the SPI register. Normal operation resumes after nSLEEP cycling or a power cycling. This mode is the default mode for a OTSD event.

7.3.11.6.2 Automatic Recovery (OTSD_MODE = 1b)

In this mode, after a OTSD event all the outputs are disabled and the nFAULT pin is driven low. The FAULT, TF and OTS bits are latched high in the SPI register. Normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} - T_{HYS_OTSD}$). The FAULT, TF and OTS bits remains latched high indicating that a thermal event occurred until a clear faults command is issued either through the CLR FLT bit or an nSLEEP reset pulse.

7.3.11.7 Overtemperature Warning (OTW)

If the die temperature exceeds the trip point of the overtemperature warning (T_{OTW}), the OTW and TF bits are set in the SPI register. The device performs no additional action and continues to function. When the die temperature falls below the hysteresis point (T_{HYS_OTW}) of the overtemperature warning, the OTW and TF bits clear automatically. The OTW bit can also be configured to report on the nFAULT pin, and set the FAULT bit in the device, by setting the TW_REP bit to 1b through the SPI registers. The charge pump remains active during this condition.

7.3.11.8 Undertemperature Warning (UTW)

If the die temperature falls below the trip point of the undertemperature warning (T_{UTW}), the UTW and TF bits are set in the SPI register. The device performs no additional action and continues to function. When the die temperature exceeds the hysteresis point (T_{HYS_UTW}) of the undertemperature warning, the UTW and TF bits clear automatically. The UTW bit can also be configured to report on the nFAULT pin, and set the FAULT bit in the device, by setting the TW_REP bit to 1b through the SPI registers. The charge pump remains active during this condition.

FAULT	CONDITION	CONFIGU RATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V _{UVLO} (max 4.35 V)	_	nFAULT / SPI	Disabled	Disabled	Disabled	Reset (V _{VM} < 3.9 V)	Automatic: VM > V _{UVLO} (max 4.45 V)
VCP undervoltage (CPUV)	VCP < V _{CPUV} (typ VM + 2.25 V)	—	nFAULT / SPI	Disabled	Operating	Operating	Operating	VCP > V _{CPUV} (typ VM + 2.7 V)

Table 9. Fault Condition Summary

	Ta	Table 9. Fault Condition Summary (continued)												
FAULT	CONDITION	CONFIGU RATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY						
Overeurrent (OCD)	I _{OUT} > I _{OCP}	OCP_MO DE = 0b	nFAULT / SPI	Disabled	Operating	Operating	Operating	Latched: CLR_FLT / nSLEEP						
Overcurrent (OCP)	(min 2.4 A)	OCP_MO DE = 1b	nFAULT / SPI	Disabled	Operating	Operating	Operating	Automatic retry: t _{RETRY}						
Open Load (OL)	No load detected	EN_OL = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	Report only						
Stall Detection (STALL)	Stall / stuck motor	STL_REP = 0b	SPI	Operating	Operating	Operating	Operating	No action						
	Stall / Stuck Motor	STL_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	Report only						
Overtemperature	T _J > T _{OTW}	TW_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	No action						
Warning (OTW)		TW_REP = 0b	SPI	Operating	Operating	Operating	Operating	Automatic: T _J < T _{OTW} - T _{HYS_OTW}						
Undertemperature	T . T	TW_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	No action						
Warning (UTW)	$T_J < T_{UTW}$	TW_REP = 0b	SPI	Operating	Operating	Operating	Operating	Automatic: T _J > T _{UTW} + T _{HYS_UTW}						
Thermal Shutdown	Т.Т	OTSD_MO DE = 0b	nFAULT / SPI	Disabled	Disabled	Operating	Operating	Latched: CLR_FLT / nSLEEP						
(OTSD)	T _J > T _{OTSD}	OTSD_MO DE = 1b	SPI	Disabled	Disabled	Operating	Operating	Automatic: T _J < T _{OTSD} - T _{HYS_OTSD}						

Table 9. Fault Condition Summary (continued)

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The device state is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled, the DVDD regulator is disabled, the charge pump is disabled, and the SPI is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Disable Mode (nSLEEP = 1, DRVOFF = 1)

The DRVOFF pin is used to enable or disable the half bridges in the device. When the DRVOFF pin is high, the output drivers are disabled in the Hi-Z state.

The DIS_OUT bit can also be used to disable the output drivers. When the DIS_OUT bit is '1', the output drivers are disabled in the Hi-Z state. DIS_OUT is OR'ed with DRVOFF pin.

			-
nSLEEP	DRVOFF	DIS_OUT	H-BRIDGE
0	Don't Care	Don't Care	Disabled
1	0	0	Operating
1	0	1	Disabled
1	1	0	Disabled
1	1	1	Disabled

Table 10. Conditions to Enable or Disable Output Drivers



7.4.3 Operating Mode (nSLEEP = 1, DRVOFF = 0)

When the nSLEEP pin is high, the DRVOFF pin is low, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.4 nSLEEP Reset Pulse

In addition to the CLR_FLT bit in the SPI register, a latched fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 18 μ s and shorter than 35 μ s. If nSLEEP is low for longer than 35 μ s but less than 75 μ s, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see Figure 32). This reset pulse resets any SPI faults and does not affect the status of the charge pump or other functional blocks.

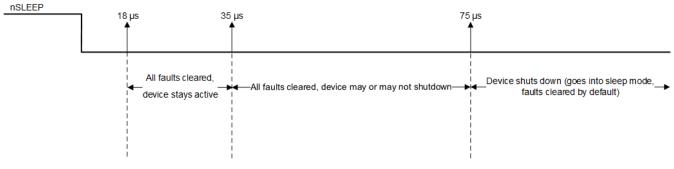


Figure 32. nSLEEP Reset Pulse

lists a summary of the functional modes.

Table 11. Functional Modes Summary										
CONFIGURA	H-BRIDGE	DVDD	CHARGE PUMP							

C	CONDITION		CONFIGURA H-BRIDGE TION		CHARGE PUMP	INDEXER	Logic	
Sleep mode	4.5 V < VM < 45 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled	Disabled	
Operating	4.5 V < VM < 45 V	nSLEEP pin = 1 DRVOFF pin = 0	Operating	Operating	Operating	Operating	Operating	
Disabled	4.5 V < VM < 45 V	nSLEEP pin = 1 DRVOFF pin = 1	Disabled	Operating	Operating	Operating	Operating	

7.5 Programming

7.5.1 Serial Peripheral Interface (SPI) Communication

The device SPI has full duplex, 4-wire synchronous communication. This section describes the SPI protocol, the command structure, and the control and status registers. The device can be connected with the MCU in the following configurations:

- One slave device
- Multiple slave devices in parallel connection
- Multiple slave devices in series (daisy chain) connection

7.5.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit 14)
- 5 address bits, A (bits 13 through 9)
- 8 data bits, D (bits 7 through 0)



Programming (continued)

The SDO output-data word is 16 bits long and the first 8 bits make up the Status Register (S1). The Report word (R1) is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

Table 12. SDI Input Data Word Format

	R/W	ADDRESS			DON'T CARE	DATA									
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	W0	A4	A3	A2	A1	A0	Х	D7	D6	D5	D4	D3	D2	D1	D0

Table 13. SDO Output Data Word Format

	STATUS						REPORT								
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	UVLO	CPUV	OCP	STL	TF	OL	D7	D6	D5	D4	D3	D2	D1	D0

7.5.1.2 SPI for a Single Slave Device

The SPI is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in slave mode. The SPI input-data (SDI) word consists of a 16-bit word, with 8 bits command and 8 bits of data. The SPI output data (SDO) word consists of 8 bits of status register with fault status indication and 8 bits of register data. Figure 33 shows the data sequence between the MCU and the SPI slave driver.

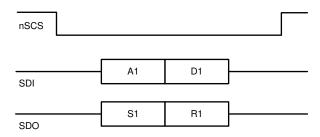


Figure 33. SPI Transaction Between MCU and the device

A valid frame must meet the following conditions:

- The SCLK pin must be low when the nSCS pin goes low and when the nSCS pin goes high.
- The nSCS pin should be taken high for at least 500 ns between frames.
- When the nSCS pin is asserted high, any signals at the SCLK and SDI pins are ignored, and the SDO pin is in the high-impedance state (Hi-Z).
- Full 16 SCLK cycles must occur.
- Data is captured on the falling edge of the clock and data is driven on the rising edge of the clock.
- The most-significant bit (MSB) is shifted in and out first.
- If the data word sent to SDI pin is less than 16 bits or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

NSTRUMENTS

ÈXAS



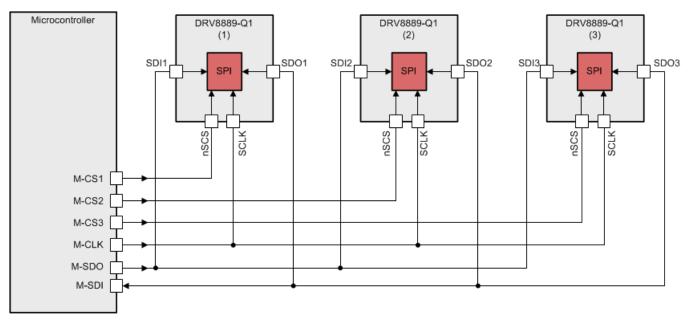


Figure 34. Three DRV8889-Q1 Devices Connected in Parallel Configuration

7.5.1.4 SPI for Multiple Slave Devices in Daisy Chain Configuration

The DRV8889-Q1 device can be connected in a daisy chain configuration to keep GPIO ports available when multiple devices are communicating to the same MCU. Figure 35 shows the topology when three devices are connected in series.

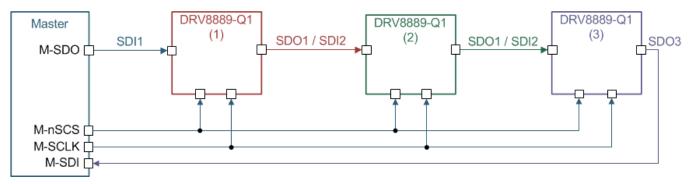


Figure 35. Three DRV8889-Q1 Devices Connected in Daisy Chain

The first device in the chain receives data from the MCU in the following format for 3-device configuration: 2 bytes of header (HDRx) followed by 3 bytes of address (Ax) followed by 3 bytes of data (Dx).

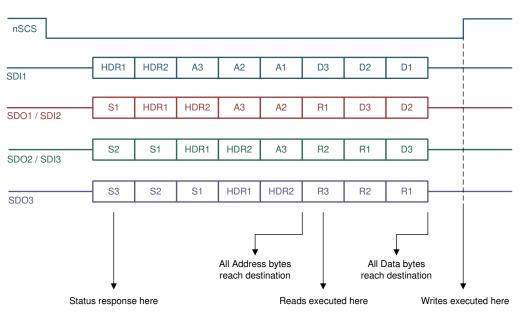


Figure 36. SPI Frame With Three Devices

After the data has been transmitted through the chain, the MCU receives the data string in the following format for 3-device configuration: 3 bytes of status (Sx) followed by 2 bytes of header followed by 3 bytes of report (Rx).

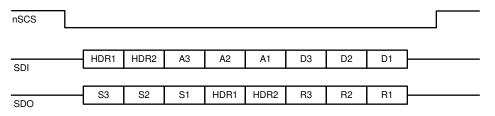
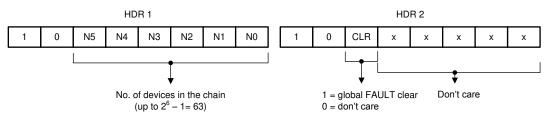


Figure 37. SPI Data Sequence for Three Devices

The header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. Header values N5 through N0 are 6 bits dedicated to show the number of devices in the chain. Up to 63 devices can be connected in series for each daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.





The status byte provides information about the fault status register for each device in the daisy chain so that the MCU does not have to initiate a read command to read the fault status from any particular device. This keeps additional read commands for the MCU and makes the system more efficient to determine fault conditions flagged in a device. Status bytes must start with 1 and 1 for the two MSBs.

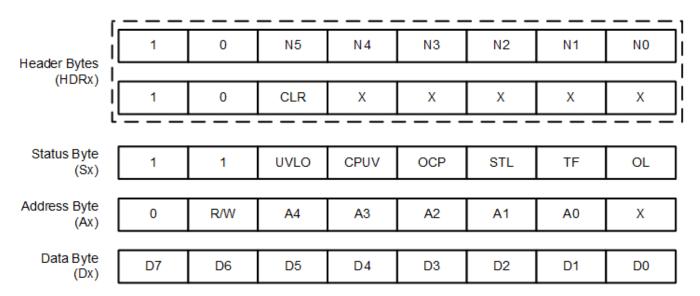
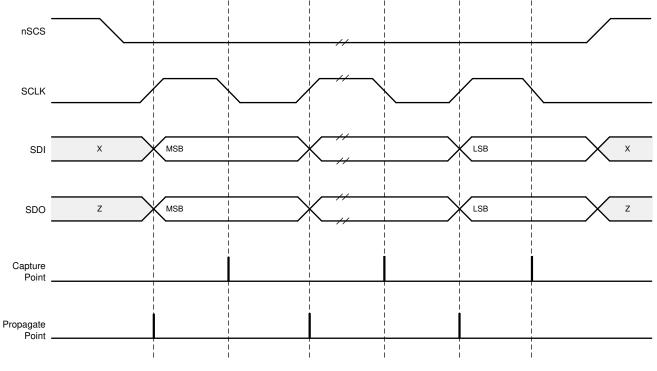


Figure 39. Contents of Header, Status, Address, and Data Bytes for DRV8889-Q1

When data passes through a device, it determines the position of itself in the chain by counting the number of status bytes it receives followed by the first header byte. For example, in this 3-device configuration, device 2 in the chain receives two status bytes before receiving the HDR1 byte which is then followed by the HDR2 byte.

From the two status bytes, the data can determine that its position is second in the chain. From the HDR2 byte, the data can determine how many devices are connected in the chain. In this way, the data only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a 1-device connection. The report bytes (R1 through R3), as shown in Figure 37, are the content of the register being accessed.







7.6 Register Maps

Table 14 lists the memory-mapped registers for the DRV8889-Q1 device. All register addresses not listed in Table 14 should be considered as reserved locations and the register contents should not be modified.

Register Name	7	6	5	4	3	2	1	0	Access Type	Address
FAULT Status	FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL	R	0x00
DIAG Status 1	OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A	R	0x01
DIAG Status 2	UTW	OTW	OTS	STL_LRN_OK	STALL	RSVD	OL_B	OL_A	R	0x02
CTRL1		TRQ_D	AC [3:0]	C [3:0]		RSVD SLEW_RATE [1:0]				0x03
CTRL2	DIS_OUT	RS	VD	TOFF	TOFF [1:0] DECAY [2:0]			RW	0x04	
CTRL3	DIR	STEP	SPI_DIR	SPI_STEP		MICROSTEP	_MODE [3:0]		RW	0x05
CTRL4	CLR_FLT		LOCK [2:0]		EN_OL	OCP_MODE	OTSD_MODE	TW_REP	RW	0x06
CTRL5	RS	SVD	STL_LRN	EN_STL	STL_REP	STL_REP RSVD				0x07
CTRL6		STALL_TH [7:0]					RW	0x08		
CTRL7		TRQ_COUNT [7:0]							R	0x09
CTRL8		RS	VD			REV_I	D [3:0]		R	0x0A

Table 14. Memory Map

Complex bit access types are encoded to fit into small table cells. Table 15 shows the codes that are used for access types in this section.

		••
Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default	Value	
-n		Value after reset or the default value

Table 15. Access Type Codes



7.6.1 Status Registers

The status registers are used to reporting warning and fault conditions. Status registers are read-only registers

Table 16 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 16 should be considered as reserved locations and the register contents should not be modified.

Table 16. Status Registers Summary Table

Address	Register Name	Section
0x00	FAULT status	Go
0x01	DIAG status 1	Go
0x02	DIAG status 2	Go

7.6.1.1 FAULT Status Register Name (address = 0x00)

FAULT status is shown in Figure 41 and described in .

Read-only

Figure 41. FAULT Status Register

7	6	5	4	3	2	1	0
FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 17. FAULT Status Register Field Descriptions

Bit	Field	Туре	Default	Description
7	FAULT	R	0b	When nFAULT pin is at 1, FAULT bit is 0. When nFAULT pin is at 0, FAULT bit is 1.
6	SPI_ERROR	R	Ob	Indicates SPI protocol errors, such as more SCLK pulses than are required or SCLK is absent even though nSCS is low. Becomes high in fault and the nFAULT pin is driven low. Normal operation resumes when the protocol error is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.
5	UVLO	R	0b	Indicates an undervoltage lockout fault condition.
4	CPUV	R	0b	Indicates charge pump undervoltage fault condition.
3	OCP	R	0b	Indicates overcurrent fault condition
2	STL	R	0b	Indicates motor stall condition.
1	TF	R	0b	Logic OR of the overtemperature warning, undertemperature warning and overtemperature shutdown.
0	OL	R	0b	Indicates open-load condition.

7.6.1.2 DIAG Status 1 (address = 0x01)

DIAG Status 1 is shown in Figure 42 and described in Table 18.

Read-only

Figure 42.	DIAG	Status	1	Register
------------	------	--------	---	----------

7	6	5	4	3	2	1	0
OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A
R-0b							



Table 18. DIAG Status 1 Register Field Descriptions

Bit	Field	Туре	Default	Description
7	OCP_LS2_B	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2 in BOUT
6	OCP_HS2_B	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2 in BOUT
5	OCP_LS1_B	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1 in BOUT
4	OCP_HS1_B	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1 in BOUT
3	OCP_LS2_A	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2 in AOUT
2	OCP_HS2_A	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2 in AOUT
1	OCP_LS1_A	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1 in AOUT
0	OCP_HS1_A	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1 in AOUT

7.6.1.3 DIAG Status 2 (address = 0x02)

DIAG Status 2 is shown in Figure 43 and described in Table 19.

Read-only

Figure 43. DIAG Status 2 Register

7	6	5	4	3	2	1	0	
UTW	OTW	OTS	STL_LRN_OK	STALL	RSVD	OL_B	OL_A	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	

Table 19. DIAG Status 2 Register Field Descriptions

Bit	Field	Туре	Default	Description
7	UTW	R	0b	Indicates undertemperature warning.
6	OTW	R	0b	Indicates overtemperature warning.
5	OTS	R	0b	Indicates overtemperature shutdown.
4	STL_LRN_OK	R	0b	Indicates stall detection learning is successful
3	STALL	R	0b	Indicates motor stall condition
2	RSVD	R	0b	Reserved.
1	OL_B	R	0b	Indicates open-load detection on BOUT
0	OL_A	R	0b	Indicates open-load detection on AOUT

7.6.2 Control Registers

The IC control registers are used to configure the device. Status registers are read and write capable.

Table 20 lists the memory-mapped registers for the control registers. All register offset addresses not listed in Table 20 should be considered as reserved locations and the register contents should not be modified.

ISTRUMENTS

EXAS

Table 20. Control Registers Summary Table

Address	Register Name	Section
0x03	CTRL1	Go
0x04	CTRL2	Go
0x05	CTRL3	Go
0x06	CTRL4	Go
0x07	CTRL5	Go
0x08	CTRL6	Go
0x09	CTRL7	Go

7.6.2.1 CTRL1 Control Register (address = 0x03)

CTRL1 control is shown in Figure 44 and described in Table 21.

Read/Write

Figure 44. CTRL1 Control Register

7	6	5	4	3	2	1	0
	TRQ_DAC [3:0]				SVD	SLEW_RATE [1:0]	
	R/W-0000b			R/W	/-00b	R/W-00b	

Bit	Field	Туре	Default	Description
7-4	TRQ_DAC [3:0]	R/W	0000b	0000b = 100%
				0001b = 93.75%
				0010b = 87.5%
				0011b = 81.25%
				0100b = 75%
				0101b = 68.75%
				0110b = 62.5%
				0111b = 56.25%
				1000b = 50%
				1001b = 43.75%
				1010b = 37.5%
				1011b = 31.25%
				1100b = 25%
				1101b = 18.75%
				1110b = 12.5%
				1111b = 6.25%
3-2	RSVD	R/W	00b	Reserved
1-0	SLEW_RATE [1:0]	R/W	00b	00b = 10-V/µs
				01b = 35-V/µs
				10b = 50-V/µs
				11b = 105-V/µs

Table 21. CTRL1 Control Register Field Descriptions

7.6.2.2 CTRL2 Control Register (address = 0x04)

CTRL2 is shown in Figure 45 and described in Table 22. Read/Write



Figure 45. CTRL2 Control Register

7	6	5	4	3	2	1	0	
DIS_OUT	RSV	D	TOFF	TOFF [1:0]		DECAY [2:0]		
R/W-0b	R/W-0	0b	R/W	-01b		R/W-111b		

Table 22. CTRL2 Control Register Field Descriptions

Bit	Field	Туре	Default	Description
7	DIS_OUT	R/W	Ob	Write '1' to Hi-Z all outputs. OR'ed with DRVOFF pin. Ensure OL fault detection is disabled by writing '0' to EN_OL bit, before making the outputs Hi-Z by writing '1' to DIS_OUT.
6-5	RSVD	R/W	00b	Reserved
4-3	TOFF [1:0]	R/W	01b	00b = 7 μs 01b = 16 μs 10b = 24 μs 11b = 32 μs
2-0	DECAY [2:0]	R/W	111b	000b = Increasing SLOW, decreasing SLOW001b = Increasing SLOW, decreasing MIXED 30%010b = Increasing SLOW, decreasing MIXED 60%011b = Increasing SLOW, decreasing FAST100b = Increasing MIXED 30%, decreasing MIXED 30%101b = Increasing MIXED 60%, decreasing MIXED 60%110b = Smart tune Dynamic Decay111b = Smart tune Ripple Control

7.6.2.3 CTRL3 Control Register (address = 0x05)

CTRL3 is shown in Figure 46 and described in Table 23.

Read/Write

Figure 46. CTRL3 Control Register

7	6	5	4	3	2	1	0
DIR	STEP	SPI_DIR	SPI_STEP		MICROSTEP	_MODE [3:0]	
R/W-0b	R/W-0b	R/W-0b	R/W-0b		R/W-0	0000b	

Bit	Field	Туре	Default	Description
7	DIR	R/W	0b	Direction input. Logic '1' sets the direction of stepping, when $SPI_DIR = 1$.
6	STEP	R/W	Ob	Step input. Logic '1' causes the indexer to advance one step, when SPI_STEP = 1. This bit is self-clearing, automatically becomes '0' after writing '1'.
5	SPI_DIR	R/W	0b	0b = Outputs follow input pin for DIR 1b = Outputs follow SPI registers DIR
4	SPI_STEP	R/W	0b	0b = Outputs follow input pin for STEP 1b = Outputs follow SPI registers STEP

STRUMENTS

XAS

			J	
Bit	Field	Туре	Default	Description
3-0	MICROSTEP_MODE [3:0]	R/W	0000b	0000b = Full step (2-phase excitation) with 100% current
				0001b = Full step (2-phase excitation) with 71% current
				0010b = Non-circular 1/2 step
				0011b = 1/2 step
				0100b = 1/4 step
				0101b = 1/8 step
				0110b = 1/16 step
				0111b = 1/32 step
				1000b = 1/64 step
				1001b = 1/128 step
				1010b = 1/256 step
				1011b to 1111b = Reserved

Table 23. CTRL3 Control Register Field Descriptions (continued)

7.6.2.4 CTRL4 Control Register (address = 0x06)

CTRL4 is shown in Figure 47 and described in Table 24.

Read/Write

Figure 47. CTRL4 Control Register

7	6	5	4	3	2	1	0
CLR_FLT		LOCK [2:0]		EN_OL	OCP_MODE	OTSD_MODE	TW_REP
R/W-0b		R/W-011b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

Bit	Field	Туре	Default	Description	
7	CLR_FLT	R/W	0b	Write '1' to this bit to clear all latched fault bits. This bit automatically resets after being written.	
6-4	LOCK [2:0]	R/W	011b	Write 110b to lock the settings by ignoring further register wri except to these bits and address 0x06h bit 7 (CLR_FLT). Writ any sequence other than 110b has no effect when unlocked.	
				Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.	
3	EN_OL	R/W	0b	Write '1' to enable open load detection	
2	OCP_MODE	R/W	0b	0b = Overcurrent condition causes a latched fault 1b = Overcurrent condition causes an automatic retrying fault	
1	OTSD_MODE	R/W	0b	0b = Overtemperature condition will cause latched fault 1b = Overtemperature condition will cause automatic recovery fault	
0	TW_REP	R/W	0b	0b = Overtemperature or undertemperature warning is no reported on the nFAULT line	
				1b = Overtemperature or undertemperature warning is reported on the nFAULT line	

Table 24. CTRL4 Control Register Field Descriptions

7.6.2.5 CTRL5 Control Register (address = 0x07)

CTRL5 control is shown in Figure 48 and described in Table 25.

Read/Write



Figure 48. CTRL5 Control Register

7	6	5	4	3	2	1	0
RS	SVD	STL_LRN	EN_STL	STL_REP		RSVD	
R/W	V-00b	R/W-0b	R/W-0b	R/W-1b		R/W-000b	

Table 25. CTRL5 Control Register Field Descriptions

Bit	Field	Туре	Default	Description	
7-6	RSVD	R/W	00b	Reserved. Should always be '00'.	
5	STL_LRN	R/W	Ob	Write '1' to learn stall count for stall detection. This bit automatically returns to '0' when the stall learning process is complete.	
4	EN_STL	R/W	0b	0b = Stall detection is disabled 1b = Stall detection is enabled	
3	STL_REP	R/W	1b	0b = Stall detection is not reported on nFAULT 1b = Stall detection is reported on nFAULT	
2-0	RSVD	R/W	000b	Reserved. Should always be '000'.	

7.6.2.6 CTRL6 Control Register (address = 0x08)

CTRL6 is shown in Figure 49 and described in Table 26.

Read/Write

Figure 49. CTRL6 Control Register

7	6	5	4	3	2	1	0
STALL_TH [7:0]							
			R/W-000	001111b			

Table 26. CTRL6 Control Register Field Descriptions

Bit	Field	Туре	Default	Description
7-0	STALL_TH [7:0]	R/W	00001111 b	00000000b = 0 count XXXXXXXb = 1 to 254 counts 11111111b = 255 counts

7.6.2.7 CTRL7 Control Register (address = 0x09)

CTRL7 is shown in Figure 50 and described in Table 27.

Read-only

Figure 50. CTRL7 Control Register

7	6	5	4	3	2	1	0
TRQ_COUNT [7:0]							
	R-1111111b						

Table 27. CTRL7 Control Register Field Descriptions

Bit	Field	Туре	Default	Description
7-0	TRQ_COUNT [7:0]	R	11111111 b	00000000b = 0 count XXXXXXXb = 1 to 254 counts 1111111b = 255 counts

7.6.2.8 CTRL8 Control Register (address = 0x0A)

CTRL8 is shown in Figure 51 and described in Table 28.

Read-only

Figure 51. CTRL8 Control Register

7	6	5	4	3	2	1	0
RSVD			REV_ID [3:0]				
R-0000b				R-00)10b		

Table 28. CTRL8 Control Register Field Descriptions

Bit	Field	Туре	Default	Description
7-4	RSVD	R	0000b	Reserved
3-0	REV_ID	R	0010b	Silicon Revision Identification. 0000b indicates 1 st Prototype Revision. 0001b indicates 2 nd Prototype Revision. 0010b indicates Production Revision.



8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8889-Q1 device is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8889-Q1 device.

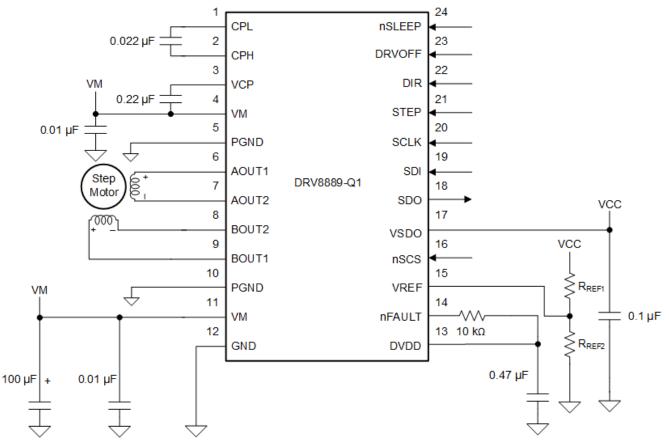


Figure 52. Typical Application Schematic (HTSSOP package)



Typical Application (continued)

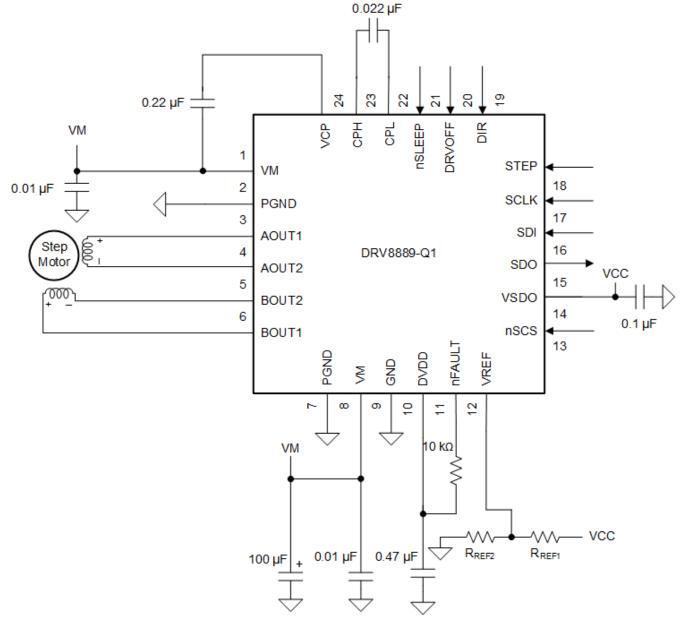


Figure 53. Typical Application Schematic (VQFN package)

8.2.1 Design Requirements

Table 29 lists the design input parameters for a typical adaptive headlight application.

	J	
DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	9 V to 16 V, 13.5 V Nominal
Motor winding resistance	RL	7.7 Ω/phase
Motor full step angle	θ_{step}	15°/step
Target microstepping level	n _m	1/8 step

Table 29. Design Parameters



Table 29. Design Parameters (continued)			
DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE	
Target motor speed	V	300 rpm	
Target full-scale current	I _{FS}	500 mA	

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the device requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed. Use Equation 2 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step})

$$f_{\text{step}} (\text{steps / s}) = \frac{v (\text{rpm}) \times 360 (^{\circ}/\text{rot})}{\theta_{\text{step}} (^{\circ}/\text{step}) \times n_{\text{m}} (\text{steps / microstep}) \times 60 (\text{s / min})}$$
(2)

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor.

For example, the motor in this adaptive headlight application is required to rotate at 15°/step for a target of 300 rpm at 1/8 microstep mode. Using Equation 2, f_{step} can be calculated as 960 Hz.

For the DRV8889-Q1 device, the microstepping level is set by the MICROSTEP_MODE bits in the SPI register and can be any of the settings listed in Table 30. Higher microstepping results in a smoother motor motion and less audible noise, but increases switching losses and requires a higher f_{step} to achieve the same motor speed.

MICROSTEP_MODE	STEP MODE
0000b	Full step (2-phase excitation) with 100% current
0001b	Full step (2-phase excitation) with 71% current
0010b	Non-circular 1/2 step
0011b	1/2 step
0100b	1/4 step
0101b	1/8 step
0110b	1/16 step
0111b	1/32 step
1000b	1/64 step
1001b	1/128 step
1010b	1/256 step

Table 30. Microstepping Indexer Settings

8.2.2.2 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREF voltage and the TRQ_DAC setting.

The maximum allowable voltage on the VREF pin is 3.3 V. DVDD can be used to provide VREF through a resistor divider.

During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step.

$$I_{FS}(A) = \frac{V_{REF}(V)}{K_{V}(V/A)} \times TRQ_{DAC}(\%) = \frac{V_{REF}(V) \times TRQ_{DAC}(\%)}{2.2(V/A)}$$
(3)

DRV8889-Q1

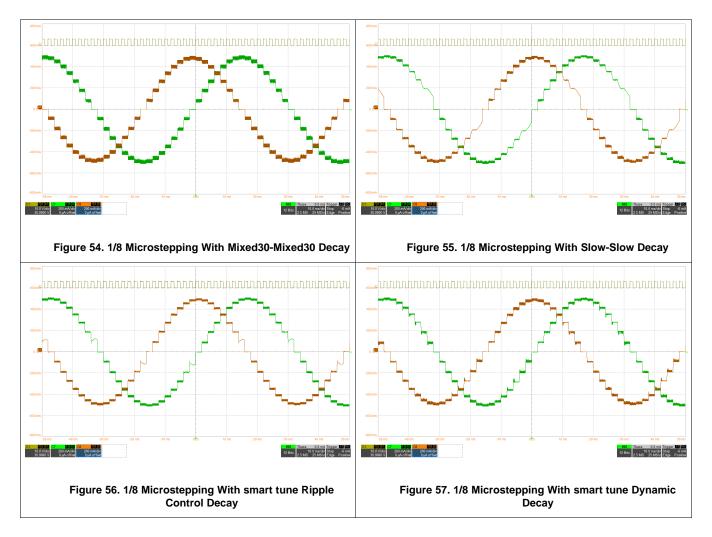
SLVSEE9B-JANUARY 2020-REVISED JANUARY 2020



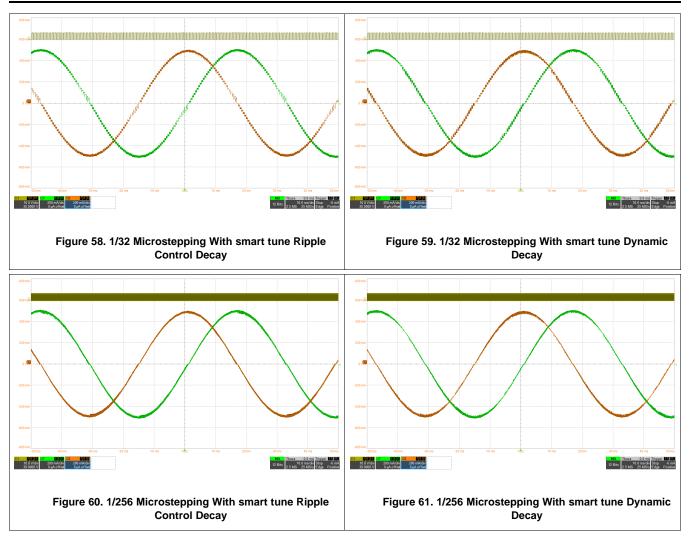
8.2.2.3 Decay Modes

The device supports eight different decay modes, as shown in Table 7. The current through the motor windings is regulated using an adjustable fixed-time-off scheme which means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the device places the winding in one of the eight decay modes for t_{OFF} . After t_{OFF} , a new drive phase starts.

8.2.3 Application Curves







SLVSEE9B-JANUARY 2020-REVISED JANUARY 2020

8.2.4 Thermal Application

www.ti.com

(4)

(5)

STRUMENTS

This section presents the power dissipation calculation and junction temperature estimation of the DRV8889-Q1.

8.2.4.1 Power Dissipation

The total power dissipation in the DRV8889-Q1 constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

8.2.4.1.1 Conduction Loss

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of the other half-bridge. The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in Equation 4.

 $P_{\text{COND}} = 2 \text{ x } (I_{\text{RMS}})^2 \text{ x } (R_{\text{DS(ONH)}} + R_{\text{DS(ONL)}})$

The conduction loss for the typical application shown in Design Requirements is calculated in Equation 5.

 $P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (500 \text{-mA} / \sqrt{2})^2 \times (0.45 \text{-}\Omega + 0.45 \text{-}\Omega) = 225 \text{-mW}$

_

NOTE This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side on-resistance of the FETs. For more accurate calculation, consider the dependency of on-resistance of FETs with device temperature.

8.2.4.1.2 Switching Loss

The power loss due to the PWM switching frequency depends on the slew rate (t_{SR}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses during rise-time and fall-time are calculated as shown in Equation 6 and Equation 7.

$P_{SW_RISE} = 0.5 \text{ x } V_{VM} \text{ x } I_{RMS} \text{ x } t_{RISE_PWM} \text{ x } f_{PWM}$	(6)
$P_{SW_FALL} = 0.5 \text{ x } V_{VM} \text{ x } I_{RMS} \text{ x } t_{FALL_PWM} \text{ x } f_{PWM}$	(7)

Both $t_{\text{RISE}_{PWM}}$ and $t_{\text{FALL}_{PWM}}$ can be approximated as V_{VM} / t_{SR} . After substituting the values of various parameters, and assuming 105 V/µs slew rate and 30-kHz PWM frequency, the switching losses are calculated as shown below -

$$P_{SW RISE} = 0.5 \times 13.5 \text{-V} \times (500 \text{-mA} / \sqrt{2}) \times (13.5 \text{-V} / 105 \text{V/}\mu\text{s}) \times 30 \text{-kHz} = 9.2 \text{-mW}$$
 (8)

 $P_{SW FALL} = 0.5 \times 13.5 \text{-V} \times (500 \text{-mA} / \sqrt{2}) \times (13.5 \text{-V} / 105 \text{ V/}\mu\text{s}) \times 30 \text{-kHz} = 9.2 \text{-mW}$ (9)

The total switching loss (P_{SW}) is calculated as the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_RISE}) switching loss as shown below -

 $P_{SW} = P_{SW_RISE} + P_{SW_FALL} = 9.2-mW + 9.2-mW = 18.4-mW$

(10)

NOTE

The rise-time (t_{RISE}) and the fall-time (t_{FALL}) are calculated based on typical values of the slew rate (t_{SR}). This parameter is expected to change based on the supply-voltage, temperature and device to device variation.

The switching loss is inversely proportional to the output slew rate. 10 V/µs slew rate will result in approximately ten times higher switching loss than 105 V/µs slew rate. However, lower slew rates tend to result in better EMC performance of the driver. A careful trade-off analysis needs to be performed to arrive at an appropriate slew rate for an application.

The switching loss is directly proportional to the PWM switching frequency. The PWM frequency in an application will depend on the supply voltage, inductance of the motor coil, back emf voltage and OFF time or the ripple current (for smart tune ripple control decay mode).

8.2.4.1.3 Power Dissipation Due to Quiescent Current

The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below



 $P_Q = V_{VM} \times I_{VM}$

Substituting the values, quiescent power loss can be calculated as shown below -	

 $P_Q = 13.5$ -V x 5-mA = 67.5-mW

(12)

(13)

(11)

DRV8889-Q1

SLVSEE9B - JANUARY 2020 - REVISED JANUARY 2020

NOTE

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variation.

8.2.4.1.4 Total Power Dissipation

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in Equation 13.

 $P_{TOT} = P_{COND} + P_{SW} + P_{Q} = 225 \text{-mW} + 18.4 \text{-mW} + 67.5 \text{-mW} = 310.9 \text{-mW}$

8.2.4.2 PCB Types

Thermal analysis in this section is focused for the 2-layer and 4-layer PCB with two different copper thickness (1oz and 2-oz) and six different copper areas (1-cm², 2-cm², 4-cm², 8-cm², 16-cm² and 32-cm²), for both HTSSOP and VQFN packages.

Figure 62 and Figure 63 show the top-layer which is applicable for both 2/4-layer PCB, for HTSSOP and VQFN packages respectively. The top-layer, mid-layer-1 and bottom-layer of the PCB is filled with ground plane, whereas, the mid-layer-2 is filled with power plane.

For the HTSSOP, 4 x 3 array of thermal vias with 300 µm drill diameter and 25 µm Cu plating were placed below the device package. For the VQFN, 2 x 2 array of thermal vias with 300 µm drill diameter and 25 µm Cu plating were placed below the device package. Thermal vias contacted top-layer, bottom-layer, and mid-layer-1 (ground plane) if applicable. The mid-layers and the bottom-layer were modeled with size A * A for both 2-layer and 4-layer designs. For the VQFN package, there was no copper on top layer outside of device land area.

The thickness of copper for different PCB layers in different PCB types is summarized in Table 31. The PCB dimension (A) for different PCB copper area is summarized in Table 32 for the HTSSOP package, and in Table 33 for the VQFN package.

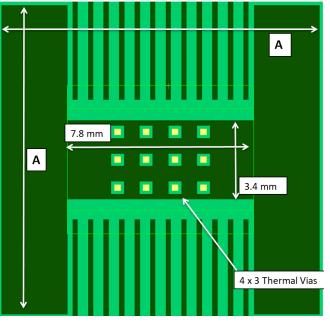
PCB Type	Copper Thickness	Top Layer	Bottom Layer	Mid-Layer 1	Mid-Layer 2
2-Layer	1-oz PCB	1-oz	1-oz	Ν	/A
	2-oz PCB	2-oz	2-oz	IN.	/A
4-Layer	1-oz PCB	1-oz	1-oz	1-oz	1-oz
	2-oz PCB	2-oz	2-oz	1-oz	1-oz

Table 31. PCB Type and Copper Thickness

ISTRUMENTS

EXAS

SLVSEE9B-JANUARY 2020-REVISED JANUARY 2020



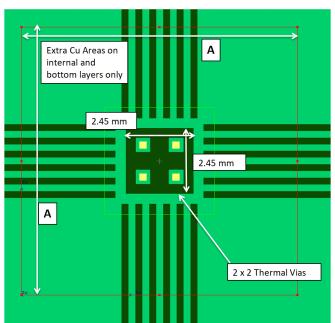


Figure 62. PCB - Top Layer (4/2-Layer PCB) for HTSSOP Package

Figure 63. PCB - Top Layer (4/2-Layer PCB) for VQFN Package

Tuble 02.1 OB Dimension for Theodor publicage		
DIMENSION (A) (mm)		
13.31 mm		
17.64 mm		
23.62 mm		
31.98 mm		
43.76 mm		
60.36 mm		

Table 32. PCB Dimension for HTSSOP package

COPPER AREA (cm ²)	DIMENSION (A) (mm)
1 cm ²	10.00 mm
2 cm ²	14.14 mm
4 cm ²	20.00 mm
8 cm ²	28.28 mm
16 cm ²	40.00 mm
32 cm ²	56.57 mm

Table 33. PCB Dimension for VQFN package

8.2.4.3 Thermal Parameters for HTSSOP Package

The variation of thermal parameters such as the R_{θ JA} (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter) is highly dependent on the PCB type, package type, copper thickness and the copper pad area.

Figure 64 and Figure 65 show the variation of the $R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter) with copper-pad area for 2-layer PCB, for the HTSSOP package. As shown in these curves, the thermal resistance is lower for the higher copper thickness PCB and the higher copper pad-area.

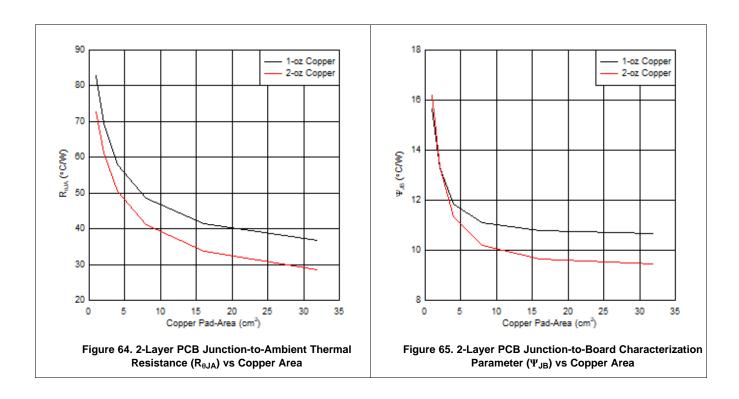
Similarly, Figure 66 and Figure 67 show the variation of the $R_{\theta JA}$ and Ψ_{JB} with copper-pad area for 4-layer PCB respectively, for the HTSSOP package.

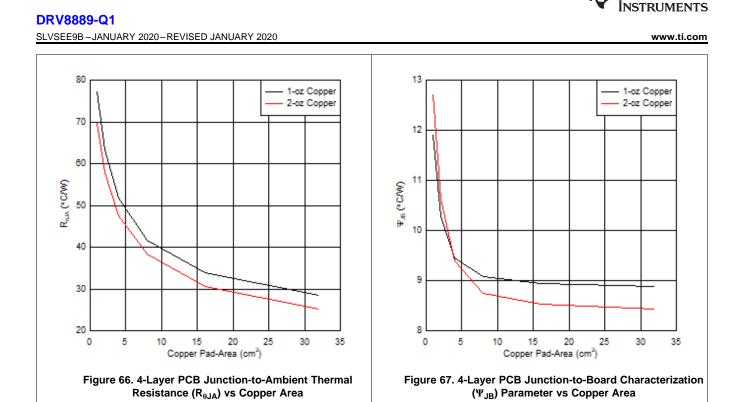


NOTE

The thermal parameters (R_{θ JA} (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter)) are calculated considering the ambient temperature of 25°C and with 2-W power evenly dissipated between high-side and low-side FET's. The thermal parameters calculated considering the power dissipation at the actual location of the power-FETs rather than an averaged estimation.

The thermal parameters are highly dependent on the external conditions such as altitude, package geometry etc. Refer to Application Report for more details.





8.2.4.4 Thermal Parameters for VQFN Package

Figure 68 and Figure 69 show the variation of the $R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter) with copper-pad area for 2-layer PCB, for the VQFN package. As shown in these curves, the thermal resistance is lower for the higher copper thickness PCB and the higher copper pad-area.

Similarly, Figure 70 and Figure 71 show the variation of the $R_{\theta JA}$ and Ψ_{JB} with copper-pad area for 4-layer PCB respectively, for the VQFN package.

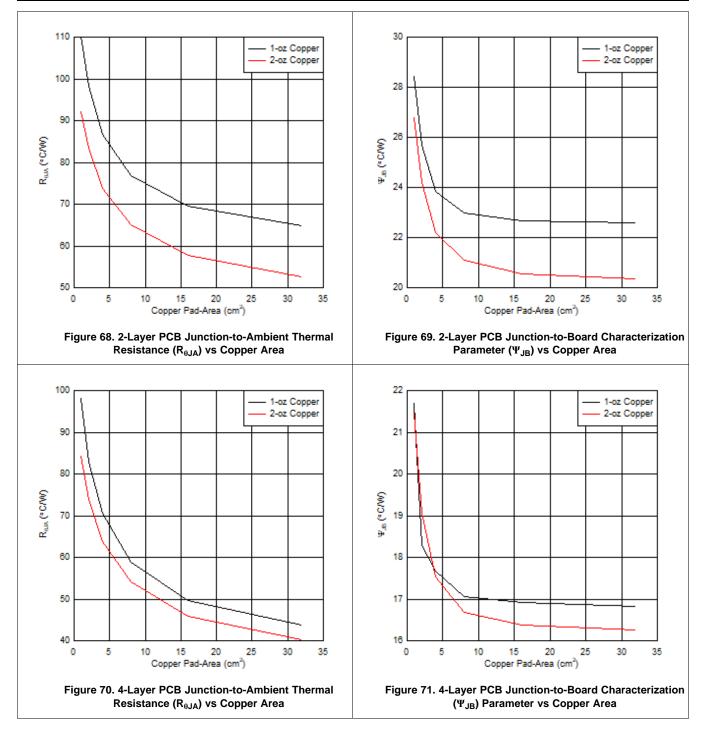
NOTE

The thermal parameters (R_{θ JA} (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter)) are calculated considering the ambient temperature of 25°C and with 2-W power evenly dissipated between high-side and low-side FET's. The thermal parameters calculated considering the power dissipation at the actual location of the power-FETs rather than an averaged estimation.

The thermal parameters are highly dependent on the external conditions such as altitude, package geometry etc. Refer to Application Report for more details.

EXAS





8.2.4.5 Device Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as shown in Equation 14.

$$ConsideriT_{J} = T_{A} + (P_{TOT} \times R_{\theta JA})$$

ng a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 30.9 °C/W for the HTSSOP package and 40.7 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as shown below -

Copyright © 2020, Texas Instruments Incorporated

(14)



SLVSEE9B – JANUARY 2020 – REVISED JANUARY 2020	www.ti.com
T _J = 25°C + (0.3109-W x 30.9°C/W) = 34.61 °C	(15)
The junction temperature for the VQFN package is calculated as shown below -	
$T_J = 25^{\circ}C + (0.3109 - W \times 40.7^{\circ}C/W) = 37.65^{\circ}C$	(16)



9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 45 V. A 0.01- μ F ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

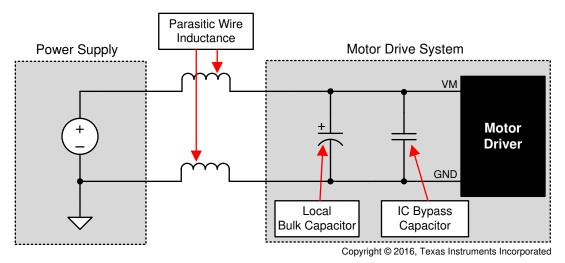


Figure 72. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 μ F rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 μ F rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 μ F rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 μ F rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground.



10.2 Layout Example

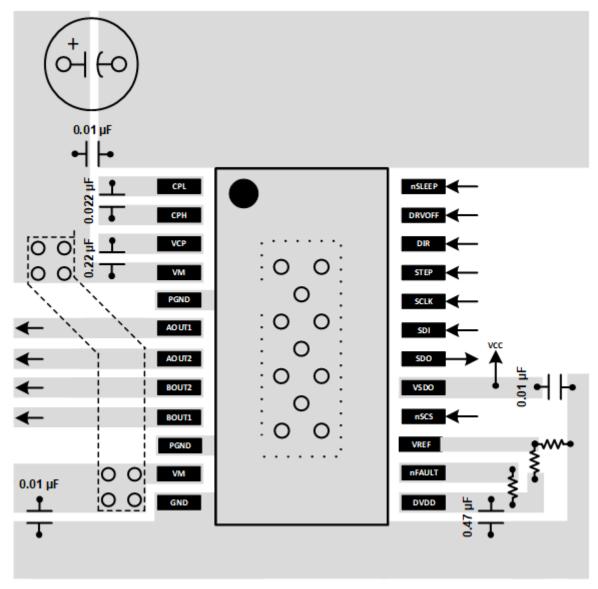


Figure 73. HTSSOP Layout Recommendation



Layout Example (continued)

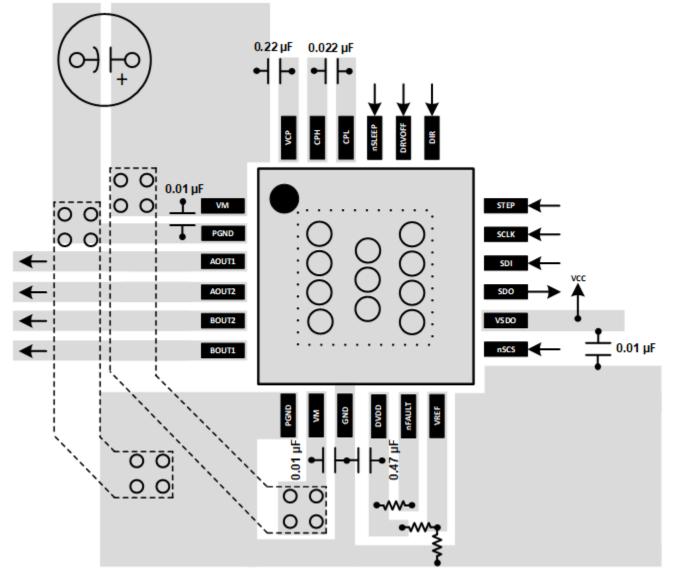


Figure 74. QFN Layout Recommendation



11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Sensorless Stall Detection With the DRV8889-Q1 application report
- Texas Instruments, Calculating Motor Driver Power Dissipation application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, How AutoTune[™] regulates current in stepper motors white paper
- Texas Instruments, Industrial Motor Drive Solution Guide
- Texas Instruments, PowerPAD™ Made Easy application report
- Texas Instruments, PowerPAD[™] Thermally Enhanced Package application report
- Texas Instruments, Stepper motors made easy with AutoTune[™] white paper
- Texas Instruments, Understanding Motor Driver Current Ratings application report
- Texas Instruments, Motor Drives Layout Guide application report
- Texas Instruments, DRV8889-Q1 Evaluation Module (EVM) tool folder

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.



12 Mechanical, Packaging, and Orderable Information

For the device mechanical, packaging, and orderable information, refer to the *Mechanical, Packaging, and Orderable Information* section of the data sheet available in the DRV8889-Q1 product folder



EXAS

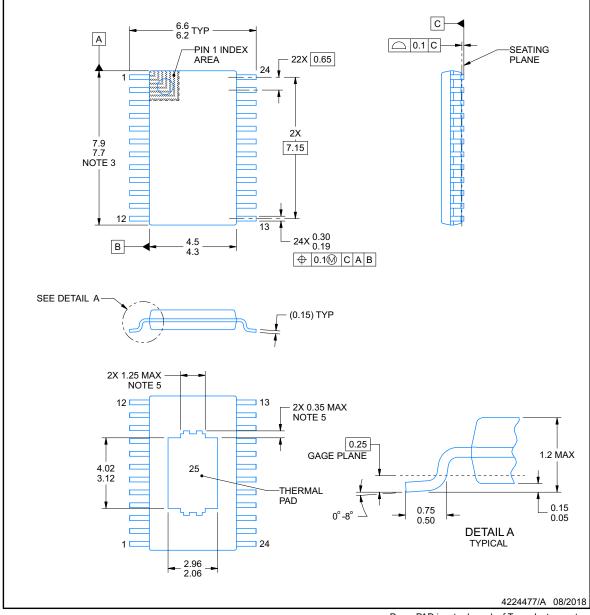
INSTRUMENTS

PWP0024N

PACKAGE OUTLINE

PowerPAD[™] TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.
 Features may differ or may not be present.





EXAMPLE BOARD LAYOUT

PowerPAD[™] TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



– (3.4) – NOTE 9 (2.96)METAL COVERED SYMM 24X (1.5) BY SOLDER MASK 1 24X (0.45) 24 SEE DETAILS (R0.05) TYP (4.02) 22X (0.65) 0 0 (0.6) SYMM 25 (7.8) NOTE 9 đ ሐ Ð (1.2) TYP SOLDER MASK DEFINED PAD ŧ Ð (Ø 0.2) TYP VIA 12 13 (1.2) TYP (5.8) -LAND PATTERN EXAMPLE EXPOSED METAL SHOWN SCALE: 8X METAL UNDER SOLDER MASK SOLDER MASK -METAL SOLDER MASK OPENING OPENING EXPOSED METAL EXPOSED METAL 0.05 MAX 0.05 MIN ALL AROUND ALL AROUND NON-SOLDER MASK SOLDER MASK DEFINED DEFINED SOLDER MASK DETAILS 4224477/A 08/2018

NOTES: (continued)

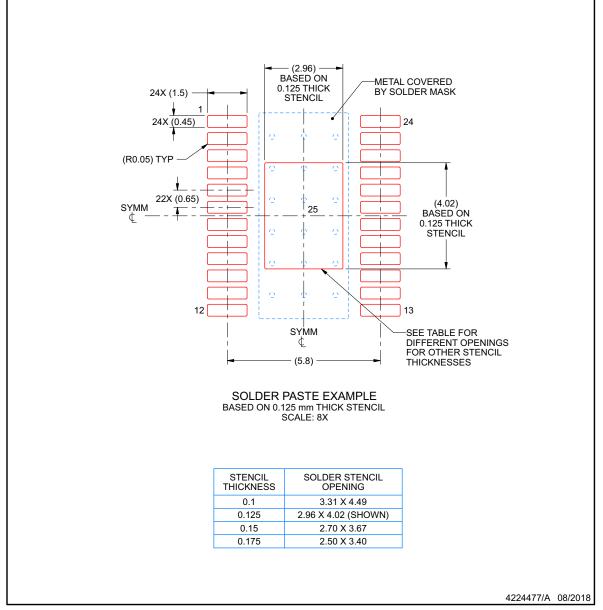
- Publication IPC-7351 may have alternate designs.
 Solder mask tolerances between and around signal pads can vary based on board fabrication site.
 This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



EXAMPLE STENCIL DESIGN

PowerPAD[™] TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations. 12. Board assembly site may have different recommendations for stencil design.



www.ti.com



NSTRUMENTS

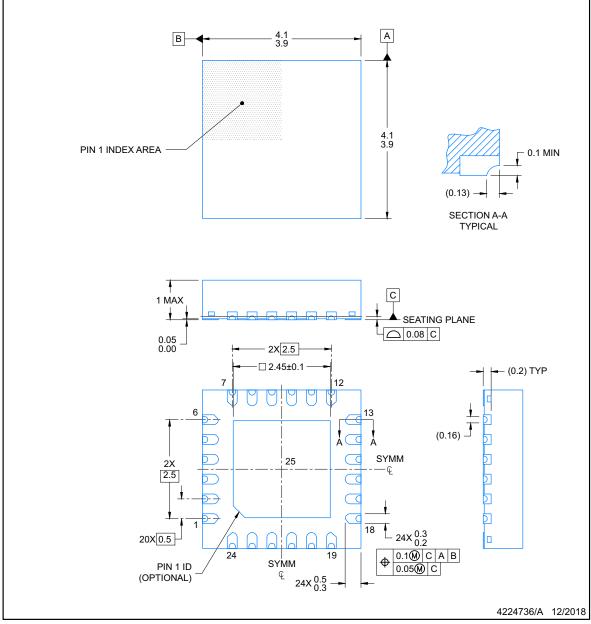
Texas

www.ti.com

PACKAGE OUTLINE VQFN - 1 mm max height

RGE0024N

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

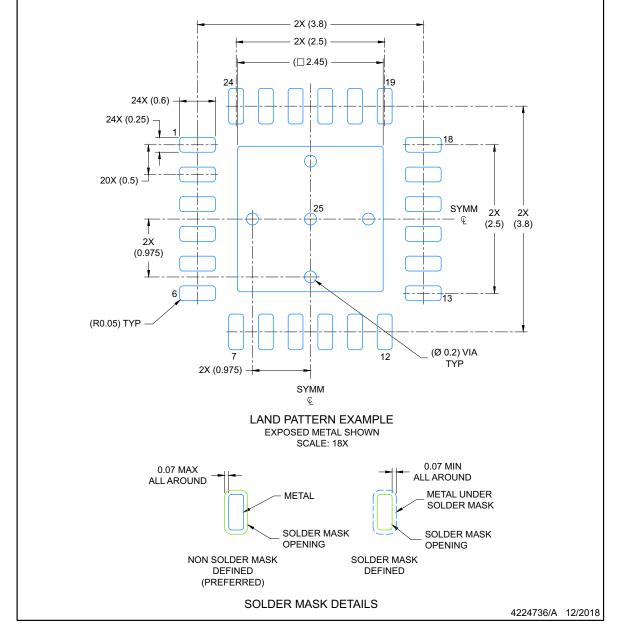


DRV8889-Q1 SLVSEE9B - JANUARY 2020 - REVISED JANUARY 2020

EXAMPLE BOARD LAYOUT

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature 4. number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



EXAS

RGE0024N

ISTRUMENTS



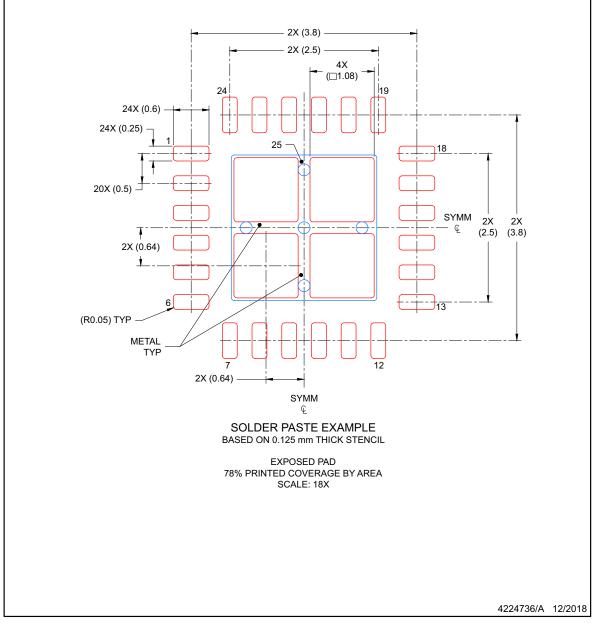
www.ti.com

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGE0024N

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





12-Feb-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8889QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8889	Samples
DRV8889QWRGERQ1	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 8889	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



www.ti.com

PACKAGE OPTION ADDENDUM

12-Feb-2020

PACKAGE MATERIALS INFORMATION

www.ti.com

Texas Instruments

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8889QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV8889QWRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TEXAS INSTRUMENTS

www.ti.com

PACKAGE MATERIALS INFORMATION

29-Jan-2020



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8889QPWPRQ1	HTSSOP	PWP	24	2000	367.0	367.0	38.0
DRV8889QWRGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0

PWP 24

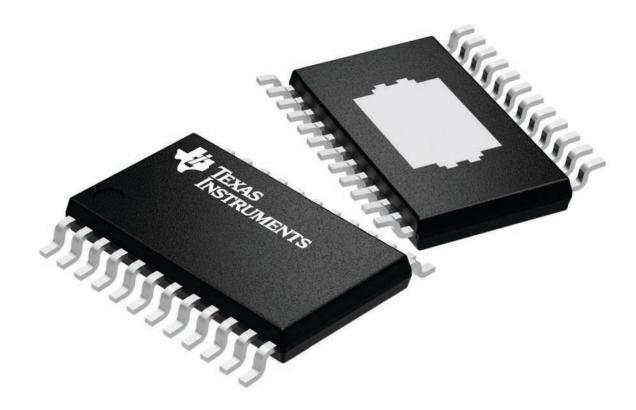
GENERIC PACKAGE VIEW

PLASTIC SMALL OUTLINE

PowerPAD[™] TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





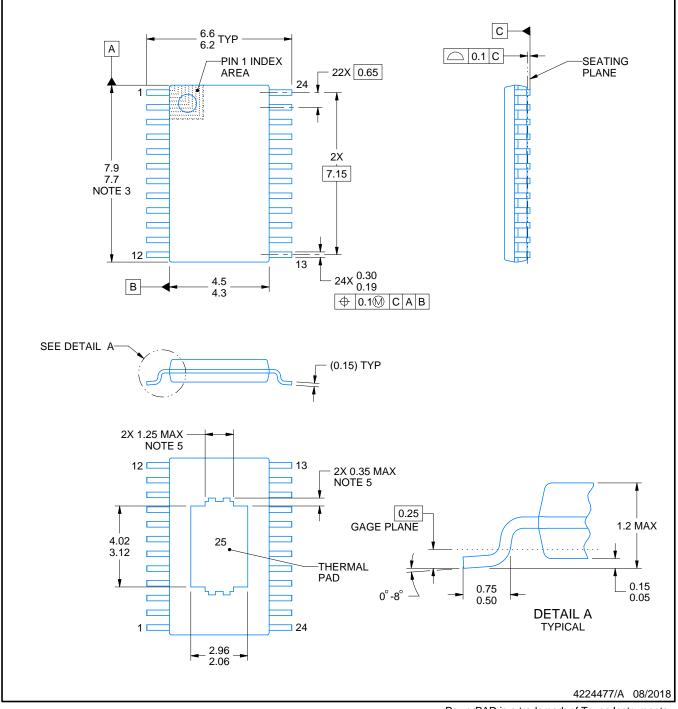
PWP0024N



PACKAGE OUTLINE

PowerPAD[™] TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side. 4. Reference JEDEC registration MO-153.
- 5. Features may differ or may not be present.

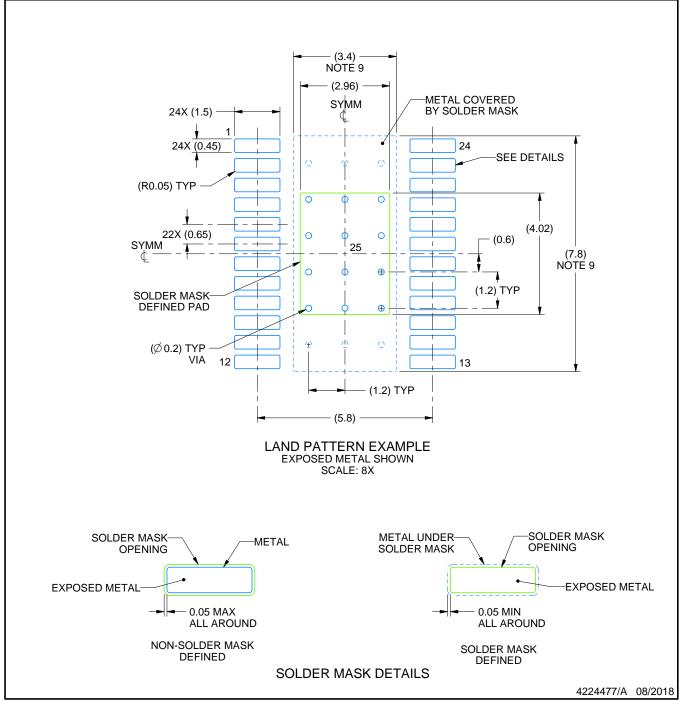


PWP0024N

EXAMPLE BOARD LAYOUT

PowerPAD[™] TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

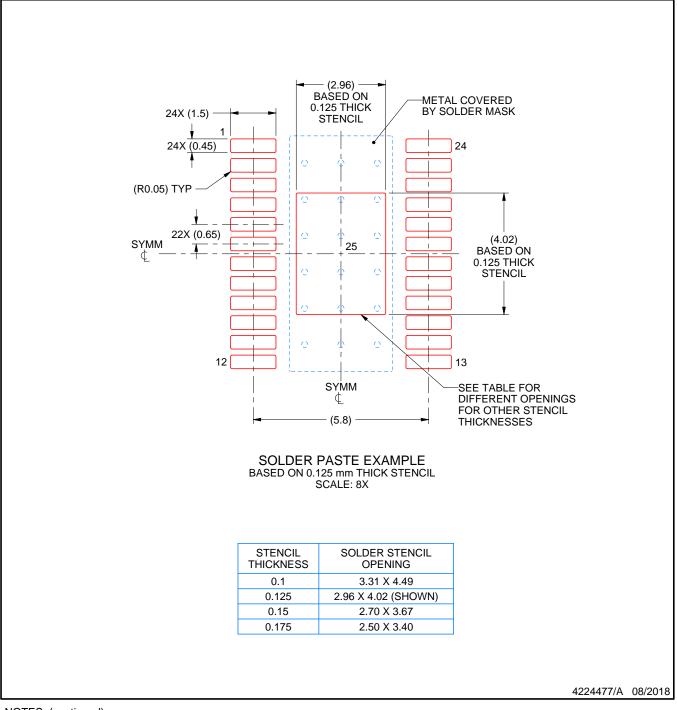


PWP0024N

EXAMPLE STENCIL DESIGN

PowerPAD[™] TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12. Board assembly site may have different recommendations for stencil design.



GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2020, Texas Instruments Incorporated