KSZ9021GN to KSZ9031MNX

Migration Guide

Rev. 1.1

Introduction

This document summarizes the hardware pin and software register differences for migrating from an existing board design using the KSZ9021GN PHY to a new board design using the KSZ9031MNX PHY. For hardware and software details, consult reference schematic and data sheet of each respective device.

Data sheets and support documentations can be found on Micrel's web site at: www.micrel.com.

Differences Summary

Table 1 summarizes the supported device attribute differences between KSZ9021GN and KSZ9031MNX PHY devices.

Device Attribute	KSZ9021GN	KSZ9031MNX
Transceiver (AVDDH) Voltage	3.3V only	3.3V or 2.5V (commercial temperature only)
Digital I/O (DVDDH) Voltage	3.3V or 2.5V	3.3V, 2.5V or 1.8V
Indirect Register Access	Proprietary (Micrel defined) – Extended Registers	IEEE defined – MDIO Manageable Device (MMD) Registers
Energy-Detect Power-Down (EDPD) Mode	Not Supported	Supported for further power consumption reduction when cable is disconnected; Disabled as the power-up default and enable using MMD register
IEEE 802.3az Energy Efficient Ethernet (EEE) Mode	Not Supported	Supported with: • Low Power Idle (LPI) mode for 1000Base-T and 100Base-TX • Transmit Amplitude reduction for 10Base-T (10Base-Te) • Associated MMD registers for EEE
Wake-on-LAN (WOL)	Not Supported	Supported with: • Wake-up using detection of Link Status, Magic Packet, or Custom-Packet • PME_N interrupt output signal • Associated MMD registers for WOL

Table 1. Summary of Device Attribute Differences between KSZ9021GN and KSZ9031MNX

Pin Differences

Table 2 summarizes the pin differences between KSZ9021GN and KSZ9031MNX PHY devices.

Pin #	KSZ9021GN			KSZ9031RNX		
	Pin Name	Type	Pin Function	Pin Name	Type	Pin Function
1	AVDDH	P	3.3V analog V_{DD}	AVDDH	P	3.3V/2.5V (commercial temp only) analog V_{DD}
16	AVDDH	P	3.3V analog V_{DD}	AVDDH	P	3.3V/2.5V (commercial temp only) analog V_{DD}
18	DVDDH	P	3.3V / 2.5V digital V_{DD}	DVDDH	P	3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$
19	LED1 / PHYAD0	I/O	LED Output: Programmable LED1 Output Config Mode: The pull-up/pull-down value is latched as PHYAD[0] during power-up / reset.	LED1 / PHYAD0 / PME_N1	I/O	LED1 output: Programmable LED1 output Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of PHYAD[0]. PME_N output: Programmable PME_N output (pin option 1). This pin function requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0kΩ to 4.7kΩ. When asserted low, this pin signals that a WOL event has occurred. When WOL is not enabled, this pin function behaves as per the KSZ9021GN pin definition. This pin is not an open-drain for all operating modes.
30	DVDDH	P	3.3V / 2.5V digital V_{DD}	DVDDH	P	3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$
40	DVDDH	P	3.3V / 2.5V digital V_{DD}	DVDDH	P	3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$
46	DVDDH	P	3.3V / 2.5V digital V_{DD}	DVDDH	P	3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$
53	INT_N	O	Interrupt Output This pin provides a programmable interrupt output and requires an external pull-up resistor to DVDDH in the range of 1K to 4.7K ohms for active low assertion. This pin is an open-drain.	INT_N/ PME_N2	O	Interrupt Output This pin provides a programmable interrupt output and requires an external pull-up resistor to DVDDH in the range of 1K to 4.7K ohms for active low assertion. PME_N output: Programmable PME_N output

						(pin option 2). When asserted low, this pin signals that a WOL event has occurred. When WOL is not enabled, this pin function behaves as per the KSZ9021GN pin definition. This pin is not an open-drain for all operating modes.
62	AVDDH	P	3.3V analog V_{DD}	NC	–	No connect This pin is not bonded and can be connected to AVDDH power for footprint compatibility with the Micrel KSZ9021GN Gigabit PHY.
63	ISET	I/O	Set transmit output level Connect a 4.99KΩ 1% resistor to ground on this pin.	ISET	I/O	Set the transmit output level Connect a 12.1kΩ 1% resistor to ground on this pin.

Table 2. Pin Differences between KSZ9021GN and KSZ9031MNX

Strapping Option Differences

There is no strapping pin difference between KSZ9021GN and KSZ9031MNX.

Register Map Differences

The register space within the KSZ9021GN and KSZ9031MNX consists of direct-access registers and indirect-access registers.

Direct-access Registers

The direct-access registers comprise of IEEE-Defined Registers (0h – Fh) and Vendor-Specific Registers (10h – 1Fh).

Between the KSZ9021GN and KSZ9031MNX, the direct-access registers and their bits have the same definitions, except for the following registers in Table 3.

Direct-access Register	KSZ9021GN		KSZ9031MNX	
	Name	Description	Name	Description
3h	PHY Identifier 2	Bits [15:10] (part of OUI) – same as KSZ9031MNX Bits [9:4] (model number) – unique for KSZ9021GN Bits [3:0] (revision number) – unique depending on chip revision	PHY Identifier 2	Bits [15:10] (part of OUI) – same as KSZ9021GN Bits [9:4] (model number) – unique for KSZ9031MNX Bits [3:0] (revision number) – unique depending on chip revision
Bh	Extended Register – Control	Indirect Register Access Select read/write control and page/address of Extended Register	Reserved	Reserved Do not change the default value of this register
Ch	Extended Register – Data Write	Indirect Register Access Value to write to Extended Register Address	Reserved	Reserved Do not change the default value of this register
Dh	Extended Register – Data Read	Indirect Register Access Value read from Extended Register Address	MMD Access – Control	Indirect Register Access Select read/write control and MMD device address
Eh	Reserved	Reserved Do not change the default value of this register	MMD Access – Register/Data	Indirect Register Access Value of register address/data for the selected MMD device address
1Fh, bit [1]	Software Reset	1 = Reset chip, except all registers 0 = Disable reset	Reserved	Reserved

Table 3. Direct-access Register Differences between KSZ9021GN and KSZ9031MNX

Indirect-access Registers

The indirect register mapping and read/write access are completely different for the KSZ9021GN (uses Extended Registers) and KSZ9031MNX (uses MMD Registers). Refer to respective devices' data sheets for details.

Indirect registers provide access to the following commonly used functions:

- 1000Base-T link-up time control (KSZ9031MNX only)
- Pin strapping status
- Pin strapping override
- Skew adjustments for GMII clocks and control signals (KSZ9031MNX only)
- Energy-Detect Power-Down Mode enable/disable (KSZ9031MNX only)
- Energy Efficient Ethernet function (KSZ9031MNX only)
- Wake-on-LAN function (KSZ9031MNX only)

Revision History

Revision	Date	Summary of Changes
1.0	12/7/12	Migration Guide created
1.1	6/7/13	Indicate PME_N1 (pin 19) for KSZ9031MNX is not an open-drain. Indicate INT_N (pin 53) is an open-drain for KSZ9021GN, but is not an open-drain for KSZ9031MNX. Indicate direct-access register 1Fh, bit [1] difference.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com