KSZ9031MNX Errata Sheet

The following errata apply to the following products (silicon revision):

- KSZ9031MNX (rev-A, A2)

Item #	Erratum (description of problem)	Solution / Workaround
1	KSZ9031 fails to link up after register 4h, bit [11] (Asymmetrical Pause) is set.	Do not enable (set to 1) register 4h, bit [11] for Asymmetric PAUSE support. or Disconnect and re-connect cable after setting register 4h bit [11] to 1.
2	The 125MHz reference clock (CLK125_NDO pin) output has duty cycle variation when the KSZ9031 links up in 1000Base-T Slave mode, resulting in wide variation on the falling clock edge.	Use only rising edge of CLK125_NDO output for PLL locking. or Set KSZ9031 to always link up in 1000Base-T Master mode by setting register 9h, bits [12:11] to '11'.
3	For Tri-color Dual-LED mode, the LED[2:1] pins' toggle rate for transmit/receive activity indication is tied to the data rate. At low data rate, the LED[2:1] pins still toggle but the on/off toggling of the LED indicators is not visible to the eye.	Use external circuits to stretch the high assertions (LED indicator off periods) of the LED[2:1] outputs to make them visible to the eye. The LED[2:1] outputs are low when there is link-up and no activity. or Use Single-LED Mode

For any questions about this errata and sample request, please contact your Micrel FAE or local Sales Representative.