KSZ9031MNX Evaluation-Socket Board Revision 1.1

REVISION HISTORY

DATE	DESCRIPTION	REVISION
8/16/12	Initial Release	1.0
9/28/12	Changed U1 (KSZ9031MNX) pin 62 from AVDDH to NC.	1.1

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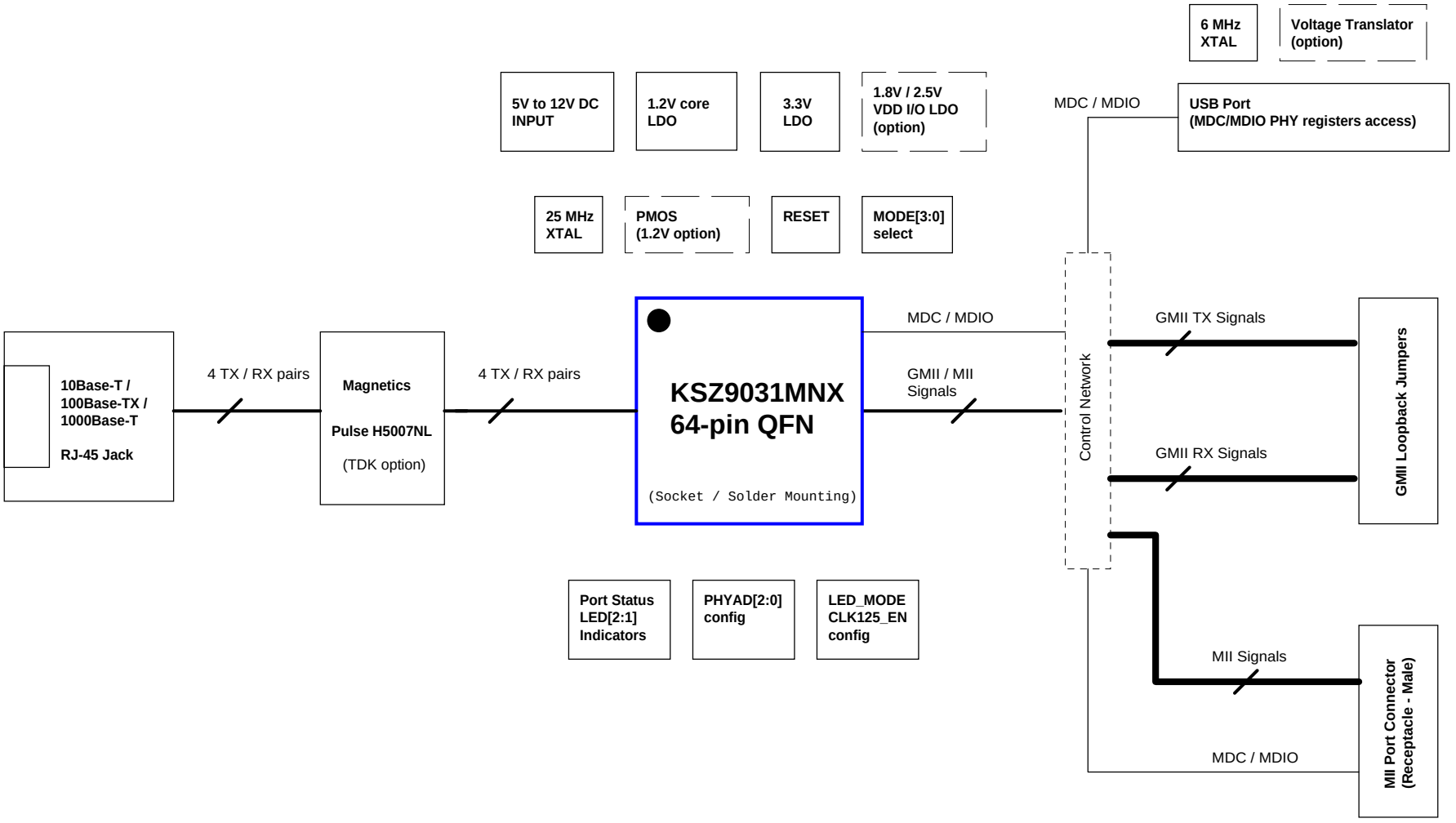
KSZ9031MNX EVALUATION-SOCKET BOARD - BLOCK DIAGRAM



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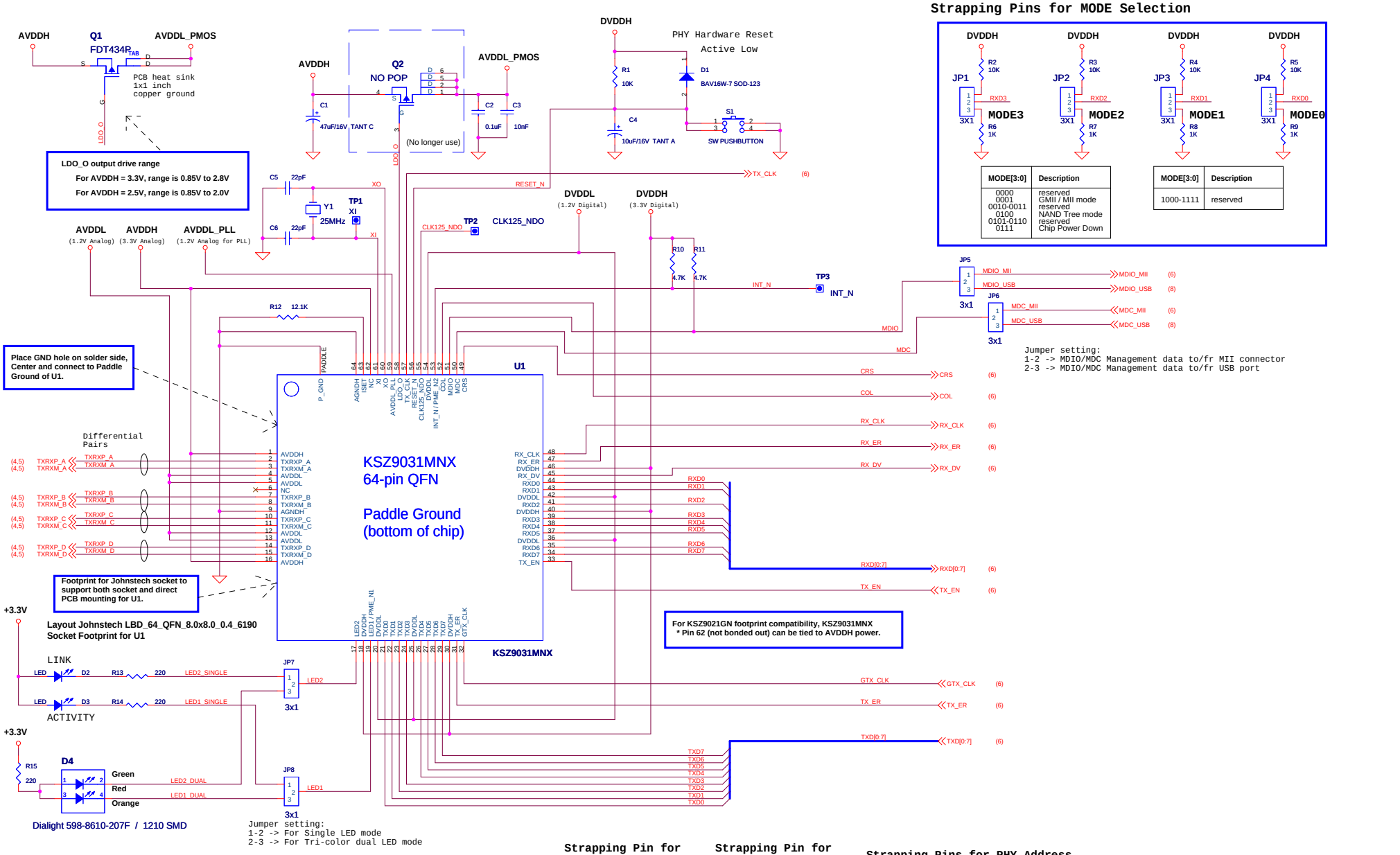
Strapping Pins for MODE Selection
JP1 MODE3
JP2 MODE2
JP3 MODE1
JP4 MODE0
MODE[3:0] Description
0000 reserved
0001 GMII / MII mode
0010-0011 reserved
0100 NAND Tree mode
0101-0110 reserved
0111 Chip Power Down
1000-1111 reserved
KSZ9031MNX
64-pin QFN
Paddle Ground
(bottom of chip)
U1
Q1 FDT434P
Q2 NO POP
PCB heat sink
1x1 inch
copper ground
LDO_O output drive range
For AVDDH = 3.3V, range is 0.85V to 2.8V
For AVDDH = 2.5V, range is 0.85V to 2.0V
PHY Hardware Reset
Active Low
BAV16W-7 SOD-123
SW PUSHBUTTON
(No longer use)
Place GND hole on solder side, Center and connect to Paddle Ground of U1.
Differential Pairs
Footprint for Johnstech socket to support both socket and direct PCB mounting for U1.
Layout Johnstech LBD_64_QFN_8.0x8.0_0.4_6190
Socket Footprint for U1
Jumper setting:
1-2 -> MDIO/MDC Management data to/fr MII connector
2-3 -> MDIO/MDC Management data to/fr USB port
For KSZ9021GN footprint compatibility, KSZ9031MNX
* Pin 62 (not bonded out) can be tied to AVDDH power.
LINK
ACTIVITY
Dialight 598-8610-207F / 1210 SMD
Jumper setting:
1-2 -> For Single LED mode
2-3 -> For Tri-color dual LED mode
Tri-color Dual LED Mode
Pins [LED2, LED1] Description Dual LED Color
[0, 1] [toggling, 1] Solid Color : 1G Link Blinking : Activity (RX, TX) Green
[1, 0] [1, toggling] Solid Color : 100M Link Blinking : Activity (RX, TX) Red
[0, 0] [toggling, toggling] Solid Color : 10M Link Blinking : Activity (RX, TX) Orange
[1, 1] Link off None
Single LED Mode
Pin Description
LED2 1 : Link off 0 : Link on (any speed), solid color
LED1 Blinking : Activity (RX, TX)
Strapping Pin for LED Mode
LED_MODE
Pull-up: Single LED Mode
Strapping Pin for CLK125 Enable
CLK125_EN
Pull-up: Enable 125MHz clock on Pin 56
Strapping Pins for PHY Address
PHYAD2 PHYAD1 PHYAD0
PHY address bits [4:3] are always set to "00"
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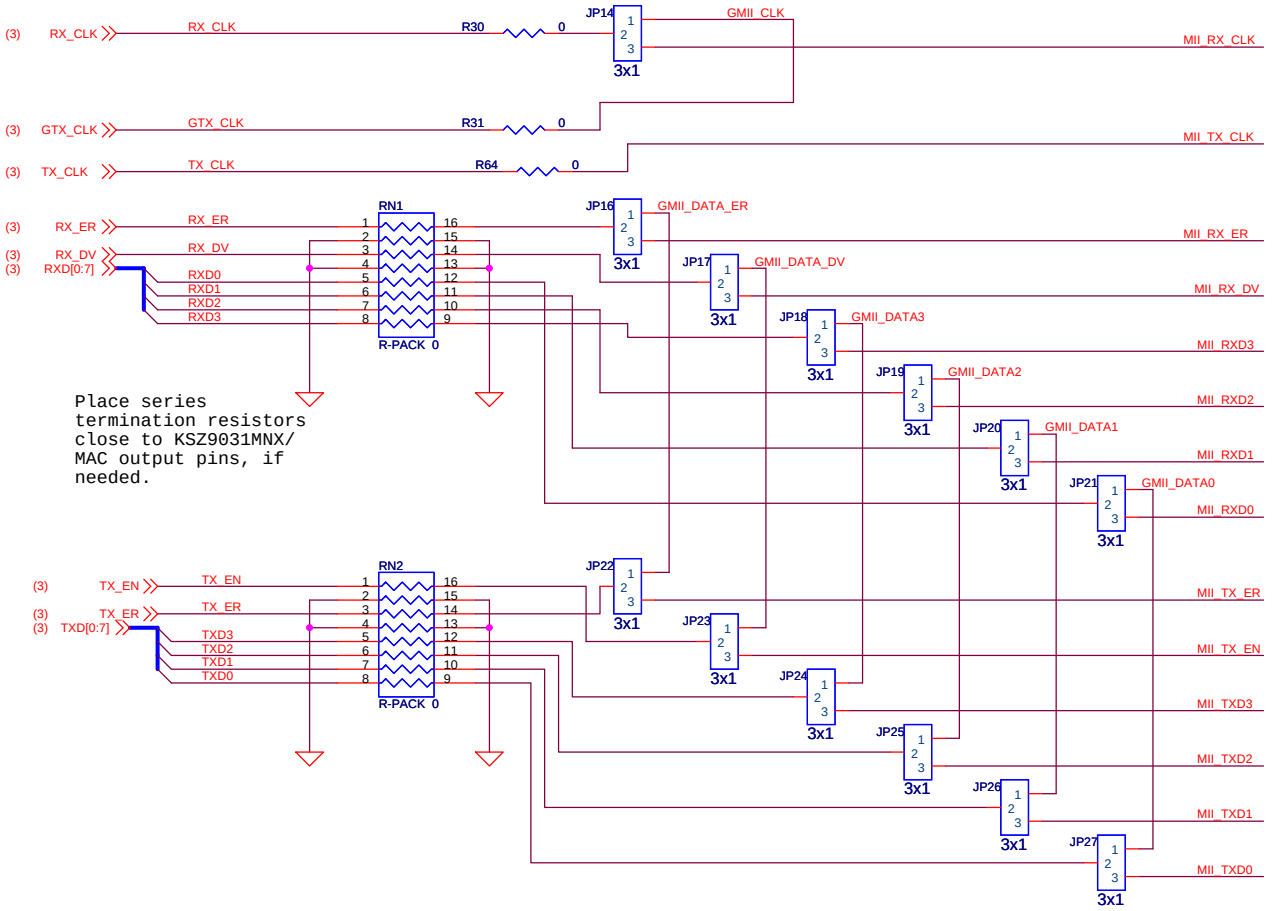
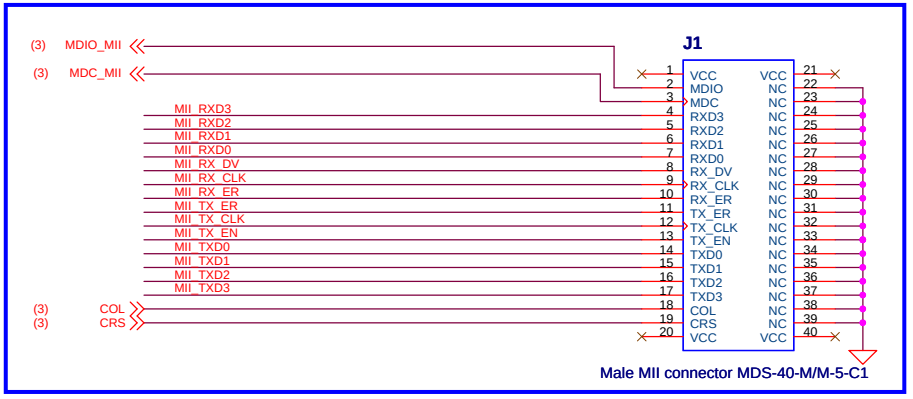
* GTX_CLK (sourced by GMAC) in GMII Mode for 1000Mbps speed

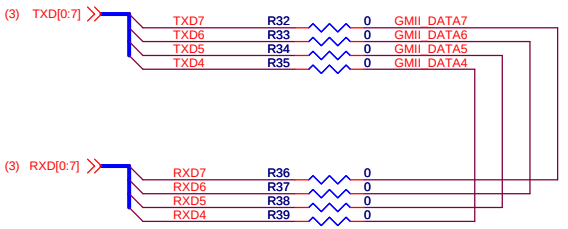
* TX_CLK (sourced by KSZ9031MNX) in MII Mode for 10/100Mbps speed

All Jumpers:
1-2 for GMII mode to loopback
2-3 for MII mode to connector



MII Port





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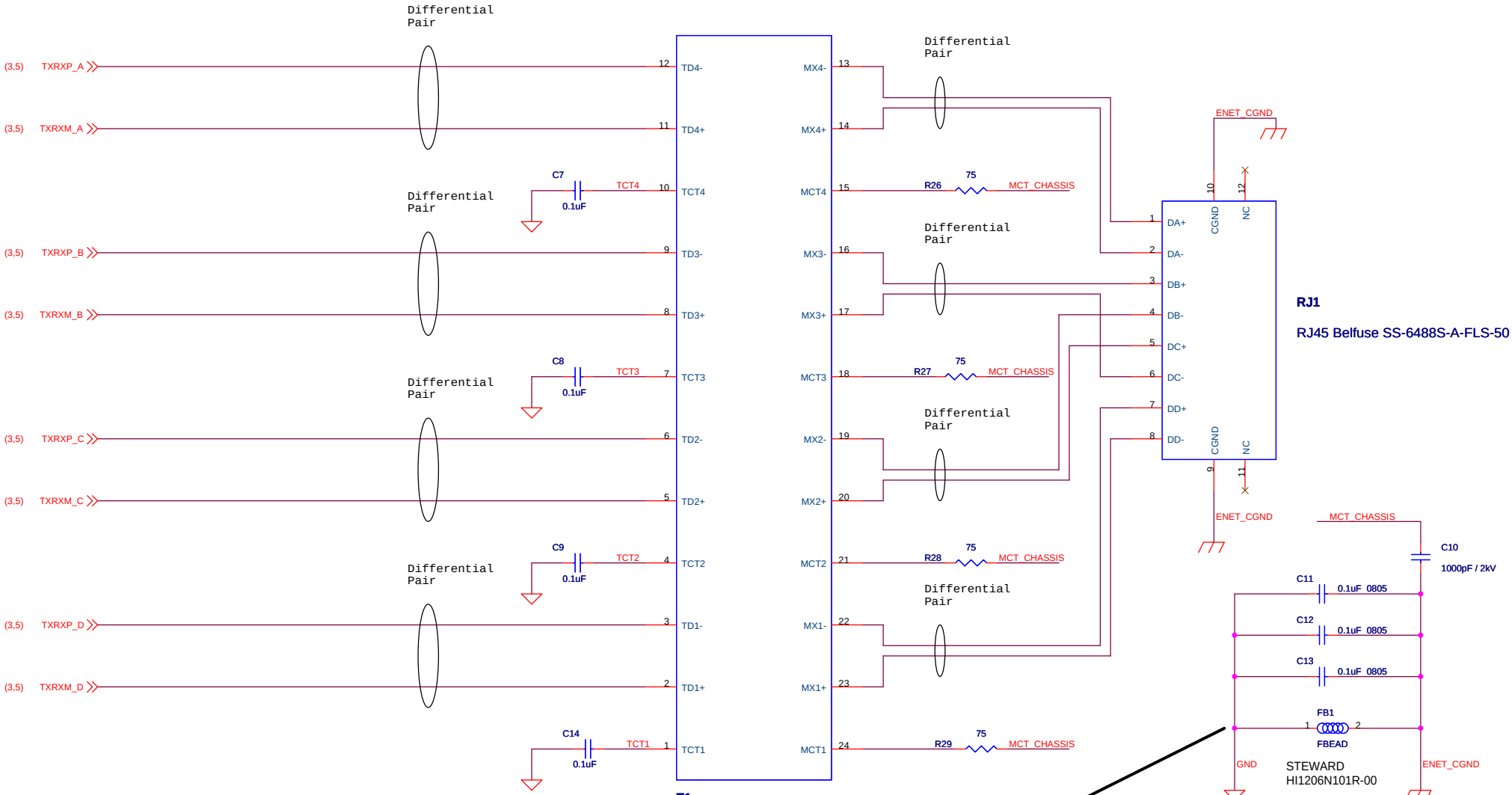

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Size	Document Number: RJ-45 Connector / Pulse H5007NL Transformer	Rev: 1.1
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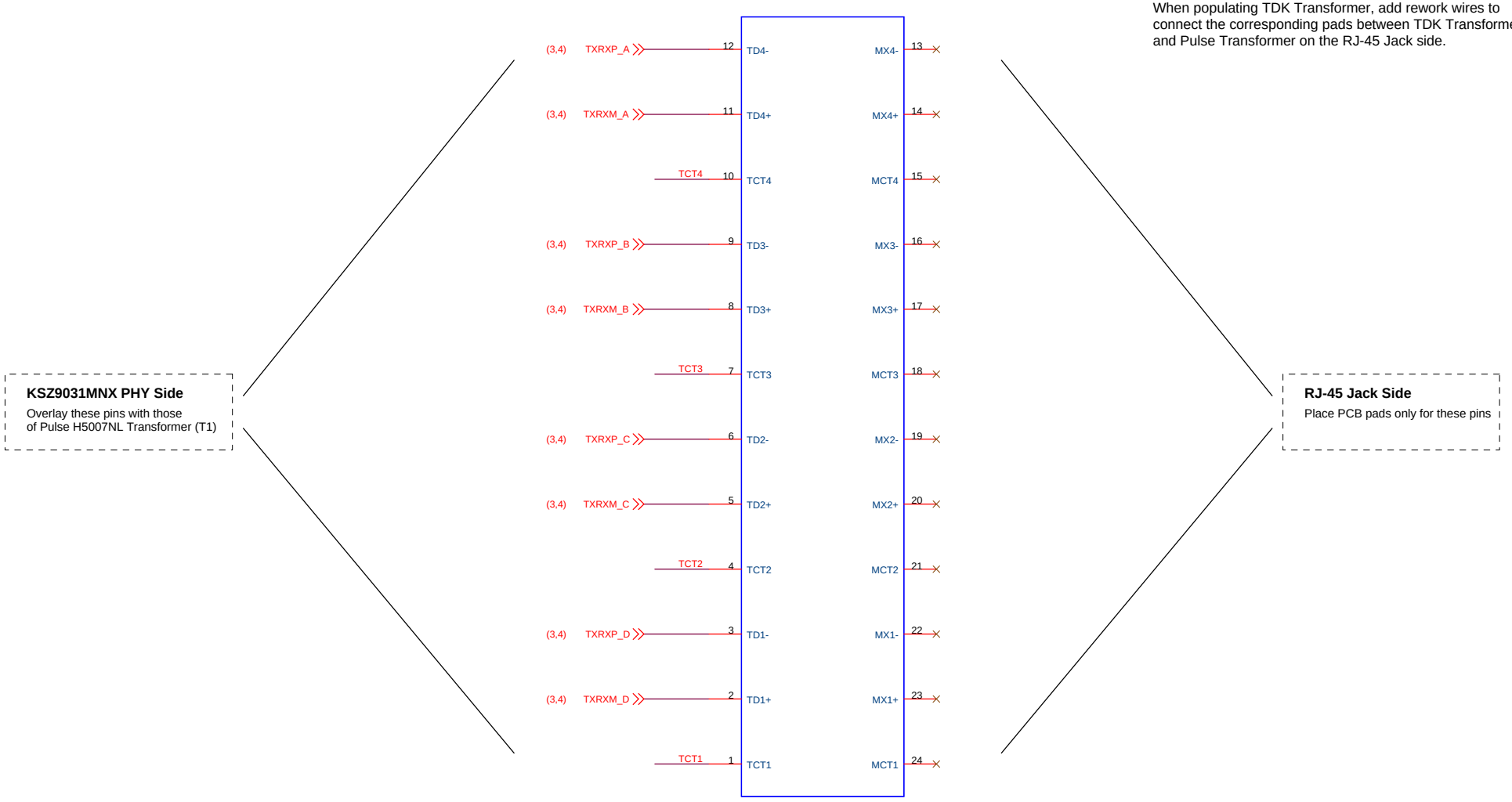
TDK TLA-7T101LF Transformer Option

TDK Transformer has the same pinouts as the Pulse H5007NL (T1), but is narrower.

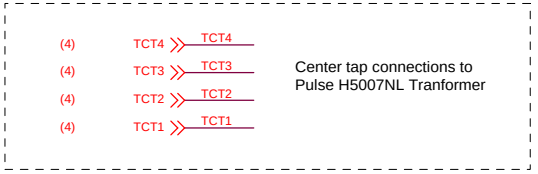
Layout TDK Transformer as detailed on this page.

When populating TDK Transformer, add rework wires to connect the corresponding pads between TDK Transformer and Pulse Transformer on the RJ-45 Jack side.



T2

TDK TLA-7T101LF Transformer



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USB Port - MDC/MDIO Register Access

DC_IN +(5V to 12V) DC INPUT

U5 MIC5207-5.0YM5

MIC5207-5.0YM5 has very low dropout voltage (typically 165mV @ 150mA).

FTDI FT2232D can operate down to +4.35V for its 5V input power (5V_USB).

STEWARD HI1206N101R-00

U6 - FTDI FT2232D Decouple Pins (3, 42)

U6 - FTDI FT2232D Decouple Pins (14, 31)

U6 FTDI FT2232D

MDC/MDIO Voltage Translator option when DVDDH=1.8V or 2.5V

U7 TI PCA9306

Jumper setting:
ON: DVDDH=3.3V without MDC/MDIO voltage translator option
OFF: DVDDH=1.8V or 2.5V with MDC/MDIO voltage translator option

USB Configuration
* Self Power
* Multi-Protocol Synchronous Serial Engine (MPSSE) Mode

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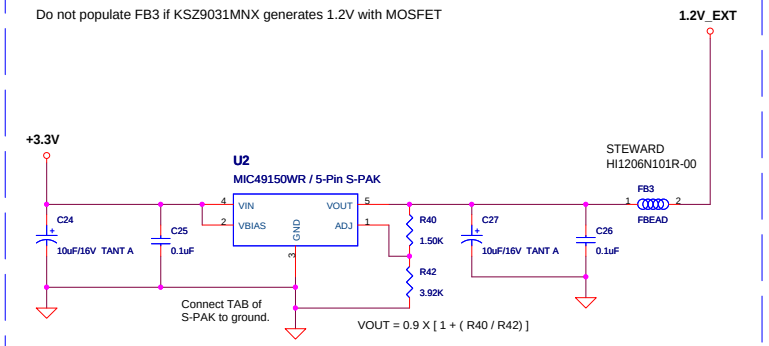
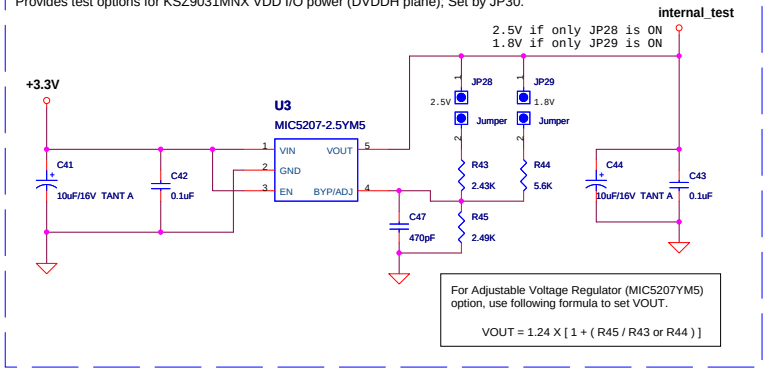
1.2V Power option

Do not populate FB3 if KSZ9031MNX generates 1.2V with MOSFET

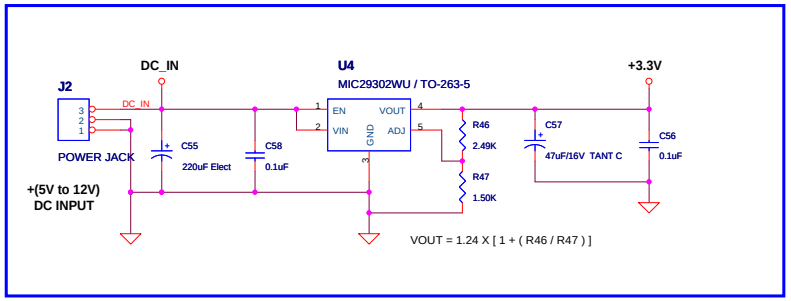


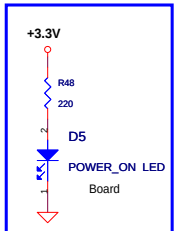
VDD I/O (DVDDH) Test Option

Provides test options for KSZ9031MNX VDD I/O power (DVDDH plane); Set by JP30.



+(5V to 12V) DC Input

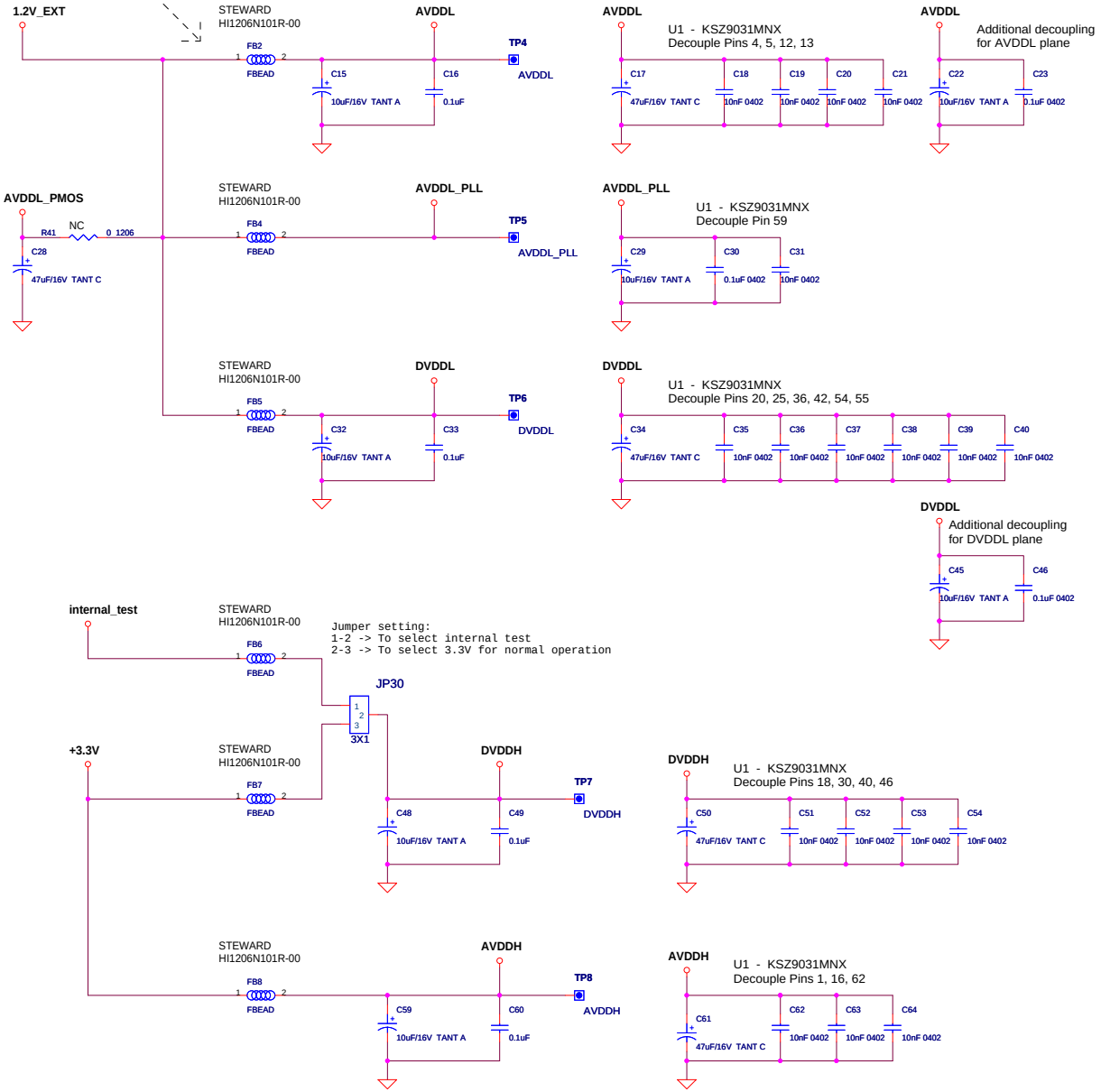




Place GND test points evenly across PCB.

TP9 GND TP10 GND TP11 GND TP12 GND

AVDDL is the feedback for the KSZ9031MNX on-chip LDO controller.
Change FB2 from ferrite bead to 0 Ohm when PMOS (Q1) is populated.



MICREL

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