19-5040; Rev 1; 6/10

6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

General Description

The MAX16068 flash-configurable system manager monitors and manages up to six system voltages simultaneously. The MAX16068 integrates an analog-to-digital converter (ADC). Device configuration information, including overvoltage and undervoltage limits, time delay settings is stored in nonvolatile flash memory. During a fault condition, fault flags and channel voltages can be automatically stored in the nonvolatile flash memory for later readback.

The internal 1% accurate, 10-bit ADC measures each input and compares the result to one overvoltage and one undervoltage limit. A fault signal asserts when a monitored voltage falls outside the set limits.

The MAX16068 supports a power-supply voltage of up to 14V and can be powered directly from the 12V intermediate bus in many systems.

The MAX16068 includes six programmable general-purpose inputs/outputs (GPIOs). GPIOs are flash configurable as a fault output, as a watchdog input or output, or as a manual reset.

The MAX16068 features nonvolatile fault memory for recording information during system shutdown events. The fault logger records a failure in the internal flash and sets a lock bit protecting the stored fault data from accidental erasure.

An SMBus™ or a JTAG serial interface configures the MAX16068. The MAX16068 is available in a 28-pin, 5mm x 5mm, TQFN package and is fully specified over the -40°C to +85°C extended temperature range.

Features

- **Operates from 2.8V to 14V**
- **1% Accurate, 10-Bit ADC Monitors 6 Voltage Inputs**
- **Analog EN Monitoring Input**
- **6 Monitored Inputs with Overvoltage and Undervoltage Limits**
- **Nonvolatile Fault Event Logger**
- **Six General-Purpose Inputs/Outputs Configurable as:**
  - **Dedicated Fault Output**
  - **Watchdog Timer Function**
  - **Manual Reset**
  - **SMBus Alert**
  - **Fault Propagation Input/Output**
- **SMBus and JTAG Interface**
- **Supports Cascading with MAX16065/MAX16066**
- **Flash-Configurable Time Delays and Thresholds**
- **-40°C to +85°C Extended Operating Temperature Range**

Applications

Networking Equipment

Telecom Equipment (Base Stations, Access)

Storage/RAID Systems

Servers

Typical Operating Circuit appears at end of data sheet.

Ordering Information/Selector Guide

PART	PIN-PACKAGE	VOLTAGE-DETECTOR INPUTS	GENERAL-PURPOSE INPUTS/ OUTPUTS
MAX16068ETI+	28 TQFN-EP*	6	6

Note: *This device is specified over the -40°C to +85°C extended temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

SMBus is a trademark of Intel Corp.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +15V
MON_, SCL, SDA, A0 to GND .....-0.3V to +6V
EN, TCK, TMS, TDI to GND .....-0.3V to +4V
TDO to GND .....-0.3V to (V_{DBP} + 0.3V)
RESET, GPIO_
(configured as open-drain) to GND.....-0.3V to +6V
RESET, GPIO_ (configured as push-pull)
to GND .....-0.3V to (V_{DBP} + 0.3V)
DBP, ABP to GND .....-0.3V to minimum of (4V and (V_{CC} + 0.3V))
Continuous Current (all pins) ..... ±20mA

*As per JEDEC 51 Standard, Multilayer Board (PCB).

Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C)..... 2759mW*
Thermal Resistance (Note 1)
θ_{JA}.....29°C/W
θ_{JC} ..... 2°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.8V to 14V, T_A = T_J = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	RESET output asserted low	1.2			V
			2.8		14	
Undervoltage Lockout	V_{UVLO}	Minimum voltage on V_{CC} to ensure the device is flash configurable			2.7	V
Undervoltage Lockout Hysteresis	$UVLO_{HYS}$			55		mV
Minimum Flash Operating Voltage	V_{FLASH}	Minimum voltage on V_{CC} to ensure flash erase and write operations	2.7			V
Supply Current	I_{CC1}	No load on any output		2.8	4	mA
	I_{CC2}	No load on any output, during flash writing cycle		7.7	14	
		V_{CC} = V_{ABP} = V_{DBP} = 3.6V (Note 3)			5	
DBP Regulator Voltage	V_{DBP}	V_{CC} = 5V, C_{DBP} = 1µF, no load	2.8	3	3.2	V
ABP Regulator Voltage	V_{ABP}	V_{CC} = 5V, C_{ABP} = 1µF, no load	2.85	3	3.15	V
Boot Time	t_{BOOT}	V_{CC} > V_{UVLO}		100	200	µs
Flash Writing Time		8-byte word		122		ms
Internal Timing Accuracy		(Note 4)	-10		+10	%
ADC						
Resolution				10		Bits
Gain Error	ADC_{GAIN}	T_A = +25°C			0.35	%
		T_A = -40°C to +85°C			0.75	
Offset Error	ADC_{OFF}				1.5	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = T_J = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Integral Nonlinearity	ADC_{INL}				1	LSB
Differential Nonlinearity	ADC_{DNL}				1	LSB
ADC Total Monitoring Cycle Time	t_{CYCLE}	Monitoring all 6 inputs, no MON_ fault detected		24	30	µs
ADC MON_ Ranges	ADC_{RNG}	MON_ range set to '00'		5.552		V
		MON_ range set to '01'		2.776		
		MON_ range set to '10'		1.388		
ADC LSB Step Size	ADC_{LSB}	MON_ range set to '00'		5.42		mV
		MON_ range set to '01'		2.71		
		MON_ range set to '10'		1.35		
ADC Input Leakage Current					1	µA
ENABLE INPUT (EN)						
EN Input-Voltage Threshold	$V_{TH_EN_R}$	EN voltage rising		1.24		V
	$V_{TH_EN_F}$	EN voltage falling	1.195	1.215	1.235	
EN Input Current	I_{EN}		-0.5		+0.5	µA
EN Input-Voltage Range			0		3.6	V
OUTPUTS (RESET, GPIO_)						
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
		I_{SINK} = 10mA, GPIO_ only			0.7	
		V_{CC} = 1.2V, I_{SINK} = 100µA (RESET only)			0.3	
Maximum Output Sink Current		Total current into RESET, GPIO_, V_{CC} = 3.3V		18		mA
Output-Voltage High (Push-Pull)	V_{OH}	I_{SOURCE} =100µA	2.4			V
Output Leakage Current (Open-Drain)	I_{OUT_LKG}				1	µA
INPUTS (A0, GPIO_)						
Input Logic-Low	V_{IL}				0.8	V
Input Logic-High	V_{IH}		20			V
WDI Pulse Width	t_{WDI}		100			ns
$\overline{MR}$ Pulse Width	t_{MR}		2			µs
SMBus INTERFACE						
Logic-Input Low Voltage	V_{IL}	Input voltage falling			0.8	V
Logic-Input High Voltage	V_{IH}	Input voltage rising	2.0			V
Input Leakage Current		V_{CC} shorted to GND, $V_{MON_}$ = 0 or 6V	-1		+1	µA
Output Sink Current	V_{OL}	I_{SINK} = 3mA			0.4	V
Input Capacitance	C_{IN}			5		pF

6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = T_J = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SMBus TIMING							
Serial Clock Frequency	f_{SCL}					400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}			1.3			µs
START Condition Setup Time	$t_{SU:STA}$			0.6			µs
START Condition Hold Time	$t_{HD:STA}$			0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$			0.6			µs
Clock Low Period	t_{LOW}			1.3			µs
Clock High Period	t_{HIGH}			0.6			µs
Data Setup Time	$t_{SU:DAT}$			100			ns
Output Fall Time	t_{OF}	10pF ≤ C_{BUS} ≤ 400pF				250	ns
Data Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	Receive	0.15			µs
			Transmit	0.3		0.9	
Pulse Width of Spike Suppressed	t_{SP}				250		ns
SMBus Timeout	$t_{TIMEOUT}$	SMBCLK time low for reset		22		35	ms
JTAG INTERFACE							
TDI, TMS, TCK Logic-Low Input Voltage	V_{IL}	Input voltage falling				0.8	V
TDI, TMS, TCK Logic-High Input Voltage	V_{IH}	Input voltage rising		2.0			V
TDO Logic-Output Low Voltage	V_{OL_TDO}	I_{SINK} = 3mA				0.4	V
TDO Logic-Output High Voltage	V_{OH_TDO}	I_{SOURCE} = 200µA		2.4			V
TDI, TMS Pullup Resistors	R_{JPU}	Pullup to DBP		30	50	65	kΩ
I/O Capacitance	$C_{I/O}$				5		pF
TCK Clock Period	t_1					1000	ns
TCK High/Low Time	t_2, t_3			50	500		ns
TCK to TMS, TDI Setup Time	t_4			15			ns
TCK to TMS, TDI Hold Time	t_5			15			ns
TCK to TDO Delay	t_6					500	ns
TCK to TDO High-Z Delay	t_7					500	ns

Note 2: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.

Note 3: For V_{CC} of 3.6V or lower, connect V_{CC}, DBP, and ABP together. For higher supply applications, connect only V_{CC} to the supply rail.

Note 4: Applies to RESET (except for a reset timeout period of 25µs), fault, autoretry, sequence delays, and watchdog timeout.

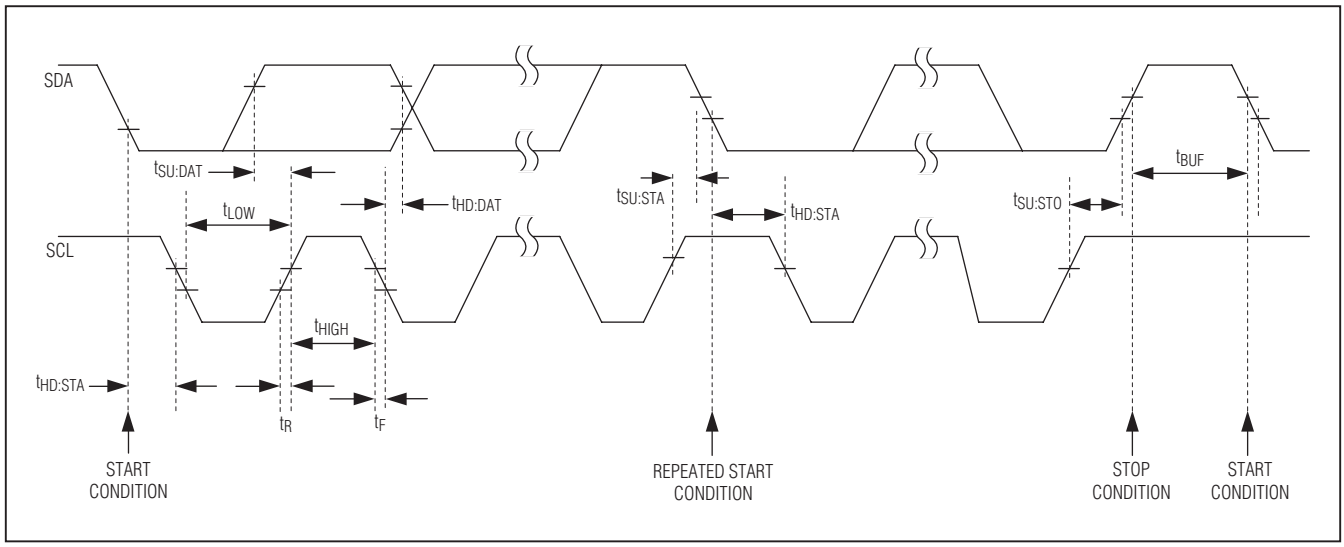


Figure 1. SMBus Timing Diagram

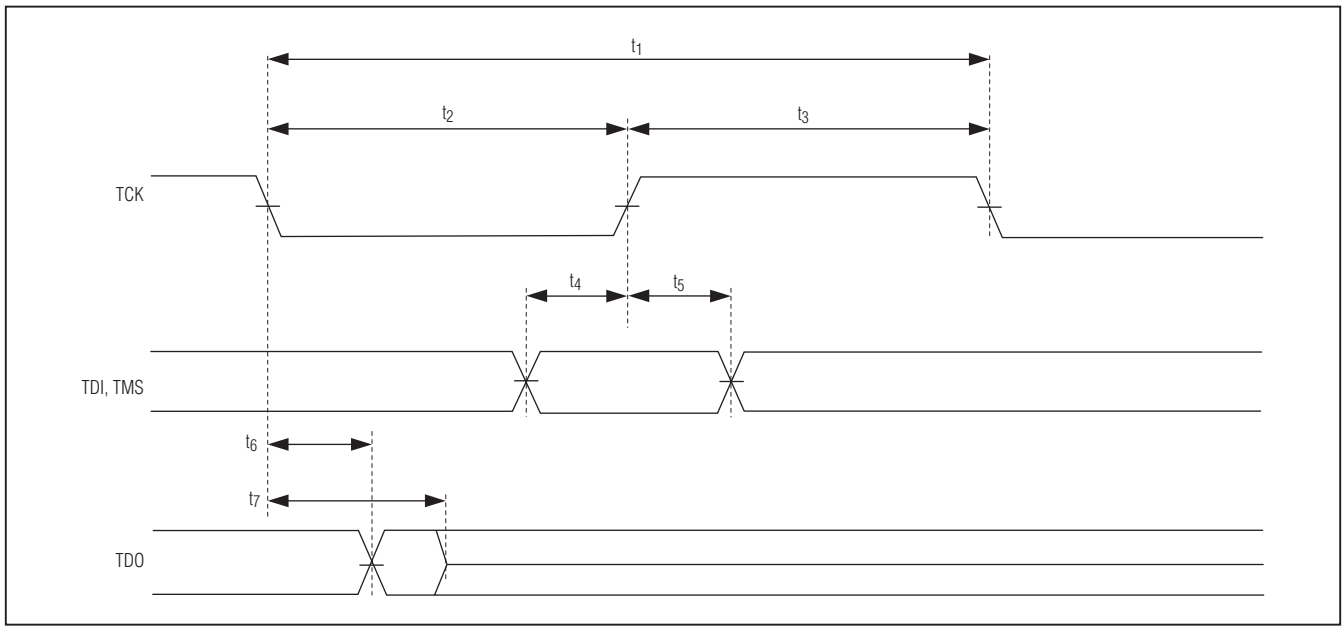


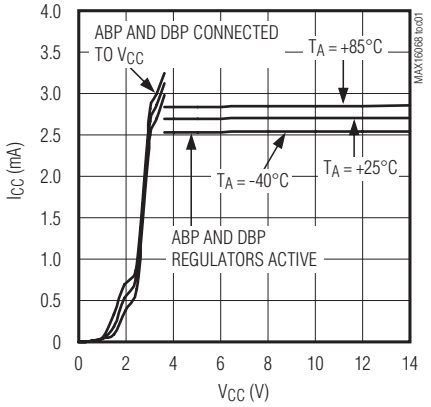
Figure 2. JTAG Timing Diagram

6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

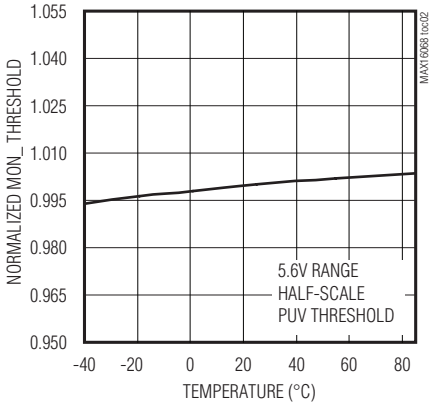
Typical Operating Characteristics

(Typical values are at V_{CC} = 3.3V, T_A = +25°C.)

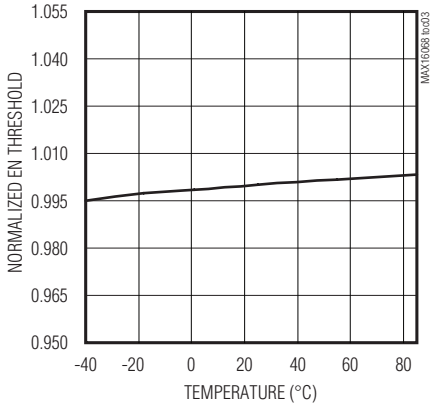
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE



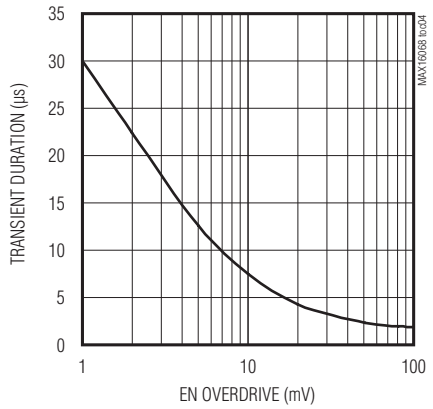
NORMALIZED MON_THRESHOLD vs. TEMPERATURE



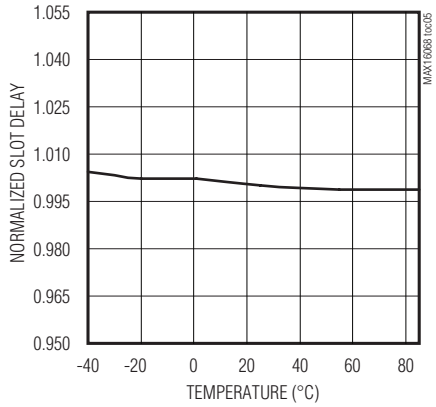
NORMALIZED EN THRESHOLD vs. TEMPERATURE



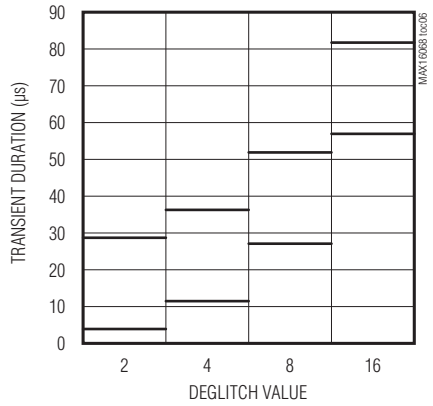
TRANSIENT DURATION vs. THRESHOLD OVERDRIVE (EN)



NORMALIZED TIMING ACCURACY vs. TEMPERATURE



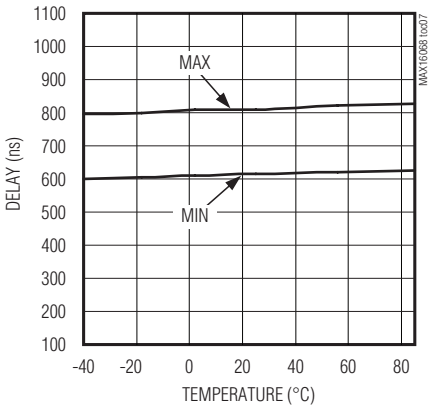
TRANSIENT DURATION vs. MON_ DEGLITCH



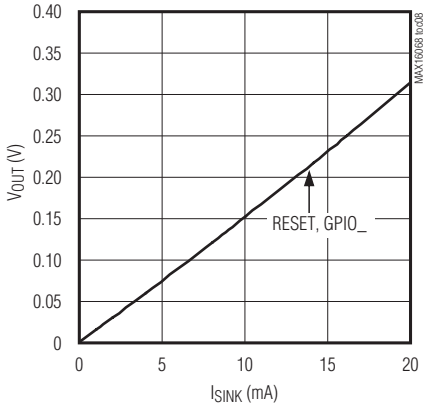
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = 3.3V, T_A = +25°C.)

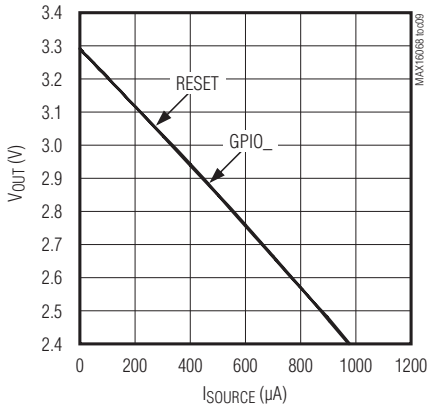
$\overline{MR}$ TO RESET PROPAGATION DELAY vs. TEMPERATURE



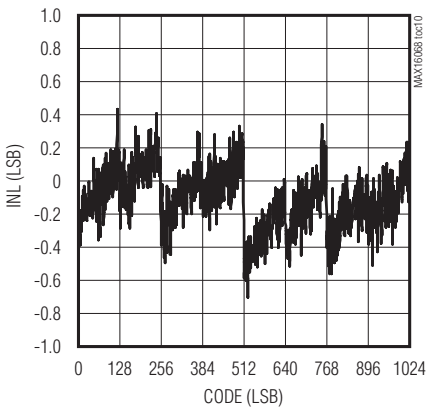
OUTPUT VOLTAGE vs. SINK CURRENT (OUT = LOW)



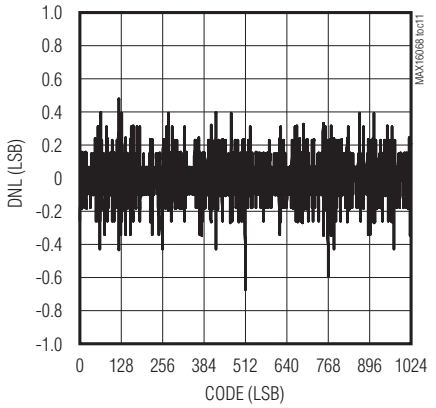
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (PUSH-PULL OUTPUT)



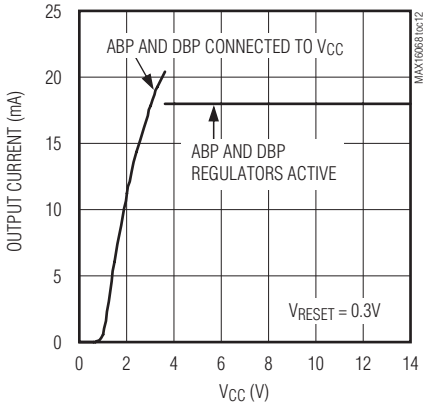
INTEGRAL NONLINEARITY vs. CODE



DIFFERENTIAL NONLINEARITY vs. CODE

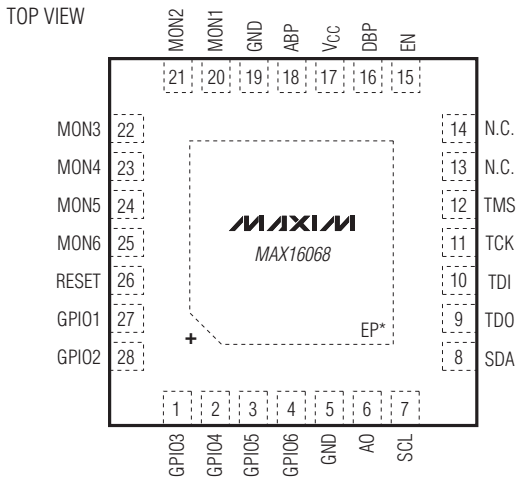


RESET OUTPUT CURRENT vs. V_{CC} SUPPLY VOLTAGE



6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

Pin Configuration



THIN QFN
(5mm x 5mm)

*CONNECT EXPOSED PAD TO GND.

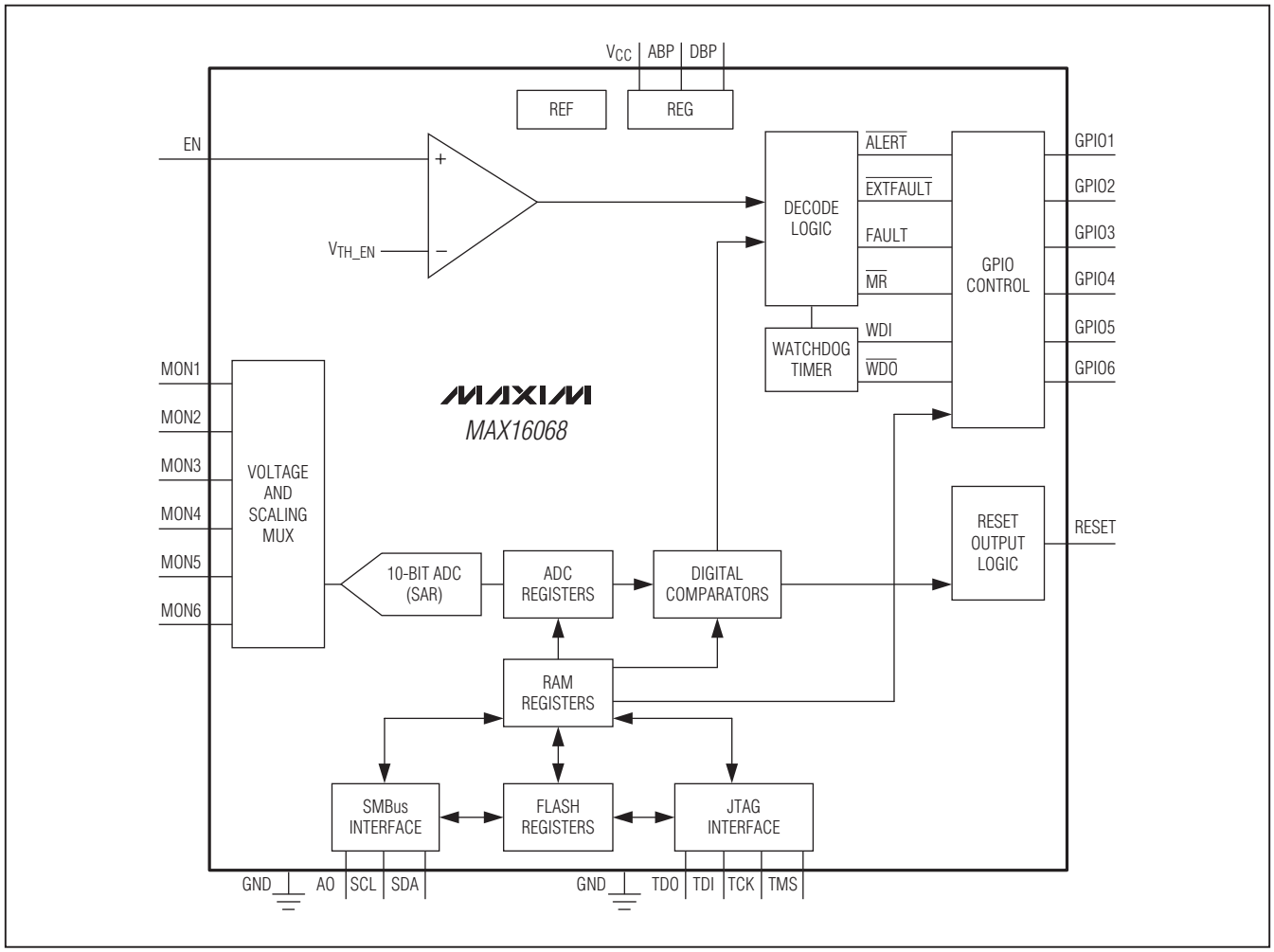
Pin Description

PIN	NAME	FUNCTION
1–4, 27, 28	GPIO3–GPIO6, GPIO1, GPIO2	General-Purpose Inputs/Outputs. Each GPIO_ can be configured to act as an input, a push-pull output, an open-drain output, or a special function.
5, 19	GND	Ground. Connect all GNDs together.
6	A0	Four-State SMBus Address. Address is sampled upon POR.
7	SCL	SMBus Serial-Clock Input
8	SDA	SMBus Serial-Data Open-Drain Input/Output
9	TDO	JTAG Test Data Output
10	TDI	JTAG Test Data Input
11	TCK	JTAG Test Clock
12	TMS	JTAG Test Mode Select
13, 14	N.C.	No Connection. Not internally connected.
15	EN	Analog Enable Input. All outputs deassert when V_{EN} is below the enable threshold.

Pin Description (continued)

PIN	NAME	FUNCTION
16	DBP	Digital Bypass. All push-pull outputs are referenced to DBP. Bypass DBP with a 1µF capacitor to GND.
17	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 10µF ceramic capacitor.
18	ABP	Analog Bypass. Bypass ABP to GND with a 1µF ceramic capacitor.
20–25	MON1–MON6	Monitor Voltage Inputs. Set the monitor voltage range through the configuration registers. Measured values are written to the ADC registers and can be read back through the SMBus or JTAG interface.
26	RESET	Configurable Reset Output
—	EP	Exposed Pad. Internally connected to GND. Connect to ground, but do not use EP as the main ground connection.

Functional Diagram



6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

Detailed Description

The MAX16068 monitors up to six system power supplies. The monitoring phase begins after boot-up if EN is high and the software enable bit is set to '1'. An internal multiplexer cycles through each MON_ input. At each multiplexer stop, the 10-bit ADC converts the monitored analog voltage to a digital result and stores the result in a register. Each time a conversion cycle (5µs, max) completes, internal logic circuitry compares the conversion results to the overvoltage and undervoltage thresholds stored in memory. When a result violates a programmed threshold, the conversion can be configured to generate a fault. GPIO_ can be programmed to assert on combinations of faults. Additionally, faults can be configured to trigger the nonvolatile fault logger, which writes all fault information automatically to the flash and write-protects the data to prevent accidental erasure.

The MAX16068 contains both SMBus and JTAG serial interfaces for accessing registers and flash. Use only one interface at any given time. For more information on how to access the internal memory through these interfaces, see the *SMBus-Compatible Serial Interface* and *JTAG Serial Interface* sections. The memory map is divided into three pages with access controlled by special SMBus and JTAG commands.

The factory-default values at POR (power-on reset) for all RAM registers are '0's. POR occurs when V_{CC} reaches the undervoltage-lockout threshold (UVLO) of 2.7V (max). At POR, the device begins a boot-up sequence. During the boot-up sequence, all monitored inputs are masked from initiating faults and flash contents are copied to the respective register locations. During boot-up, the MAX16068 is not accessible through the serial interface. The boot-up sequence takes up to 150µs, after which the device is ready for normal operation. RESET is asserted low up to the boot-up phase after which it assumes its programmed active state. RESET remains active for its programmed timeout period once all monitored channels are within their respective thresholds. Up to the boot-up phase, the GPIO_s are high impedance.

Power

Apply 2.8V to 14V to V_{CC} to power the MAX16068. Bypass V_{CC} to ground with a 10µF capacitor. Two internal voltage regulators, ABP and DBP, supply power to the analog and digital circuitry within the device. For operation at 3.6V or lower, disable the regulators by connecting ABP and DBP to V_{CC}.

ABP is a 3.0V (typ) voltage regulator that powers the internal analog circuitry. Bypass ABP to GND with a 1µF ceramic capacitor installed as close as possible to the device.

DBP is an internal 3.0V (typ) voltage regulator. DBP powers flash and digital circuitry. All push-pull outputs refer to DBP. DBP supplies the input voltage to the internal charge pump when the programmable outputs are configured as charge-pump outputs. Bypass the DBP output to GND with a 1µF ceramic capacitor installed as close as possible to the device.

Do not power external circuitry from ABP or DBP.

Enable Input (EN)

To enable monitoring, the voltage at EN must be above 1.24V (typ) and the software enable bit in r73h[0] must be set to '1.' To disable monitoring, either pull EN below 1.215V (typ) or set the software enable bit to '0.' See Table 1 for the software enable bit configurations. Connect EN to ABP if not used.

Table 1. Software Enable Configurations

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
73h	273h	[0]	Software Enable 1 = Sequencing enabled 0 = Power-down
		[1]	Reserved
		[2]	1 = Margin mode enabled
		[3]	Reserved
		[4]	Independent watchdog mode enable 1 = Watchdog timer is independent of EN input 0 = Watchdog timer boots after EN goes high and the boot-up delay completes

When in the monitoring state, and when EN falls below the undervoltage threshold, a register bit, ENRESET (r20h[2]), is set to a '1.' This register bit latches and must be cleared through software. This bit indicates if RESET is asserted low due to EN going under the threshold. The POR state of ENRESET is '0.' The bit is only set on a falling edge of the EN comparator output or the software enable bit. If operating in latch-on fault mode, toggle EN or toggle the software enable bit to clear the latch condition and restart the device once the fault condition has been removed.

Set r73h[2] to '1' to enable monitoring functionality. Faults are not recorded when the device is in margining mode. Set r73h[2] to '0' for normal functionality.

Voltage Monitoring

The MAX16068 features an internal 10-bit ADC that monitors the MON_ voltage inputs. An internal multiplexer cycles through each of the enabled inputs, taking less than 24µs for a complete monitoring cycle. Each acquisition takes approximately 4µs. At each multiplexer stop, the 10-bit ADC converts the analog input to a digital result and stores the result in a register. ADC conversion results are stored in registers r00h–r0Bh (see Table 2). Use the SMBus or JTAG serial interface to read ADC conversion results.

The MAX16068 provides six inputs, MON1–MON6, for voltage monitoring. Each input-voltage range is programmable in registers r43h–r44h (see Table 3). When MON_ configuration registers are set to '11,' MON_ voltages are not monitored and the multiplexer does not stop at these inputs, decreasing the total cycle time. These inputs cannot be configured to trigger fault conditions.

The two programmable thresholds for each monitored voltage include an overvoltage and an undervoltage threshold. See the *Faults* section for more information on setting overvoltage and undervoltage thresholds. All voltage thresholds are 8 bits wide. The 8 MSBs of the 10-bit ADC conversion result are compared to these overvoltage and undervoltage thresholds.

For any undervoltage or overvoltage condition to be monitored and any faults detected, the MON_ input must be assigned to monitoring mode. Inputs that are not enabled are not converted by the ADC; they contain the last value acquired before that channel was disabled. The ADC conversion result registers are reset to 00h at boot-up. These registers are not reset when a reboot command is executed.

To temporarily disable voltage monitoring during voltage margining conditions, set r73h[2] to '1' to enable margining mode functionality. Faults (except for faults triggered by $\overline{\text{EXTFAULT}}$ being pulled low externally) are not recorded when the device is in margining mode, but the ADC continues to run and conversion results continue to be available. Set r73h[2] back to '0' for normal functionality.

Table 2. ADC Conversion Results (Read Only)

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
00h	[7:0]	MON1 result (MSB)
01h	[7:6]	MON1 result (LSB)
02h	[7:0]	MON2 result (MSB)
03h	[7:6]	MON2 result (LSB)
04h	[7:0]	MON3 result (MSB)
05h	[7:6]	MON3 result (LSB)
06h	[7:0]	MON4 result (MSB)
07h	[7:6]	MON4 result (LSB)
08h	[7:0]	MON5 result (MSB)
09h	[7:6]	MON5 result (LSB)
0Ah	[7:0]	MON6 result (MSB)
0Bh	[7:6]	MON6 result (LSB)

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Table 3. ADC Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
43h	243h	[1:0]	MON1 Full-Scale Range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	MON2 Full-Scale Range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	MON3 Full-Scale Range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	MON4 Full-Scale Range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
44h	244h	[1:0]	MON5 Full-Scale Range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	MON6 Full-Scale Range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:4]	Not used

Boot-Up Delay

Once EN is above its threshold and the software enable bit is set, a boot-up delay occurs before monitoring begins. This delay is configured in register r77h as shown in Table 4, and it is stored as an 8-bit value calculated as follows:

$$t_{BOOT} = (5 \times 10^{-6}) \times 2^{a} \times (16 + b) + 480\mu s$$

where t_{BOOT} is in seconds, a is the decimal value of the 4 MSBs and b is the decimal value of the 4 LSBs.

Table 4. Boot-Up Delay

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
77h	277h	[7:0]	Boot-up delay

General-Purpose Inputs/Outputs

GPIO1–GPIO6 are programmable general-purpose inputs/outputs. GPIO1–GPIO6 are configurable as a manual reset input, a watchdog timer input and output, logic inputs/outputs, and fault-dependent outputs. When programmed as outputs, GPIO_s are open-drain or push-pull. See Tables 5 and 6 for more detailed information on configuring GPIO1–GPIO6.

When GPIO1–GPIO6 are configured as general-purpose inputs/outputs, read values from the GPIO_ ports through r1Eh and write values to GPIO_s through r3Eh. Note that r3Eh has a corresponding flash register, which programs the default state of a general-purpose output. See Table 7 for more information on reading and writing to the GPIO_.

Table 5. GPIO_ Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
3Fh	23Fh	[1:0]	GPIO1 configuration
		[3:2]	GPIO2 configuration
		[5:4]	GPIO3 configuration
		[7:6]	GPIO4 configuration
40h	240h	[1:0]	GPIO5 configuration
		[3:2]	GPIO6 configuration
		[4]	ARAEN bit
		[7:5]	Not used

Table 6. GPIO_ Function Configuration Bits

	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6
00	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input
01	Logic output (push-pull)	Logic output (push-pull)	Logic output (push-pull)	Logic output (push-pull)	Logic output (push-pull)	Logic output (push-pull)
10	Logic output (open drain)	Logic output (open drain)	Logic output (open drain)	Logic output (open drain)	Logic output (open drain)	Logic output (open drain)
11	$\overline{\text{ALERT}}$ (open drain)	FAULT (open drain)	$\overline{\text{MR}}$ input	WDI	$\overline{\text{WDO}}$ (open drain)	$\overline{\text{EXTFAULT}}$ (open drain)

Table 7. GPIO_ State Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
1Eh	—	[0]	GPIO1 input state
		[1]	GPIO2 input state
		[2]	GPIO3 input state
		[3]	GPIO4 input state
		[4]	GPIO5 input state
		[5]	GPIO6 input state
		[7:6]	Not used
3Eh	23Eh	[0]	GPIO1 output state
		[1]	GPIO2 output state
		[2]	GPIO3 output state
		[3]	GPIO4 output state
		[4]	GPIO5 output state
		[5]	GPIO6 output state
		[7:6]	Not used

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ALERT

GPIO1 is configurable as the SMBus alert signal, ALERT. ALERT asserts when any fault condition occurs. When the SMBus host sends the ARA (Alert Response Address), the MAX16068 responds with its slave address and deasserts ALERT. ALERT is an open-drain output.

Set the ARAEN bit in r40h[4] to '1' to disable the ARA feature. Under these conditions, the device does not respond to an ARA on the SMBus line.

FAULT

GPIO2 is configurable as a dedicated fault output, FAULT. FAULT asserts when an overvoltage or undervoltage condition occurs on the selected inputs. FAULT dependencies are set using registers r36h and r37h (see Table 8). When FAULT depends on more than one MON_, the fault output asserts when one or more MON_ exceeds a programmed threshold voltage. FAULT acts independently of the critical fault system, described in the *Critical Faults* section. Use r37h[7] to set the polarity of FAULT.

Manual Reset (MR)

GPIO3 is configurable to act as an active-low manual reset input, MR. Drive MR low to assert RESET. RESET remains asserted for the selected reset timeout period after MR transitions from low to high. When connecting MR to a pushbutton, use a pullup resistor. See the *Reset Output* section for more information on selecting a reset timeout period.

Watchdog Input (WDI) and Output (WDO)

GPIO4 and GPIO5 are configurable as the watchdog timer input (WDI) and output, WDO, respectively. See Table 16 for configuration details. WDO is an open-drain, active-low output. See the *Watchdog Timer* section for more information about the operation of the watchdog timer.

External Fault (EXTFAULT)

GPIO6 is configurable as the external fault input/output, EXTFAULT. EXTFAULT asserts if any monitored voltage exceeds an overvoltage or undervoltage threshold. EXTFAULT also asserts if a power-up or power-down sequencing fault occurs. This signal can be used to cascade multiple MAX16068s.

For the MAX16068, if register bit r6Dh[2] is set in addition to r72h[5], EXTFAULT going low triggers a nonvolatile fault log operation.

Table 8. FAULT Dependencies

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
36h	236h	[0]	FAULT depends on MON1 undervoltage threshold
		[1]	FAULT depends on MON2 undervoltage threshold
		[2]	FAULT depends on MON3 undervoltage threshold
		[3]	FAULT depends on MON4 undervoltage threshold
		[4]	FAULT depends on MON5 undervoltage threshold
		[5]	FAULT depends on MON6 undervoltage threshold
		[7:6]	Not used
37h	237h	[0]	FAULT depends on MON1 overvoltage threshold
		[1]	FAULT depends on MON2 overvoltage threshold
		[2]	FAULT depends on MON3 overvoltage threshold
		[3]	FAULT depends on MON4 overvoltage threshold
		[4]	FAULT depends on MON5 overvoltage threshold
		[5]	FAULT depends on MON6 overvoltage threshold
		[6]	Not used
		[7]	0 = FAULT is an active-low digital output 1 = FAULT is an active-high digital output

Faults

The MAX16068 monitors the input (MON_) channels and compares the results with an overvoltage threshold and an undervoltage threshold. Based on these conditions, the MAX16068 asserts various fault outputs and save specific information about the channel conditions and voltages into the nonvolatile flash. Once a critical fault event occurs, the failing channel condition, ADC conversions at the time of the fault, or both can be saved by configuring the event logger. The event logger records a single failure in the internal flash and sets a lock bit that protects the stored fault data from accidental erasure on a subsequent power-up.

The MAX16068 is capable of measuring overvoltage and undervoltage fault events. Fault conditions are detected at the end of each ADC conversion. An overvoltage event occurs when the voltage at a monitored input exceeds the overvoltage threshold for that input. An undervoltage event occurs when the voltage at a monitored input falls below the undervoltage threshold. Fault thresholds are set in registers r49h–r59h as shown in Table 9. Disabled inputs are not monitored for fault conditions and are skipped over by the input multiplexer. Only the upper 8 bits of a conversion result are compared with the programmed fault thresholds.

Table 9. Fault Threshold Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
48h	248h	[7:0]	Not used
49h	249h	[7:0]	MON1 overvoltage threshold
4Ah	24Ah	[7:0]	MON1 undervoltage threshold
4Bh	24Bh	[7:0]	Not used
4Ch	24Ch	[7:0]	MON2 overvoltage threshold
4Dh	24Dh	[7:0]	MON2 undervoltage threshold
4Eh	24Eh	[7:0]	Not used
4Fh	24Fh	[7:0]	MON3 overvoltage threshold
50h	250h	[7:0]	MON3 undervoltage threshold
51h	251h	[7:0]	Not used
52h	252h	[7:0]	MON4 overvoltage threshold
53h	253h	[7:0]	MON4 undervoltage threshold
54h	254h	[7:0]	Not used
55h	255h	[7:0]	MON5 overvoltage threshold
56h	256h	[7:0]	MON5 undervoltage threshold
57h	257h	[7:0]	Not used
58h	258h	[7:0]	MON6 overvoltage threshold
59h	259h	[7:0]	MON6 undervoltage threshold

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Deglitch

Fault conditions are detected at the end of each conversion. When the voltage on an input falls outside a monitored threshold for one acquisition, the input multiplexer remains on that channel and performs several successive conversions. To trigger a fault, the input must stay outside the threshold for a certain number of acquisitions as determined by the deglitch setting in r74h[6:5] (see Table 10).

Fault Flags

Fault flags indicate the fault status of a particular input. The fault flag of any monitored input in the device can be read at any time from registers r1Bh and r1Ch, as shown in Table 11. Clear a fault flag by writing a '1' to the appropriate bit in the flag register. Unlike the fault signals sent to the fault outputs, these bits are masked by the critical fault enable bits (see Table 12). The fault flag is only set when the matching enable bit in the critical fault enable register is also set.

Table 10. Deglitch Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
74h	274h	[6:5]	Voltage Comparator Deglitch Configuration 00 = 2 cycles 01 = 4 cycles 10 = 8 cycles 11 = 16 cycles

Table 11. Fault Flags

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
1Bh	[0]	MON1 undervoltage threshold
	[1]	MON2 undervoltage threshold
	[2]	MON3 undervoltage threshold
	[3]	MON4 undervoltage threshold
	[4]	MON5 undervoltage threshold
	[5]	MON6 undervoltage threshold
	[7:6]	Reserved
1Ch	[0]	MON1 overvoltage threshold
	[1]	MON2 overvoltage threshold
	[2]	MON3 overvoltage threshold
	[3]	MON4 overvoltage threshold
	[4]	MON5 overvoltage threshold
	[5]	MON6 overvoltage threshold
	[6]	External fault ($\overline{\text{EXTFAULT}}$)
	[7]	SMB alert

If GPIO6 is configured as the $\overline{\text{EXTFAULT}}$ input/output and $\overline{\text{EXTFAULT}}$ is pulled low by an external circuit, bit r1Ch[6] is set.

The SMB Alert ($\overline{\text{ALERT}}$) bit is set if the MAX16068 has asserted the SMBus Alert output. Clear by writing a '1'. See the *SMBALERT ($\overline{\text{ALERT}}$)* section for more details.

Critical Faults

During normal operation, a fault condition can be stored in the flash memory by setting the appropriate critical fault enable bits. Set the appropriate critical fault enable bits in registers r6Eh–r72h (see Table 12) for a fault condition to trigger a critical fault.

Table 12. Critical Fault Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
6Dh	26Dh	[1:0]	Fault Information to Log 00 = Save failed line flags and ADC values in flash 01 = Save only failed line flags in flash 10 = Save only ADC values in flash 11 = Do not save anything
		[2]	1 = Fault log triggered when $\overline{\text{EXTFAULT}}$ is pulled low externally
		[7:3]	Not used
6Eh	26Eh	[0]	1 = Fault log triggered when MON1 is below its undervoltage threshold
		[1]	1 = Fault log triggered when MON2 is below its undervoltage threshold
		[2]	1 = Fault log triggered when MON3 is below its undervoltage threshold
		[3]	1 = Fault log triggered when MON4 is below its undervoltage threshold
		[4]	1 = Fault log triggered when MON5 is below its undervoltage threshold
		[5]	1 = Fault log triggered when MON6 is below its undervoltage threshold
		[7:6]	Not used
6Fh	26Fh	[3:0]	Not used
		[4]	1 = Fault log triggered when MON1 is above its overvoltage threshold
		[5]	1 = Fault log triggered when MON2 is above its overvoltage threshold
		[6]	1 = Fault log triggered when MON3 is above its overvoltage threshold
		[7]	1 = Fault log triggered when MON4 is above its overvoltage threshold
70h	270h	[0]	1 = Fault log triggered when MON5 is above its overvoltage threshold
		[1]	1 = Fault log triggered when MON6 is above its overvoltage threshold
		[7:2]	Not used
71h	271h	[7:0]	Not used
72h	272h	[4:0]	Not used
		[5]	1 = $\overline{\text{EXTFAULT}}$ pulled low externally causes the device to stop monitoring until EN is toggled or the autoretry delay expires (see *Autoretry/Latch Mode* section) 0 = $\overline{\text{EXTFAULT}}$ pulled low externally does not cause the device to stop monitoring
		[7:6]	Not used

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Logged fault information is stored in flash registers r200h–r208h (see Table 13). After fault information is logged, the flash is locked and must be unlocked to enable a new fault log to be stored. Write a '0' to r8Ch[1] to unlock the configuration flash. Fault information can be configured to store ADC conversion results and/or fault flags in registers. Select the critical fault configuration in r6Dh[1:0]. Set r6Dh[1:0] to '11' to turn off the fault logger. All stored ADC results are 8 bits wide (MSBs of the conversion).

Autoretry/Latch Mode

The MAX16068 can be configured for one of two fault management methods: autoretry or latch-on-fault. Set r74h[4:3] to '00' to select the latch-on-fault mode. The device does not reinitiate monitoring until EN is toggled or the software enable bit is toggled. See the *Enable Input (EN)* section for more information on setting the software enable bit.

Table 13. Nonvolatile Fault Log Registers

FLASH ADDRESS	BIT RANGE	DESCRIPTION
200h	[7:0]	Reserved
201h	[0]	Fault log triggered on MON1 falling below its undervoltage threshold
	[1]	Fault log triggered on MON2 falling below its undervoltage threshold
	[2]	Fault log triggered on MON3 falling below its undervoltage threshold
	[3]	Fault log triggered on MON4 falling below its undervoltage threshold
	[4]	Fault log triggered on MON5 falling below its undervoltage threshold
	[5]	Fault log triggered on MON6 falling below its undervoltage threshold
	[7:6]	Not used
202h	[0]	Fault log triggered on MON1 exceeding its overvoltage threshold
	[1]	Fault log triggered on MON2 exceeding its overvoltage threshold
	[2]	Fault log triggered on MON3 exceeding its overvoltage threshold
	[3]	Fault log triggered on MON4 exceeding its overvoltage threshold
	[4]	Fault log triggered on MON5 exceeding its overvoltage threshold
	[5]	Fault log triggered on MON6 exceeding its overvoltage threshold
	[6]	Fault log triggered on $\overline{\text{EXTFAULT}}$
	[7]	Not used
203h	[7:0]	MON1 ADC output (8 MSBs)
204h	[7:0]	MON2 ADC output (8 MSBs)
205h	[7:0]	MON3 ADC output (8 MSBs)
206h	[7:0]	MON4 ADC output (8 MSBs)
207h	[7:0]	MON5 ADC output (8 MSBs)
208h	[7:0]	MON6 ADC output (8 MSBs)

Set r74h[4:3] to a value other than '00' to select autoretry mode (see Table 14). In this configuration, the device stops monitoring after a critical fault event then monitors again following the boot-up delay plus 20ms (see the *Boot-Up Delay* section). Use r74h[2:0] to select an autoretry delay from 20ms to 1.6s. See Table 14 for more information on setting the autoretry delay.

When fault information is stored in flash (see the *Critical Faults* section) and autoretry mode is selected, set an autoretry delay greater than the time required for the storing operation. When fault information is stored in flash and latch-on-fault mode is chosen, toggle EN or reset the software enable bit only after the completion of the storing operation. When saving information about the failed lines only, ensure a delay of at least 102ms before the restart procedure. Otherwise, ensure a minimum 153ms timeout, to ensure that ADC conversions are completed and values are stored correctly in flash.

Reset Output

The reset output, RESET, indicates the status of the monitored inputs. It asserts during the boot phase and deasserts following the reset timeout period once the monitored input voltage is within the undervoltage/overvoltage.

During normal monitoring, RESET can be configured to assert when any combination of MON_ inputs violates configurable combinations of undervoltage or overvoltage thresholds. Select the combination of MON_ inputs using r3Ch[5:0] and r3Dh[5:0]. Note that MON_ inputs configured as critical faults always cause RESET to assert regardless of these configuration bits.

RESET can be configured as push-pull or open drain using r3Bh[3], and active high or active low using r3Bh[2]. Select the reset timeout by loading a value from Table 15 into r3Bh[7:4].

To generate a one-shot pulse on RESET, write a '1' into r3Bh[0]. The pulse width is the configured reset timeout. Register bit r3Bh[0] clears automatically (see Table 15). The current state of RESET can be checked by reading r20h[0].

Table 14. Autoretry Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
74h	274h	[2:0]	Retry Delay 000 = 20ms 001 = 40ms 010 = 80ms 011 = 150ms 100 = 280ms 101 = 540ms 110 = 1s 111 = 2s
		[4:3]	Autoretry/Latch Mode 00 = Latch 01 = Retry 1 time 10 = Retry 3 times 11 = Always retry

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Table 15. Reset Output Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
3Bh	23Bh	[0]	RESET Soft Trigger 0 = Normal RESET behavior 1 = Force RESET to assert
		[1]	Not used
		[2]	0 = Active low 1 = Active high
		[3]	0 = Open drain 1 = Push-pull
		[7:4]	Reset Timeout Period 0000 = 25µs 0001 = 1.5ms 0010 = 2.5ms 0011 = 4ms 0100 = 6ms 0101 = 10ms 0110 = 15ms 0111 = 25ms 1000 = 40ms 1001 = 60ms 1010 = 100ms 1011 = 150ms 1100 = 250ms 1101 = 400ms 1110 = 600ms 1111 = 1s
3Ch	23Ch	[0]	1 = RESET depends on MON1 undervoltage
		[1]	1 = RESET depends on MON2 undervoltage
		[2]	1 = RESET depends on MON3 undervoltage
		[3]	1 = RESET depends on MON4 undervoltage
		[4]	1 = RESET depends on MON5 undervoltage
		[5]	1 = RESET depends on MON6 undervoltage
		[7:6]	Not used
3Dh	23Dh	[0]	1 = RESET depends on MON1 overvoltage
		[1]	1 = RESET depends on MON2 overvoltage
		[2]	1 = RESET depends on MON3 overvoltage
		[3]	1 = RESET depends on MON4 overvoltage
		[4]	1 = RESET depends on MON5 overvoltage
		[5]	1 = RESET depends on MON6 overvoltage
		[7:6]	Not used

Watchdog Timer

The watchdog timer operates together with or independently of the MAX16068. When operating in dependent mode, the watchdog is not activated until RESET is deasserted. When operating in independent mode, the watchdog timer activates immediately after V_{CC} exceeds the UVLO threshold and the boot phase is complete. Set r73h[4] to '0' to configure the watchdog in dependent mode. Set r73h[4] to '1' to configure the watchdog in independent mode. See Table 16 for more information on configuring the watchdog timer in dependent or independent mode. The watchdog timer can be reset by toggling the WDI inputs (GPIO4) or by writing a '1' to r75h[5].

Dependent Watchdog Timer Operation

Use the watchdog timer to monitor µP activity in two modes. Flexible timeout architecture provides an adjustable watchdog startup delay of up to 300s, allowing complicated systems to complete lengthy boot-up routines. An adjustable watchdog timeout allows the supervisor to provide quick alerts when the processor activity fails. After each reset event (V_{CC} drops below UVLO then returns above UVLO, software reboot, manual reset ($\overline{MR}$), EN input going low then high, or watchdog reset), the watchdog startup delay provides an extended time for the system to power up and fully initialize all µP and system components before assuming responsibility for routine watchdog updates. Set r76h[6:4] to a value other than '000' to enable the watchdog startup delay. Set r76h[6:4] to '000' to disable the watchdog startup delay.

The normal watchdog timeout period, t_{WDI}, begins after the first transition on WDI before the conclusion of the long startup watchdog period, $t_{WDI_STARTUP}$ (Figures 3 and 4). During the normal operating mode, $\overline{WDO}$ asserts if the µP does not toggle WDI with a valid transition (high-to-low or low-to-high) within the standard timeout period, t_{WDI}. $\overline{WDO}$ remains asserted until WDI is toggled or RESET is asserted (Figure 4).

While EN is low, the watchdog timer is in reset. The watchdog timer does not begin counting until the monitoring starts and RESET is deasserted. The watchdog timer is reset and $\overline{WDO}$ deasserts any time RESET is asserted (Figure 5). The watchdog timer is held in reset while RESET is asserted.

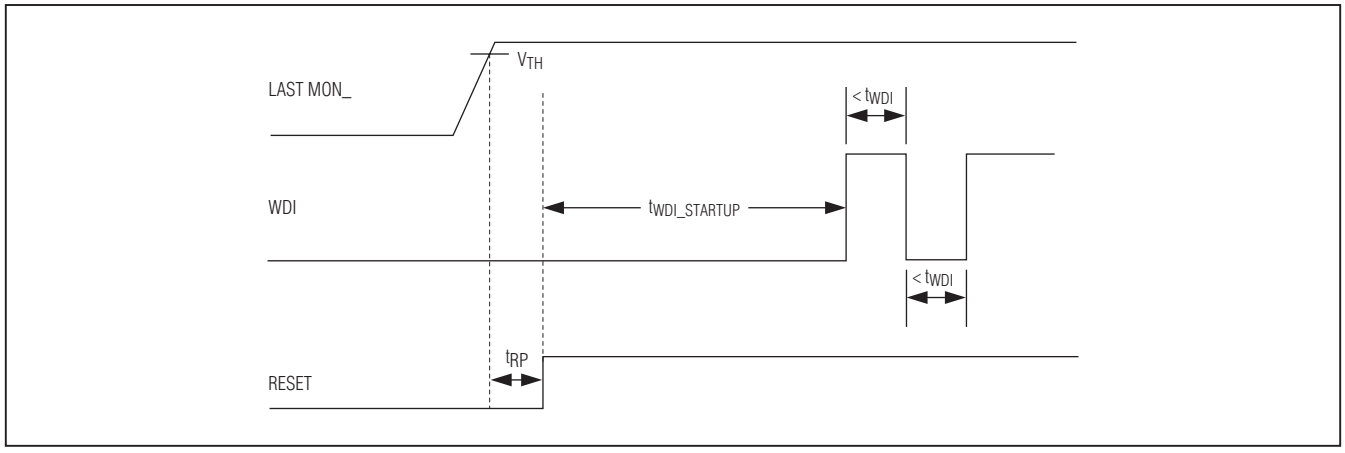


Figure 3. Normal Watchdog Startup Sequence

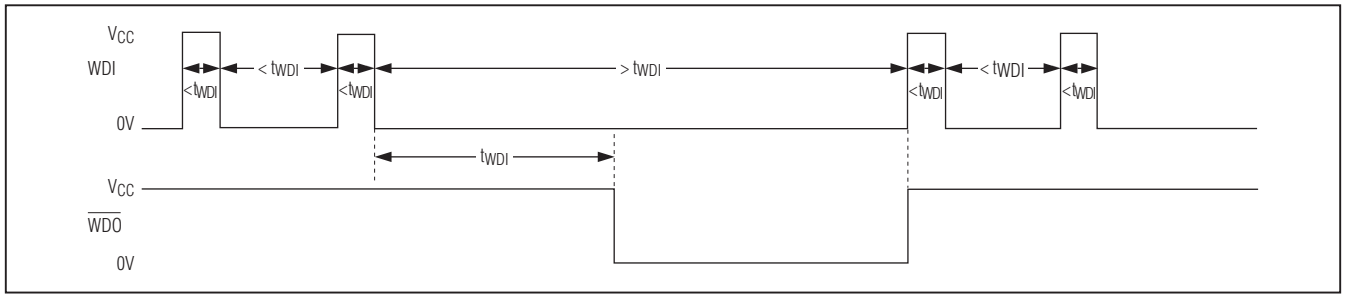


Figure 4. Watchdog Timer Operation

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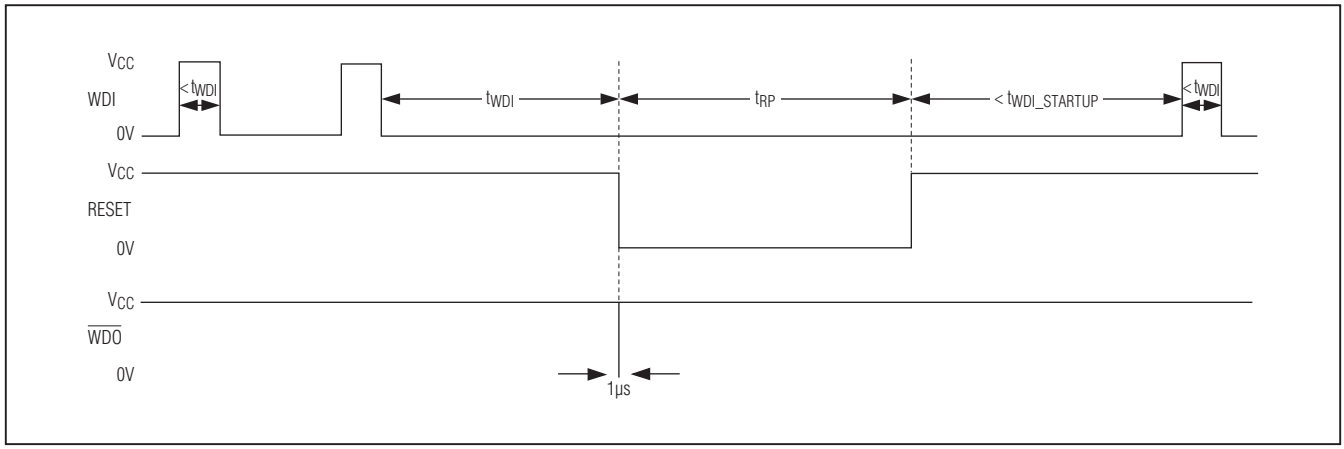


Figure 5. Watchdog Startup Sequence with Watchdog Reset Output Enable Bit Set to '1'

Table 16. Watchdog Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
73h	273h	[4]	1 = Independent mode 0 = Dependent mode
76h	276h	[7]	1 = Watchdog reset output enabled 0 = Watchdog reset output disabled
		[6:4]	Watchdog Startup Delay 000 = No initial timeout 001 = 30s 010 = 40s 011 = 80s 100 = 120s 101 = 160s 110 = 220s 111 = 300s
		[3:0]	Watchdog Timeout 0000 = Watchdog disabled 0001 = 1ms 0010 = 2ms 0011 = 4ms 0100 = 8ms 0101 = 14ms 0110 = 27ms 0111 = 50ms 1000 = 100ms 1001 = 200ms 1010 = 400ms 1011 = 750ms 1100 = 1.4s 1101 = 2.7s 1110 = 5s 1111 = 10s

The watchdog can be configured to control the RESET output as well as the WDO output. RESET asserts for the reset timeout, t_{RP}, when the watchdog timer expires and the Watchdog Reset Output Enable bit (r76h[7]) is set to '1'. When RESET is asserted, the watchdog timer is cleared and WDO is deasserted, therefore, WDO pulses low for a short time (approximately 1µs) when the watchdog timer expires. RESET is not affected by the watchdog timer when the Watchdog Reset Output Enable bit (r76h[7]) is set to '0'. If a RESET is asserted by the watchdog timeout, the WDRESET bit is set to '1'. A connected processor can check this bit to see the reset was due to a watchdog timeout.

See Table 16 for more information on configuring watchdog functionality.

Independent Watchdog Timer Operation

When r73h[4] is '1,' the watchdog timer operates in the independent mode. In the independent mode, the watchdog timer operates as if it were a separate device. The watchdog timer is activated immediately upon V_{CC} exceeding UVLO and once the boot-up sequence is finished. When RESET is asserted by EN being low, the watchdog timer and WDO are not affected.

There is a startup delay if r76h[6:4] is set to a value different than '000'. If r76h[6:4] is set to '000', there is not a startup delay. See Table 16 for delay times.

In independent mode, if the Watchdog Reset Output Enable bit (r76h[7]) is set to '1,' when the watchdog timer expires, WDO asserts then RESET asserts. WDO then deasserts. WDO is low for approximately 1µs. If the Watchdog Reset Output Enable bit (r76h[7]) is set to '0,' when the watchdog timer expires, WDO asserts but RESET is not affected.

User-Defined Register

Register r8Ah provides storage space for a user-defined configuration or firmware version number. Note that this register controls the contents of the JTAG USERCODE register bits 7-0. The user-defined register is stored at r28Ah in the flash memory.

Memory Lock Bits

Register r8Ch contains the lock bits for the configuration registers, configuration flash, user flash, and fault register lock. See Table 17 for details.

SMBus-Compatible Serial Interface

The MAX16068 features an SMBus-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX16068 and the master device at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The MAX16068 is a transmit/receive, slave-only device, relying upon a master device to generate a clock signal. The master device (typically a microcontroller) initiates a data transfer on the bus and generates SCL to permit that transfer.

Table 17. Memory Lock Bits

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
8Ch	28Ch	[0]	Configuration Register Lock 1 = Locked 0 = Unlocked
		[1]	Flash Fault Register Lock 1 = Locked 0 = Unlocked
		[2]	Flash Configuration Lock 1 = Locked 0 = Unlocked
		[3]	User Flash Lock 1 = Locked 0 = Unlocked
		[7.4]	Not used

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A master device communicates to the MAX16068 by transmitting the proper address followed by command and/or data words. The slave address input, A0, is capable of detecting four different states, allowing multiple identical devices to share the same serial bus. The slave address is described further in the *Slave Address* section. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse. SCL is a logic input, while SDA is an open-drain input/output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7kΩ for most applications.

Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (Figure 6); otherwise, the MAX16068 registers a START or STOP condition (Figure 7) from the master. SDA and SCL idle high when the bus is not busy.

START and STOP Conditions

A master device signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. The master device issues a STOP condition by transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the block read protocol (see Figure 1, SMBus Timing Diagram).

Early STOP Conditions

The MAX16068 recognizes a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal SMBus format; at least one clock pulse must separate any START and STOP condition.

REPEATED START Conditions

A REPEATED START can be sent instead of a STOP condition to maintain control of the bus during a read operation. The START and REPEATED START conditions are functionally identical.

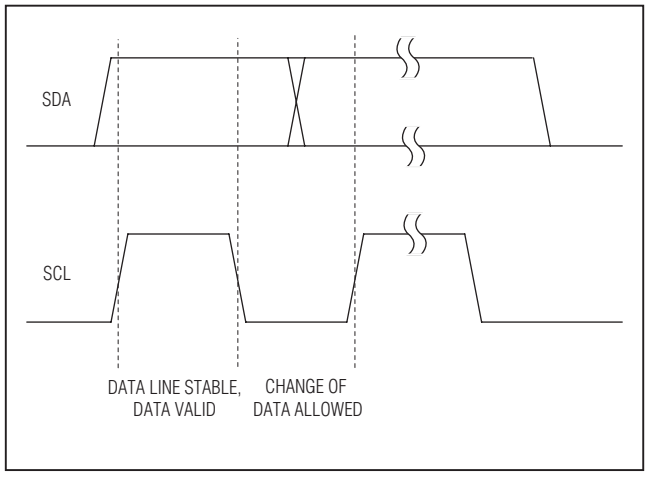


Figure 6. Bit Transfer

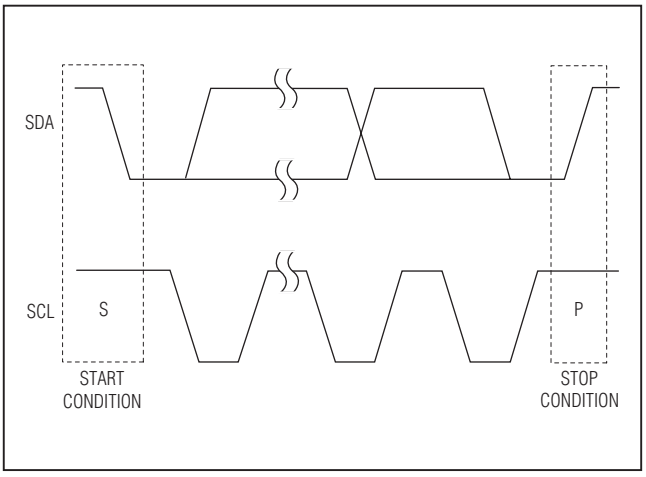


Figure 7. START and STOP Conditions

Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX16068 generates an ACK when receiving an address or data by pulling SDA low during the 9th clock period (Figure 8). When transmitting data, such as when the master device reads data back from the MAX16068, the device waits for the master device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication at a later time. The MAX16068 generates a NACK after the command byte received during a software reboot, while writing to the flash, or when receiving an illegal memory address.

Slave Address

Use the slave address input, A0, to allow multiple identical devices to share the same serial bus. Connect A0 to GND, DBP (or an external supply voltage greater than 2V), SCL, or SDA to set the device address on the bus. See Table 18 for a listing of all possible 7-bit addresses.

The slave address can also be set to a custom value by loading the address into register r8Bh[6:0]. See Table 19. If r8Bh[6:0] is loaded with 00h, the address is set by input A0. Do not set the address to 09h or 7Fh to avoid address conflicts. The slave address setting takes effect immediately after writing to the register.

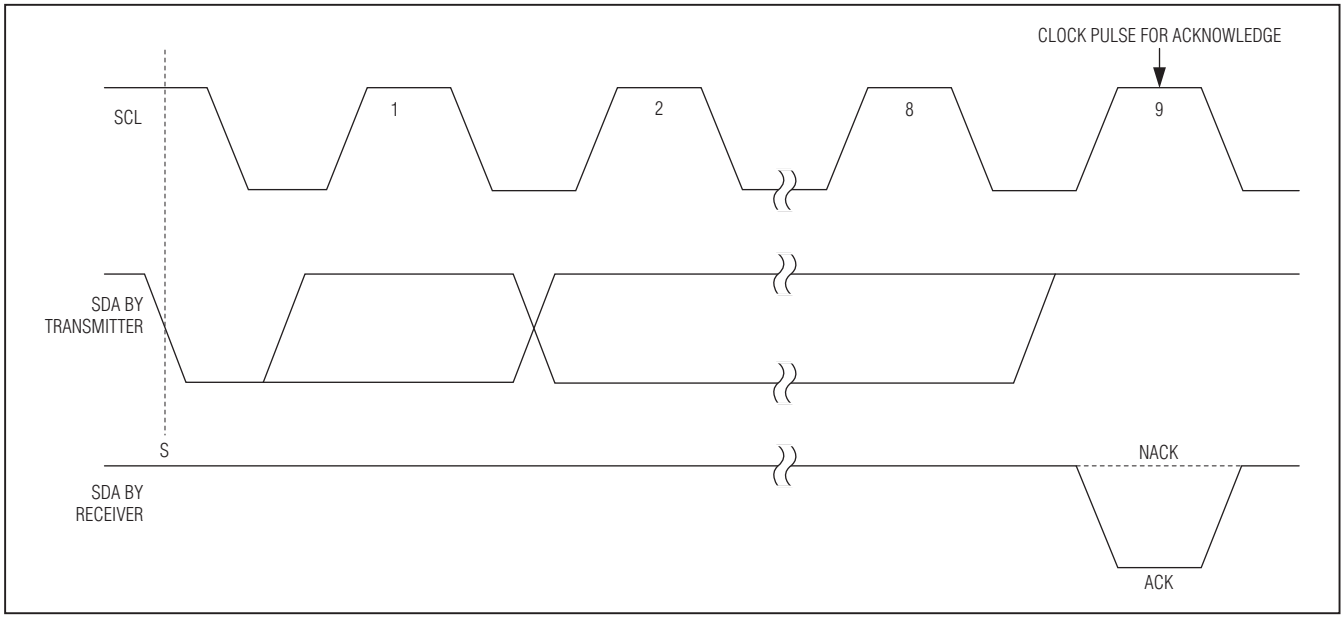


Figure 8. Acknowledge

Table 18. Setting the SMBus Slave Address

SLAVE ADDRESSES	
A0	**SLAVE ADDRESS**
0	1010 100R
1	1010 101R
SCL	1010 110R
SDA	1010 111R

R = Read/write select bit.

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Packet Error Checking (PEC)

The MAX16068 features a packet-error checking (PEC) mode that is useful to improve the reliability of the communication bus by detecting bit errors. By enabling PEC, an extra CRC-8 error check byte is added in the data string during each read and/or write sequence. Enable PEC by writing a '1' to r8Bh[7].

The CRC-8 byte is calculated using the polynomial:

$$C = X^8 + X^2 + X + 1$$

The PEC calculation includes all bytes in the transmission, including address, command, and data. The PEC calculation does not include ACK, NACK, START, STOP, or REPEATED START.

Command Codes

The MAX16068 uses eight command codes for block read, block write, and other commands. See Table 20 for a list of command codes.

To initiate a software reboot, send A7h using the send byte format. A software-initiated reboot is functionally the same as a hardware-initiated power-on reset. During boot-up, flash configuration data in the range of 230h–28Ch is copied to r30h–r8Ch registers in the default page.

Send command code A8h to trigger a fault store to flash. Configure the Critical Fault Log Control register (r6Dh) to store ADC conversion results and/or fault flags.

While in the flash page, send command code A9h to access the flash page (addresses from 230h–28Dh). Once command code A9h has been sent, all addresses are recognized as flash addresses only. Send command code AAh to return to the default page (addresses from 000h–08Dh). Send command code ABh to access the user flash-page (addresses from 300h–3FFh), and send command code ACh to return to the flash page.

Restrictions When Writing to Flash

Flash must be written to 8 bytes at a time. The initial address must be aligned to 8-byte boundaries—the 3 LSBs of the initial address must be '000'. Write the 8 bytes using a single block write command or using eight successive Write Byte commands. A write operation requires 122ms for each 8-byte block. After programming a block, check r20h[1] (see Table 25) to make sure the write operation is complete before attempting to write the next block.

Table 19. SMBus Settings Register

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
8Bh	28Bh	[6:0]	SMBus Slave Address Register. Set to 00h to use A0 pin address setting.
		[7]	1 = Enable PEC (Packet Error Check).

Table 20. Command Codes

COMMAND CODE	ACTION
A5h	Block write
A6h	Block read
A7h	Reboot flash in register file
A8h	Trigger emergency save to flash
A9h	Flash page access ON
AAh	Flash page access OFF
ABh	User flash access ON (must be in flash page already)
ACh	User flash access OFF (return to flash page)

Send Byte

The send byte protocol allows the master device to send one byte of data to the slave device (see Figure 9). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send a memory address or command code that is not allowed. If the master sends A5h or A6h, the data is ACK, because this could be the start of the write block or read block. If the master sends a STOP condition before the slave asserts an ACK, the internal address pointer does not change. If the master sends A7h, this signifies a software reboot. The send byte procedure is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit memory address or command code.
5) The addressed slave asserts an ACK (or NACK) on SDA.
6) The master sends a STOP condition.

Receive Byte

The receive byte protocol allows the master device to read the register content of the MAX16068 (see Figure 9). The flash or register address must be preset with a send byte or write word protocol first. Once the read is complete, the internal pointer increases by one. Repeating the receive byte protocol reads the contents of the next address. The receive byte procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a read bit (high).
3) The addressed slave asserts an ACK on SDA.
4) The slave sends 8 data bits.
5) The master asserts a NACK on SDA.
6) The master generates a STOP condition.

Write Byte

The write byte protocol (see Figure 9) allows the master device to write a single byte in the default page, extended page, or flash page, depending on which page is currently selected. The write byte procedure is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit memory address.
5) The addressed slave asserts an ACK on SDA.
6) The master sends an 8-bit data byte.
7) The addressed slave asserts an ACK on SDA.
8) The master sends a STOP condition.

To write a single byte, only the 8-bit memory address and a single 8-bit data byte are sent. The data byte is written to the addressed location if the memory address is valid. The slave asserts a NACK at step 5 if the memory address is not valid.

When PEC is enabled, the Write Byte protocol becomes:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends an 8-bit memory address.
5) The active slave asserts an ACK on the data line.
6) The master sends an 8-bit data byte.
7) The slave asserts an ACK on the data line.
8) The master sends an 8-bit PEC byte.
9) The slave asserts an ACK on the data line (if PEC is good, otherwise NACK).
10) The master generates a STOP condition.

Read Byte

The read byte protocol (see Figure 9) allows the master device to read a single byte located in the default page, extended page, or flash page depending on which page is currently selected. The read byte procedure is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit memory address.
5) The addressed slave asserts an ACK on SDA.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address and a read bit (high).
8) The addressed slave asserts an ACK on SDA.

9) The slave sends an 8-bit data byte.
10) The master asserts a NACK on SDA.
11) The master sends a STOP condition.

If the memory address is not valid, it is NACKed by the slave at step 5 and the address pointer is not modified.

When PEC is enabled, the Read Byte protocol becomes:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends 8-bit memory address.
5) The active slave asserts an ACK on the data line.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave ID plus a read bit (high).
8) The addressed slave asserts an ACK on the data line.
9) The slave sends 8 data bits.
10) The master asserts an ACK on the data line.
11) The slave sends an 8-bit PEC byte.
12) The master asserts a NACK on the data line.
13) The master generates a STOP condition.

Block Write

The block write protocol (see Figure 9) allows the master device to write a block of data (1–16 bytes) to memory. Preload the destination address by a previous send byte command; otherwise the block write command begins to write at the current address pointer. After the last byte is written, the address pointer remains preset to the next valid address. If the number of bytes to be written causes the address pointer to exceed 8Fh for configuration registers or configuration flash or FFh for user flash, the address pointer stays at 8Fh or FFh, respectively, overwriting this memory address with the remaining bytes of data. The slave generates a NACK at step 5 if the command code is invalid or if the device is busy, and the address pointer is not altered.

The block write procedure is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends the 8-bit command code for block write (A5h).
5) The addressed slave asserts an ACK on SDA.
6) The master sends the 8-bit byte count (1 byte to 16 bytes), n.
7) The addressed slave asserts an ACK on SDA.
8) The master sends 8 bits of data.
9) The addressed slave asserts an ACK on SDA.
10) Repeat steps 8 and 9 n - 1 times.
11) The master sends a STOP condition.

When PEC is enabled, the Block Write protocol becomes:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends 8 bits of the block write command code.
5) The slave asserts an ACK on the data line.
6) The master sends 8 bits byte count (min 1, max 16) n.
7) The slave asserts an ACK on the data line.
8) The master sends 8 bits of data.
9) The slave asserts an ACK on the data line.
10) Repeat 8 and 9 n - 1 times.
11) The master sends an 8-bit PEC byte.
12) The slave asserts an ACK on the data line (if PEC is good, otherwise NACK).
13) The master generates a STOP condition.

Block Read The block read protocol (see Figure 9) allows the master device to read a block of up to 16 bytes from memory. Read fewer than 16 bytes of data by issuing an early STOP condition from the master, or by generating a NACK with the master. The destination address should be preloaded by a previous send byte command; otherwise, the block read command begins to read at the current address pointer. If the number of bytes to be read causes the address pointer to exceed 8Fh for the configuration register or configuration flash or FFh in user flash, the address pointer stays at 8Fh or FFh, respectively.

The block read procedure is the following:

SEND BYTE FORMAT

S	ADDRESS	R/W	ACK	COMMAND	ACK	P
↓	7 BITS	0	0	8 BITS	0	↑

SLAVE ADDRESS: Address of the slave on the serial interface bus.

DATA BYTE: Presets the internal address pointer or represents a command.

RECEIVE BYTE FORMAT

S	ADDRESS	R/W	ACK	DATA	NACK	P
↓	7 BITS	1	0	8 BITS	1	↑

SLAVE ADDRESS: Address of the slave on the serial interface bus.

DATA BYTE: Data is read from the location pointed to by the internal address pointer.

WRITE BYTE FORMAT

S	ADDRESS	R/W	ACK	COMMAND	ACK	DATA	ACK	P
↓	7 BITS	0	0	8 BITS	0	8 BITS	0	↑

SLAVE ADDRESS: Address of the slave on the serial interface bus.

COMMAND BYTE: Sets the internal address pointer.

DATA BYTE: Data is written to the locations set by the internal address pointer.

SMBALERT#

S	ADDRESS	R/W	ACK	DATA	NACK	P
↓	0001100	D.C.	0	8 BITS	1	↑

ALERT RESPONSE ADDRESS: Only the device that interrupted the master responds to this address.

SLAVE ADDRESS: Slave places its own address on the serial bus.

READ BYTE FORMAT

S	SLAVE ADDRESS	R/W	ACK	COMMAND	ACK	SR	SLAVE ADDRESS	R/W	ACK	DATA BYTE	NACK	P
↓	7 BITS	0	0	8 BITS	0	↓	7 BITS	1	0	8 BITS	1	↑

SLAVE ADDRESS: Address of the slave on the serial interface bus.

COMMAND BYTE: Sets the internal address pointer.

DATA BYTE: Data is read from the locations set by the internal address pointer.

BLOCK WRITE FORMAT

S	ADDRESS	R/W	ACK	COMMAND	ACK	BYTE COUNT = N	ACK	DATA BYTE 1	ACK	DATA BYTE …	ACK	DATA BYTE N	ACK	P
↓	7 BITS	0	0	8 BITS	0	8 BITS	0	8 BITS	0	8 BITS	0	8 BITS	0	↑

SLAVE ADDRESS: Address of the slave on the serial interface bus.

COMMAND BYTE: A5h

DATA BYTE: Data is written to the locations set by the internal address pointer.

SLAVE TO MASTER

MASTER TO SLAVE

BLOCK READ FORMAT

S	ADDRESS	R/W	ACK	COMMAND	ACK	SR	ADDRESS	R/W	ACK	BYTE COUNT = N	ACK	DATA BYTE 1	ACK	DATA BYTE …	ACK	DATA BYTE N	NACK	P
↓	7 BITS	0	0	8 BITS	0	↓	7 BITS	1	0	8 BITS	0	8 BITS	0	8 BITS	0	8 BITS	1	↑

SLAVE ADDRESS: Address of the slave on the serial interface bus.

COMMAND BYTE: A6h

SLAVE ADDRESS: Address of the slave on the serial interface bus.

DATA BYTE: Data is read from the locations set by the internal address pointer.

WRITE BYTE FORMAT WITH PEC

S	ADDRESS	R/W	ACK	COMMAND	ACK	DATA	ACK	PEC	ACK	P
↓	7 BITS	0	0	8 BITS	0	8 BITS	0	8 BITS	0	↑

READ BYTE FORMAT WITH PEC

S	ADDRESS	R/W	ACK	COMMAND	ACK	SR	ADDRESS	R/W	ACK	DATA	ACK	PEC	NACK	P
↓	7 BITS	0	0	8 BITS	0	↓	7 BITS	1	0	8 BITS	0	8 BITS	1	↑

BLOCK WRITE WITH PEC

S	ADDRESS	R/W	ACK	COMMAND	ACK	BYTE COUNT N	ACK	DATA BYTE 1	ACK	DATA BYTE …	ACK	DATA BYTE N	ACK	PEC	ACK	P
↓	7 BITS	0	0	8 BITS	0	8 BITS	0	8 BITS	0	8 BITS	0	8 BITS	0	8 BITS	0	↑

BLOCK READ WITH PEC

S	ADDRESS	R/W	ACK	COMMAND	ACK	SR	ADDRESS	R/W	ACK	BYTE COUNT N	ACK	DATA BYTE 1	ACK	DATA BYTE …	ACK	DATA BYTE N	ACK	PEC	NACK	P
↓	7 BITS	0	0	8 BITS	0	↓	7 BITS	1	0	8 BITS	0	8 BITS	0	8 BITS	0	8 BITS	0	8 BITS	1	↑

S = START CONDITION
P = STOP CONDITION
Sr = REPEATED START CONDITION
D.C. = DON'T CARE

ACK = ACKNOWLEDGE, SDA PULLED LOW DURING RISING EDGE OF SCL.
NACK = NOT ACKNOWLEDGE, SDA LEFT HIGH DURING RISING EDGE OF SCL.

ALL DATA IS CLOCKED IN/OUT OF THE DEVICE ON RISING EDGES OF SCL.

↓ = SDA TRANSITIONS FROM HIGH TO LOW DURING PERIOD OF SCL.

↑ = SDA TRANSITIONS FROM LOW TO HIGH DURING PERIOD OF SCL.

Figure 9. SMBus Protocols

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1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends 8 bits of the block read command (A6h).
5) The slave asserts an ACK on SDA, unless busy.
6) The master generates a REPEATED START condition.
7) The master sends the 7-bit slave address and a read bit (high).
8) The slave asserts an ACK on SDA.
9) The slave sends the 8-bit byte count (16).
10) The master asserts an ACK on SDA.
11) The slave sends 8 bits of data.
12) The master asserts an ACK on SDA.
13) Repeat steps 11 and 12 up to fifteen times.
14) The master asserts a NACK on SDA.
15) The master sends a STOP condition.

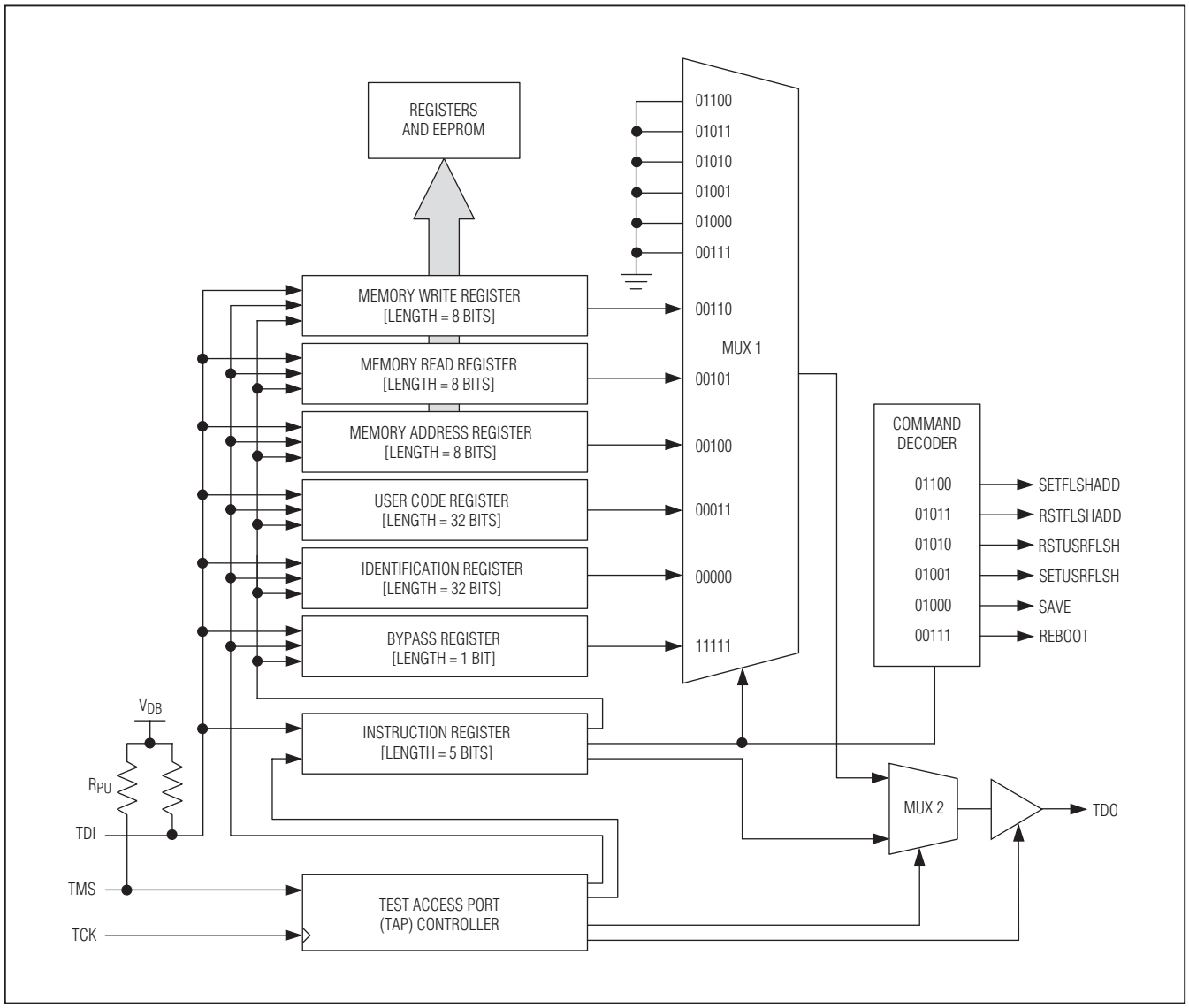


Figure 10. JTAG Block Diagram

When PEC is enabled, the Block Read protocol becomes:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends 8 bits of the block read command code.
5) The slave asserts an ACK on the data line unless busy.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave ID plus a read bit (high).
8) The slave asserts an ACK on the data line.
9) The slave sends 8-bit byte count (16).
10) The master asserts an ACK on the data line.
11) The slave sends 8 bits of data.
12) The master asserts an ACK on the data line.
13) Repeat 11 and 12 up to 15 times.
14) The slave sends an 8-bit PEC byte.
15) The master asserts a NACK on the data line.
16) The master generates a STOP condition.

SMBALERT ($\overline{ALERT}$)

The MAX16068 supports the SMBus alert protocol. To enable the SMBus alert output, set r40h[4] to '1', then configure GPIO1 to act as the SMBus alert ($\overline{ALERT}$) according to Table 12. This output is open drain and uses the wired-OR configuration with other devices on the SMBus. During a fault, the MAX16068 asserts $\overline{ALERT}$ low, signaling the master that an interrupt has occurred. The master responds by sending the ARA (Alert Response Address) protocol on the SMBus. This protocol is a read byte with 09h as the slave address. The slave acknowledges the ARA (09h) address and sends its own SMBus address to the master. The slave then deasserts $\overline{ALERT}$. The master can then query the slave and determine the cause of the fault. By checking r1C[7], the master can confirm that the MAX16068 triggered the SMBus alert. The master must send the ARA before clearing r1Ch[7]. Clear r1Ch[7] by writing a '1'. If GPIO1 is configured as the SMBus alert output but the SMBus alert feature is disabled (r40h[4] is set to '0'), GPIO1 acts as an additional fault output.

JTAG Serial Interface

The MAX16068 features a JTAG port that complies with a subset of the IEEE® 1149.1 specification. Either the SMBus or the JTAG interface can be used to access internal memory; however, only one interface is allowed to run at a time. The MAX16068 contains extra JTAG instructions and registers not included in the JTAG specification that provide access to internal memory. The extra instructions include LOAD ADDRESS, WRITE DATA, READ DATA, REBOOT, and SAVE.

Test Access Port (TAP)

Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at TMS on the rising edge of TCK. See Figure 11 for a diagram of the finite state machine. The possible states are described as follows:

Test-Logic-Reset: At power-up, the TAP controller is in the test-logic-reset state. The instruction register contains the IDCODE instruction. All system logic of the device operates normally. This state can be reached from any state by driving TMS high for five clock cycles.

Run-Test/Idle: The run-test/idle state is used between scan operations or during specific tests. The instruction register and test data registers remain idle.

Select-DR-Scan: All test data registers retain their previous state. With TMS low, a rising edge of TCK moves the controller into the capture-DR state and initiates a scan sequence. TMS high during a rising edge on TCK moves the controller to the select-IR-scan state.

Capture-DR: Data can be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected test data register does not allow parallel loads, the test data register remains at its current value. On the rising edge of TCK, the controller goes to the shift-DR state if TMS is low or it goes to the exit1-DR state if TMS is high.

Shift-DR: The test data register selected by the current instruction connects between TDI and TDO and shifts data one stage toward its serial output on each rising edge of TCK while TMS is low. On the rising edge of TCK, the controller goes to the exit1-DR state if TMS is high.

Exit1-DR: While in this state, a rising edge on TCK puts the controller in the update-DR state. A rising edge on TCK with TMS low puts the controller in the pause-DR state.

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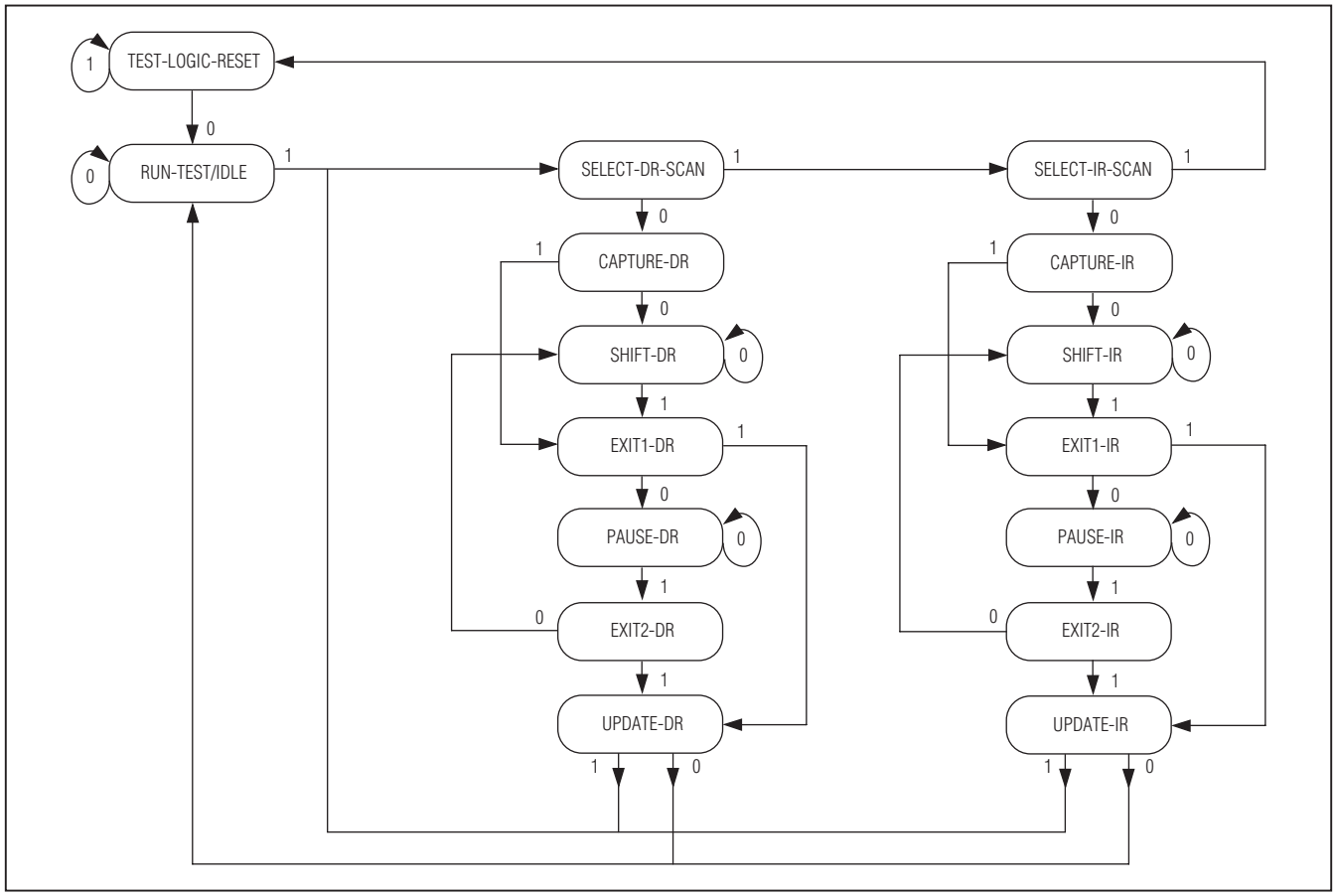


Figure 11. Tap Controller State Diagram

Pause-DR: Shifting of the test data registers halts while in this state. All test data registers retain their previous state. The controller remains in this state while TMS is low. A rising edge on TCK with TMS high puts the controller in the exit2-DR state.

Exit2-DR: A rising edge on TCK with TMS high while in this state puts the controller in the update-DR state. A rising edge on TCK with TMS low enters the shift-DR state.

Update-DR: A falling edge on TCK while in the update-DR state latches the data from the shift register path of the test data registers into a set of output latches. This prevents changes at the parallel output because of changes in the shift register. On the rising edge of TCK, the controller goes to the run-test/idle state if TMS is low or goes to the select-DR-scan state if TMS is high.

Select-IR-Scan: All test data registers retain the previous states. The instruction register remains unchanged during this state. With TMS low, a rising edge on TCK moves the controller into the capture-IR state. TMS high during a rising edge on TCK puts the controller back into the test-logic-reset state.

Capture-IR: Use the capture-IR state to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of TCK. If TMS is high on the rising edge of TCK, the controller enters the exit1-IR state. If TMS is low on the rising edge of TCK, the controller enters the shift-IR state.

Shift-IR: In this state, the shift register in the instruction register connects between TDI and TDO and shifts data one stage for every rising edge of TCK toward the TDO serial output while TMS is low. The parallel outputs of the instruction register as well as all test data registers remain at the previous states. A rising edge on TCK with TMS high moves the controller to the exit1-IR state. A rising edge on TCK with TMS low keeps the controller in the shift-IR state while moving data one stage through the instruction shift register.

Exit1-IR: A rising edge on TCK with TMS low puts the controller in the pause-IR state. If TMS is high on the rising edge of TCK, the controller enters the update-IR state.

Pause-IR: Shifting of the instruction shift register halts temporarily. With TMS high, a rising edge on TCK puts the controller in the exit2-IR state. The controller remains in the pause-IR state if TMS is low during a rising edge on TCK.

Exit2-IR: A rising edge on TCK with TMS high puts the controller in the update-IR state. The controller loops back to shift-IR if TMS is low during a rising edge of TCK in this state.

Update-IR: The instruction code that has been shifted into the instruction shift register latches to the parallel outputs of the instruction register on the falling edge of TCK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on TCK with TMS low puts the controller in the run-test/idle state. With TMS high, the controller enters the select-DR-scan state.

Instruction Register

The instruction register contains a shift register as well as a latched 5-bit wide parallel output. When the TAP controller enters the shift-IR state, the instruction shift register connects between TDI and TDO. While in the shift-IR state, a rising edge on TCK with TMS low shifts the data one stage toward the serial output at TDO. A rising edge on TCK in the exit1-IR state or the exit2-IR state with TMS high moves the controller to the update-IR state. The falling edge of that same TCK latches the data in the instruction shift register to the instruction register parallel output. Table 21 shows the instructions supported by the MAX16068 and the respective operational binary codes.

BYPASS: When the BYPASS instruction is latched into the instruction register, TDI connects to TDO through the 1-bit bypass test data register. This allows data to pass from TDI to TDO without affecting the device's operation.

IDCODE: When the IDCODE instruction is latched into the parallel instruction register, the identification data register is selected. The device identification code is loaded into the identification data register on the rising edge of TCK following entry into the capture-DR state. Shift-DR can be used to shift the identification code out serially through TDO. During test-logic-reset, the IDCODE instruction is forced into the instruction register. The identification code always has a '1' in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version. See Table 22.

Table 21. JTAG Instruction Set

INSTRUCTION	CODE	NOTES
BYPASS	0x1F	Mandatory instruction code
IDCODE	0x00	Load manufacturer ID code/part number
USERCODE	0x03	Load user code
LOAD ADDRESS	0x04	Load address register content
READ DATA	0x05	Read data pointed by current address
WRITE DATA	0x06	Write data pointed by current address
REBOOT	0x07	Reboot FLASH data content into register file
SAVE	0x08	Trigger emergency save to flash
SETFLSHADD	0x09	Flash page access ON
RSTFLSHADD	0x0A	Flash page access OFF
SETUSRFLSH	0x0B	User flash access ON (must be in flash page already)
RSTUSRFLSH	0x0C	User flash access OFF (return to flash page)

Table 22. 32-Bit Identification Code

MSB			LSB
VERSION (4 BITS)	PART NUMBER (16 BITS)	MANUFACTURER (11 BITS)	FIXED VALUE (1 BIT)
0001	1000000000000010	00011001011	1

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USERCODE: When the USERCODE instruction latches into the parallel instruction register, the user-code data register is selected. The device user-code loads into the user-code data register on the rising edge of TCK following entry into the capture-DR state. Shift-DR can be used to shift the user-code out serially through TDO. See Table 24. This instruction can be used to help identify multiple MAX16068 devices connected in a JTAG chain.

LOAD ADDRESS: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16068. When the LOAD ADDRESS instruction latches into the instruction register, TDI connects to TDO through the 8-bit memory address test data register during the shift-DR state.

READ DATA: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16068. When the READ DATA instruction latches into the instruction register, TDI connects to TDO through the 8-bit memory read test data register during the shift-DR state.

WRITE DATA: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16068. When the WRITE DATA instruction latches into the instruction register, TDI connects to TDO through the 8-bit memory write test data register during the shift-DR state.

REBOOT: This is an extension to the standard IEEE 1149.1 instruction set to initiate a software-controlled reset to the MAX16068. When the REBOOT instruction latches into the instruction register, the MAX16068 resets and immediately begins the boot-up sequence.

SAVE: This is an extension to the standard IEEE 1149.1 instruction set that triggers a fault log. The current ADC conversion results along with fault information are saved to flash depending on the configuration of the Critical Fault Log Control register (r6Dh).

SETFLSHADD: This is an extension to the standard IEEE 1149.1 instruction set that allows access to the flash page. Flash registers include ADC conversion results and GPIO_ input/output data. Use this page to access registers 200h–2FFh.

RSTFLSHADD: This is an extension to the standard IEEE 1149.1 instruction set. Use RSTFLSHADD to return to the default page and disable access to the flash page.

SETUSRFLSH: This is an extension to the standard IEEE 1149.1 instruction set that allows access to the user flash page. When on the configuration flash page, send the SETUSRFLSH command, all addresses are recognized as flash addresses only. Use this page to access registers 300h–3FFh.

RSTUSRFLSH: This is an extension to the standard IEEE 1149.1 instruction set. Use RSTUSRFLSH to return to the configuration flash page and disable access to the user flash.

Restrictions When Writing to Flash

Flash must be written to 8 bytes at a time. The initial address must be aligned to 8-byte boundaries—the 3 LSBs of the initial address must be '000'. Write the 8 bytes using eight successive WRITE DATA commands. A write operation requires 122ms for each 8-byte block. After programming a block, check r20h[1] (see Table 25) to make sure the write operation is complete before attempting to write the next block.

Table 23. 32-Bit User-Code Data

MSB		LSB
DON'T CARE	**SMBUS SLAVE ID**	**USER ID (r8Ah[7:0])**
00000000000000000	See Table 18	

Table 24. Maximum Write Time

r6Dh[1:0] VALUE	DESCRIPTION	MAXIMUM WRITE TIME (ms)
00	Save flags and ADC readings	153
01	Save flags	102
10	Save ADC readings	153
11	Do not save anything	—

Table 25. RESET State, Flash State, and Reset Reason

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
r20h	[0]	Reset output state 0 = RESET is low 1 = RESET is high
	[1]	1 = Flash memory is busy
	[2]	1 = Last reset asserted due to EN going low
	[3]	1 = Last reset asserted due to watchdog timeout
	[7:4]	Not used

Applications Information

Device Behavior at Power-Up

When V_{CC} is ramped from 0V, the RESET output is high impedance until V_{CC} reaches 1.4V, at which point RESET goes low. All other outputs are high impedance until V_{CC} reaches 2.7V, then the flash contents are copied into register memory. This takes 150µs (max) after which the outputs assume their programmed states.

Programming the MAX16068 in Circuit

The MAX16068 can be programmed in the application circuit by taking into account the following points during circuit design:

- The MAX16068 needs to be powered from an intermediate voltage bus or an auxiliary voltage supply so programming can occur even when the board's power supplies are off. This could also be achieved by using ORing diodes so that power can be provided through the programming connector.
- The SMBus or JTAG bus lines should not connect through a bus multiplexer powered from a voltage rail controlled by the MAX16068. If the device needs to be controlled by an on-board µP, consider connecting the µP to one bus (such as SMBus) and use the other bus for in-circuit programming.

Maintaining Power During a Fault Condition

Power to the MAX16068 must be maintained for a specific period of time to ensure a successful flash fault log operation during a fault that removes power to the circuit. Table 25 shows that the amount of time required depends on the settings in the fault control register (r6Dh[1:0]).

Maintain power for shutdown during fault conditions in applications where the always-on power supply cannot be relied upon by placing a diode and a large capacitor between the voltage source, V_{IN}, and V_{CC} (Figure 12). The capacitor value depends on V_{IN} and the time delay required, t_{FAULT_SAVE}. Use the following formula to calculate the capacitor size:

$$C = (t_{FAULT_SAVE} \times I_{CC(MAX)})/(V_{IN} - V_{DIODE} - V_{UVLO})$$

where the capacitance is in Farads and t_{FAULT_SAVE} is in seconds, $I_{CC(MAX)}$ is 14mA, V_{DIODE} is the voltage drop across the diode, and V_{UVLO} is 2.7V. For example, with a V_{IN} of 14V, a diode drop of 0.7V, and a t_{FAULT_SAVE} of 153ns, the minimum required capacitance is 202µF.

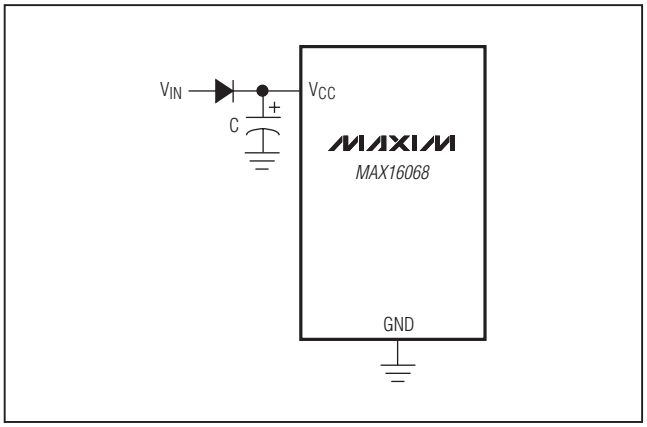


Figure 12. Power Circuit for Shutdown During Fault Conditions

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Configuring the Device

An evaluation kit and a graphical user interface (GUI) are available to create a custom configuration for the device (Figure 13).

Refer to the MAX16068 Evaluation Kit for configuration.

Cascading Multiple MAX16068s

Multiple MAX16068s can be cascaded to monitor more power supplies. There are many ways to cascade the devices depending on the desired behavior. In general, there are several techniques as follows:

- Configure a GPIO_ on each device to be $\overline{\text{EXTFAULT}}$ (open drain). Externally wire them together with a single pullup resistor. Set register bits r72h[5] and r6Dh[2] to '1' so that all faults propagate between devices. If a critical fault occurs on one device, $\overline{\text{EXTFAULT}}$ asserts, triggering the nonvolatile fault logger in all cascaded devices and recording a snapshot of all system voltages.
- Connect open-drain RESET outputs together to obtain a master system reset signal.
- Connect all EN inputs together for a master enable signal.

Layout and Bypassing

Bypass DBP and ABP each with a 1µF ceramic capacitor to GND. Bypass V_{CC} with a 10µF capacitor to ground. Avoid routing digital return currents through a sensitive analog area, such as an analog supply input return path or ABP's bypass capacitor ground connection. Use dedicated analog and digital ground planes. Connect the capacitors as close as possible to the device.

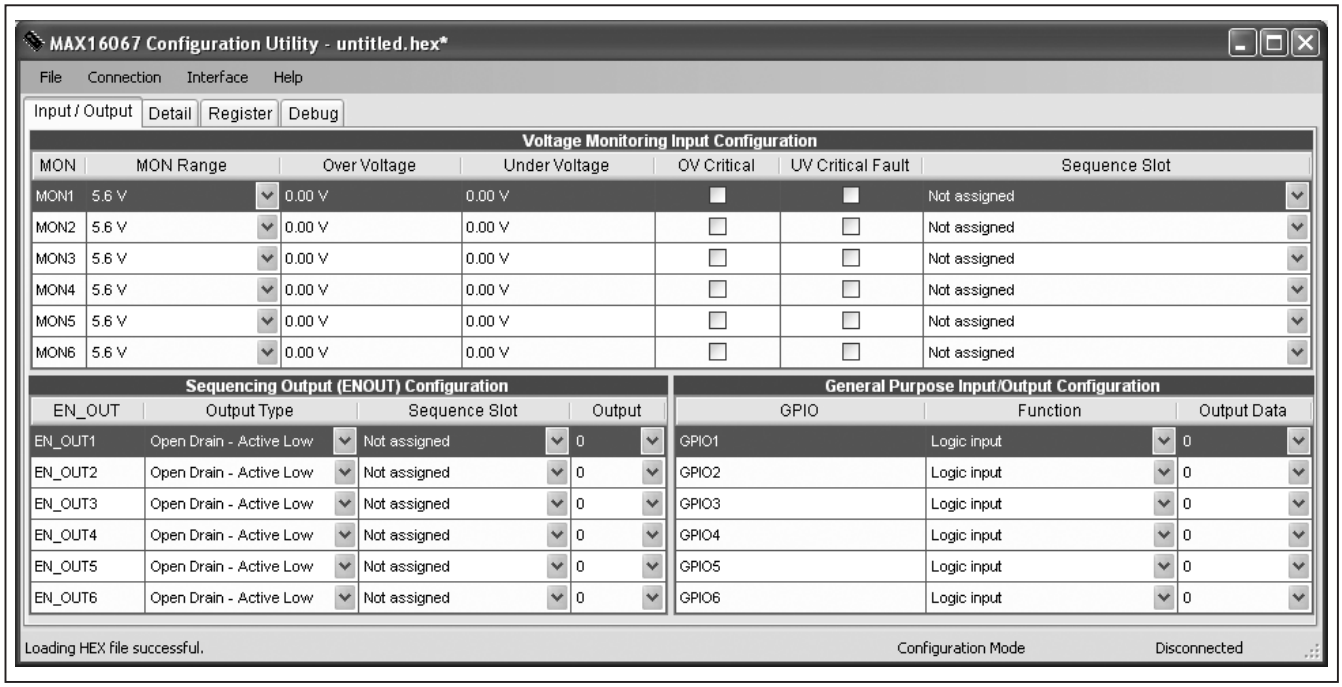


Figure 13. Graphical User Interface Screenshot

Register Map

FLASH ADDRESS	REGISTER ADDRESS	READ/ WRITE	DESCRIPTION
ADC VALUES, FAULT REGISTERS, GPIO_s AS INPUT PORTS—NOT IN FLASH			
—	000	R	MON1 ADC output, MSBs
—	001	R	MON1 ADC output, LSBs
—	002	R	MON2 ADC output, MSBs
—	003	R	MON2 ADC output, LSBs
—	004	R	MON3 ADC output, MSBs
—	005	R	MON3 ADC output, LSBs
—	006	R	MON4 ADC output, MSBs
—	007	R	MON4 ADC output, LSBs
—	008	R	MON5 ADC output, MSBs
—	009	R	MON5 ADC output, LSBs
—	00A	R	MON6 ADC output, MSBs
—	00B	R	MON6 ADC output, LSBs
—	00C–01A	—	Reserved
—	01B	R/W	Fault register—failed line flags
—	01C	R/W	Fault register—failed line flags
—	01D	—	Reserved
—	01E	R	GPIO_ data in (read only)
—	01F	—	Reserved
—	020	R/W	Flash status/reset output monitor
—	021	—	Reserved
GPIO_ AND OUTPUT DEPENDENCIES/CONFIGURATIONS			
230	030	—	Reserved
231	031	—	Reserved
232	032	—	Reserved
233	033	—	Reserved
234	034	—	Reserved
235	035	—	Reserved
236	036	R/W	FAULT dependencies
237	037	R/W	FAULT dependencies
238–23A	038–03A	—	Reserved
23B	03B	R/W	RESET output configuration
23C	03C	R/W	RESET output dependencies
23D	03D	R/W	RESET output dependencies
23E	03E	R/W	GPIO data out
23F	03F	R/W	GPIO configuration
240	040	R/W	GPIO configuration, ARANEN (ARA Enable)
241–242	041–042	—	Reserved

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Register Map (continued)

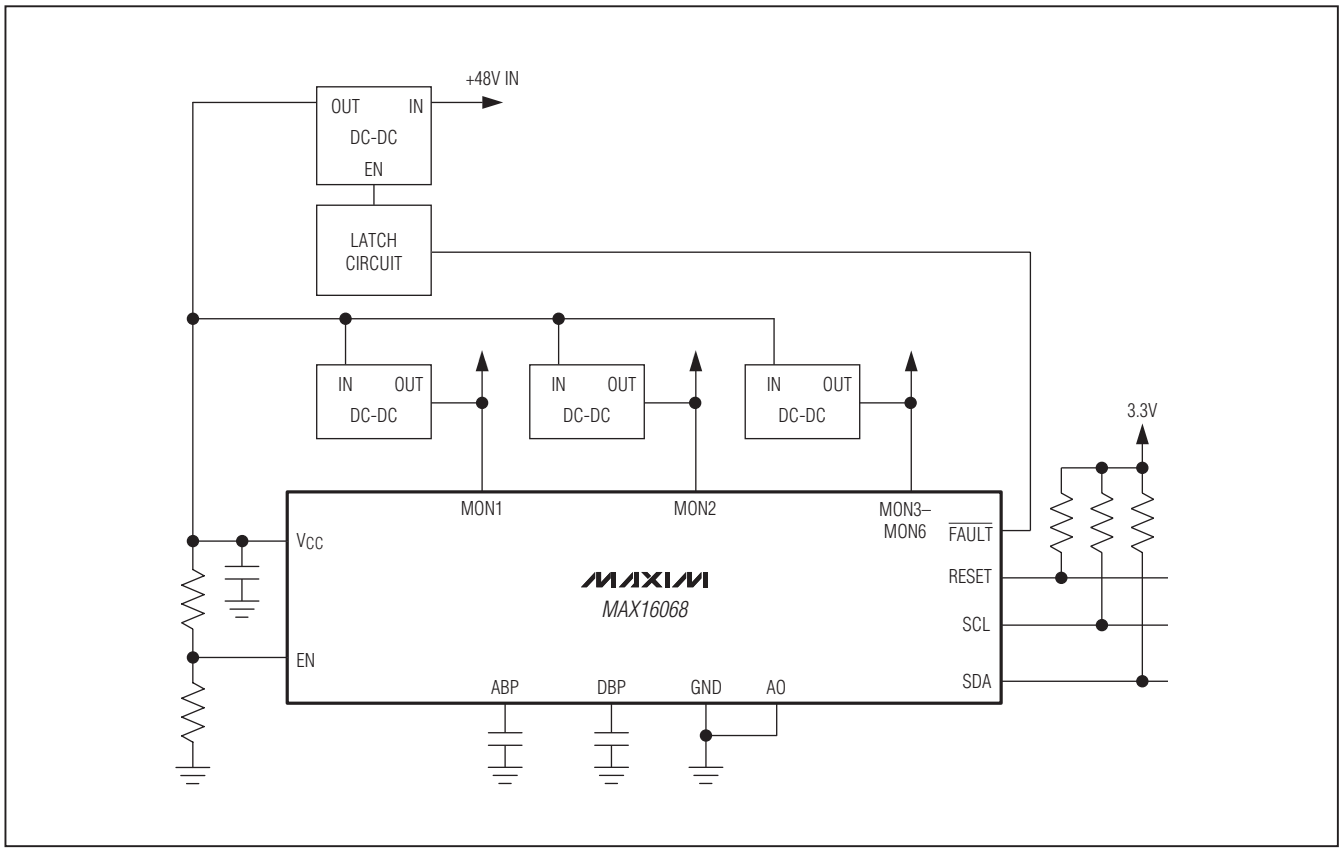
FLASH ADDRESS	REGISTER ADDRESS	READ/ WRITE	DESCRIPTION
ADC—CONVERSIONS			
243	043	R/W	ADCs voltage ranges for MON_ monitoring
244	044	R/W	ADCs voltage ranges for MON_ monitoring
245–247	045–047	—	Reserved
INPUT THRESHOLDS			
248	048	—	Reserved
249	049	R/W	MON1 OV threshold
24A	04A	R/W	MON1 UV threshold
24B	04B	—	Reserved
24C	04C	R/W	MON2 OV threshold
24D	04D	R/W	MON2 UV threshold
24E	04E	—	Reserved
24F	04F	R/W	MON3 OV threshold
250	050	R/W	MON3 UV threshold
251	051	—	Reserved
252	052	R/W	MON4 OV threshold
253	053	R/W	MON4 UV threshold
254	054	—	Reserved
255	055	R/W	MON5 OV threshold
256	056	R/W	MON5 UV threshold
257	057	—	Reserved
258	058	R/W	MON6 OV threshold
259	059	R/W	MON6 UV threshold
25A–26C	05A–06C	—	Reserved
FAULT SETUP			
26D	06D	R/W	Save after $\overline{\text{EXTFAULT}}$ fault control
26E	06E	R/W	Faults causing store in flash
26F	06F	R/W	Faults causing store in flash
270	070	R/W	Faults causing store in flash
271	071	—	Reserved
272	072	R/W	$\overline{\text{EXTFAULT}}$ enable

Register Map (continued)

FLASH ADDRESS	REGISTER ADDRESS	READ/ WRITE	DESCRIPTION
TIMEOUTS			
273	073	R/W	Watchdog independent mode, $\overline{\text{MARGIN}}$ enabled, soft RESET functionality
274	074	R/W	ADC fault deglitch/autoretry configuration
275	075	R/W	WDI toggle/fault timeout, reverse sequencing bit
276	076	R/W	WDRESET, WD timers
277	077	R/W	Boot-up delay
278	078	—	Reserved
279	079	—	Reserved
27A	07A	—	Reserved
27B	07B	—	Reserved
27C	07C	—	Reserved
27D	07D	—	Reserved
MISCELLANEOUS			
27E	07E	—	Reserved
27F	07F	—	Reserved
280	080	—	Reserved
281–283	081–083	—	Reserved
284	084	—	Reserved
285	085	—	Reserved
286	086	—	Reserved
287–289	087–089	—	Reserved
28A	08A	R/W	Customer use (version)
28B	08B	R/W	PEC enable/SMBus address
28C	08C	R/W	Lock bits
28D	08D	R	Revision code
USER FLASH			
300	39F	R/W	User flash
3A0	3AF	—	Reserved
3B0	3FF	R/W	User flash

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Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2855+6	21-0140	90-0026

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release	—
1	6/10	Updated the *Absolute Maximum Ratings*, *Typical Operating Characteristics*, *Detailed Description* and other sections, Table 23, Figure 9, and the *Register Map*.	2, 7, 23, 24, 28–31, 34, 39

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