



CSD25202W15 20-V P-Channel NexFET™ Power MOSFET

1 Features

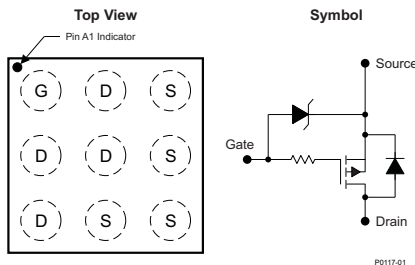
- Low-Resistance
- Small Footprint 1.5 mm × 1.5 mm
- Gate ESD Protection –3 kV
- Pb Free
- RoHS Compliant
- Halogen Free
- Gate-Source Voltage Clamp

2 Applications

- Battery Management
- Battery Protection

3 Description

This 21 mΩ, 20 V device is designed to deliver the lowest on resistance and gate charge in a small 1.5 mm × 1.5 mm chip scale package with excellent thermal characteristics in an ultra-low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	5.8		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.8		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = -1.8\text{ V}$	40	mΩ
		$V_{GS} = -2.5\text{ V}$	26	mΩ
		$V_{GS} = -4.5\text{ V}$	21	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.75		V

Ordering Information⁽¹⁾

Device	Qty	Media	Package	Ship
CSD25202W15	3000	7-Inch Reel	1.5-mm × 1.5-mm Wafer Level Package	Tape and Reel
CSD25202W15T	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

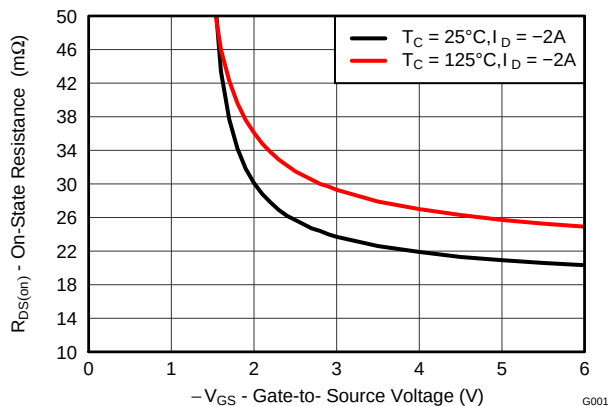
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–6	V
I_D	Continuous Drain Current ⁽¹⁾	–4	A
	Pulsed Drain Current ⁽²⁾	–38	A
I_G	Continuous Gate Current ⁽¹⁾	–0.5	A
	Pulsed Gate Current ⁽²⁾	–7	A
P_D	Power Dissipation	0.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Ball limited

(2) Typical $R_{\theta JA} = 220^\circ\text{C/W}$, pulse duration $\leq 100\text{ }\mu\text{s}$, duty cycle $\leq 1\%$

$R_{DS(on)}$ vs V_{GS}



Gate Charge

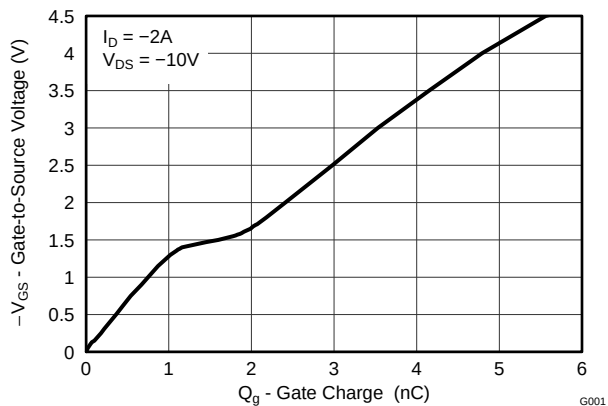


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4 Revision History

Changes from Original (June 2014) to Revision A	Page
• Corrected "Drain-to-Drain Voltage" to state "Drain-to-Source Voltage"	1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _{DS} = –250 μA	–20			V
BV _{GSS}	Gate-to-Source Voltage	V _{DS} = 0 V, I _G = –250 μA	–6		–7.2	V
I _{DDS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = –16 V			–1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = –6 V			–100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = –250 μA	–0.45	–0.75	–1.05	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = –1.8 V, I _{DS} = –2 A	40		52	mΩ
		V _{GS} = –2.5 V, I _{DS} = –2 A	26		32	mΩ
		V _{GS} = –4.5 V, I _{DS} = –2 A	21		26	mΩ
g _{fs}	Transconductance	V _{DS} = –2 V, I _{DS} = –2 A	16			S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = –10 V, f = 1 MHz	778		1010	pF
C _{OSS}	Output Capacitance		400		520	pF
C _{RSS}	Reverse Transfer Capacitance		21		27	pF
R _G	Series Gate Resistance ⁽¹⁾		31			Ω
Q _g	Gate Charge Total (–4.5 V)	V _{DS} = –10 V, I _D = –2 A	5.8		7.5	nC
Q _{gd}	Gate Charge - Gate-to-Drain		0.8			nC
Q _{gs}	Gate Charge - Gate-to-Source		1.1			nC
Q _{g(th)}	Gate Charge at V _{th}		0.6			nC
Q _{OSS}	Output Charge	V _{DS} = –9.5 V, V _{GS} = 0 V	8.7			nC
t _{d(on)}	Turn On Delay Time ⁽²⁾	V _{DS} = –10 V, V _{GS} = –4.5 V, I _{DS} = –2 A, R _G = 2 Ω	15			ns
t _r	Rise Time ⁽²⁾		12			ns
t _{d(off)}	Turn Off Delay Time ⁽²⁾		64			ns
t _f	Fall Time ⁽²⁾		28			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{DS} = –2 A, V _{GS} = 0 V	–0.75		–1	V
Q _{rr}	Reverse Recovery Charge	V _{SD} = –10 V, I _F = –2 A, di/dt = 200 A/μs	19			nC
t _{rr}	Reverse Recovery Time		26			ns

(1) Includes gate clamp resistor

(2) External R_G is in addition to the internal gate clamp resistor

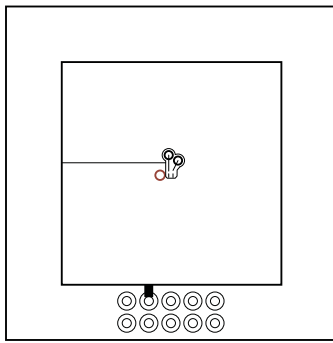
5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾		220		°C/W
	Junction-to-Ambient Thermal Resistance ⁽²⁾		140		

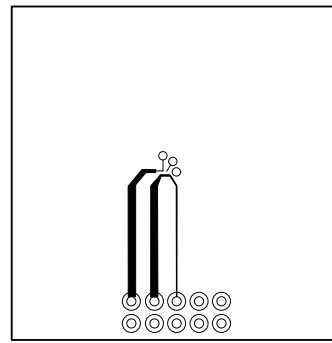
(1) Device mounted on FR4 material with minimum Cu mounting area.

(2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



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Typ $R_{\theta JA} = 140^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.



M0150-01

Typ $R_{\theta JA} = 220^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

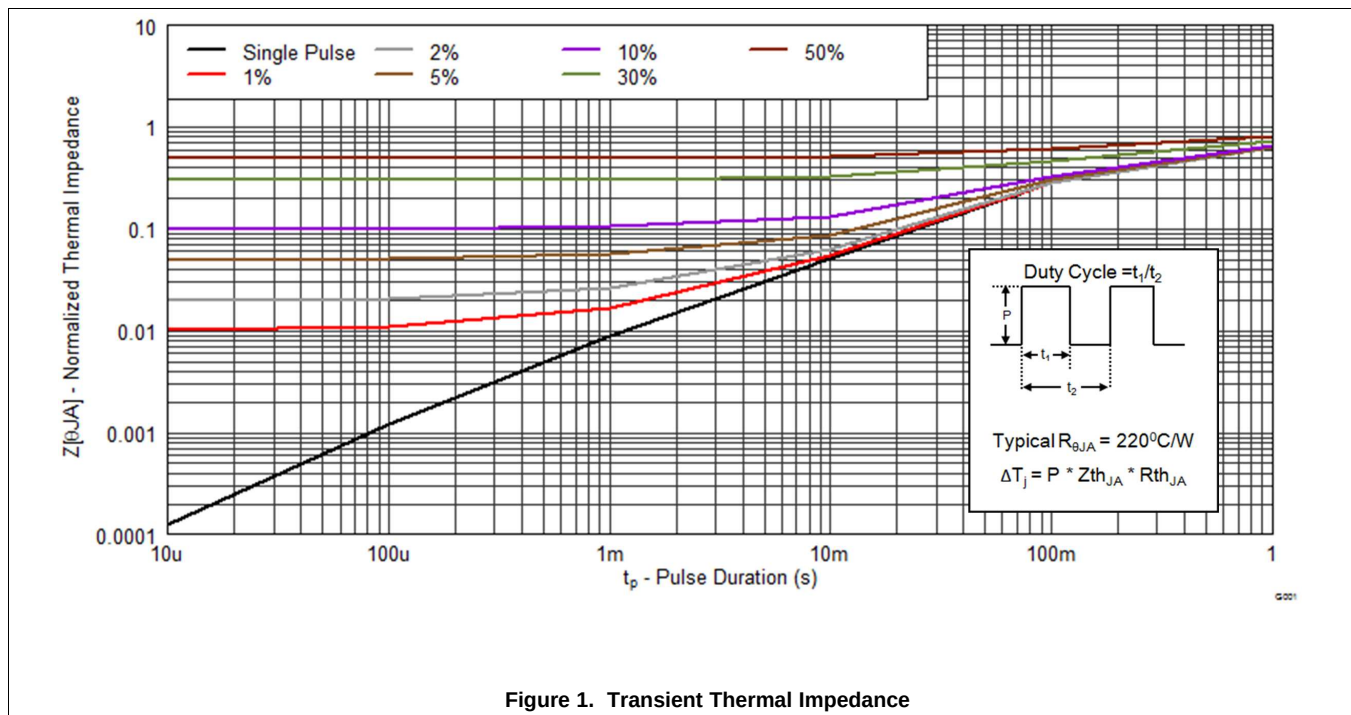


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

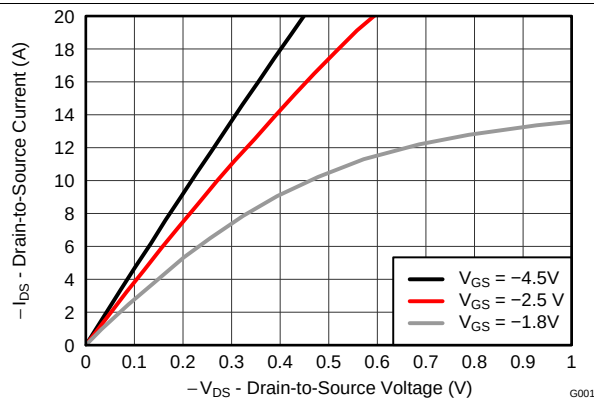


Figure 2. Saturation Characteristics

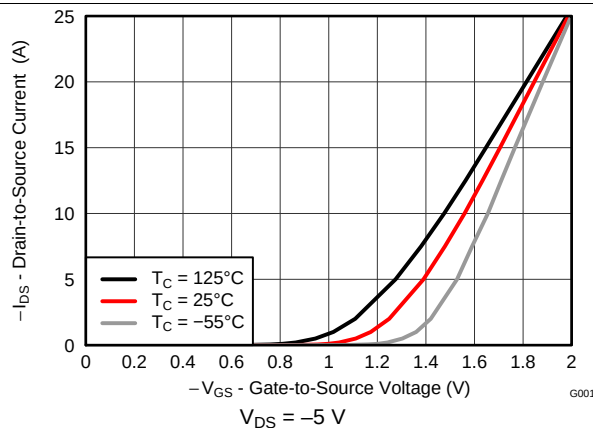


Figure 3. Transfer Characteristics

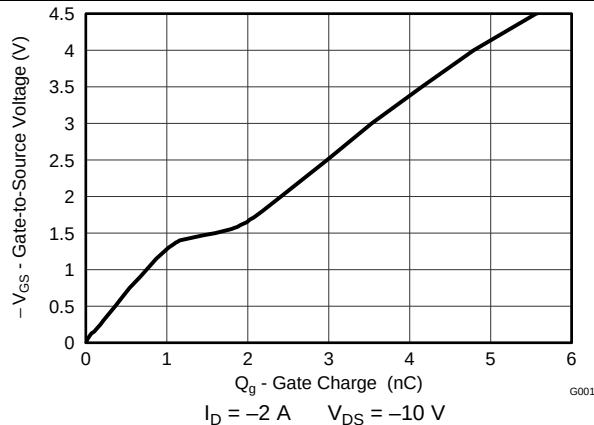


Figure 4. Gate Charge

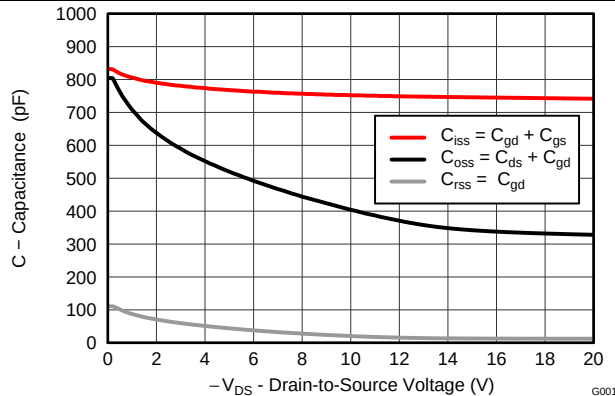


Figure 5. Capacitance

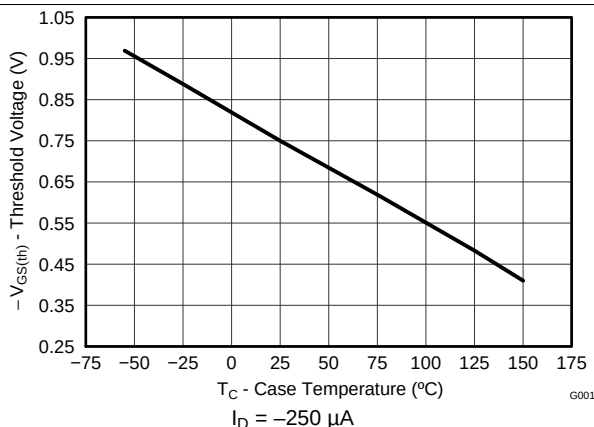


Figure 6. Threshold Voltage vs Temperature

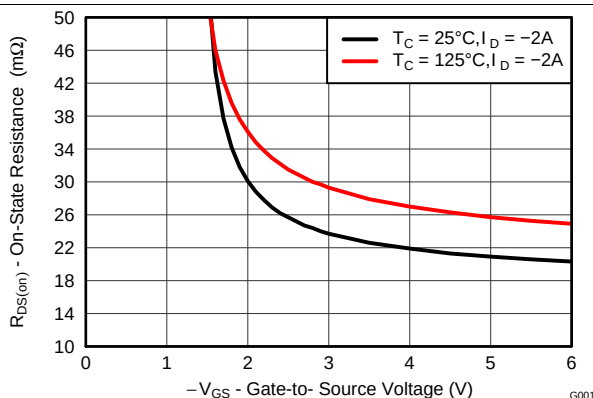


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

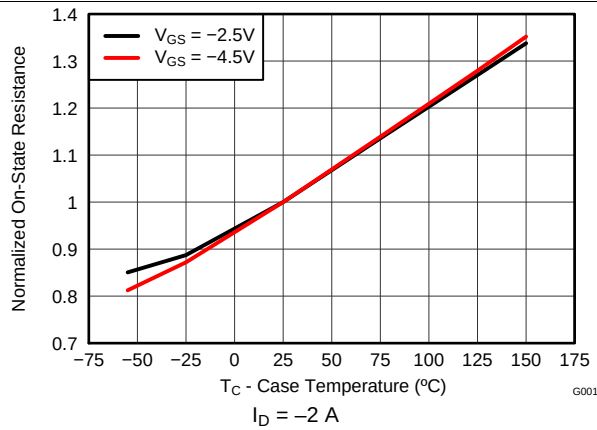


Figure 8. Normalized On-State Resistance vs Temperature

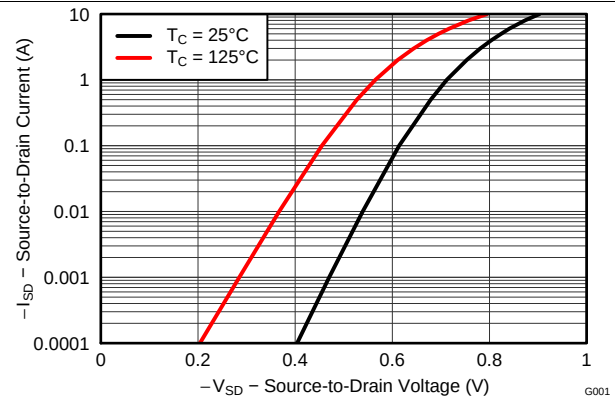


Figure 9. Typical Diode Forward Voltage

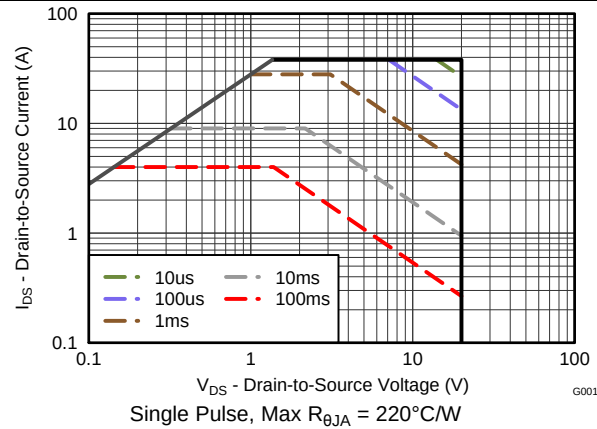


Figure 10. Maximum Safe Operating Area

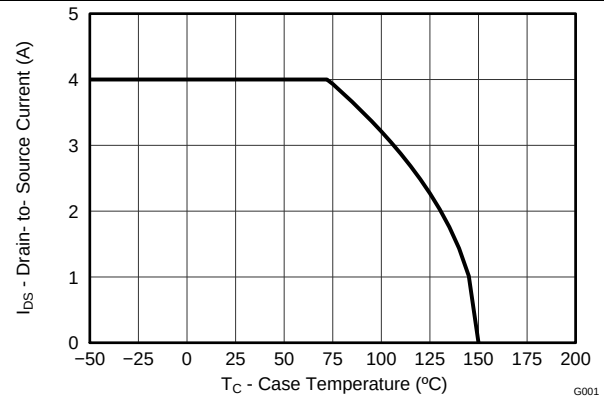


Figure 11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

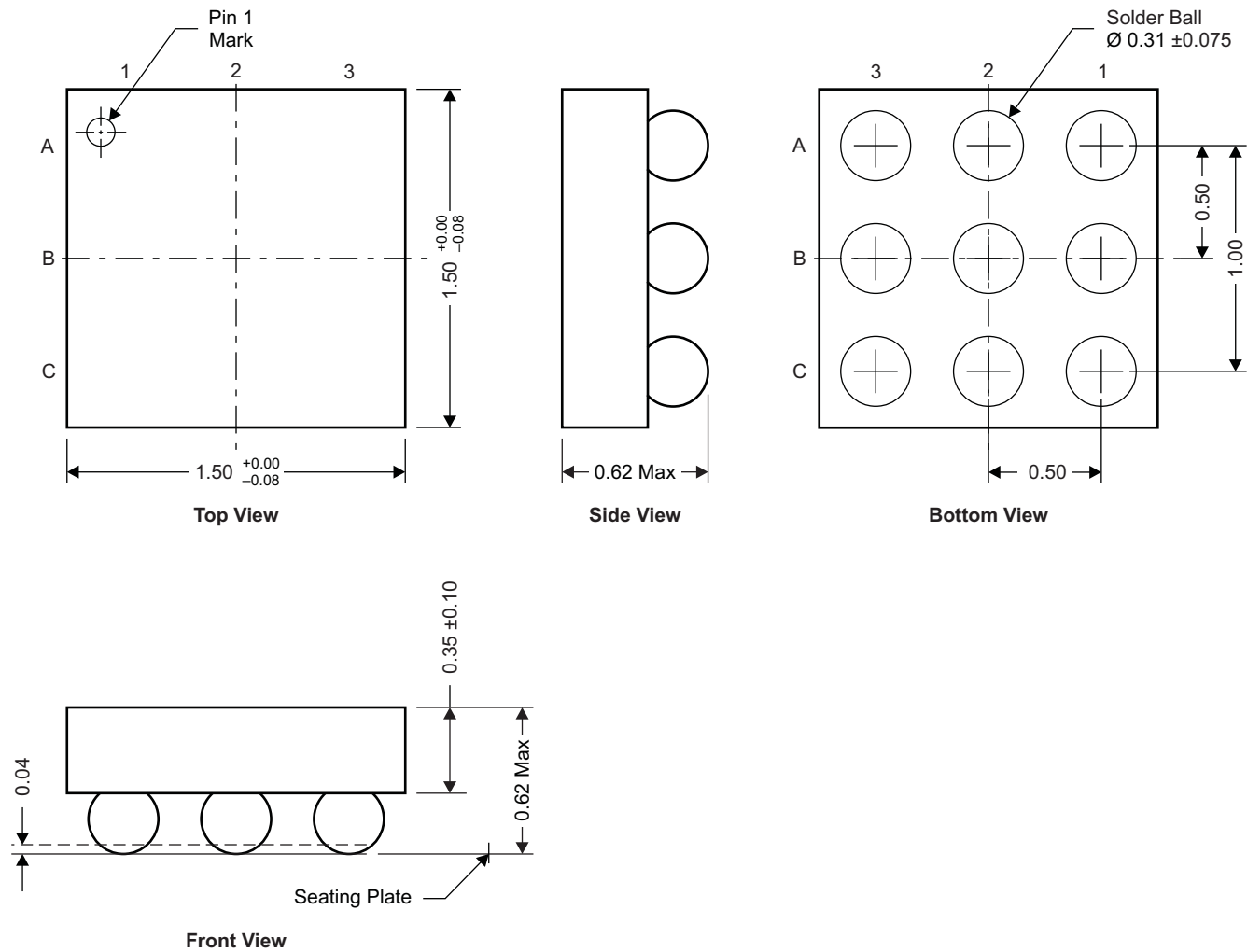
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD25202W15 Package Dimensions



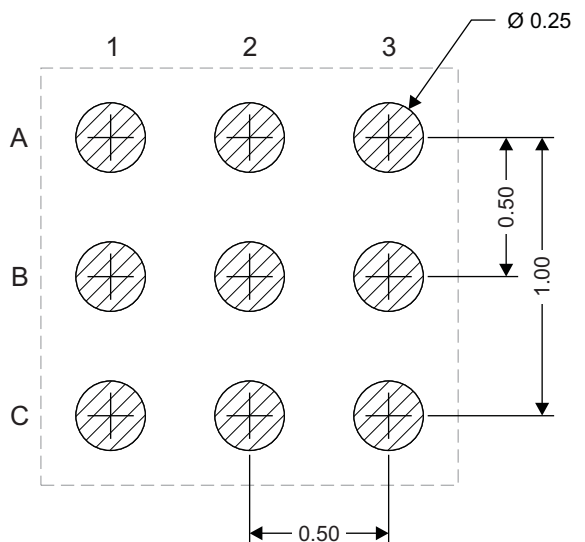
NOTE: All dimensions are in mm (unless otherwise specified)

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Pinout

POSITION	DESIGNATION
A1	Gate
A2, B1, B2, C1	Drain
A3, B3, C2, C3	Source

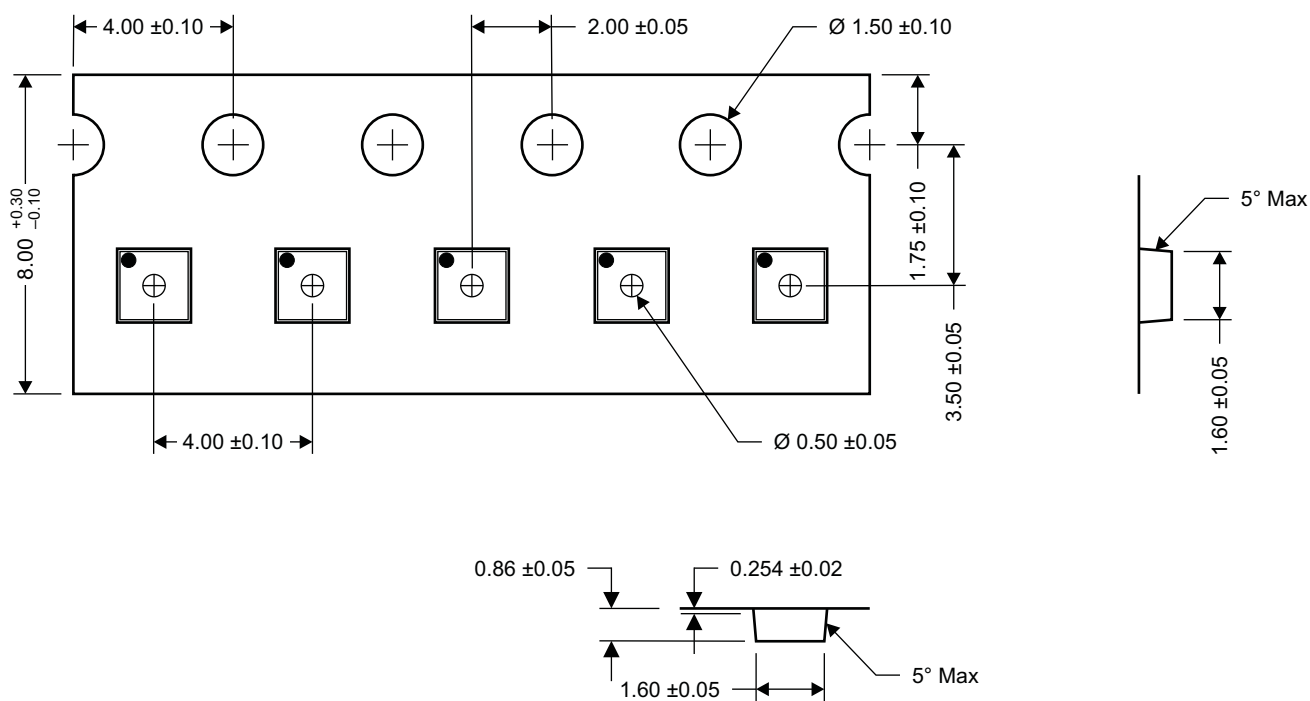
7.2 Recommended Land Pattern



M0172-01

NOTE: All dimensions are in mm (unless otherwise specified)

7.3 Tape and Reel Information



M0173-01

- NOTES:
1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
 2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
 3. Material: black static-dissipative polystyrene
 4. All dimensions are in mm (unless otherwise specified).
 5. Thickness: 0.30 ± 0.05 mm
 6. MSL1 260°C (IR and convection) PbF-reflow compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25202W15	ACTIVE	DSBGA	YZF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		25202	Samples
CSD25202W15T	ACTIVE	DSBGA	YZF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	25202	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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