PIC18F97J94

PIC18F97J94 Family
Silicon Errata and Data Sheet Clarification

The PIC18F97J94 family devices that you have received conform functionally to the current Device Data Sheet (DS30575**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1 The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F97J94 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F97J94 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A3
PIC18F65J94	320h	03h
PIC18F66J94	31Fh	03h
PIC18F66J99	31Eh	03h
PIC18F67J94	31Dh	03h
PIC18F85J94	31Ch	03h
PIC18F86J94	31Bh	03h
PIC18F86J99	31Ah	03h
PIC18F87J94	319h	03h
PIC18F95J94	318h	03h
PIC18F96J94	317h	03h
PIC18F96J99	316h	03h
PIC18F97J94	315h	03h

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F97J94 Family Flash Microcontroller Programming Specification"* (DS30000677) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A3
96 MHz PLL	Clock Switching	1.	Using several features involving clock switching may lead to undesired operation.	X
Deep Sleep	Sleep	2.	The part can experience a current spike if left in deep Sleep for a long duration of time.	X
Timer1/3/5	Interrupt	3.	When the timer is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur.	X
I/O Ports	Weak Pull-up	4.	Weak pull-up cannot be enabled on RF3 and RF4 pins when the USB module is not active.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: 96 MHz PLL

When using the 96 MHz PLL (PLLDIV = 0000-0111) as the system clock, the following features should not be used:

- Two-Speed Start-up
- Fail-Safe Clock Monitor
- Clock switching from other system clocks to the 96 MHz PLL
- Entering Sleep mode while the 96 MHz PLL clock source is still selected

Work around

For FRCPLL, it is possible to make a clock switch from FRC 500 kHz to FRCPLL without causing the undesired functionality, and hence if an application needs to perform a clock switch to FRCPLL, it can do so if it first performs a clock switch to FRC 500 kHz. For Two-Speed Start-up, Fail-Safe Clock Monitor and any clock switching to PRIPLL, there is no work around.

If the firmware is running from the FRCPLL output and wishes to go to Sleep mode, it should first clock switch to some other source (such as FRC at 8 MHz), which is not derived from the 96 MHz PLL, prior to entering Sleep. Upon waking from Sleep, the firmware should then make an intermediate clock switch to FRC at 500 kHz, prior to switching back to the FRCPLL output.

EXAMPLE 1: ENTRY AND EXIT FROM SLEEP WHEN USING FRCPLL

```
//Required sequence for entry into Sleep when running from the FRCPLL
OSCCON2bits.CLKLOCK = 0; //Make sure clock switching is enabled
                         //Switch away from FRCPLL, prior to entry into Sleep
OSCCON = 0x00;           //Select the FRC 8MHz (without PLL) as the clock source
SLEEP();                 //Enter Sleep mode

//After device wakes up, temporarily clock switch to fixed FRC 500 kHz, before switching back to FRCPLL
                         //mode
OSCCON = 0x06;           //Make sure clock switch has taken effect, as indicated by COSC bits getting
                         //set to FRC 500 kHz
while((OSCCON & 0x70) != 0x60);
                         //Now clock switch back to the FRCPLL setting
OSCCON3 = 0x01;          //Make sure 4 MHz is selected from FRC, since the 96 MHz PLL wants a 4 MHz
                         //input
OSCCON = 0x01;           //Request switch to FRCPLL output
```

Affected Silicon Revisions

A3							
X							

2. Module: Deep Sleep

A current spike of roughly 10X of normal deep Sleep current occurs if:

- The part is left in deep Sleep for a long duration of time (actual time depends on capacitance on VCAP pin).
- Current spike occurs when voltage on VCAP pin is between 0.7V and 0.5V.

Work around

None.

Affected Silicon Revisions

A3							
X							

3. Module: Timer1/3/5

When Timer1, Timer3 or Timer5 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to 0x0000 when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 2.

EXAMPLE 2: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;         //Stop timer from incrementing
PIE1bits.TMR1IE = 0;          //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                 //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;         //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);          //Wait for 2 timer increments more than the Updated Timer
                              //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                        //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;          //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;          //Now re-enable interrupt vectoring for Timer1
```

Affected Silicon Revisions

A3							
X							

4. Module: I/O Ports

Weak pull-up cannot be enabled on pins RF3 and RF4 when RFPU bit of PADCFG register is set and the USB module is disabled.

Work around

None.

Affected Silicon Revisions

A3							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30575**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Peripheral Module Disable

Register 4-8 in the PIC18F97J94 device data sheet is incorrect. Refer to the register below for the correct naming conventions that are in bold.

REGISTER 4-8: PMD3: PERIPHERAL MODULE DISABLE REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DSMMD	CTMUMD	ADCMD	RTCCMD	LCDMD	PSPMD	REFO1MD	REFO2MD
bit 7							bit 0

bit 7 **DSMMD:** Modulator Output Module Disable bit
1 = The Modulator Output module is disabled. All Modulator Output registers are held in Reset and are not writable.
0 = The Modulator Output module is enabled.

2. Module: Analog-to-Digital Converter

Section 22.11.3 incorrectly refers to the nonexistent ADSIDL bit to control whether the module stops or continues operation in Idle. Instead, the section should read as follows:

"The module will continue normal operation when the device enters Idle mode. If the A/D interrupt is enabled (ADIE = 1), the device will wake-up from Idle mode when the A/D interrupt occurs. If the respective global interrupt enable bit(s) are also set, program execution will resume at the A/D Interrupt Service Routine (ISR). After the ISR completes, execution will continue from the instruction after the SLEEP instruction that placed the device in Idle mode."

3. Module: Analog-to-Digital Converter

Registers 22-14, 22-15, 22-16, and 22-17 are incorrectly named. The correct names for these registers are ADCHIT1H, ADCHIT1L, ADCHIT0H and ADCHIT0L, respectively.

4. Module: Analog-to-Digital Converter

Table 22-1 contains incorrect names for several registers and bits. The corrected table is as follows:

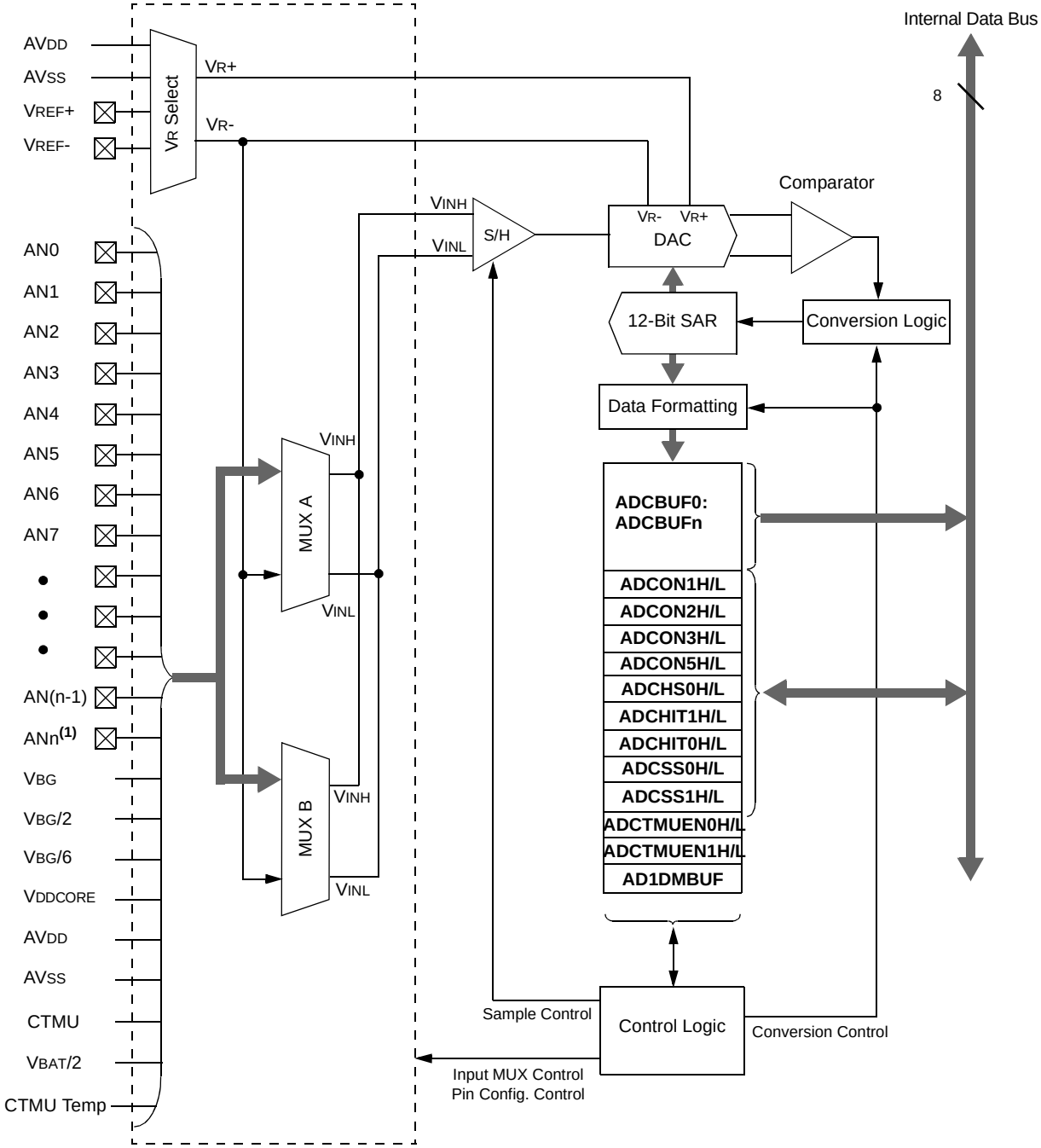
TABLE 22-1: A/D MODULE FUNCTIONS BY REGISTERS AND BITS

A/D Function	Register(s)	Specific Bits
Input	**ADCON2H/L**	PVCFG<1:0>, NVCFG, OFFCAL, CSCNA, ALTS
	ADCON5H/L	CTMREQ, BGREQ, VRSREQ
	ADCHS0H/L	CH0NB<2:0>, CH0SB<4:0>, CH0NA<2:0>, CH0SA<4:0>
	ADCSS0H/L	**CSS<15:0>**
	ADCSS1H/L	**CSS<30:16>**
	ADCTMUEN0H/L	CTMEN<15:0>
	ADCTMUEN1H/L	CTMEN<31:16>
Conversion	**ADCON1H/L**	ADON, ADSIDL, SSRC<3:0>, ASAM, SAMP, DONE, **MODE12**
	ADCON2H/L	SMPI<4:0>
	ADCON3H/L	EXTSAM
	ADCON5H/L	ASEN, LPEN, ASINT<1:0>
Timing	**ADCON3H/L**	ADRC, SAMC<4:0>, ADCS<7:0>
Output	**ADCON1H/L**	FORM<1:0>
	ADCON2H/L	BUFS, BUFM, BUFREGEN
	ADCON5H/L	WM<1:0>, CM<1:0>

5. Module: Analog-to-Digital Converter

The block diagram in Figure 22-1 contains incorrect names for several registers. The corrected figure is as follows:

FIGURE 22-1: 12-BIT A/D CONVERTER BLOCK DIAGRAM (PIC18F97J94)



Note 1: AN16 through AN23 are implemented on 80-pin and 100-pin devices only.

6. Module: Analog-to-Digital Converter

The note on page 458 incorrectly mentions the AD1CON3 and AD1CSSL registers. It should refer to ADCON3H, ADCON3L, ADCSS0L and ADCSS0H registers.

7. Module: Analog-to-Digital Converter

The code in Example 22-1 will not compile properly. The corrected code is as follows:

EXAMPLE 22-1: CONVERTING ONE CHANNEL, MANUAL SAMPLE START, MANUAL CONVERSION START CODE

```
int ADCValue;

ANCON1= 0x02;                    // AN2 as analog, all other pins are digital
ADCON1L = 0x00;                  // SAMP bit = 0 ends sampling and starts converting
ADCHS0L = 0x02;                  // Connect AN2 as S/H+ input
                                 // in this example AN2 is the input
ADCSS0L = 0;
ADCON3L = 0x02;                  // Manual Sample, Tad = 3Tcy
ADCON2L = 0;
ADCON1Hbits.ADON = 1;            // turn ADC ON

while (1)                        // repeat continuously
{
    ADCON1Hbits.SAMP = 1;        // start sampling...
    Delay();                     // Ensure the correct sampling time has elapsed
                                 // before starting conversion.
    ADCON1Hbits.SAMP = 0;        // start converting
    while (!ADCON1Lbits.DONE){}; // conversion done?
    ADCValue = ADCBUF0;          // yes then get ADC value
}
```

8. Module: Analog-to-Digital Converter

The code in Example 22-2 will not compile properly. The corrected code is as follows:

EXAMPLE 22-2: CONVERTING ONE CHANNEL, MANUAL SAMPLE START, TAD-BASED CONVERSION START CODE

```
int ADCValue;

ANCON2  = 0x10;                      // all PORTB = Digital; RB12 = analog
ADCON1L = 0x70;                      // SSRC<2:0> = 111 implies internal counter ends sampling
                                     // and starts converting.
ADCHS0L = 0x0C;                      // Connect AN12 as S/H input.
                                     // in this example AN12 is the input
ADCSS0H = 0;
ADCON3H = 1F;                        // Sample time = 31Tad, Tad = 3Tcy
ADCON3L = 02;
ADCON2L = 0;
ADCON1Hbits.ADON = 1;                // turn ADC ON
while (1)                            // repeat continuously
{
    ADCON1Lbits.SAMP = 1;            // start sampling, then after 31Tad go to conversion
    while (!ADCON1Lbits.DONE){};     // conversion done?
    ADCValue = ADCBUF0;              // yes then get ADC value
}                                    // repeat
```

9. Module: Analog-to-Digital Converter

The note in Section 22.6, “A/D Results Buffer,” incorrectly refers to AD1CON5<3:2>. It should refer to ADCON5L<3:2>.

10. Module: Analog-to-Digital Converter

The note in 22.7.1, “Operating Modes,” incorrectly refers to AD1CON2<10>. It should refer to ADCON2H<2>.

11. Module: I/O Ports

In Table 1-4 on page 20 and Table 11-3 on page 205, RC0 and RC1 are listed as general purpose I/O pins. Actually, the RC0 and RC1 pins should be listed as general purpose input pins, with no output available on those pins.

TABLE 1-4: PIC18F97J94 PINOUT I/O DESCRIPTION

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	100	80	64			
SOSCO/SCLKI/ PWRLCLK/RC0	45	36	30			
SOSCO				O	—	SOSC oscillator output
SCLKI				I	ST	Digital SOSC input
PWRLCLK				I	ST	SOSC input at 50 Hz or 60 Hz only (RTCCLKSEL<1:0> = 11 or 10)
RC0				I	**ST**	**General purpose Input pin**
SOSCI/RC1	44	35	29			
SOSCI				I	Analog	Timer1 oscillator input.
RC1				I	**ST**	**General purpose Input pin**

TABLE 11-3: PORTC FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RC0/ PWRLCLK/ SCLKI/SOSCO	**RC0**	1	I	ST	PORTC<0> data input
	PWRLCLK	1	I	ST	Optional RTCC input from power line clock (50 or 60 Hz)
	SCLKI	x	I	ST	Digital SOSC input.
	SOSCO	x	O	ANA	Secondary Oscillator (SOSC) feedback output connection
RC1/SOSCI	**RC1**	1	I	ST	PORTC<1> data input
	SOSCI	x	I	ANA	Secondary Oscillator (SOSC) input connection

Also, the RF3 and RF4 pins show output functionality in Table 11-6 on page 211. However, RF3 and RF4 have input only, with no output available on those pins.

Furthermore, RF3 and RF4 pins do not have remappable pin functionality. Therefore, RP41 and RP45 do not exist. All references to RP41 and RP45 should be removed.

TABLE 11-6: PORTF FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RF3/D-	**RF3**	1	I	ST	PORTF<3> data input.
	D-	x	I	XCVR	USB bus minus line output.
		x	O	XCVR	USB bus minus line input.
RF4/D+	**RF4**	1	I	ST	PORTF<4> data input.
	D+	x	I	XCVR	USB bus plus line input.
		x	O	XCVR	USB bus plus line output.

In addition, Table 6-2 on page 126 lists TRISC0, TRISC1, TRISF3, TRISF4, LATC0, LATC1, LATF3 and LATF4. None of these bits have any effect on the pins in question and should be ignored.

TABLE 6-2: REGISTER FILE SUMMARY

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F9Ah	TRISJ	TRISJ7	TRISJ6	TRISJ5	TRISJ4	TRISJ3	TRISJ2	TRISJ1	TRISJ0
F99h	TRISH	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0
F98h	TRISG	TRISG7	TRISG6	—	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0
F97h	TRISF	TRISF7	TRISF6	TRISF5	—	—	TRISF2	—	—
F96h	TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0
F95h	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
F94h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	—	—
F93h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
F92h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
F91h	LATJ	LATJ7	LATJ6	LATJ5	LATJ4	LATJ3	LATJ2	LATJ1	LATJ0
F90h	LATH	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0
F8Fh	LATG	LATG7	LATG6	—	LATG4	LATG3	LATG2	LATG1	LATG0
F8Eh	LATF	LATF7	LATF6	LATF5	—	—	LATF2	—	—
F8Dh	LATE	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0
F8Ch	LATD	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0
F8Bh	LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	—	—

12. Module: Master Synchronous Serial Port (MSSP)

Note 1 on page 397, below Table 20-2, is inaccurate and should be disregarded.

TABLE 20-2: I^2C CLOCK RATE w/BRG

FOSC	FCY	FCY * 2	BRG Value	FSCL (Two Rollovers of BRG)
64 MHz	16 MHz	32 MHz	27h	400 kHz
64 MHz	16 MHz	32 MHz	32h	313.72 kHz
64 MHz	16 MHz	32 MHz	9Fh	100 kHz
16 MHz	4 MHz	8 MHz	09h	400 kHz
16 MHz	4 MHz	8 MHz	0Ch	308 kHz
16 MHz	4 MHz	8 MHz	27h	100 kHz
4 MHz	1 MHz	2 MHz	02h	333 kHz
4 MHz	1 MHz	2 MHz	09h	100 kHz
16 MHz	4 MHz	8 MHz	03h	1 MHz(1)

Note 1: A minimum of 16 MHz FOSC is required to get 1 MHz I^2C.

13. Module: I/O Ports

The two notes in Section 11.1.1, “Output Pin Drive,” on page 197 of the data sheet list the incorrect pin count devices. They should read:

Note 1: These ports are not available on **64**-pin devices.

2: These ports are not available on **64**-pin or **80**-pin devices.

14. Module: Oscillator

Step 4 of the clock switching sequence in Section 3.13.2, “Oscillator Switching Sequence,” on page 58 of the data sheet refers to the OSWEN bit, which is not implemented on this device. As such, this step does not occur and should be disregarded.

15. Module: Analog-to-Digital Converter

The ANCFG register, while present on the part, is not documented in the data sheet. Below is the reference information for the ANCFG register.

ANCFG: ANALOG INPUT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	VBG6EN	VBG2EN	VBGEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **VBG6EN:** Band Gap Divide-by-6 Control bit
1 = Reference voltage on
0 = Reference voltage off

bit 1 **VBG2EN:** Band Gap Divide-by-2 Control bit
1 = Reference voltage on
0 = Reference voltage off

bit 0 **VBGEN:** Band Gap Control bit
1 = Reference voltage on
0 = Reference voltage off

16. Module: Oscillator

A new **Section 3.9.4 "SOSC Crystal Selection"** is added with the following text:

3.9.4 SOSC CRYSTAL SELECTION

"A typical 50K ESR and 12.5 pF CL (capacitive loading) rated crystal is recommended for reliable operation of the SOSC. The duty cycle of the SOSC output can be measured on the REFO pin and is recommended to be within +/-15% from a 50% duty cycle."

17. Module: Oscillator

Table 3-3 in Section 3.8.1, "Oscillator Modes and USB Operation", should be corrected as shown below:

TABLE 3-3: 96 MHz PLL DERIVED SYSTEM CLOCK OPTIONS

MCU Clock Division (CPDIV<1:0>)	System Clock Frequency (Instruction Rate in MIPS)
None (00)	64 MHz (16)
÷2 (01)	32 MHz (8)(1)
÷4 (10)	**16** MHz (4)(1)
÷8 (11)	**8** MHz (**2**)(1)

Note 1: These options are not compatible with USB operation. They may be used whenever the PLL branch is selected and the USB module is disabled.

18. Module: Analog-to-Digital Converter

All references to TCY in Section 22.0, "12-Bit A/D Converter with Threshold Scan," are substituted with the 2/FOSC value.

Therefore, Equation 22-1 should be corrected as shown below:

EQUATION 22-1: A/D CONVERSION CLOCK PERIOD

$$T_{AD} = (2/F_{OSC}) \bullet (ADCS + 1)$$

$$ADCS = \left(\frac{T_{AD} \bullet F_{OSC}}{2}\right) - 1$$

Note: PLL is disabled.

Register 22-9 ADCON3L incorrectly references Tcy; it should be substituted with (2/FOSC).

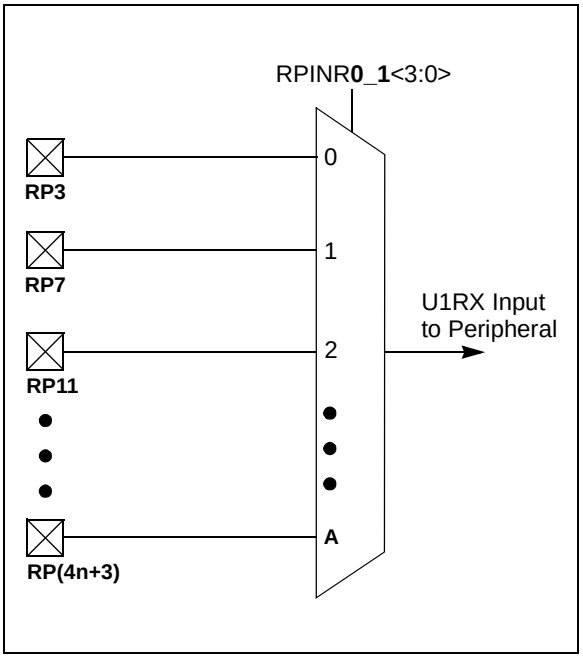
19. Module: PPS

The example given in Section 11.15.3.1, "Input Mapping", on how to assign U1RX to the RP2 pin is incorrect. The U1RX input cannot be assigned to the RP2 pin. The last paragraph of the above-mentioned section should therefore read:

"For example, to assign U1RX to **RP3**, write the value, h'0, to RPINR**0_1**<3:0>. Figure 11-7 illustrates remappable pin selection for the U1RX input."

Additionally, Figure 11-7 indicates that the U1RX input can be assigned to any RPn pin, which is incorrect. The U1Rx pin can only be remapped to one of the following RP(4n+3) pins, as indicated in Table 11-13: RP3, RP7, RP11, RP15, RP19, RP23, RP27, RP31, RP35, RP39, RP43.

FIGURE 11-7: REMAPPABLE INPUT FOR U1RX



20. Module: I/O Ports

The PORT registers names in Section 11.14, "Virtual PORT", are PORTVR, LATVR and TRISVR. They should instead be PORTVP, LATVP and TRISVP, respectively. Thus, the following sentence in Section 11.14 is changed to read: "The virtual PORT is controlled through the **PORTVP, LATVP** and **TRISVP** registers."

21. Module: I/O Ports

In Table 11-12, Table 11-13 and Table 11-14, the individual pins of the virtual PORT are labeled as PBIO0-7. They should instead be labeled as RVP0-7.

22. Module: I/O Ports

Example 11-6 shows incorrect settings of the ANCON1 and ANCON registers. The correct code is as follows:

EXAMPLE 11-6: INITIALIZING PORTF

```
CLRF     PORTF    ; Initialize PORTF by
                  ; clearing output
                  ; data latches
CLRF     LATF     ; Alternate method
                  ; to clear output
                  ; data latches
BANKSEL  ANCON1   ; Select bank with ANCON1 register
MOVLW    BFh      ; Make RF2 digital
MOVWF    ANCON1   ;
BANKSEL  ANCON2   ;
MOVLW    F1h      ; Make RF5, RF6, RF7 digital
MOVWF    ANCON2   ;
BANKSEL  TRISF    ; Select bank with TRISF register
MOVLW    0F3h     ; Value used to
                  ; initialize data
                  ; direction
MOVWF    TRISF    ; Set RF3:RF2 as outputs
                  ; RF7:RF4 as inputs
```

23. Module: Comparator

The descriptions of bits 1-0 (CCH<1:0>) in Register 23-1 on page 490, are inverted for settings '10' and '00'. The corrected settings are:

"10 = Inverting input of comparator connects to **C2INB** pin"

and

"00 = Inverting input of comparator connects to **CxINx** pin(2)"

Also, Note 2 of the same register is corrected as shown below:

"Comparator 1 and Comparator 3 use C2INB as the input to the inverting terminal. Comparator 2 uses **C2IND** as the input to the **inverting** terminal."

24. Module: Interrupts

In Section 10.9, "INTx Pin Interrupts," external interrupts INT1, INT2, INT3 are mentioned multiplexed with the RB1, RB2, RB3 pins, respectively. This is incorrect. These interrupts can only be used via remappable pins as per Table 11-13 of the data sheet.

25. Module: Configuration Word

In Register 28-4, CONFIG2H, the description for PLLDIV setting '0110' is incorrect. The correct description should be:

"0110 = 96 MHz PLL is selected; oscillator divided by **8** (**32** MHz input)"

26. Module: Electrical Specifications

The title for Table 31-17 on page 646 should be changed to read "**4/6/8x** PLL Clock Timing Specifications."

The table below is added to the data sheet following Table 31-17.

96 MHz PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 2.0V to 3.6V)

Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions
F_{PLLIN}	PLL Input Frequency Range (after prescaling)	3.94	4	4.06	MHz	V_{DD} = 2.0-3.6V, -40°C to +85°C
F_{SYS}	On-Chip VCO System Frequency	—	96	—	MHz	V_{DD} = 2.0-3.6V, -40°C to +85°C
t_{rc}	PLL Start-up Time (Lock Time)	—	—	200	µs	
Δ_{CLK}	CLKOUT Stability (Jitter)	-0.25	—	+0.25	%	

27. Module: Analog-to-Digital Converter

In Register 22-5, ADCON1L, the description for bit 7-4 SSRC<3:0> for setting '1xxx' is incorrect. The correct description should be:

SSRC<3:0>: Sample Clock Source Selects bits

1111-1110 = Reserved, do not use
1101 = CMP1
1100 = Reserved, do not use
1011 = CCP4
1010 = ECCP3
1001 = ECCP2
1000 = ECCP1
0111 = The SAMP bit is cleared after SAMC<4:0> number of T_{AD} clocks following the SAMP bit being set (Auto-Convert mode); no extended sample time is present
0110 = Reserved, do not use
0101 = TMR1
0011 = TMR5
0010 = TMR3
0001 = INT0
0000 = The SAMP bit must be cleared by software to start conversion.

28. Module: I/O Ports

In section 11.1, the statement "All of the digital ports are 3.6V tolerant" should be removed.

And the absolute maximum ratings of the I/O pins should also be modified to the following:

RA2, RA3 = -300mV to (V_{DD} + 300mV)

RA6, RA7, RC0, RC1 = -300mV to (V_{DD} + 300mV) (Note 1)

RF3/RF4 (the USB D+/D- pins) = supports "USB specific levels" (ex: -1.0V to +4.6V, but only when the external source impedance is >= 28 ohms, and the VUSB3V3 pin voltage is >= 3.0V, otherwise: -500mV to (VUSB3V3+500mV))

All other general purpose I/O pins (including $\overline{MCLR}$), when V_{DD} is < 2.0V: -300mV to +4.0V

All other general purpose I/O pins (including $\overline{MCLR}$), when V_{DD} is >= 2.0V: -300mV to +6.0V (Note 2)

Note 1: When the pins are used to drive a crystal or ceramic resonator, natural oscillation waveforms slightly exceeding the -300mV to (V_{DD}+300mV) range may sometimes occur, and if present, such waveforms are allowed. If these pins are instead used as general purpose inputs, the external driving source should adhere to the -300mV to (V_{DD}+300mV) specification.

Note 2: In addition to the above absolute maximums, any I/O pin voltage that is actively selected at runtime by the ADC channel select MUX must also meet the Vain requirements (param. A25 in Table 31-36).

29. Module: Electrical Specifications

V_{IH} Input High Voltage Min. and Max. specifications have been corrected as follows:

TABLE 11-4: DC CHARACTERISTICS: POWER-DOWN AND SUPPLY CURRENT PIC18F97J94 FAMILY (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	V_{IL}	**Input Low Voltage**				
		All I/O Ports:				
D031		Schmitt Trigger Buffer	Vss	0.2 V_{DD}	V	2V ≤ V_{DD} ≤ 3.6V
D031A		RC3 and RC4	Vss	0.3 V_{DD}	V	I^2C enabled
D031B			Vss	0.8	V	SMBus enabled
D032		$\overline{MCLR}$	Vss	0.2 V_{DD}	V	
D033		OSC1	Vss	0.2 V_{DD}	V	LP, MS, HS modes
D033A		OSC1	Vss	0.2 V_{DD}	V	EC modes
D034		SOSCI	Vss	0.3 V_{DD}	V	
	V_{IH}	**Input High Voltage**				
		All I/O Ports:				
D041		Schmitt Trigger Buffer	**0.8 V_{DD}**	**V_{DD}**	V	2V ≤ V_{DD} ≤ 3.6V
D041A		RC3 and RC4	0.7 V_{DD}	**V_{DD}**	V	I^2C enabled
D041B			2.1	**V_{DD}**	V	SMBus enabled
D042		$\overline{MCLR}$	0.8 V_{DD}	V_{DD}	V	
D043		OSC1	0.9 V_{DD}	V_{DD}	V	RC mode
D043A		OSC1	0.7 V_{DD}	V_{DD}	V	HS mode
D044		SOSCI	0.7 V_{DD}	V_{DD}	V	
	I_{IL}	**Input Leakage Current**[1]				
D060		I/O Ports	±50	±500	nA	Vss ≤ V_{PIN} ≤ V_{DD} Pin at high-impedance
D061		$\overline{MCLR}$	—	±500	nA	Vss ≤ V_{PIN} ≤ V_{DD}
D063		OSC1	—	1	µA	Vss ≤ V_{PIN} ≤ V_{DD}
D070	I_{PU}	**Weak Pull-up Current**				
		Weak Pull-up Current	50	400	µA	V_{DD} = 3.6V, V_{PIN} = Vss
	V_{OL}	**Output Low Voltage**				
D080		I/O Ports:	—	0.4	V	I_{OL} = 6.6 mA, V_{DD} = 3.6V
		All Ports	—	0.4	V	I_{OL} = 5.0 mA, V_{DD} = 2V
D083		OSC2/CLKO	—	0.4	V	I_{OL} = 6.6 mA, V_{DD} = 3.6V
		(EC modes)	—	0.4	V	I_{OL} = 5.0 mA, V_{DD} = 2V
	V_{OH}	**Output High Voltage**[1]				
D090		I/O Ports:	3.0	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
		All Ports	2.4	—	V	I_{OH} = -6.0 mA, V_{DD} = 3.6V
			1.6	—	V	I_{OH} = -1.0 mA, V_{DD} = 2V
D092		OSC2/CLKO	1.4	—	V	I_{OH} = -3.0 mA, V_{DD} = 2V
		(INTOSC, EC modes)				
			2.4	—	V	I_{OH} = -6.0 mA, V_{DD} = 3.6V
			1.4	—	V	I_{OH} = -1.0 mA, V_{DD} = 2V
		Capacitive Loading Specs on Output Pins				
D100	COSC2	OSC2 Pin	—	20	pF	In HS mode when external clock is used to drive OSC1
D101	C_{IO}	All I/O Pins and OSC2	—	50	pF	To meet the AC Timing Specifications
D102	C_B	SCLx, SDAx	—	400	pF	I^2C Specification

Note 1: Negative current is defined as current sourced by the pin.

30. Module: 12-Bit A/D Converter with Threshold Scan

The title for the following registers should be read as follows:

- *Register 22-1: ANCON1: Analog Select Control Register 1 (for **ANSEL7-ANSEL0**)*
- *Register 22-2: ANCON2: Analog Select Control Register 2 (for **ANSEL15-ANSEL8**)*
- *Register 22-3: ANCON3: Analog Select Control Register 3 (for **ANSEL23-ANSEL16**)*

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (11/2012)

Initial release.

Rev B Document (5/2013)

Data Sheet Clarifications: Added Modules 11 through 15; Other minor corrections.

Rev C Document (9/2014)

Updated Table 2; Updated Module 1 (96 MHz PLL); Added Module 3 (Timer1/3/5); Other minor corrections.

Data Sheet Clarifications: Updated Modules 2, 5, and 9 (Analog-to-Digital Converter) and 11 (I/O Ports); Added Modules 16 (Oscillator), 17 (Oscillator), 18 (Analog-to-Digital Converter), 19 (PPS), 20 (I/O Ports), 21 (I/O Ports), 22 (I/O Ports), 23 (Comparator), 24 (Interrupts), 25 (Configuration Word), 26 (Electrical Specifications), 27 (Analog-to-Digital Converter and 28 (I/O Ports).

Rev D Document (4/2015)

Added Module 4 (I/O Ports).

Rev E Document (8/2015)

Data Sheet Clarifications: Added Modules 29 and 30.

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