100 MHz to 30 GHz, Silicon, SP4T Switch

Data Sheet

ADRF5044

FEATURES

- Ultrawideband frequency range: 100 MHz to 30 GHz
- Nonreflective 50 Ω design
- Low insertion loss: 2.6 dB at 20 GHz to 30 GHz
- High isolation: 43 dB at 20 GHz to 30 GHz
- High input linearity
  - P1dB: 28 dBm typical
  - IP3: 50 dBm typical
- High power handling
  - 24 dBm through path
  - 24 dBm terminated path
- No low frequency spurious
- 0.1 dB settling time (50% V_{CTL} to 0.1 dB of final RF output): 37 ns
- 24-terminal LGA package

APPLICATIONS

- Test instrumentation
- Microwave radios and very small aperture terminals (VSATs)
- Military radios, radars, and electronic counter measures (ECMs)
- Broadband telecommunications systems

FUNCTIONAL BLOCK DIAGRAM

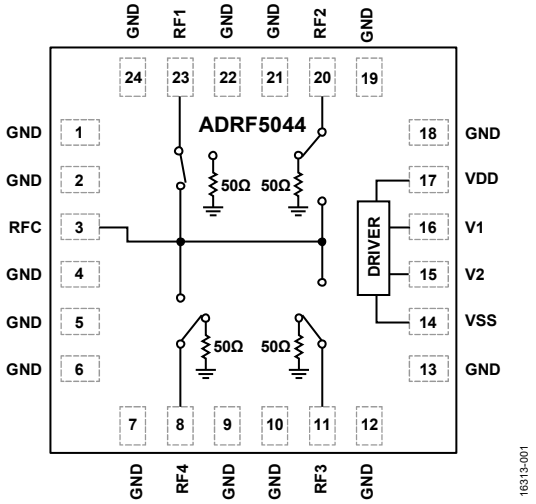


Figure 1.

GENERAL DESCRIPTION

The ADRF5044 is a general-purpose, single-pole, four-throw (SP4T) switch manufactured using a silicon process. It comes in a 24-terminal land grid array (LGA) package and provides high isolation and low insertion loss from 100 MHz to 30 GHz.

This broadband switch requires dual-supply voltages, +3.3 V and −3.3 V, and provides complementary metal-oxide semiconductor (CMOS)/low voltage transistor-transistor logic (LVTTL) logic-compatible control.

Rev. A

Document Feedback

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REVISION HISTORY

3/2020—Rev. 0 to Rev. A

Changes to Digital Control Inputs Parameter, Table 2 ... 5
Added Endnote 1, Table 2; Renumbered Sequentially ... 5
Changes to Theory of Operation Section ... 10

12/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V1 = 0 V or 3.3 V, V2 = 0 V or 3.3 V, and T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			100		30,000	MHz
INSERTION LOSS						
Between RFC and RF1 to RF4 (On) (Worst Case)		100 MHz to 10 GHz		1.7		dB
		10 GHz to 20 GHz		2.1		dB
		20 GHz to 30 GHz		2.6		dB
ISOLATION						
Between RFC and RF1 to RF4 (Off) (Worst Case)		100 MHz to 10 GHz		55		dB
		10 GHz to 20 GHz		52		dB
		20 GHz to 30 GHz		43		dB
RETURN LOSS						
RFC and RF1 to RF4 (On)		100 MHz to 10 GHz		16		dB
		10 GHz to 20 GHz		22		dB
		20 GHz to 30 GHz		22		dB
RF1 to RF4 (Off)		100 MHz to 10 GHz		24		dB
		10 GHz to 20 GHz		24		dB
		20 GHz to 30 GHz		16		dB
SWITCHING TIME						
Rise and Fall	t_{RISE}, t_{FALL}	10% to 90% of radio frequency (RF) output		4		ns
On and Off	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		19		ns
Settling						
0.1 dB		50% V_{CTL} to 0.1 dB of final RF output		37		ns
0.05 dB		50% V_{CTL} to 0.05 dB of final RF output		50		ns
INPUT LINEARITY						
Power Compression						
0.1 dB	P0.1dB			26		dBm
1 dB	P1dB			28		dBm
Third-Order Intercept	IP3	Two-tone input power = 14 dBm each tone, Δf = 1 MHz		50		dBm
SUPPLY CURRENT		VDD, VSS pins				
Positive	I_{DD}	Typical at V_{CTL} = 0 V or 3.3 V, maximum at V_{CTL} = 0.8 V or 1.4 V		12	20	µA
Negative	I_{SS}	Typical at V_{CTL} = 0 V or 3.3 V, maximum at V_{CTL} = 0.8 V or 1.4 V		110	130	µA
DIGITAL CONTROL INPUTS		V1, V2 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTL}		0		V_{DD}	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RFx Input Power	P_{IN}	T_{CASE} = 85°C				
Through Path		RF signal is applied to RFC or through connected RF1/RF2			24	dBm
Terminated Path		RF signal is applied to terminated RF1/RF2			24	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			21	dBm
Case Temperature	T_{CASE}		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Supply Voltage	
Positive	−0.3 V to +3.6 V
Negative	−3.6 V to +0.3 V
Digital Control Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 3.3 mA, whichever occurs first
RFx Input Power[2] (f = 400 MHz to 30 GHz, T_{CASE} = 85°C)	
Through Path	25 dBm
Terminated Path	25 dBm
Hot Switching	22 dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow (Moisture Sensitivity Level 3 (MSL3) Rating)	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	
RFC and RF1 to RF4 Pins	375 V
Other Pins	2000 V

[1] Overvoltages at digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.
[2] For power derating less than 400 MHz, see Figure 2 and Figure 3.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-24-4		
Through Path	400	°C/W
Terminated Path	160	°C/W

POWER DERATING CURVES

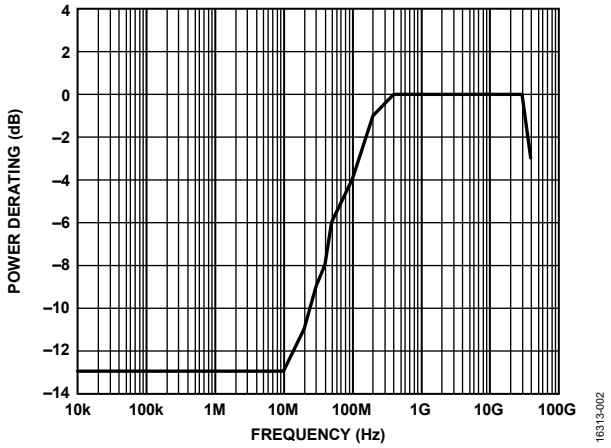


Figure 2. Power Derating for Through Path and Hot Switching vs. Frequency, T_{CASE} = 85°C

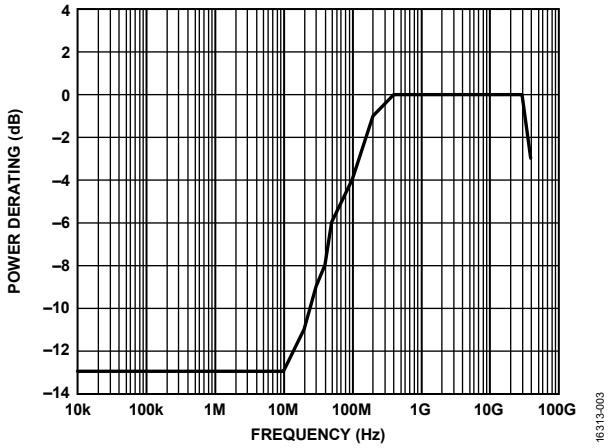


Figure 3. Power Derating for Terminated Path vs. Frequency, T_{CASE} = 85°C

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

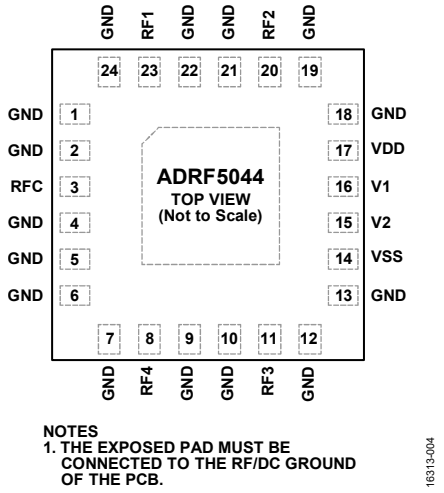


Figure 4. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 9, 10, 12, 13, 18, 19, 21, 22, 24	GND	Ground. These pins must be connected to the RF/dc ground of the PCB.
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
8	RF4	RF4 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
11	RF3	RF3 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
14	VSS	Negative Supply Voltage.
15	V2	Control Input 2. See Table 5 for the control voltage truth table.
16	V1	Control Input 1. See Table 5 for the control voltage truth table.
17	VDD	Positive Supply Voltage.
20	RF2	RF2 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
23	RF1	RF1 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

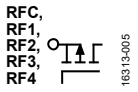


Figure 5. RFx Pins (RFC and RF1 to RF4) Interface Schematic

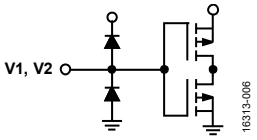


Figure 6. Digital Pins (V1 and V2) Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

Insertion loss and return loss measured on the probe matrix board using ground signal ground (GSG) probes close to the RFx pins; isolation measured on the evaluation board because signal coupling between the probes limits the isolation performance of the ADRF5044 on the probe matrix board.

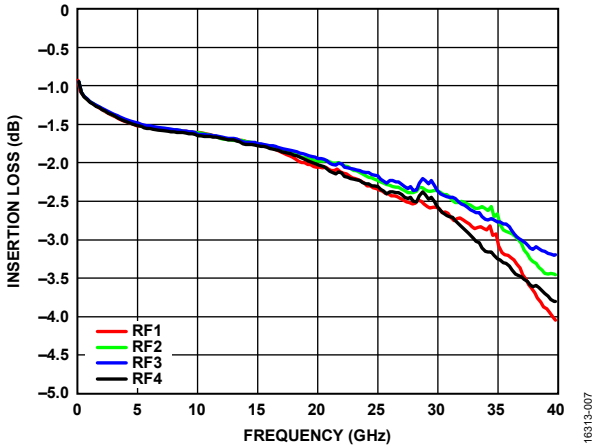


Figure 7. Insertion Loss vs. Frequency for RF1, RF2, RF3, and RF4

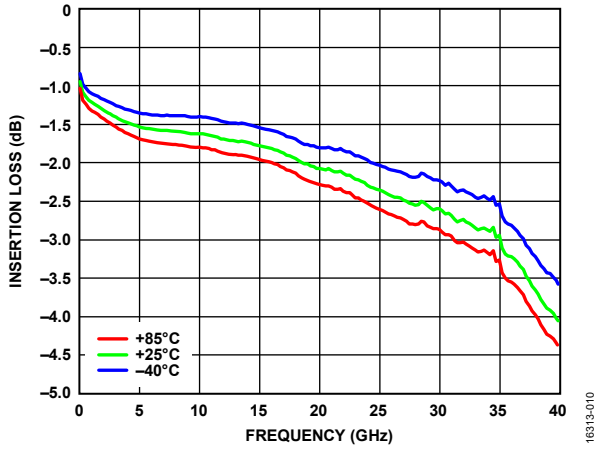


Figure 10. Insertion Loss vs. Frequency over Various Temperatures Between RFC and RF1

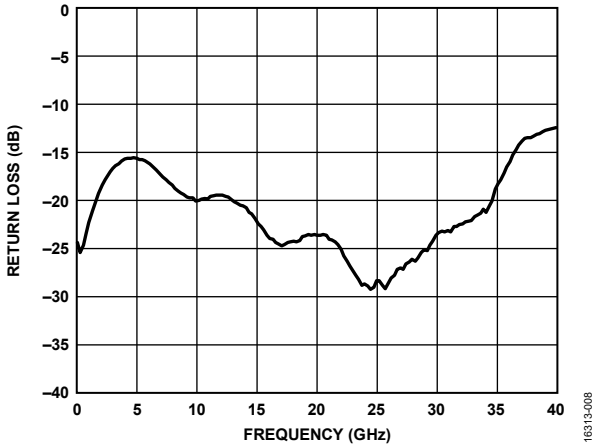


Figure 8. Return Loss vs. Frequency for RFC

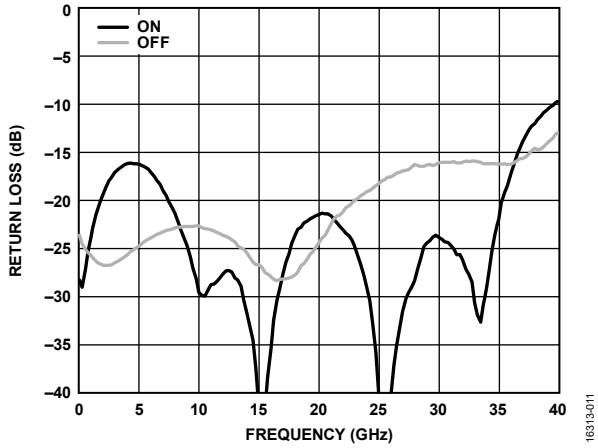


Figure 11. Return Loss vs. Frequency for RF1, RF2, RF3, and RF4

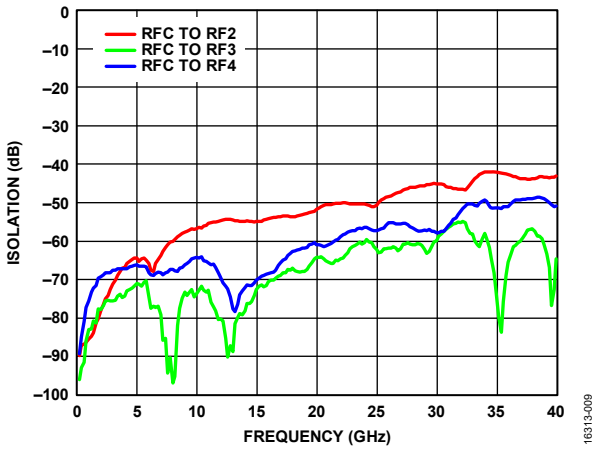


Figure 9. Isolation vs. Frequency, RFC to RF1 On

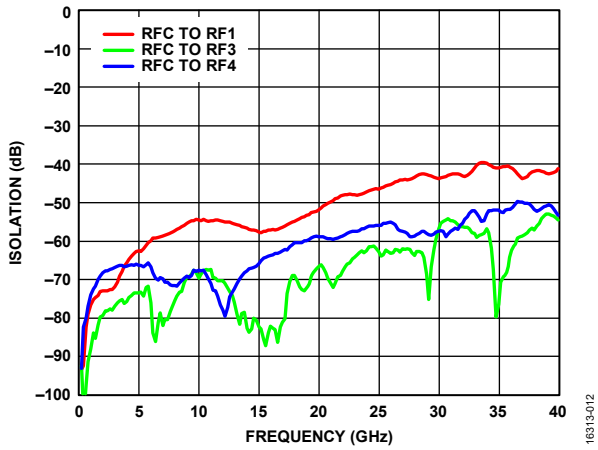


Figure 12. Isolation vs. Frequency, RFC to RF2 On

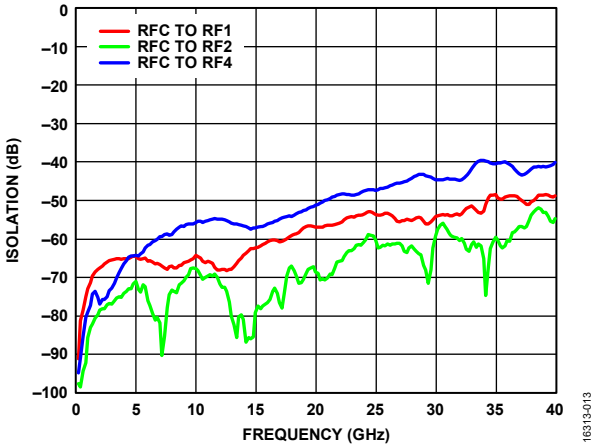


Figure 13. Isolation vs. Frequency, RFC to RF3 On

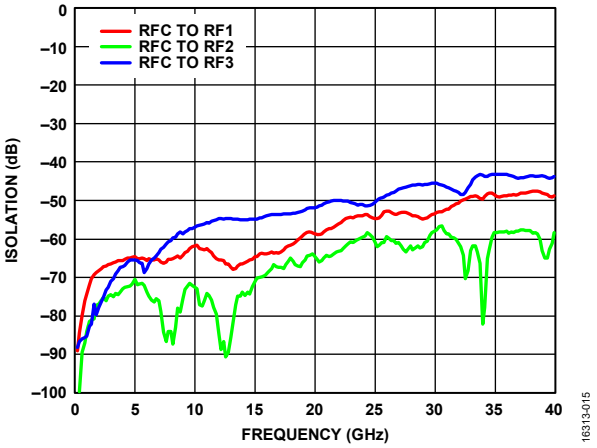


Figure 15. Isolation vs. Frequency, RFC to RF4 On

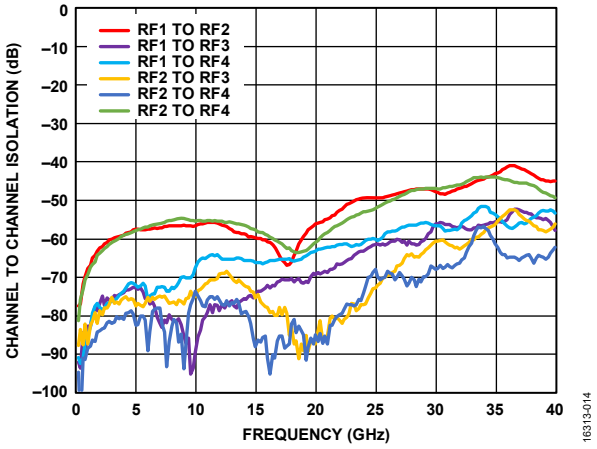


Figure 14. Channel to Channel Isolation vs. Frequency, RFC to RF1 On

INPUT 0.1 dB, 1 dB POWER COMPRESSION, AND THIRD-ORDER INTERCEPT

All large signal performance parameters were measured on the evaluation board.

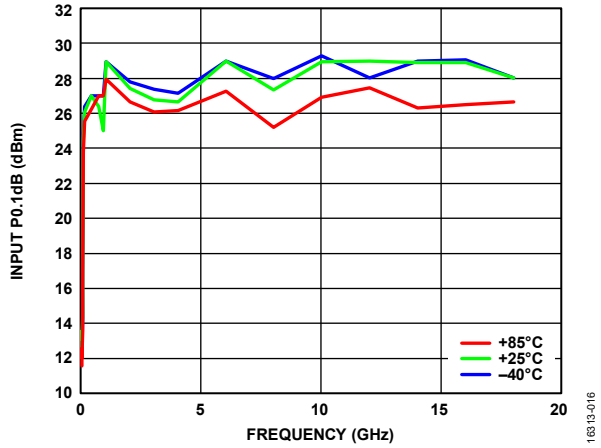


Figure 16. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency over Various Temperatures

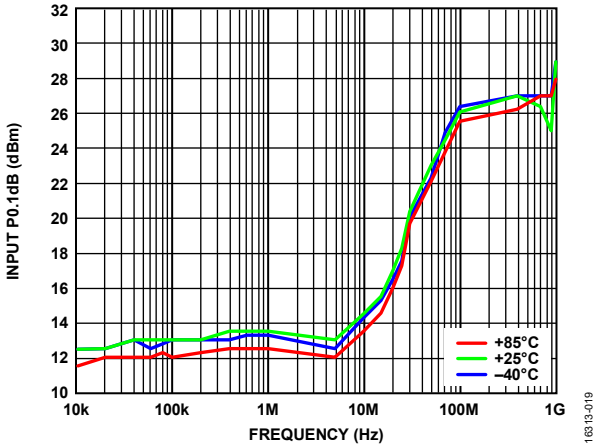


Figure 19. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency over Various Temperatures (Low Frequency Detail)

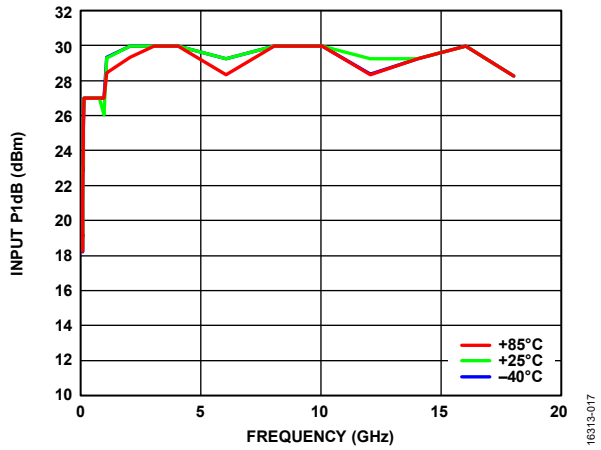


Figure 17. Input 1 dB Power Compression (P1dB) vs. Frequency over Various Temperatures

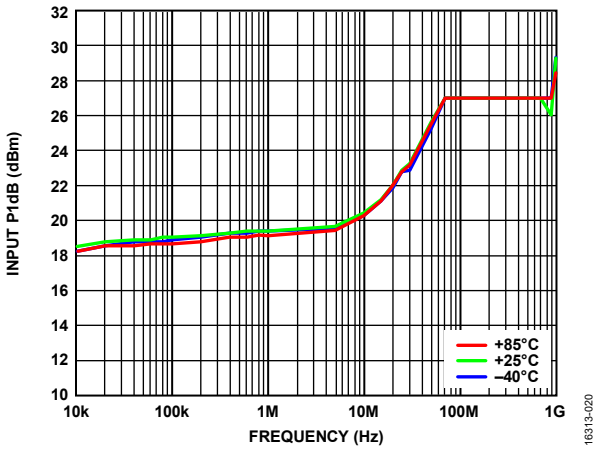


Figure 20. Input 1 dB Power Compression (P1dB) vs. Frequency over Various Temperatures (Low Frequency Detail)

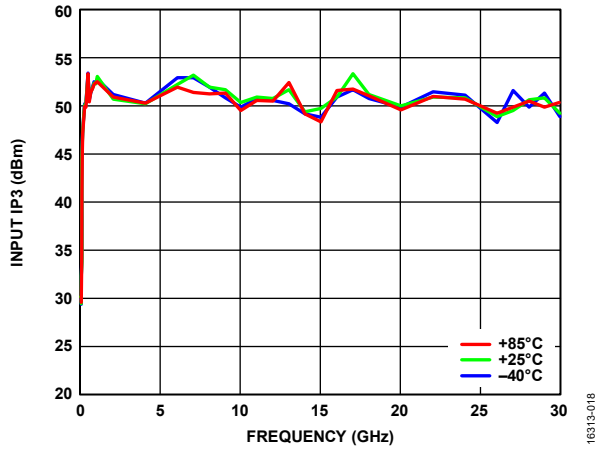


Figure 18. Input IP3 vs. Frequency over Various Temperatures

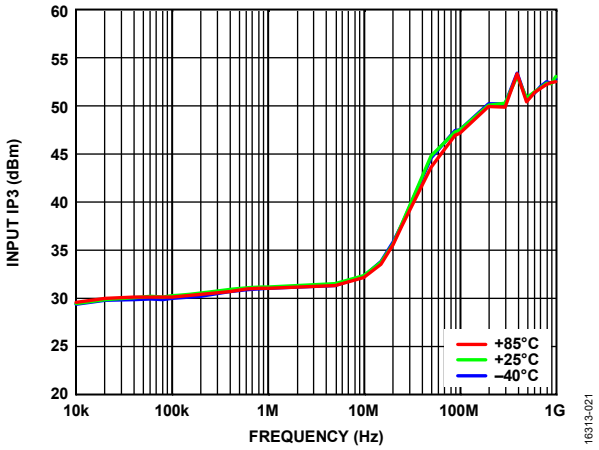


Figure 21. Input IP3 vs. Frequency over Various Temperatures (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5044 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ADRF5044 incorporates a driver to perform logic functions internally and to provide the user with the advantage of a simplified control interface. The driver features two digital control input pins (V1 and V2) that control the state of the RF paths. Depending on the logic level applied to the V1 and V2 pins, one RF path is in an insertion loss state, while the other three paths are in an isolation state (see Table 5). The insertion loss path conducts the RF signal equally well in both directions between the RF throw port and the RF common port, and the isolation paths provides high loss between the RF throw ports terminated to internal 50 Ω resistors and the insertion loss path.

The ideal power-up sequence for the ADRF5044 is as follows:

1. Connect GND.
2. Power up VDD and VSS. Powering up VSS after VDD avoids current transients on VDD during ramp-up.
3. Apply digital control inputs, V1 and V2. Applying the digital control inputs before the VDD supply may inadvertently forward bias and damage the internal ESD protection structures. In this case, use a series 1 kΩ resistor to limit the current flowing in to the control pin. If the control pins are not driven to a valid logic state (for example, if the controller output is in a high impedance state) after VDD is powered up, it is recommended to use pull-up and pull-down resistors.
4. Apply an RF input signal. The design is bidirectional. The RF input signal can be applied to the RFC port, while the RF throw ports are outputs, or vice versa. The RF ports are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 5. Control Voltage Truth Table

Digital Control Input		RF Paths			
V1	**V2**	**RF1 to RFC**	**RF2 to RFC**	**RF3 to RFC**	**RF4 to RFC**
Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

EVALUATION BOARD

Figure 22 shows the top view of the ADRF5044-EVALZ, and Figure 23 shows the cross sectional view of the ADRF5044-EVALZ.

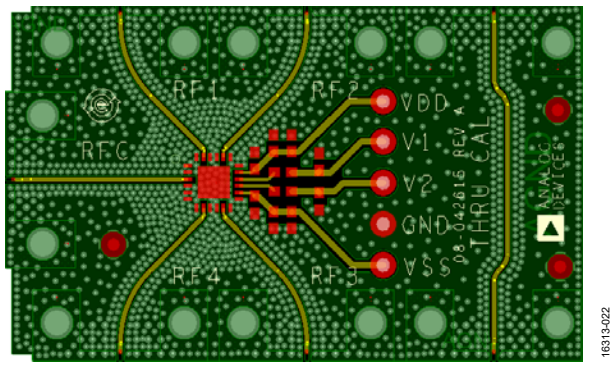


Figure 22. Evaluation Board Layout, Top View

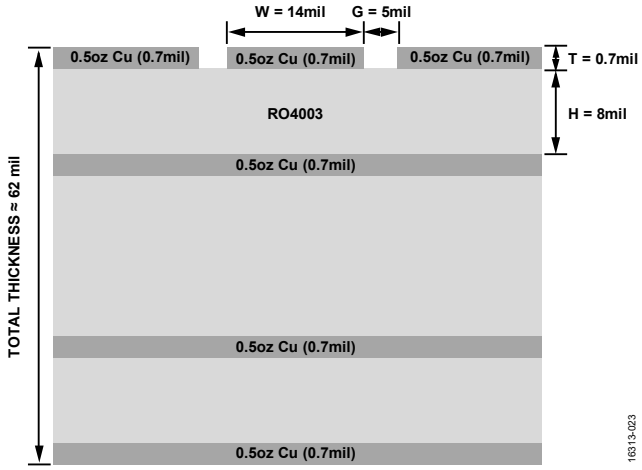


Figure 23. Evaluation Board (Cross Sectional View)

The ADRF5044-EVALZ is a 4-layer evaluation board. Each copper layer is 0.7 mil (0.5 oz) and separated by dielectric materials. All RF and dc traces are routed on the top copper layer, and the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, which allows 2.4 mm RF launchers to be connected at the board edges.

The RF transmission lines were designed using a coplanar waveguide (CPWG) model, with a trace width of 14 mil and a ground clearance of 5 mil, to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many plated through vias as possible are arranged around the transmission lines and under the exposed pad of the package.

Figure 24 shows the actual ADRF5044 evaluation board with component placement. Two power supply ports are connected to the VDD and VSS test points (TP1 and TP4), control voltages are connected to the V1 and V2 test points (TP2 and TP3), and the ground reference is connected to the GND test point (TP5).

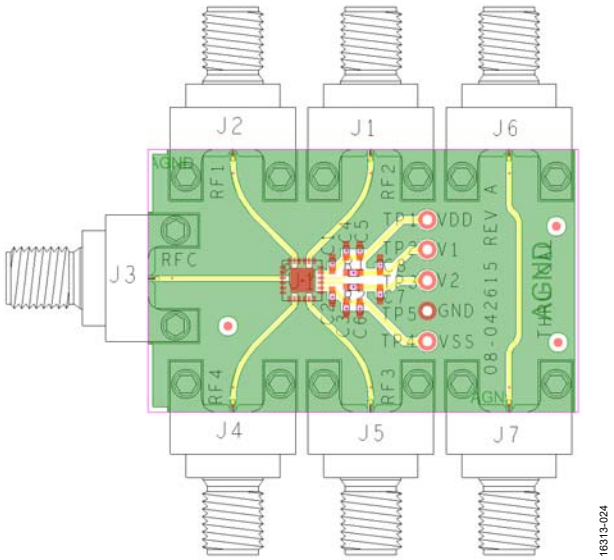


Figure 24. Evaluation Board Component Placement

On the control traces, V1 and V2, a 0 Ω resistor connects the test points to the pins on the ADRF5044. On the supply traces, VDD and VSS, a 100 pF bypass capacitor filters the high frequency noise. Additionally, unpopulated components positions are available for applying extra bypass capacitors.

The RF input and output ports (RFC, RF1, RF2, RF3, and RF4) are connected through 50 Ω transmission lines to the 2.4 mm RF launchers (J1 to J5). These high frequency RF launchers are by contact and not soldered onto the board. A thru calibration line connects the unpopulated J6 and J7 launchers; this transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

The schematic of the ADRF5044-EVALZ is shown in Figure 25.

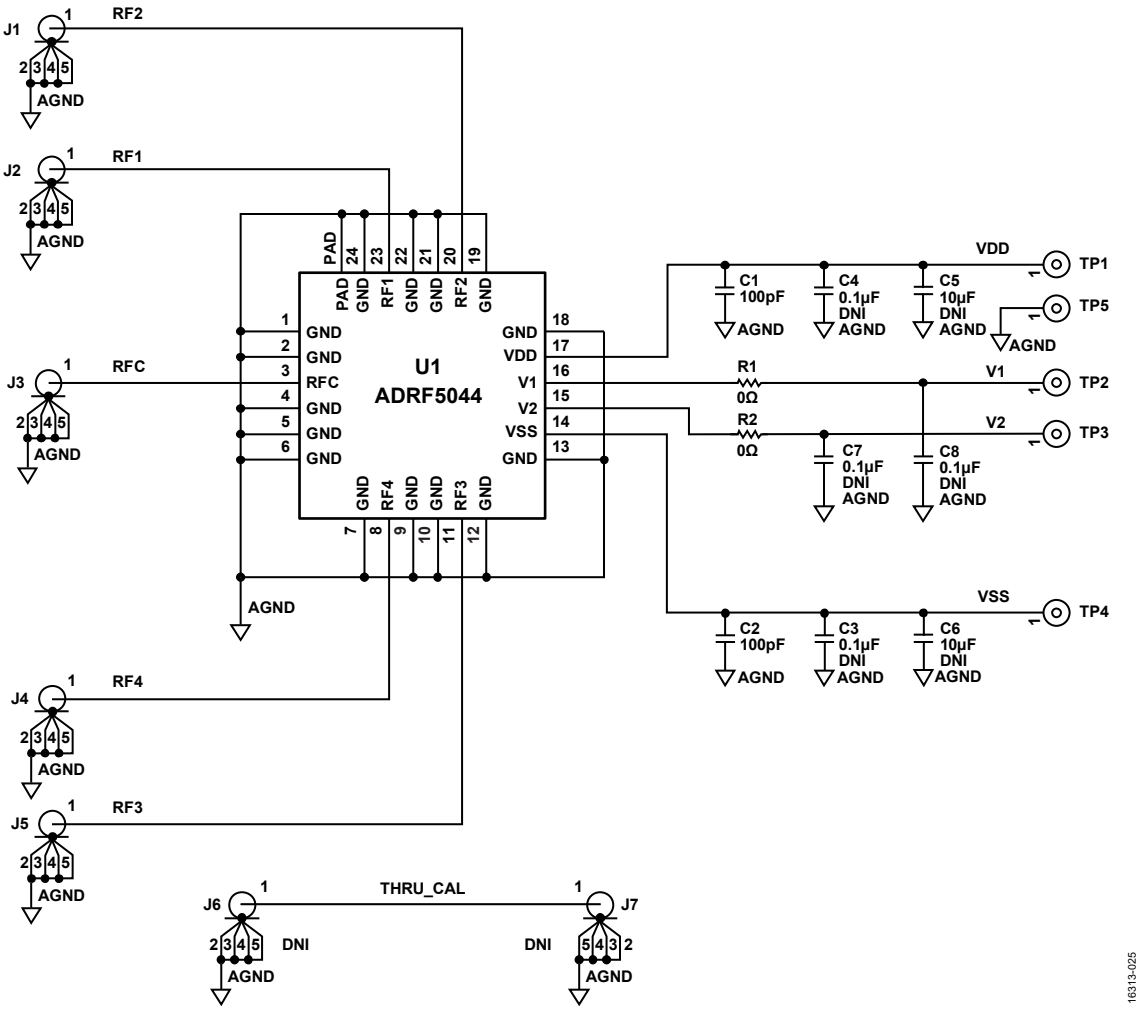


Figure 25. ADRF5044-EVALZ Schematic

Table 6. Evaluation Board Components

Component	Default Value	Description
C1, C2	100 pF	Capacitors, C0402 package
C5, C6	10 µF	Capacitors C3216 package, do not install (DNI)
C3, C4, C7, C8	0.1 µF	Capacitors, C0402 package, DNI
J1 to J7	Not applicable	2.4 mm end launch connector (Southwest Microwave: 1492-04A-5)
R1, R2	0 Ω	Resistors, 0402 package
TP1 to TP5	Not applicable	Through-hole mount test point
U1	ADRF5044	ADRF5044 digital attenuator, Analog Devices, Inc.
PCB	08-042615-01	Evaluation PCB, Analog Devices

PROBE MATRIX BOARD

The probe matrix board is a 4-layer board that uses a 12 mil Rogers RO4003 as the top dielectric material. The external copper layer is 0.7 mil, and the internal copper layers are 1.4 mil. The RF transmission lines were designed using a CPWG model, with a 16 mil width and a ground spacing of 6 mil, to have a characteristic impedance of 50 Ω.

Figure 26 shows the cross sectional view of the probe matrix board, and Figure 27 shows the top view of the probe matrix board. Measurements were made using 535 µm GSG probes at close proximity to the RFx pins. Unlike the ADRF5044-EVALZ, probing reduces reflections caused by mismatch arising from connectors, cables, and board layout, resulting in a more accurate measurement of the performance of the ADRF5044.

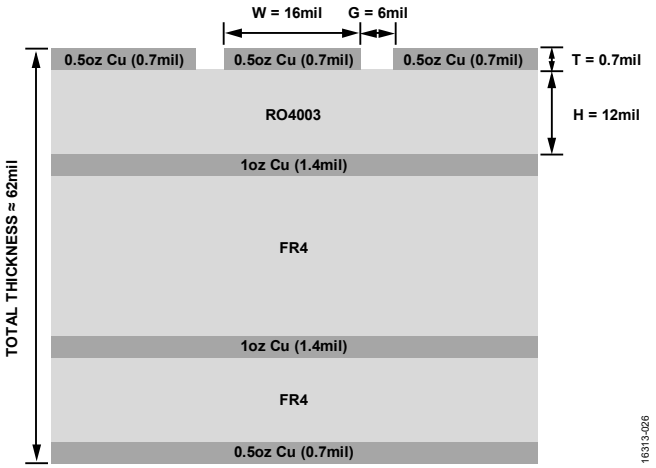


Figure 26. Probe Matrix Board (Cross Sectional View)

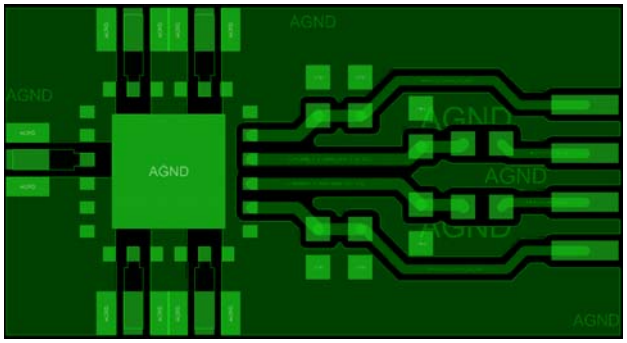


Figure 27. Probe Board Layout (Top View)

RF traces for a through reflect line (TRL) calibration are designed on the board itself. A nonzero line length compensates for board loss at calibration. The actual board duplicates the same layout in matrix form to assemble multiple devices at once. Insertion loss and input and output return losses were measured on this probe matrix board. Isolation performance measured on the probe matrix board is limited due to signal coupling between the RF probes that are in close proximity. Therefore, RF port to port isolation was measured on the ADRF5044-EVALZ.

OUTLINE DIMENSIONS

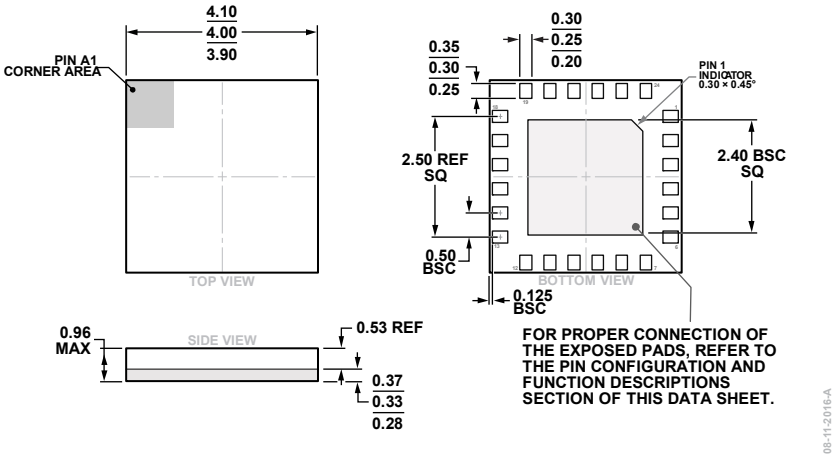


Figure 28. 24-Terminal Land Grid Array [LGA]
(CC-24-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF5044BCCZN	−40°C to +85°C	24-Terminal Land Grid Array [LGA]	CC-24-4
ADRF5044BCCZN-R7	−40°C to +85°C	24-Terminal Land Grid Array [LGA]	CC-24-4
ADRF5044-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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