ML52*x* User Guide

Virtex-5 FPGA RocketIO Characterization Platform

UG225 (v2.1) August 4, 2010

XILINX®

0402527-03

Xilinx is disclosing this user guide, manual, release note, and/or specification (the “Documentation”) to you solely for use in the development of designs to operate with Xilinx hardware devices. You may not reproduce, distribute, republish, download, display, post, or transmit the Documentation in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx. Xilinx expressly disclaims any liability arising out of your use of the Documentation. Xilinx reserves the right, at its sole discretion, to change the Documentation without notice at any time. Xilinx assumes no obligation to correct any errors contained in the Documentation, or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information.

THE DOCUMENTATION IS DISCLOSED TO YOU “AS-IS” WITH NO WARRANTY OF ANY KIND. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE DOCUMENTATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS. IN NO EVENT WILL XILINX BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOSS OF DATA OR LOST PROFITS, ARISING FROM YOUR USE OF THE DOCUMENTATION.

© 2007–2010 Xilinx, Inc. All rights reserved.

XILINX, the Xilinx logo, the Brand Window, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/02/07	1.0	Initial Xilinx release.
08/06/07	1.1	Removed *UG091, Xilinx Generic Interface (XGI) SuperClock Module User Guide* from“Package Contents.” Removed “Power Bus and Switches” diagram from Figure 1. Added Power Supply Block Diagram, Figure 3. Updated Micron part number in “18. DDR2 Memory,” page 21. Corrected DDR to DDR2 throughout. Updated ML521 connections for A11 and A12 in Table 15. Corrected CK0N and CK0P pin numbers in Table 15.
04/17/08	2.0	Added GTX transceiver and FXT device information. Updated VCCINT for ML525 in Table 2. Modified the power brick connection in Figure 3 for consistency and accuracy. Added Voltage Adjust Potentiometer column in Table 3. Added Platform Cable USB to “3. FPGA Configuration.” Corrected ML521 pins in Table 9. Updated Infineon and Micron part numbers in “18. DDR2 Memory.” Corrected numerous pins in Table 15. Corrected CTS and RXD pins in Table 18. Corrected the RS232 and DB9 reference designators in Figure 4. Corrected J113 and J135 column headings in Table 19. Renumbered XGI pins in columns E and F and corrected XGI pin F27 description in Table 20. Renumbered XGI pins in columns A and B in Table 22. Several updates to Table 23.
08/04/10	2.1	Section “Features,” page 10: Corrected the number of pairs of transceiver SMA connectors from “32 to 96” to “16 to 48.” Figure 1, page 11, corrected the number of transceivers/SMAs in FF665 from 12/48 to 8/32, and the number of clocks/SMAs in FF665 from 6/12 to 4/8. Section “19. GTP/GTX Transceiver Clock Input SMAs,” page 25, removed material from introductory paragraph describing the lack of AC coupling. Table 22, page 33, corrected ML523 pin for signal XGI_SE_30 from AH32 to AH34.

Table of Contents

Preface: About This Guide

Additional Documentation 5
Additional Support Resources 6
Typographical Conventions 7
Online Document 7

ML52*x* User Guide

Package Contents 9
Additional Information 9
Related Documents 10
Introduction 10
Features 10
Detailed Description 12
1. Power Switch 13
2. Power Regulation 13
3. FPGA Configuration 15
4. Program Switch (Active-Low) 15
5. DONE LED 15
6. INIT LED 15
7. System ACE Controller 16
8. Reset Switch (Active-Low) 16
9. Configuration Address DIP Switch 16
10. JTAG Isolation Jumpers 16
11. System ACE MPU Port 17
12. Oscillator Sockets 18
13. Single-Ended SMA Clock Inputs 18
14. Differential SMA Global Clock Inputs 18
15. User LEDs (Active-High) 19
16. User DIP Switches (Active-High) 20
17. User Pushbutton Switches (Active-High) 20
18. DDR2 Memory 21
19. GTP/GTX Transceiver Clock Input SMAs 25
20. GTP/GTX Transceiver Pins 26
21. RS-232 Port Pins 29
22. Xilinx Generic Interface (XGI) 29
References 35

About This Guide

This user guide describes the features and operation of the Virtex®-5 FPGA ML52x series of RocketIO™ characterization platforms.

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.

- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.

- Virtex-5 FPGA User Guide

  Chapters in this guide cover the following topics:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources

- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

  This guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT and SXT platforms.

- Virtex-5 FPGA RocketIO GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 FXT platform.

- Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, and FXT platforms.

- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, and FXT platforms used for PCI Express® designs.

- XtremeDSP Design Considerations

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E slice.

- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.

- Virtex-5 FPGA Packaging and Pinout Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

- Virtex-5 FPGA PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the Virtex-5 *FPGA Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

This document uses the following conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Support Resources" for details. Refer to "DMA Operation" in Chapter 13 for details.
Red text	Cross-reference link to a location in another document	See Figure 2 in the *Virtex-5 FPGA Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

ML52x User Guide

Package Contents

- ML52x RocketIO characterization platform (referred to as the ML52x platform)
- UG225, *ML52x User Guide: Virtex-5 RocketIO Characterization Platform*
- SMA-to-SMA cable assemblies:
  - Four 24-inch cable assemblies
  - Two 12-inch cable assemblies
- System ACE™ CompactFlash memory card
- SuperClock module
- Power supply module
- Power supply brick
- SMA wrench

Additional Information

For current information about the ML52x RocketIO characterization platform, visit www.xilinx.com/ml52x

The information includes:

- Current version of this user guide in PDF format
- Example design files for demonstration of Virtex-5 FPGA features and technology
- Demonstration hardware and software configuration files for the System ACE controller
- MicroBlaze™ EDK reference design files (Board Support Builder)
- Full schematics in PDF format and ViewDraw schematic format
- PC board layout in Allegro PCB format
- Gerber files for the PC board (Many free or shareware Gerber file viewers are available on the Internet for viewing and printing these files)
- Additional documentation, errata, frequently asked questions, and the latest news
- Contents of the CompactFlash card provided with the ML52x platform

Related Documents

Prior to using the ML52x platforms, users should be familiar with Xilinx resources. See "References," page 35 for direct links to Xilinx and other related documentation. See the following locations for additional documentation on Xilinx tools and solutions.

- EDK: www.xilinx.com/edk
- ISE® Design Tools: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Virtex-5 FPGAs: www.xilinx.com/virtex5
- ChipScope™ Pro: www.xilinx.com/chipscope

Introduction

The ML52x RocketIO transceiver characterization platform allows designers to investigate and experiment with the features of the RocketIO transceivers (the *transceivers*). This document describes the features and operation of the boards.

> ***Caution!*** To protect the ML52x platform from damage caused by electrostatic discharge (ESD), follow standard ESD prevention measures when handling the board.

The platforms and their corresponding packages are shown in Table 1.

Table 1: **Platforms and Packages**

Platform	Device		Package
	LXT	FXT	
ML521	XC5VLX50T	XC5VFX70T	FF665
ML523	XC5VLX110T	XC5VFX100T	FF1136
ML525	XC5VLX330T	XC5VFX200T	FF1738

Features

- Virtex-5 FPGA (referred to as the device under test, or DUT, in this user guide)
- Onboard power supplies for all necessary voltages
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Parallel Cable III and Parallel Cable IV cables
- System ACE controller with 8-bit MPU port support
- Power supply module supporting all transceiver power requirements
- Two 2.5V / 3.3V global clock oscillator sockets
- Two single-ended global clock inputs with SMA connectors
- Two pairs of differential global clock inputs with SMA connectors
- SuperClock module supporting multiple frequencies
- Xilinx Generic Interface (XGI)
- 16 to 48 pairs of SMA connectors for the RocketIO transceivers
- 4 to 12 pairs of SMA connectors for RocketIO transceiver clock inputs
- Power indicator LEDs

- General purpose DIP switches, LEDs, and pushbutton switches
- 32 MB - 128 MB of DDR2 Memory

Figure 1 shows the block diagram of the board.

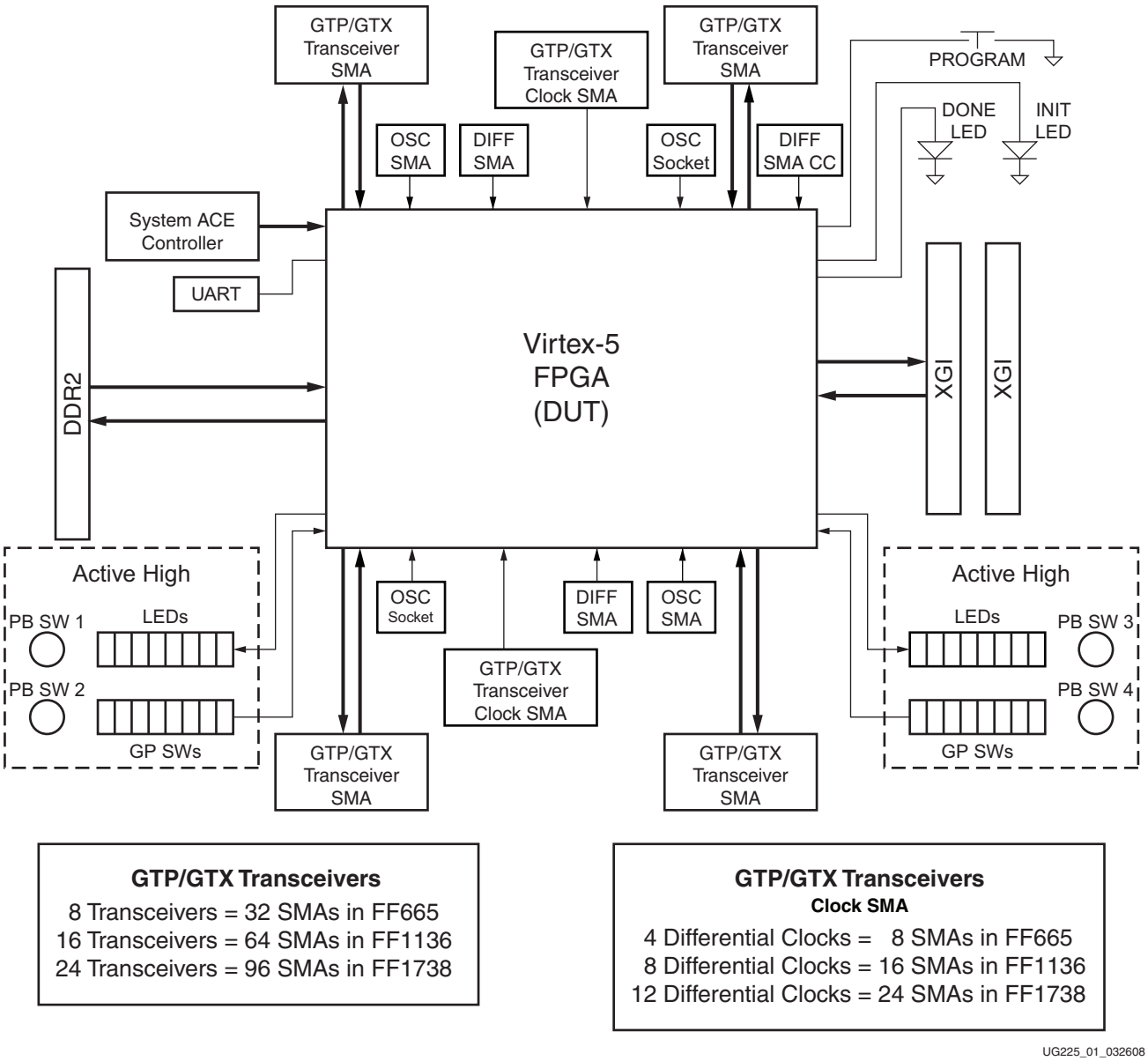
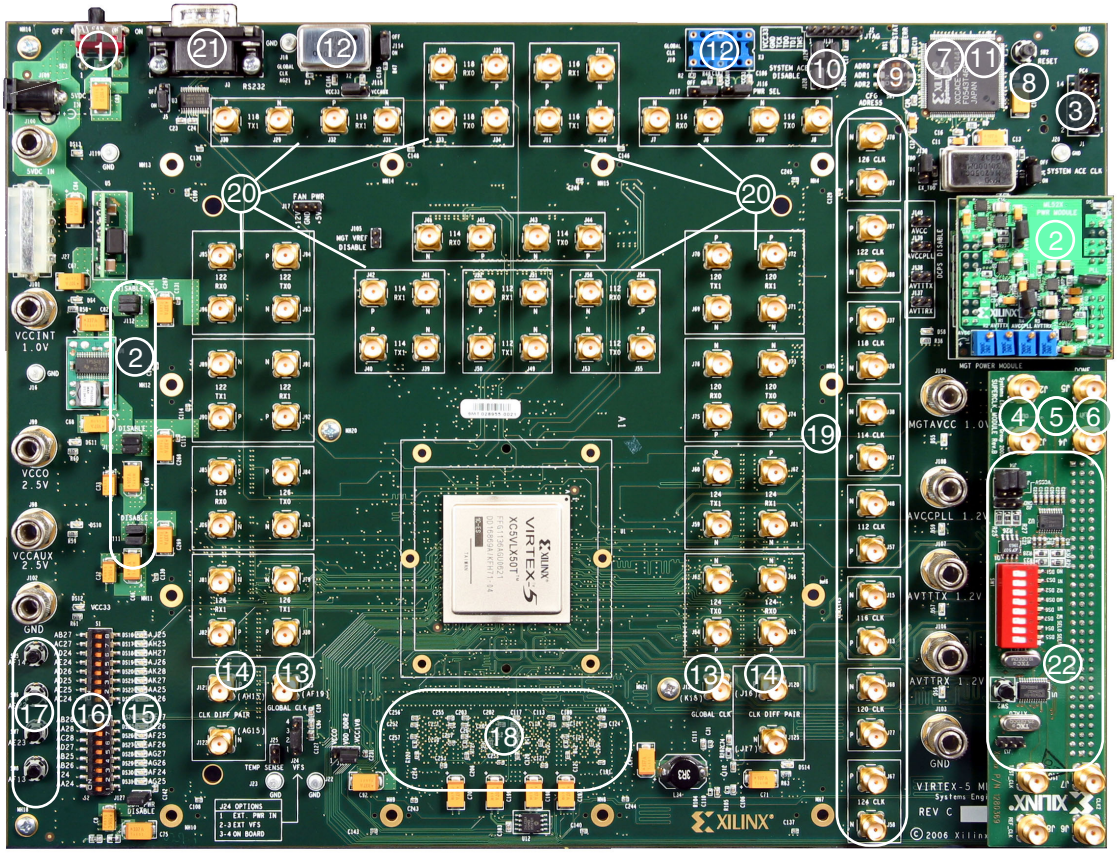


Figure 1: **Virtex-5 FPGA ML52x Platform Block Diagram**

Detailed Description

The ML52*x* platform shown in Figure 2 represents the ML52*x* series described in this user guide. Each feature is detailed in the numbered sections that follow.

Note: The image might not reflect the current revision of the board.



UG225_02_100206

Figure 2: **Detailed Description of Virtex-5 FPGA ML52x Platform Components**

1. Power Switch

The board has onboard power supplies controlled by the power switch. When the V5 LED is lit, this indicates the board is powered.

On Position

In the ON position, the power switch enables delivery of all power on the board by way of voltage regulators situated close to the left side of the board and the MGT power module situated close to the right side of the board. These regulators feed off the 5V external power brick or the 5V power supply jack.

The 5V power brick is capable of providing a maximum of 6.5A. For designs that require greater than 6.5A, an ATX power supply can be connected to the J27 hard drive power connector.

Note: 5V must always be supplied to the board to enable the 3.3V regulator for the System ACE controller chip. It is always recommended to check the power supply voltage values before testing your design or taking measurements.

Off Position

In the OFF position, the power switch disables all modes of power on the board.

2. Power Regulation

Main Board Regulation

The ML52x platform has onboard regulation for the DUT main power supplies listed in Table 2. These regulators also have a corresponding input voltage jack to supply each voltage independently from the bench-top power supply (see Figure 3, page 14). This is done by removing the power supply enable jumpers for the headers that correspond to each supply voltage listed in Table 2.

Note:

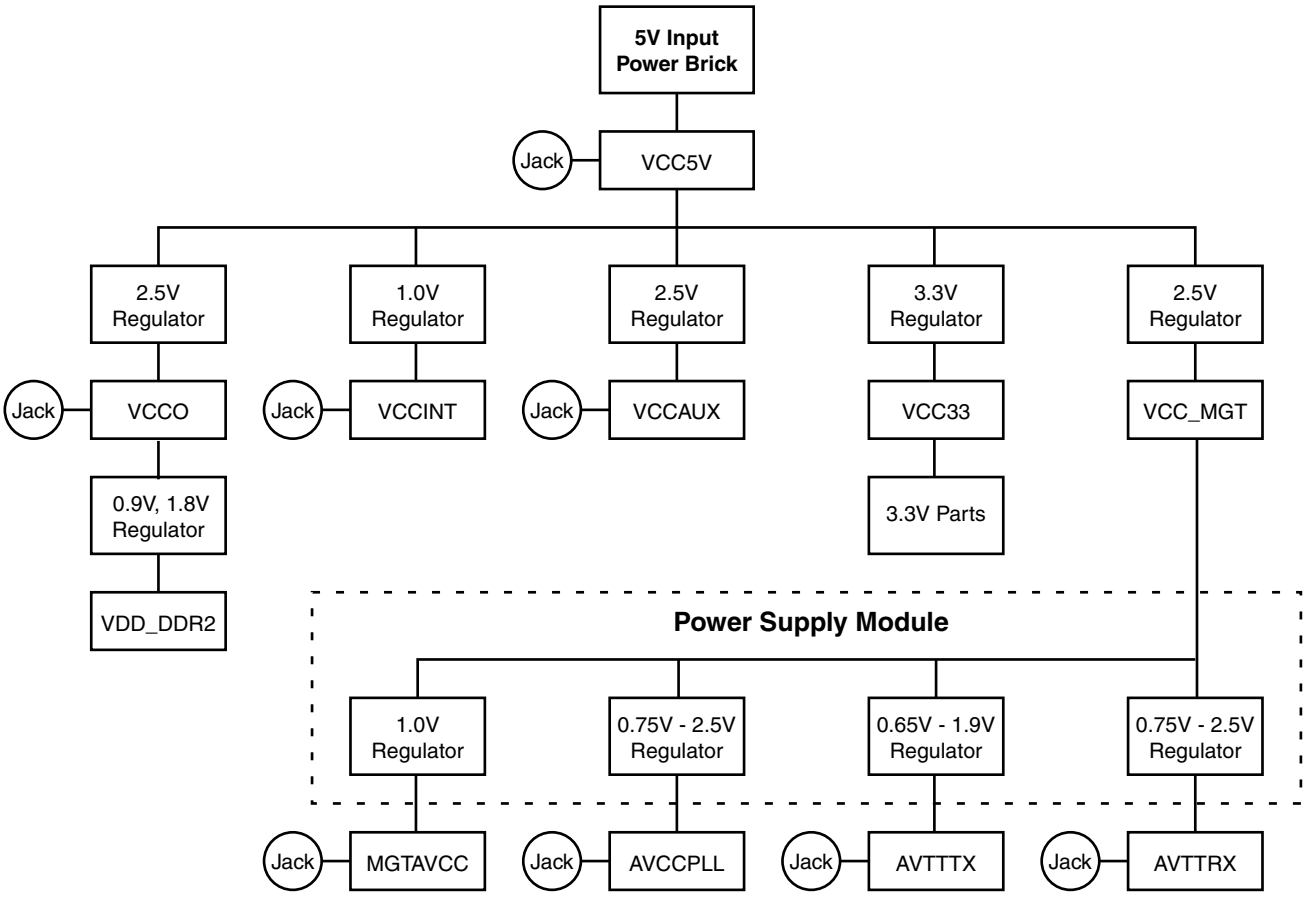
- If your design exceeds the maximum current rating for any of the onboard regulators for any given rail, that rail must be supplied by the external power jack.
- The power enable jumper must be removed before supplying an external supply on its corresponding supply jack.

Table 2: **Onboard Regulation: Voltage, Current, Jacks, and Jumpers**

Power Supply Name	Max Current Rating	Typical Voltage	Jack/ Connector	Enable Jumper	Description
5V	N/A	5V	J27 J109 J100	N/A	Main input voltage for the ML52x boards supplied through the jack, barrel connector or Molex connector.
VCC33	3.0A	3.3V	N/A	N/A	Supplies 3.3V of the System ACE chip and other onboard circuits.
VCCINT	7.0A / 30.0A	1.0V	J101	J112	Core voltage for the FPGA (DUT). Max current rating: • ML521 and ML523 boards rated at 7A • ML525 board rated at 30A

Table 2: **Onboard Regulation: Voltage, Current, Jacks, and Jumpers *(Cont'd)***

Power Supply Name	Max Current Rating	Typical Voltage	Jack/ Connector	Enable Jumper	Description
VCCO	6.0A	2.5V	J99	J19/J110	I/O voltage for the FPGA (DUT).
VCCAUX	3.0A	2.5V	J98	J111	Auxiliary voltage for the FPGA (DUT).
GND	N/A	N/A	J102/J103	N/A	Ground connection for all circuits.



NOTE:
The GTP/GTX transceiver power supply names might have the prefix *MGT* in other Xilinx documentation. Names with and without the MGT prefix are synonymous to each other.

UG225_03_100207

Figure 3: **Power Supply Block Diagram**

Power Supply Module

The power supply module supplies all voltages shown in Table 3, page 15 to the DUT RocketIO transceivers. This module plugs in on the right side of the board on header J134, J133, and J26 of the ML52x platform.

The onboard regulators also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply. This is done by installing the power supply disable jumpers for the headers that correspond to each supply voltage

listed in Table 3. The power supply disable jumper must be installed before supplying an external supply on its corresponding supply jack.

Table 3: **Power Supply Module Jumpers**

GTP/GTX Power Supply Name(1)	Max Current Rating	Typical Voltage		Voltage Adj. Pot.	Jack	Disable Jumper	Description
		LXT	FXT				
MGTAVCC	3.0A	1.0V	1.0V	R2	J104	J5	Powers all transceiver analog circuits.
AVCCPLL	1.5A	1.2V	1.0V	R4	J108	J7	Powers all transceiver PLL and clock network.
AVTTTX	1.5A	1.2V	1.2V	R1	J107	J4	Termination voltage for transceiver transmitter.
AVTTRX	1.5A	1.2V	1.2V	R3	J106	J6	Termination voltage for transceiver receiver.

Notes:

1. The GTP/GTX transceiver power supply names might have the prefix *MGT* in other Xilinx documentation. Names with and without the MGT prefix are synonymous to each other.

3. FPGA Configuration

The FPGA can only be configured in JTAG mode using one of the following options:

- Parallel Cable III cable
- Parallel Cable IV cable
- Platform Cable USB
- System ACE controller

For detailed information, see *System ACE CompactFlash Solution* [Ref 1].

Using the configuration address DIP switches, one of eight bitstreams stored in the CompactFlash memory card can be accessed through the on-board System ACE controller.

Note: The System ACE controller is bypassed when the flying wire leads or the Parallel Cable IV cable is used, thus causing no disruption in the JTAG chain.

4. Program Switch (Active-Low)

The active-Low program switch, when pressed, grounds the program pin on of the FPGA.

5. DONE LED

The DONE LED indicates the status of the DONE pin of the FPGA. The LED lights when DONE is high, indicating the FPGA configured successfully.

6. INIT LED

The INIT LED lights during initialization.

7. System ACE Controller

An onboard System ACE controller allows the user to store multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGA.

8. Reset Switch (Active-Low)

The active-Low reset switch resets the System ACE controller.

9. Configuration Address DIP Switch

This switch is used to select one of eight addresses in the CompactFlash memory card, from which a configuration bitstream can be read. The open (O) position indicates a logic 0 and the closed (C) position indicates a logic 1 as shown in Table 4.

Table 4: **DIP Switch Configuration**

Address	2	1	0
0	O	O	O
1	O	O	C
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

10. JTAG Isolation Jumpers

The 2-pin headers shown in Table 5 provide the ability for the user to isolate the DUT JTAG interface from the System ACE controller. This is done by removing the shorting jumpers. The user may also drive the DUT JTAG interface directly from these headers by attaching the flying wire JTAG cable to pin one of each header.

Table 5: **JTAG Isolation Jumpers**

Ref Des	Pin Name
J128	TDI
J129	TDO
J131	TMS
J132	TCK

11. System ACE MPU Port

The 8-bit MPU port of the System ACE controller implemented on the ML52x series boards and the port connection to the DUT are shown in Table 6. For more information on the System ACE MPU port see *System ACE CompactFlash Solution* [Ref 1].

Table 6: **System ACE Port Connections**

Pin Name	ML521	ML523	ML525
MPA00	K7	E8	N8
MPA01	K6	E9	N9
MPA02	U5	K9	G8
MPA03	R5	C13	U9
MPA04	N6	E11	V11
MPA05	P6	F11	U11
MPA06	N7	L9	K9
MPD00	U6	K8	G7
MPD01	T5	B13	U8
MPD02	H6	G13	L9
MPD03	G6	F13	M9
MPD04	L8	G12	T11
MPD05	M7	G11	T10
MPD06	T7	L8	J7
MPD07	R6	M8	J8
MPIRQ	P8	E13	L7
MPBRDY	R7	N9	M8
MPCE#	M6	M10	K8
MPOE#	N8	E12	K7
MPWE#	R8	N10	M7
CLK	G20	G23	N30

12. Oscillator Sockets

The ML52x platform has two oscillator sockets, each wired for standard LVCMOS-type oscillators. These connect to the DUT clock pins as shown in Table 7. The oscillator sockets accept both half- and full-sized oscillators and are powered by 3.3V or the VCCAUX 2.5V power supply.

Table 7: **Oscillator Sockets Connections**

Ref Des	Enable/Disable Jumper	Power Select Jumper	Pin Name	ML521	ML523	ML525
X2	J114	J115	CLK_IN_B	AB19	AG21	AP27
X3	J117	J116	CLK_IN_A	D18(1)	J19(1)	K29

Notes:

1. For ML521 and ML523, the X3 clock input is not placed on the master clock IOB site. The environment variable XIL_PLACE_ALLOW_LOCAL_BUFG_ROUTING must be set to demote this condition to a warning and allow the design to continue.

13. Single-Ended SMA Clock Inputs

The ML52x platform has two single-ended clock input SMA connections that allow connection to an external function generator. These connect to the DUT clock pins as shown in Table 8.

Table 8: **SMA Clock Pin Connections**

Ref Des	Pin Name	ML521	ML523	ML525
J123	CLK_B	AB17(1)	AF19(1)	AM27
J124	CLK_A	E17	K18	M27

Notes:

1. For ML521 and ML523, the J123 clock input is not placed on the master clock IOB site. The environment variable XIL_PLACE_ALLOW_LOCAL_BUFG_ROUTING must be set to demote this condition to a warning and allow the design to continue.

14. Differential SMA Global Clock Inputs

The ML52x platform has two pairs of differential SMA transceivers clock inputs that allow connection to an external function generator. These connect to the DUT clock pins as shown in Table 9.

Table 9: **Differential SMA clock connections**

Ref Des	Pin Name	ML521	ML523	ML525
J120	CLK_DIFF_A_P	E13	J16	L17
J125	CLK_DIFF_A_N	E12	J17	M17
J121	CLK_DIFF_B_P	AC12	AH15	AM16
J122	CLK_DIFF_B_N	AC13	AG15	AM17

15. User LEDs (Active-High)

There are 16 active-High LEDs, as shown inTable 10 and Table 11 that are connected to user I/O pins on the DUT. These LEDs can be used to indicate status or any other purpose the user sees fit.

Table 10: **User LEDs Top Column**

Ref Des	LED	ML521	ML523	ML525
DS16	LED8	AE6	AJ25	AP37
DS17	LED7	AF5	AH25	AP36
DS18	LED6	AE8	AH27	AH35
DS19	LED5	AE7	AJ26	AG36
DS20	LED4	AB6	AK28	AH34
DS21	LED3	AB7	AK27	AG34
DS22	LED2	AF12	AA25	AB33
DS23	LED1	AE12	AA26	AB32

Table 11: **User LEDs Bottom Column**

Ref Des	LED	ML521	ML523	ML525
DS24	LED16	AC8	AE27	AH36
DS25	LED15	AD8	AE26	AJ36
DS26	LED14	AD6	AF25	AN34
DS27	LED13	AC7	AF26	AM34
DS28	LED12	AF4	AG27	AM36
DS29	LED11	AF3	AG26	AN35
DS30	LED10	AE5	AF24	AP35
DS31	LED9	AD4	AG25	AN36

16. User DIP Switches (Active-High)

There are 16 active-High DIP switches, as shown in Table 12 and Table 13, that are connected to user I/O pins on the DUT. These pins can be used to set control pins or any other purpose the user sees fit.

Table 12: **User DIP Switches Top Column**

Ref Des	Net Name	ML521	ML523	ML525
S1	SW8	W9	AB27	AC33
	SW7	W8	AC27	AD32
	SW6	AE11	AD24	AL34
	SW5	AD11	AE24	AK34
	SW4	V8	AD26	AL36
	SW3	V9	AD25	AL35
	SW2	AD9	AC25	AJ35
	SW1	AC9	AC24	AK35

Table 13: **User DIP Switches Bottom Column**

Ref Des	Net Name	ML521	ML523	ML525
S2	SW16	AA7	AB28	AU38
	SW15	AA8	AA28	AU37
	SW14	AF9	AC28	AV39
	SW13	AF10	AD27	AV38
	SW12	Y7	AB25	AE33
	SW11	Y8	AB26	AE34
	SW10	AD10	Y24	AD33
	SW9	AE10	AA24	AE32

17. User Pushbutton Switches (Active-High)

There are four active-High pushbutton switches, as shown in Table 14, that are connected to user I/O pins on the DUT. These switches can be used for any purpose that the user sees fit.

Table 14: **User Pushbutton Switches**

Ref Des	Switch	ML521	ML523	ML525
SW5	PB_SW4	AA12	AF14	AM13
SW6	PB_SW3	AA18	AE22	AL30
SW7	PB_SW2	Y18	AE23	AM29
SW8	PB_SW1	AA10	AF13	AK15

18. DDR2 Memory

The DDR2 memory interface on the ML52x board consists of four 256-Mbit DDR2 SDRAM chips (Micron MT47H16M16BG-3:B or Infineon HYB18T256160AF) for a total of 1-Gbit (128-MB) capacity. The pins conform to the SSTL_1.8V standard and must connect to SSTL18_II type IOBs on the FPGA. Note that the data strobe pins (DQS*) might need to be connected to IOBs with digitally-controlled impedance (SSTL18_II_DCI). The designer can also choose to use differential IOBs (DIFF_SSTL18_II and DIFF_SSTL18_II_DCI) for clock and data strobe signals. Table 15 shows the DDR2 connections to the DUT.

For more information on the DDR2 memory devices refer to the Micron *DDR2 SDRAM* data sheet [Ref 6].

Table 15: **DDR2 Connections to the DUT**

Pin Name	ML521	ML523	ML525
A0	K26	K24	R34
A1	K25	N28	D37
A2	L24	M28	E38
A3	M24	P24	W33
A4	AF18	AE31	AH39
A5	N21	E27	V36
A6	M21	E26	U36
A7	J24	M27	G37
A8	H24	N27	H36
A9	J26	L28	G36
A10	J25	L24	P35
A11	E25	K28	F36
A12	E26	K27	F37
BA0	AC26	W24	AB34
BA1	B19	L30	N39
CAS#	C18	M30	M39
CK0N	H22	H24	J36
CK0P	G22	H25	H35
CK1N	M26	P27	V34
CK1P	N26	P26	V35
CKE	B20	P29	L39
CS#	AD19	AB30	AV40
D0	C14	F29	H39
D1	C13	E29	H38

Table 15: **DDR2 Connections to the DUT *(Cont'd)***

Pin Name	ML521	ML523	ML525
D2	C22	R29	U37
D3	D23	R28	V38
D4	A22	R31	U38
D5	B22	T31	T37
D6	C23	T29	W38
D7	B24	T28	V39
D8	C24	U28	AA36
D9	D24	U27	AA35
D10	A25	R27	Y34
D11	B25	R26	AA34
D12	C26	T26	W35
D13	B26	U26	Y35
D14	D25	T25	W37
D15	D26	U25	W36
D16	B14	G30	G38
D17	A15	J29	F40
D18	A14	H29	F39
D19	C16	E31	E40
D20	B15	F31	E39
D21	B16	L29	R39
D22	A17	G31	P37
D23	B17	H30	R37
D24	G24	M26	P36
D25	F24	M25	N36
D26	E23	J27	L36
D27	F22	G26	J35
D28	F23	G25	K35
D29	J23	F26	J37
D30	K23	G28	U33
D31	K22	H28	T34
D32	AF15	AF29	AN39
D33	AE13	AH30	AM38
D34	AF13	AJ30	AN38

Table 15: **DDR2 Connections to the DUT *(Cont'd)***

Pin Name	ML521	ML523	ML525
D35	AD13	AH29	AM37
D36	AD24	W26	AB36
D37	AD25	Y26	AC35
D38	AE26	W25	AD35
D39	AE25	V25	AC36
D40	AF19	AD31	AG39
D41	AD18	AC29	AK39
D42	AE18	AD30	AJ38
D43	AD16	AD29	AH38
D44	AE16	AE29	AJ37
D45	AE15	AK31	AM39
D46	AD15	AJ31	AL39
D47	AF14	AF30	AP38
D48	N23	N25	W32
D49	N24	P25	Y33
D50	M22	T24	AA32
D51	N22	R24	Y32
D52	G26	L26	M36
D53	F25	L25	N35
D54	G25	J25	M37
D55	H26	J24	L37
D56	AF24	W27	AD37
D57	AF25	Y27	AD36
D58	AF23	V30	AE37
D59	AD23	V27	AE38
D60	AE22	V28	AE39
D61	AC23	Y31	AG38
D62	AC24	W31	AF39
D63	AB22	V29	AF37
DQM0	A23	U30	T39
DQM1	A13	F30	G39
DQM2	A19	J31	N38
DQM3	H23	F25	K37

Table 15: **DDR2 Connections to the DUT *(Cont'd)***

Pin Name	ML521	ML523	ML525
DQM4	AD14	AG30	AL37
DQM5	AE17	AF31	AK38
DQM6	M25	N24	V33
DQM7	AC22	W29	AG37
DQS0	D21	P31	H40
DQS0#	D20	P30	J40
DQS1	B21	M31	K40
DQS1#	C21	N30	K39
DQS2	C19	K31	K38
DQS2#	D19	L31	J38
DQS3	J21	G27	U34
DQS3#	K21	H27	T35
DQS4	AF22	Y28	AN40
DQS4#	AE21	Y29	AP40
DQS5	AC21	AA29	AT39
DQS5#	AD21	AA30	AR39
DQS6	L23	E28	R35
DQS6#	L22	F28	T36
DQS7	AF20	AB31	AR40
DQS7#	AE20	AA31	AT40
ODT	A20	N29	M38
RAS#	A18	J30	P38
WE#	AD20	AC30	AU39

19. GTP/GTX Transceiver Clock Input SMAs

The ML52x series platforms provide differential SMAs that allow connection to an external function generator for all GTP/GTX transceiver reference clock inputs of the DUT. These SMAs connect to the DUT reference clock pins as shown in Table 16.

Table 16: **Transceiver Reference Clock Inputs to the DUT**

REF DES	PIN NAME(1)	ML521	ML523	ML525
J48	REFCLKN_112	K3	P3	V3
J57	REFCLKP_112	K4	P4	V4
J38	REFCLKN_114	T3	Y3	AD3
J47	REFCLKP_114	T4	Y4	AD4
J15	REFCLKN_116	D3	H3	M3
J13	REFCLKP_116	D4	H4	M4
J28	REFCLKN_118	AB3	AF3	AK3
J37	REFCLKP_118	AB4	AF4	AK4
J68	REFCLKN_120		D4	F3
J77	REFCLKP_120		E4	F4
J88	REFCLKN_122		AL4	AT3
J97	REFCLKP_122		AL5	AT4
J58	REFCLKN_124		C8	C3
J67	REFCLKP_124		D8	C4
J78	REFCLKN_126		AM7	AY4
J87	REFCLKP_126		AL7	AW4
J147	REFCLKN_128			C10
J155	REFCLKP_128			D10
J167	REFCLKN_130			AY9
J175	REFCLKP_130			AW9
J179	REFCLKN_132			C16
J146	REFCLKP_132			D16
J159	REFCLKN_134			AY15
J166	REFCLKP_134			AW15

Notes:

1. The GTP/GTX transceiver clock pin names might have the prefix *MGT* in other Xilinx documentation. Names with and without the MGT prefix are synonymous to each other.

20. GTP/GTX Transceiver Pins

All DUT GTP/GTX transceiver pins are connected to differential SMA pairs. The transceiver pins and their corresponding SMA are shown in Table 17.

Table 17: **GTP/GTX Transceiver Pins**

REF DES	PIN NAME (1)	ML521	ML523	ML525
J56	RXN0_112	K1	P1	V1
J54	RXP0_112	J1	N1	U1
J53	TXN0_112	J2	N2	U2
J55	TXP0_112	H2	M2	T2
J51	RXN1_112	L1	R1	W1
J52	RXP1_112	M1	T1	Y1
J49	TXN1_112	M2	T2	Y2
J50	TXP1_112	N2	U2	AA2
J46	RXN0_114	T1	Y1	AD1
J45	RXP0_114	R1	W1	AC1
J43	TXN0_114	R2	W2	AC2
J44	TXP0_114	P2	V2	AB2
J41	RXN1_114	U1	AA1	AE1
J42	RXP1_114	V1	AB1	AF1
J39	TXN1_114	V2	AB2	AF2
J40	TXP1_114	W2	AC2	AG2
J7	RXN0_116	D1	H1	M1
J6	RXP0_116	C1	G1	L1
J10	TXN0_116	C2	G2	L2
J8	TXP0_116	B2	F2	K2
J12	RXN1_116	E1	J1	N1
J9	RXP1_116	F1	K1	P1
J14	TXN1_116	F2	K2	P2
J11	TXP1_116	G2	L2	R2
J36	RXN0_118	AB1	AF1	AK1
J35	RXP0_118	AA1	AE1	AJ1
J33	TXN0_118	AA2	AE2	AJ2
J34	TXP0_118	Y2	AD2	AH2
J31	RXN1_118	AC1	AG1	AL1
J32	RXP1_118	AD1	AH1	AM1

Table 17: **GTP/GTX Transceiver Pins *(Cont'd)***

REF DES	PIN NAME (1)	ML521	ML523	ML525
J29	TXN1_118	AD2	AH2	AM2
J30	TXP1_118	AE2	AJ2	AN2
J76	RXN0_120		A2	F1
J75	RXP0_120		A3	E1
J73	TXN0_120		B3	E2
J74	TXP0_120		B4	D2
J71	RXN1_120		C1	G1
J72	RXP1_120		D1	H1
J69	TXN1_120		D2	H2
J70	TXP1_120		E2	J2
J96	RXN0_122		AM1	AT1
J95	RXP0_122		AL1	AR1
J93	TXN0_122		AL2	AR2
J94	TXP0_122		AK2	AP2
J91	RXN1_122		AP2	AU1
J92	RXP1_122		AP3	AV1
J89	TXN1_122		AN3	AV2
J90	TXP1_122		AN4	AW2
J66	RXN0_124		A8	A4
J65	RXP0_124		A9	A5
J63	TXN0_124		B9	B5
J64	TXP0_124		B10	B6
J61	RXN1_124		A7	A3
J62	RXP1_124		A6	A2
J59	TXN1_124		B6	B2
J60	TXP1_124		B5	B1
J86	RXN0_126		AP7	BB3
J85	RXP0_126		AP6	BB2
J83	TXN0_126		AN6	BA2
J84	TXP0_126		AN5	BA1
J81	RXN1_126		AP8	BB4
J82	RXP1_126		AP9	BB5
J79	TXN1_126		AN9	BA5
J80	TXP1_126		AN10	BA6

Table 17: **GTP/GTX Transceiver Pins *(Cont'd)***

REF DES	PIN NAME (1)	ML521	ML523	ML525
J154	RXN0_128			A10
J156	RXP0_128			A11
J152	TXN0_128			B11
J153	TXP0_128			B12
J150	RXN1_128			A9
J151	RXP1_128			A8
J148	TXN1_128			B8
J149	TXP1_128			B7
J174	RXN0_130			BB9
J176	RXP0_130			BB8
J172	TXN0_130			BA8
J173	TXP0_130			BA7
J170	RXN1_130			BB10
J171	RXP1_130			BB11
J168	TXN1_130			BA11
J169	TXP1_130			BA12
J158	RXN0_132			A16
J145	RXP0_132			A17
J144	TXN0_132			B17
J157	TXP0_132			B18
J142	RXN1_132			A15
J143	RXP1_132			A14
J21	TXN1_132			B14
J141	TXP1_132			B13
J178	RXN0_134			BB15
J165	RXP0_134			BB14
J164	TXN0_134			BA14
J177	TXP0_134			BA13
J162	RXN1_134			BB16
J163	RXP1_134			BB17
J160	TXN1_134			BA17
J161	TXP1_134			BA18

Notes:

1. The GTP/GTX transceiver pin names might have the prefix *MGT* in other Xilinx documentation. Names with and without the MGT prefix are synonymous to each other.

21. RS-232 Port Pins

The RS-232 port pin connections to the DUT are as shown in Table 18. The pins are set up in DTE mode as shown in Figure 4.

Table 18: **RS-232 Port Pins**

Pin Name	Direction	Port Name	ML521	ML523	ML525
TXD	OUT	T1IN	G14	L16	P17
RTS	OUT	T2IN	H13	L15	P18
RXD	IN	R1OUT	G16	L20	P25
CTS	IN	R2OUT	G15	L21	N25

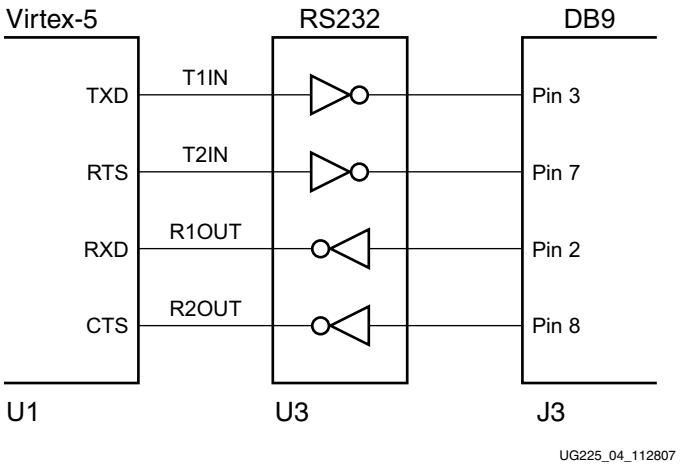


Figure 4: **RS-232 Pins in DTE Mode**

22. Xilinx Generic Interface (XGI)

The XGI is an expansion interface for plug-in modules (for example, the SuperClock module) and provides the user access to the I/O pins listed in the tables below.

Table 19 (spanning multiple pages) shows the schematic pinout of the XGI interface converted to an alphanumeric column and row format.

Table 19: **Top View of PCB**

	Column			Column		
	F	E	D	C	B	A
Row	J113		J135	J136	J118	
1	1	2	1	1	1	2
2	3	4	2	2	3	4
3	5	6	3	3	5	6
4	7	8	4	4	7	8
5	9	10	5	5	9	10

Table 19: **Top View of PCB *(Cont'd)***

	Column			Column		
	F	E	D	C	B	A
Row	J113		J135	J136	J118	
6	11	12	6	6	11	12
7	13	14	7	7	13	14
8	15	16	8	8	15	16
9	17	18	9	9	17	18
10	19	20	10	10	19	20
11	21	22	11	11	21	22
12	23	24	12	12	23	24
13	25	26	13	13	25	26
14	27	28	14	14	27	28
15	29	30	15	15	29	30
16	31	32	16	16	31	32
17	33	34	17	17	33	34
18	35	36	18	18	35	36
19	37	38	19	19	37	38
20	39	40	20	20	39	40
21	41	42	21	21	41	42
22	43	44	22	22	43	44
23	45	46	23	23	45	46
24	47	48	24	24	47	48
25	49	50	25	25	49	50
26	51	52	26	26	51	52
27	53	54	27	27	53	54
28	55	56	28	28	55	56
29	57	58	29	29	57	58
30	59	60	30	30	59	60
31	61	62	31	31	61	62
32	63	64	32	32	63	64

The XGI pin connections to the DUT are shown in Table 20, page 31, Table 21, page 32 and Table 22, page 33.

Table 20: **XGI Pin Connections to the DUT (J113 and J135)**

J113							J135	
XGI Pin #	Description	XGI Pin #	Description	ML521	ML523	ML525	XGI Pin #	Description
F1	GND	E2	XGI_DIFF_0P	F7	B33	F41	D1	VCCO
F3	GND	E4	XGI_DIFF_0N	F8	C33	G41	D2	VCCO
F5	GND	E6	XGI_DIFF_1P	F9	C32	H41	D3	VCCO
F7	GND	E8	XGI_DIFF_1N	G9	D32	J41	D4	VCCO
F9	GND	E10	XGI_DIFF_2P	H8	C34	J42	D5	VCCO
F11	GND	E12	XGI_DIFF_2N	J8	D34	K42	D6	VCCO
F13	GND	E14	XGI_DIFF_3P	A9	G32	L40	D7	VCCO
F15	GND	E16	XGI_DIFF_3N	A8	H32	L41	D8	VCCO
F17	GND	E18	XGI_DIFF_4P	E8	F33	L42	D9	VCCO
F19	GND	E20	XGI_DIFF_4N	E7	E34	M41	D10	VCCO
F21	GND	E22	XGI_DIFF_5P	B9	E32	M42	D11	VCCO
F23	GND	E24	XGI_DIFF_5N	C8	E33	N41	D12	VCCO
F25	GND	E26	XGI_DIFF_6P	E6	G33	N40	D13	VCCO
F27	GND	E28	XGI_DIFF_6N	D6	F34	P40	D14	VCCO
F29	GND	E30	XGI_DIFF_7P	C9	J32	W40	D15	VCCO
F31	GND	E32	XGI_DIFF_7N	D8	H33	Y40	D16	VCCO
F33	GND	E34	XGI_DIFF_8P	C7	H34	AA40	D17	VCCO
F35	GND	E36	XGI_DIFF_8N	C6	J34	AA39	D18	VCCO
F37	GND	E38	XGI_DIFF_9P	A7	L34	Y39	D19	VCCO
F39	GND	E40	XGI_DIFF_9N	B7	K34	Y38	D20	VCCO
F41	GND	E42	XGI_DIFF_10P	D9	K33	Y37	D21	VCCO
F43	GND	E44	XGI_DIFF_10N	D10	K32	AA37	D22	VCCO
F45	GND	E46	XGI_DIFF_11P	B10	L33	P41	D23	VCCO
F47	GND	E48	XGI_DIFF_11N	A10	M32	R40	D24	VCCO
F49	GND	E50	XGI_DIFF_12P	A4	P34	T40	D25	VCCO
F51	GND	E52	XGI_DIFF_12N	A3	N34	T41	D26	VCCO
F53	GND	E54	XGI_DIFF_13P	B11	P32	T42	D27	VCCO
F55	GND	E56	XGI_DIFF_13N	A12	N32	U41	D28	VCCO
F57	GND	E58	XGI_DIFF_14P	B4	T33	U42	D29	VCCO
F59	GND	E60	XGI_DIFF_14N	B5	R34	V41	D30	VCCO
F61	GND	E62	XGI_DIFF_15P	B12	R33	V40	D31	VCCO
F63	GND	E64	XGI_DIFF_15N	C12	R32	W41	D32	VCCO

Table 21: **XGI Pin Connections to the DUT (J136)**

J136				
XGI Pin #	**Description**	**ML521**	**ML523**	**ML525**
C1	VCC5	VCC5	VCC5	VCC5
C2	VCC5	VCC5	VCC5	VCC5
C3	VCC5	VCC5	VCC5	VCC5
C4	VCC5	VCC5	VCC5	VCC5
C5	NC	NC	NC	NC
C6	VCC33	VCC33	VCC33	VCC33
C7	VCC33	VCC33	VCC33	VCC33
C8	VCC33	VCC33	VCC33	VCC33
C9	VCC33	VCC33	VCC33	VCC33
C10	NC	NC	NC	NC
C11	CFG TMS	CFG TMS	CFG TMS	CFG TMS
C12	CFG TCK	CFG TCK	CFG TCK	CFG TCK
C13	EX TDO	EX TDO	EX TDO	EX TDO
C14	FPGA TDO	FPGA TDO	FPGA TDO	FPGA TDO
C15	XGI_SE_32	E5	T34	Y42
C16	XGI_SE_33	D5	U33	W42
C17	XGI_SE_34	D11	U31	AA41
C18	XGI_SE_35	C11	U32	AA42
C19	XGI_SE_36	F5	D10	R8
C20	XGI_SE_37	G5	D11	R7
C21	XGI_SE_38	W6	J11	F6
C22	XGI_SE_39	W5	K11	F7
C23	XGI_SE_40	H4	C12	T9
C24	XGI_SE_41	G4	D12	R9
C25	XGI_SE_42	V7	H9	F5
C26	XGI_SE_43	V6	H10	E5
C27	XGI_SE_44	J6	B12	V10
C28	XGI_SE_45	J5	A13	V9
C29	XGI_SE_46	T8	J9	G9
C30	XGI_SE_47	U7	J10	F9
C31	I2C SCL-R	W4	F8	E8
C32	I2C SDA-R	Y4	F9	E9

Table 22: **XGI Pin Connections to the DUT (J118)**

J118						
XGI Pin #	**Description**	**XGI Pin #**	**Description**	**ML521**	**ML523**	**ML525**
B1	GND	A2	XGI_SE_0	T24	AC32	AJ42
B3	GND	A4	XGI_SE_1	T23	AB32	AJ41
B5	GND	A6	XGI_SE_2	U25	AC34	AG42
B7	GND	A8	XGI_SE_3	T25	AD34	AH41
B9	GND	A10	XGI_SE_4	U26	Y32	AF40
B11	GND	A12	XGI_SE_5	V26	W32	AG41
B13	GND	A14	XGI_SE_6	R23	AA34	AF41
B15	GND	A16	XGI_SE_7	R22	Y34	AF42
B17	GND	A18	XGI_SE_8	P24	Y33	AE42
B19	GND	A20	XGI_SE_9	P23	AA33	AD41
B21	GND	A22	XGI_SE_10	P25	W34	AC41
B23	GND	A24	XGI_SE_11	R25	V34	AD42
B25	GND	A26	XGI_SE_12	V21	AN32	AU42
B27	GND	A28	XGI_SE_13	W21	AP32	AV41
B29	GND	A30	XGI_SE_14	U21	AN34	AT41
B31	GND	A32	XGI_SE_15	V22	AN33	AU41
B33	GND	A34	XGI_SE_16	T22	AM33	AR42
B35	GND	A36	XGI_SE_17	U22	AM32	AT42
B37	GND	A38	XGI_SE_18	P21	AL34	AP42
B39	GND	A40	XGI_SE_19	R21	AL33	AP41
B41	GND	A42	XGI_SE_20	AB24	AJ32	AM41
B43	GND	A44	XGI_SE_21	AA23	AK32	AN41
B45	GND	A46	XGI_SE_22	AB25	AG32	AL42
B47	GND	A48	XGI_SE_23	AA24	AH32	AM42
B49	GND	A50	XGI_SE_24	AA25	AK34	AL41
B51	GND	A52	XGI_SE_25	AB26	AK33	AK42
B53	GND	A54	XGI_SE_26	U24	AC33	AH40
B55	GND	A56	XGI_SE_27	V24	AB33	AJ40
B57	GND	A58	XGI_SE_28	Y23	AD32	AC40
B59	GND	A60	XGI_SE_29	W23	AE32	AC39
B61	GND	A62	XGI_SE_30	AA22	AH34	AE40
B63	GND	A64	XGI_SE_31	Y22	AJ34	AD40

Table 23 defines the default jumper positions set by the factory.

Table 23: **Default Jumper Positions**

Ref Des	Function	Shorting Jumper	Number of Jumpers	Pins
J112	VCCINT	Installed Horizontally	2/4(1)	N/A
J110	VCCO		2	
J111	VCCAUX			
J127	DDR_PWR	Not Installed	0	1-2
J5	UART	Installed	1	
J24	RSVD			
J126	DDR VOLTAGE SELECT			2-3
J114	X2 OSCILLATOR ENABLE	Installed	1	1-2
J115	X2 OSCILLATOR VOLTAGE			
J116	X3 OSCILLATOR VOLTAGE			
J117	X3 OSCILLATOR ENABLE			
J128	JTAG TDI			
J129	JTAG TDO			
J131	JTAG TMS			
J132	JTAG TCK			
J137	AVTTRX	Not Installed	0	
J138	AVTTTX			
J139	AVCCPLL			
J140	AVCC			
J130	TDI/TDO EXPANSION	Installed	1	
J4	SYSTEM ACE OSCILLATOR ENABLE			
J19	POWER SUPPLY MODULE SHUTDOWN	Not Installed	0	

Notes:

1. The ML525 board is the only board in the series requiring four jumpers for this position.

References

Users should be familiar with the following Xilinx documents:

1. DS080, *System ACE CompactFlash Solution*
2. UG091, *Xilinx Generic Interface (XGI) SuperClock Module User Guide*
3. UG190, *Virtex-5 FPGA User Guide*
4. UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*
5. UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*

Additional related documentation:

6. Micron *DDR2 SDRAM* data sheet.
   http://download.micron.com/pdf/datasheets/dram/ddr2/256MbDDR2.pdf