10-Output Ultra-Low Phase Noise Jitter Attenuating Clock Generator

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Overview
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Part:          Si5380
Design ID:     5380BP2
Created By:    ClockBuilder Pro v1.7 [2015-03-26]
Timestamp:     2015-03-26 09:24:49 GMT-05:00

Design
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Host Interface:
   I/O Power Supply: VDD (Core)
   SPI Mode: 4-Wire
   I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins)

XA/XB:
   54 MHz (XTAL - Crystal)

Inputs:
    IN0: Unused
    IN1: Unused
    IN2: Unused
    IN3: Unused

Outputs:
  OUT0A: Unused
   OUT0: Unused
   OUT1: Unused
   OUT2: Unused
   OUT3: Unused
   OUT4: Unused
   OUT5: Unused
   OUT6: Unused
   OUT7: Unused
   OUT8: Unused
   OUT9: Unused
  OUT9A: Unused

Frequency Plan
==============
No plan

Settings
========

Location      Setting Name          Decimal Value  Hex Value
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0x000B[0:6]   I2C_ADDR              104            0x68
0x0016[1]     LOL_ON_HOLD           1              0x1
0x0017[0]     SYSINCAL_INTR_MSK     0              0x0
0x0017[1]     LOSXAXB_INTR_MSK      0              0x0
0x0017[5]     SMB_TMOUT_INTR_MSK    0              0x0
0x0018[0:3]   LOS_INTR_MSK          15             0xF
0x0018[4:7]   OOF_INTR_MSK          15             0xF
0x0019[1]     LOL_INTR_MSK          0              0x0
0x0019[5]     HOLD_INTR_MSK         0              0x0
0x001A[5]     CAL_INTR_MSK          0              0x0
0x002B[3]     SPI_3WIRE             0              0x0
0x002C[0:3]   LOS_EN                0              0x0
0x002C[4]     LOSXAXB_DIS           0              0x0
0x002D[0:1]   LOS0_VAL_TIME         0              0x0
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0x002D[2:3]	LOS1_VAL_TIME	0	0x0
0x002D[4:5]	LOS2_VAL_TIME	0	0x0
0x002D[6:7]	LOS3_VAL_TIME	0	0x0
0x002E[0:15]	LOS0_TRG_THR	0	0x0000
0x0030[0:15]	LOS1_TRG_THR	0	0x0000
0x0032[0:15]	LOS2_TRG_THR	0	0x0000
0x0034[0:15]	LOS3_TRG_THR	0	0x0000
0x0036[0:15]	LOS0_CLR_THR	0	0x0000
0x0038[0:15]	LOS1_CLR_THR	0	0x0000
0x003A[0:15]	LOS2_CLR_THR	0	0x0000
0x003C[0:15]	LOS3_CLR_THR	0	0x0000
0x003F[0:3]	OOF_EN	0	0x0
0x003F[4:7]	FAST_OOF_EN	0	0x0
0x0040[0:2]	OOF_REF_SEL	4	0x4
0x0041[0:4]	OOF0_DIV_SEL	0	0x00
0x0042[0:4]	OOF1_DIV_SEL	0	0x00
0x0043[0:4]	OOF2_DIV_SEL	0	0x00
0x0044[0:4]	OOF3_DIV_SEL	0	0x00
0x0045[0:4]	OOFXO_DIV_SEL	12	0x0C
0x0046[0:7]	OOF0_SET_THR	0	0x00
0x0047[0:7]	OOF1_SET_THR	0	0x00
0x0048[0:7]	OOF2_SET_THR	0	0x00
0x0049[0:7]	OOF3_SET_THR	0	0x00
0x004A[0:7]	OOF0_CLR_THR	0	0x00
0x004B[0:7]	OOF1_CLR_THR	0	0x00
0x004C[0:7]	OOF2_CLR_THR	0	0x00
0x004D[0:7]	OOF3_CLR_THR	0	0x00
0x004E[0:2]	OOF0_DETWIN_SEL	0	0x0
0x004E[4:6]	OOF1_DETWIN_SEL	0	0x0
0x004F[0:2]	OOF2_DETWIN_SEL	0	0x0
0x004F[4:6]	OOF3_DETWIN_SEL	0	0x0
0x0051[0:3]	FAST_OOF0_SET_THR	0	0x0
0x0052[0:3]	FAST_OOF1_SET_THR	0	0x0
0x0053[0:3]	FAST_OOF2_SET_THR	0	0x0
0x0054[0:3]	FAST_OOF3_SET_THR	0	0x0
0x0055[0:3]	FAST_OOF0_CLR_THR	0	0x0
0x0056[0:3]	FAST_OOF1_CLR_THR	0	0x0
0x0057[0:3]	FAST_OOF2_CLR_THR	0	0x0
0x0058[0:3]	FAST_OOF3_CLR_THR	0	0x0
0x0059[0:1]	FAST_OOF0_DETWIN_SEL	0	0x0
0x0059[2:3]	FAST_OOF1_DETWIN_SEL	0	0x0
0x0059[4:5]	FAST_OOF2_DETWIN_SEL	0	0x0
0x0059[6:7]	FAST_OOF3_DETWIN_SEL	0	0x0
0x005A[0:25]	OOF0_RATIO_REF	0	0x0000000
0x005E[0:25]	OOF1_RATIO_REF	0	0x0000000
0x0062[0:25]	OOF2_RATIO_REF	0	0x0000000
0x0066[0:25]	OOF3_RATIO_REF	0	0x0000000
0x0092[1]	LOL_FST_EN	0	0x0
0x0093[4:7]	LOL_FST_DETWIN_SEL	0	0x0
0x0095[2:3]	LOL_FST_VALWIN_SEL	0	0x0
0x0096[4:7]	LOL_FST_SET_THR_SEL	0	0x0
0x0098[4:7]	LOL_FST_CLR_THR_SEL	0	0x0
0x009A[1]	LOL_SLOW_EN_PLL	0	0x0
0x009B[4:7]	LOL_SLW_DETWIN_SEL	0	0x0
0x009D[2:3]	LOL_SLW_VALWIN_SEL	0	0x0
0x009E[4:7]	LOL_SLW_SET_THR	0	0x0
0x00A0[4:7]	LOL_SLW_CLR_THR	0	0x0
0x00A2[1]	LOL_TIMER_EN	0	0x0
0x00A8[0:34]	LOL_CLR_DELAY	0	0x000000000
0x0102[0]	OUTALL_DISABLE_LOW	1	0x1
0x0103[0]	OUT0A_PDN	1	0x1
0x0103[1]	OUT0A_OE	0	0x0
0x0103[2]	OUT0A_RDIV_FORCE	0	0x0
0x0104[0:2]	OUT0A_FORMAT	1	0x1

0x0104[3]	OUT0A_SYNC_EN	1	0x1
0x0104[4:5]	OUT0A_DIS_STATE	0	0x0
0x0104[6:7]	OUT0A_CMOS_DRV	0	0x0
0x0105[0:3]	OUT0A_CM	11	0xB
0x0105[4:6]	OUT0A_AMPL	3	0x3
0x0106[0:2]	OUT0A_MUX_SEL	0	0x0
0x0106[6:7]	OUT0A_INV	0	0x0
0x0108[0]	OUT0_PDN	1	0x1
0x0108[1]	OUT0_OE	0	0x0
0x0108[2]	OUT0_RDIV_FORCE	0	0x0
0x0109[0:2]	OUT0_FORMAT	1	0x1
0x0109[3]	OUT0_SYNC_EN	1	0x1
0x0109[4:5]	OUT0_DIS_STATE	0	0x0
0x0109[6:7]	OUT0_CMOS_DRV	0	0x0
0x010A[0:3]	OUT0_CM	11	0xB
0x010A[4:6]	OUT0_AMPL	3	0x3
0x010B[0:2]	OUT0_MUX_SEL	0	0x0
0x010B[6:7]	OUT0_INV	0	0x0
0x010D[0]	OUT1_PDN	1	0x1
0x010D[1]	OUT1_OE	0	0x0
0x010D[2]	OUT1_RDIV_FORCE2	0	0x0
0x010E[0:2]	OUT1_FORMAT	1	0x1
0x010E[3]	OUT1_SYNC_EN	1	0x1
0x010E[4:5]	OUT1_DIS_STATE	0	0x0
0x010E[6:7]	OUT1_CMOS_DRV	0	0x0
0x010F[0:3]	OUT1_CM	11	0xB
0x010F[4:6]	OUT1_AMPL	3	0x3
0x0110[0:2]	OUT1_MUX_SEL	0	0x0
0x0110[6:7]	OUT1_INV	0	0x0
0x0112[0]	OUT2_PDN	1	0x1
0x0112[1]	OUT2_OE	0	0x0
0x0112[2]	OUT2_RDIV_FORCE2	0	0x0
0x0113[0:2]	OUT2_FORMAT	1	0x1
0x0113[3]	OUT2_SYNC_EN	1	0x1
0x0113[4:5]	OUT2_DIS_STATE	0	0x0
0x0113[6:7]	OUT2_CMOS_DRV	0	0x0
0x0114[0:3]	OUT2_CM	11	0xB
0x0114[4:6]	OUT2_AMPL	3	0x3
0x0115[0:2]	OUT2_MUX_SEL	0	0x0
0x0115[6:7]	OUT2_INV	0	0x0
0x0117[0]	OUT3_PDN	1	0x1
0x0117[1]	OUT3_OE	0	0x0
0x0117[2]	OUT3_RDIV_FORCE2	0	0x0
0x0118[0:2]	OUT3_FORMAT	1	0x1
0x0118[3]	OUT3_SYNC_EN	1	0x1
0x0118[4:5]	OUT3_DIS_STATE	0	0x0
0x0118[6:7]	OUT3_CMOS_DRV	0	0x0
0x0119[0:3]	OUT3_CM	11	0xB
0x0119[4:6]	OUT3_AMPL	3	0x3
0x011A[0:2]	OUT3_MUX_SEL	0	0x0
0x011A[6:7]	OUT3_INV	0	0x0
0x011C[0]	OUT4_PDN	1	0x1
0x011C[1]	OUT4_OE	0	0x0
0x011C[2]	OUT4_RDIV_FORCE2	0	0x0
0x011D[0:2]	OUT4_FORMAT	1	0x1
0x011D[3]	OUT4_SYNC_EN	1	0x1
0x011D[4:5]	OUT4_DIS_STATE	0	0x0
0x011D[6:7]	OUT4_CMOS_DRV	0	0x0
0x011E[0:3]	OUT4_CM	11	0xB
0x011E[4:6]	OUT4_AMPL	3	0x3
0x011F[0:2]	OUT4_MUX_SEL	0	0x0
0x011F[6:7]	OUT4_INV	0	0x0
0x0121[0]	OUT5_PDN	1	0x1
0x0121[1]	OUT5_OE	0	0x0

0x0121[2]	OUT5_RDIV_FORCE2	0	0x0
0x0122[0:2]	OUT5_FORMAT	1	0x1
0x0122[3]	OUT5_SYNC_EN	1	0x1
0x0122[4:5]	OUT5_DIS_STATE	0	0x0
0x0122[6:7]	OUT5_CMOS_DRV	0	0x0
0x0123[0:3]	OUT5_CM	11	0xB
0x0123[4:6]	OUT5_AMPL	3	0x3
0x0124[0:2]	OUT5_MUX_SEL	0	0x0
0x0124[6:7]	OUT5_INV	0	0x0
0x0126[0]	OUT6_PDN	1	0x1
0x0126[1]	OUT6_OE	0	0x0
0x0126[2]	OUT6_RDIV_FORCE2	0	0x0
0x0127[0:2]	OUT6_FORMAT	1	0x1
0x0127[3]	OUT6_SYNC_EN	1	0x1
0x0127[4:5]	OUT6_DIS_STATE	0	0x0
0x0127[6:7]	OUT6_CMOS_DRV	0	0x0
0x0128[0:3]	OUT6_CM	11	0xB
0x0128[4:6]	OUT6_AMPL	3	0x3
0x0129[0:2]	OUT6_MUX_SEL	0	0x0
0x0129[6:7]	OUT6_INV	0	0x0
0x012B[0]	OUT7_PDN	1	0x1
0x012B[1]	OUT7_OE	0	0x0
0x012B[2]	OUT7_RDIV_FORCE2	0	0x0
0x012C[0:2]	OUT7_FORMAT	1	0x1
0x012C[3]	OUT7_SYNC_EN	1	0x1
0x012C[4:5]	OUT7_DIS_STATE	0	0x0
0x012C[6:7]	OUT7_CMOS_DRV	0	0x0
0x012D[0:3]	OUT7_CM	11	0xB
0x012D[4:6]	OUT7_AMPL	3	0x3
0x012E[0:2]	OUT7_MUX_SEL	0	0x0
0x012E[6:7]	OUT7_INV	0	0x0
0x0130[0]	OUT8_PDN	1	0x1
0x0130[1]	OUT8_OE	0	0x0
0x0130[2]	OUT8_RDIV_FORCE2	0	0x0
0x0131[0:2]	OUT8_FORMAT	1	0x1
0x0131[3]	OUT8_SYNC_EN	1	0x1
0x0131[4:5]	OUT8_DIS_STATE	0	0x0
0x0131[6:7]	OUT8_CMOS_DRV	0	0x0
0x0132[0:3]	OUT8_CM	11	0xB
0x0132[4:6]	OUT8_AMPL	3	0x3
0x0133[0:2]	OUT8_MUX_SEL	0	0x0
0x0133[6:7]	OUT8_INV	0	0x0
0x0135[0]	OUT9_PDN	1	0x1
0x0135[1]	OUT9_OE	0	0x0
0x0135[2]	OUT9_RDIV_FORCE2	0	0x0
0x0136[0:2]	OUT9_FORMAT	1	0x1
0x0136[3]	OUT9_SYNC_EN	1	0x1
0x0136[4:5]	OUT9_DIS_STATE	0	0x0
0x0136[6:7]	OUT9_CMOS_DRV	0	0x0
0x0137[0:3]	OUT9_CM	11	0xB
0x0137[4:6]	OUT9_AMPL	3	0x3
0x0138[0:2]	OUT9_MUX_SEL	0	0x0
0x0138[6:7]	OUT9_INV	0	0x0
0x013A[0]	OUT9A_PDN	1	0x1
0x013A[1]	OUT9A_OE	0	0x0
0x013A[2]	OUT9A_RDIV_FORCE2	0	0x0
0x013B[0:2]	OUT9A_FORMAT	1	0x1
0x013B[3]	OUT9A_SYNC_EN	1	0x1
0x013B[4:5]	OUT9A_DIS_STATE	0	0x0
0x013B[6:7]	OUT9A_CMOS_DRV	0	0x0
0x013C[0:3]	OUT9A_CM	11	0xB
0x013C[4:6]	OUT9A_AMPL	3	0x3
0x013D[0:2]	OUT9A_MUX_SEL	0	0x0
0x013D[6:7]	OUT9A_INV	0	0x0

0x013F[0:11]	OUTX_ALWAYS_ON	0	0x000
0x0141[5]	OUT_DIS_MSK_XAXBERR	0	0x0
0x0141[6]	OUT_DIS_LOSXAXB_MSK	1	0x1
0x0142[1]	OUT_DIS_MSK_LOL_PLLB	1	0x1
0x0142[5]	OUT_DIS_MSK_HOLD	1	0x1
0x0206[0:1]	PXAXB	0	0x0
0x0208[0:47]	P0_NUM	0	0x000000000000
0x020E[0:31]	P0_DEN	0	0x00000000
0x0212[0:47]	P1_NUM	0	0x000000000000
0x0218[0:31]	P1_DEN	0	0x00000000
0x021C[0:47]	P2_NUM	0	0x000000000000
0x0222[0:31]	P2_DEN	0	0x00000000
0x0226[0:47]	P3_NUM	0	0x000000000000
0x022C[0:31]	P3_DEN	0	0x00000000
0x0231[4]	P0_FRACN_EN	0	0x0
0x0232[4]	P1_FRACN_EN	0	0x0
0x0233[4]	P2_FRACN_EN	0	0x0
0x0234[4]	P3_FRACN_EN	0	0x0
0x0235[0:43]	MXAXB_NUM	0	0x00000000000
0x023B[0:31]	MXAXB_DEN	0	0x00000000
0x0247[0:23]	R0A_REG	0	0x000000
0x024A[0:23]	R0_REG	0	0x000000
0x024D[0:23]	R1_REG	0	0x000000
0x0250[0:23]	R2_REG	0	0x000000
0x0253[0:23]	R3_REG	0	0x000000
0x0256[0:23]	R4_REG	0	0x000000
0x0259[0:23]	R5_REG	0	0x000000
0x025C[0:23]	R6_REG	0	0x000000
0x025F[0:23]	R7_REG	0	0x000000
0x0262[0:23]	R8_REG	0	0x000000
0x0265[0:23]	R9_REG	0	0x000000
0x0268[0:23]	R9A_REG	0	0x000000
0x026B[0:7]	DESIGN_ID0	53	0x35
0x026C[0:7]	DESIGN_ID1	51	0x33
0x026D[0:7]	DESIGN_ID2	56	0x38
0x026E[0:7]	DESIGN_ID3	48	0x30
0x026F[0:7]	DESIGN_ID4	66	0x42
0x0270[0:7]	DESIGN_ID5	80	0x50
0x0271[0:7]	DESIGN_ID6	50	0x32
0x0272[0:7]	DESIGN_ID7	0	0x00
0x0302[0:43]	N0_NUM	0	0x00000000000
0x0308[0:31]	N0_DEN	0	0x00000000
0x030D[0:43]	N1_NUM	0	0x00000000000
0x0313[0:31]	N1_DEN	0	0x00000000
0x0318[0:43]	N2_NUM	0	0x00000000000
0x031E[0:31]	N2_DEN	0	0x00000000
0x0323[0:43]	N3_NUM	0	0x00000000000
0x0329[0:31]	N3_DEN	0	0x00000000
0x032E[0:43]	N4_NUM	0	0x00000000000
0x0334[0:31]	N4_DEN	0	0x00000000
0x0359[0:15]	N0_DELAY	0	0x0000
0x035B[0:15]	N1_DELAY	0	0x0000
0x035D[0:15]	N2_DELAY	0	0x0000
0x035F[0:15]	N3_DELAY	0	0x0000
0x0361[0:15]	N4_DELAY	0	0x0000
0x0487[0]	ZDM_EN	0	0x0
0x0487[1:2]	ZDM_IN_SEL	0	0x0
0x0502[4]	ADD_DIV256	0	0x0
0x0508[0:5]	BW0_PLL	0	0x00
0x0509[0:5]	BW1_PLL	0	0x00
0x050A[0:5]	BW2_PLL	0	0x00
0x050B[0:5]	BW3_PLL	0	0x00
0x050C[0:5]	BW4_PLL	0	0x00
0x050D[0:5]	BW5_PLL	0	0x00

0x050E[0:5]	FAST_BW0_PLL	0	0x00
0x050F[0:5]	FAST_BW1_PLL	0	0x00
0x0510[0:5]	FAST_BW2_PLL	0	0x00
0x0511[0:5]	FAST_BW_PLL	0	0x00
0x0512[0:5]	FAST_BW4_PLL	0	0x00
0x0513[0:5]	FAST_BW5_PLL	0	0x00
0x0515[0:55]	M_NUM	0	0x00000000000000
0x051C[0:31]	M_DEN	0	0x00000000
0x0521[0:3]	M_FRAC_MODE	0	0x0
0x0521[4]	M_FRAC_EN	0	0x0
0x052A[0]	IN_SEL_REGCTRL	0	0x0
0x052A[1:3]	IN_SEL	0	0x0
0x052B[0]	FASTLOCK_AUTO_EN	1	0x1
0x052B[1]	FASTLOCK_MAN	0	0x0
0x052C[0]	HOLD_EN	1	0x1
0x052C[3]	HOLD_RAMP_BYP	1	0x1
0x052C[5:7]	HOLD_RAMP_RATE	0	0x0
0x052D[1]	HOLD_RAMPBYP_NOHIST	1	0x1
0x052E[0:4]	HOLD_HIST_LEN	0	0x00
0x052F[0:4]	HOLD_HIST_DELAY	0	0x00
0x0531[0:4]	HOLD_REF_COUNT_FRC	0	0x00
0x0532[0:23]	HOLD_15M_CYC_COUNT	1024	0x000400
0x0536[0:1]	CLK_SWITCH_MODE	2	0x2
0x0536[2]	HSW_EN	1	0x1
0x0536[3]	HSW_RAMP_BYP	1	0x1
0x0537[0:3]	IN_LOS_MSK	0	0x0
0x0537[4:7]	IN_OOF_MSK	0	0x0
0x0538[0:2]	IN0_PRIORITY	0	0x0
0x0538[4:6]	IN1_PRIORITY	0	0x0
0x0539[0:2]	IN2_PRIORITY	0	0x0
0x0539[4:6]	IN3_PRIORITY	0	0x0
0x090E[0]	XAXB_EXTCLK_EN	0	0x0
0x0943[0]	IO_VDD_SEL	0	0x0
0x0949[0:3]	IN_EN	0	0x0
0x0949[4:7]	IN_PULSED_CMOS_EN	0	0x0
0x094A[0:3]	INX_TO_PFD_EN	15	0xF
0x0A02[0:4]	N_ADD_0P5	0	0x00
0x0A03[0:4]	N_CLK_TO_OUTX_EN	31	0x1F
0x0A04[0:4]	N_PIBYP	0	0x00
0x0A05[0:4]	N_PDNB	31	0x1F
0x0B44[0:3]	PDIV_FRACN_CLK_DIS	0	0x0
0x0B44[5]	FRACN_CLK_DIS_PLL	0	0x0
0x0B46[0:3]	LOS_CLK_DIS	0	0x0
0x0B47[0:4]	OOF_CLK_DIS	0	0x00
0x0B48[0:4]	OOF_DIV_CLK_DIS	15	0x0F
0x0B4A[0:4]	N_CLK_DIS	0	0x00

This datasheet addendum is provided as supplemental information to the Si5380A datasheet, located at www.silabs.com/timing. You can search for and download any datasheet addendum for Si534x/8x part numbers. Go to http://www.silabs.com/custom-timing for more information.

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