TPS40197 4.5-V to 14-V Input, 6-A Buck Controller With Four-Bit VID Interface

1 Features

- Input Voltage Range: 4.5 V to 14 V
- 4-Bit Dynamic VID-On-The-Fly Support
- VID Programmable Output Voltage with Programmable Transition Rate
- Fixed Switching Frequency of 520 kHz
- Selectable Low-Side (Three Settings) and Fixed High-Side Thermally Compensated Overcurrent Protection
- Power Good Indicator
- Internal 5-V Regulator
- Voltage Mode Control
- Internally Fixed 5.5-ms Soft-Start Time
- Prebias Output Safe
- Thermal Shutdown at 140°C
- 16-Pin QFN Package

2 Applications

- Smart-Reflex™ DSPs
- POL Modules
- Telecom

3 Description

The TPS40197 is a synchronous buck controller that operates from 4.5 V to 14 V input supply nominally. The controller implements voltage-mode control architecture with the switching frequency fixed at 520 kHz. The higher switching frequency facilitates the use of smaller inductor and output capacitors, thereby providing a compact power-supply solution. An adaptive anti-cross conduction scheme is used to prevent shoot through current in the power FETs.

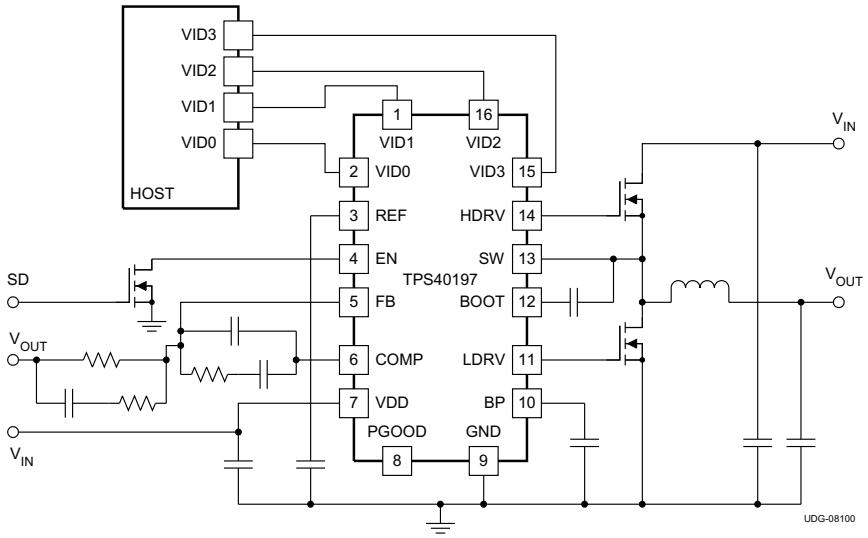
The TPS40197 integrates the PWM control and 4-bit VID interface in a single chip to allow seamless on-the-fly VID changes with programmable transition rate. It provides a simple power solution for Smart-Reflex™ DSP cores.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS40197	VQFN (16)	4.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2012) to Revision B	Page
• Editorial changes only; no technical revision	1

Changes from Original (November 2008) to Revision A	Page
• Added a new paragraph to the Enable section	13

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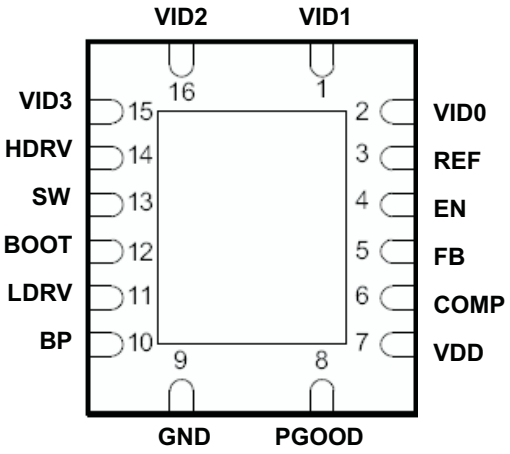
5 Description Continued

Short-circuit detection is done by sensing the voltage drop across the low-side FET when it is on and comparing it with a user selected threshold of 100 mV, 200 mV or 280 mV. The threshold is set with a single external resistor connected from COMP to GND. This resistor is sensed at startup and the selected threshold is latched. Pulse by pulse limiting (to prevent current runaway) is provided by sensing the voltage across the high-side FET when it is on and terminating the cycle when the voltage drop rises above a fixed threshold of 550 mV. When the controller senses an output short circuit, both FETs are turned off and a timeout period is observed before attempting to restart. This provides limited power dissipation in the event of a sustained fault.

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6 Pin Configuration and Functions

RGY Package
16-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	12	I	Gate drive voltage for the high-side N-channel MOSFET. A 100-nF capacitor (typical) must be connected between this pin and SW.
BP	10	O	Output bypass for the internal regulator. Connect a low ESR bypass ceramic capacitor of 1 μF or greater from this pin to GND.
COMP	6	O	Output of the error amplifier and connection node for loop feedback components.
EN	4	I	Logic level input which starts or stops the controller from an external user command. A high level turns the controller on. A weak internal pullup holds this pin high so that the pin may be left floating if this function is not used. Pulling this pin low disables the controller.
FB	5	I	Inverting input to the error amplifier.
HDRV	14	O	Bootstrapped gate drive output for the high-side N-channel MOSFET.
LDRV	11	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET.
PGOOD	8	O	Open drain power good output.
REF	3	I	Non-Inverting input to the error amplifier. Its voltage range is from 0.9 V to 1.2 V in 20-mV steps. It is also internally connected to the DAC output through a unit gain buffer with 650-μA source/sink current capability. An external capacitor connected from this pin to GND programs the output voltage transition rate when VID code changes.
VDD	7	I	Power input to the controller. Connect a 1-μF bypass capacitor closely from this pin to GND.
VID0	2	I	Logic level inputs to the internal DAC that provides the reference voltage for output regulation. These pins are internally pulled up to a 1.68-V source with 80-μA pullup current.
VID1	1	I	
VID2	16	I	
VID3	15	I	
GND	9		Ground connection to the controller

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7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input voltage	VDD, EN	–0.3 to 20	V
	SW	–5 to 25	
	BOOT, HDRV	–0.3 to 30	
	BOOT–SW, HDRV–SW	–0.3 to 6	
	FB, BP, LDRV, PGOOD, REF	–0.3 to 6	
Output voltage	COMP	–0.3 to 3.5	V
	VID0, VID1, VID2, VID3	–0.3 to 2	
Operating junction temperature range, T_J		–40 to150	°C
Storage temperature, T_{stg}		–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VDD	4.5	14	V
Operating junction temperature, T_J		–40	125	°C

7.4 Package Dissipation Ratings

PACKAGE	AIRFLOW (LFM)	$R_{\theta JA}$ HIGH-K Board(1) (°C/W)	POWER RATING (W) T_A = 25°C	POWER RATING (W) T_A = 85°C
16-Pin Plastic Quad Flatpack (RGY)	0 (Natural Convection)	49.2	2.0	0.81
	200	41.2	2.4	0.97
	400	37.7	2.6	1.00

(1) Ratings based on JEDEC High Thermal Conductivity (High K) Board. For more information on the test method, see TI Technical Brief SZZA017.

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7.5 Electrical Characteristics

–40°C ≤ T_J ≤ 85°C, V_{VDD} = 12 V, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE AND VID						
V_{FB}	FB input voltage	0.9 V ≤ V_{VID} ≤ 1.2 V, 0°C ≤ T_J ≤ 85°C	–0.5%		0.5%	V_{VID}
		0.9 V ≤ V_{VID} ≤ 1.2 V, –40°C ≤ T_J ≤ 85°C	–1.0%		1.0%	
I_{VID}	VID pullup current		50	80	120	µA
V_{VID}	VID pullup voltage		1.60	1.68	1.78	V
$t_{ANTI-SKEW}$ (1)	Anti-skew filtering time		300	550	750	ns
V_{VIDH}	VID high-level input voltage		0.8	1.0	1.3	V
V_{VIDL}	VID low-level input voltage		0.30	0.55	0.70	V
I_{REF}	REF source/sink current		400	650	850	µA
INPUT SUPPLY						
V_{VDD}	Normal input supply voltage range		4.5		14.0	V
I_{VDD}	Operating current	V_{ENABLE} = 3 V		2.5	4.5	mA
		V_{ENABLE} = 0.6 V		45	70	µA
SOFT START						
t_{SS}	Soft-start time		3.3	5.5	7	ms
t_{SSDLY}	Soft-start delay time		1.3	2.3	4	
t_{REG}	Time to regulation		5.0	8.0	11	
ON-BOARD REGULATOR						
V_{BP}	Output voltage	V_{VDD} > 6 V, I_{BP} ≤ 10 mA	5.1	5.3	5.5	V
V_{DO}	Regulator dropout voltage (V_{VDD}–V_{BP})	V_{VDD} > 5 V, I_{BP} ≤ 25 mA		350	550	mV
I_{SC}	Regulator current limit threshold		50			mA
I_{BP}	Average current				50	
OSCILLATOR						
f_{SW}	Switching frequency		420	520	600	kHz
V_{RAMP} (1)	Ramp amplitude			1		V
PWM						
D_{MAX} (1)	Maximum duty cycle		85%			
$t_{ON(min)}$ (1)	Minimum controllable pulse				110	ns
t_{DEAD}	Output driver dead time	HDRV off to LDRV on		50		
		LDRV off to HDRV on		25		
ERROR AMPLIFIER						
G_{BWP} (1)	Gain bandwidth product		7	10		MHz
A_{OL} (1)	Open loop gain		60			dB
I_{IB}	Input bias current (current out of FB pin)				100	nA
I_{EAOP}	Output source current	V_{FB} = 0 V	1			mA
I_{EAOM}	Output sink current	V_{FB} = 2 V	1			
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Turn-on voltage		3.9	4.2	4.4	V
$UVLO_{HYST}$	Hysteresis		700	850	1000	mV
SHUTDOWN						
V_{IH}	High-level input voltage, ENABLE			1.9	3	V
V_{IL}	Low-level input voltage, ENABLE		0.6	1.2		

(1) Specified by design. Not production tested.

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Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 85°C, V_{VDD} = 12 V, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	(V_{BOOT} – V_{SW}) - 4.5 V, $I_{HDR\ V}$ = – 100 mA		3	6	Ω
R_{HDLO}	High-side driver pull-down resistance	(V_{BOOT} – V_{SW}) - 4.5 V, $I_{HDR\ V}$ = 100 mA		1.5	3	
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = –100 mA		2.5	5	
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 100 mA		0.8	1.5	
t_{HRISE} (1)	High-side driver rise time	C_{LOAD} = 1 nF		15	35	ns
t_{HFALL} (1)	High-side driver fall time			10	25	
t_{LRISE} (1)	Low-side driver rise time			15	35	
t_{LFALL} (1)	Low-side driver fall time			10	25	
SHORT CIRCUIT PROTECTION						
$t_{PSS(min)}$ (1)	Minimum pulse time during short circuit			250		ns
t_{BLNK} (1)	Switch leading-edge blanking pulse time		60	90	120	
t_{OFF}	Off-time between restart attempts		30	50		ms
V_{ILIM}	Short circuit comparator threshold voltage	$R_{COMP(GND)}$ = OPEN, T_J = 25°C	160	200	240	mV
		$R_{COMP(GND)}$ = 4 kΩ, T_J = 25°C	80	100	120	
		$R_{COMP(GND)}$ = 12 kΩ, T_J = 25°C	228	280	342	
V_{ILIMH}	Short circuit threshold voltage on high-side MOSFET	T_J = 25°C	400	550	650	
POWER GOOD						
V_{OV}	Feedback voltage limit for powergood		106%	110%	114%	VID
V_{UV}			86%	90%	94%	
V_{PG_HYST}	Powergood hysteresis voltage at FB pin		10	30	70	mV
R_{PGD}	Pull-down resistance of PGD pin	V_{FB} < 90% V_{VID} mV or V_{FB} > 110% V_{VID}		7	50	Ω
I_{PDGLK}	Leakage current	90% V_{VID} ≤ V_{FB} ≤ 100% V_{VID}, V_{PGOOD} = 5 V		7	12	µA
BOOT DIODE						
V_{DFWD}		I_{BOOT} = 5 mA	0.5	0.8	1.2	V
THERMAL SHUTDOWN						
T_{JSD} (1)	Junction shutdown temperature			140		°C
T_{JSDH} (1)	Hysteresis			20		

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7.6 Typical Characteristics

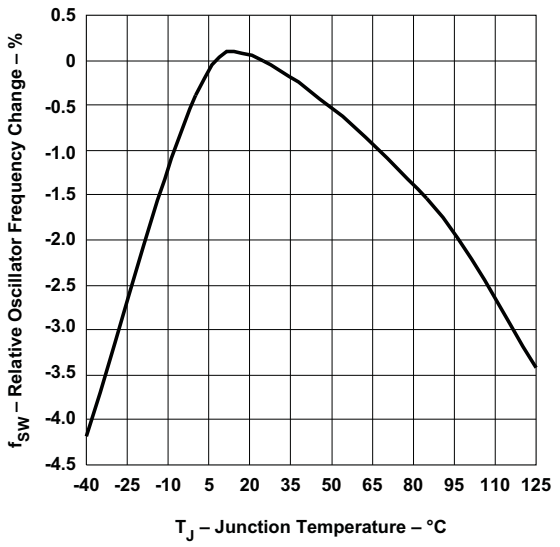


Figure 1. Relative Oscllator Frequency vs Junction Temperature

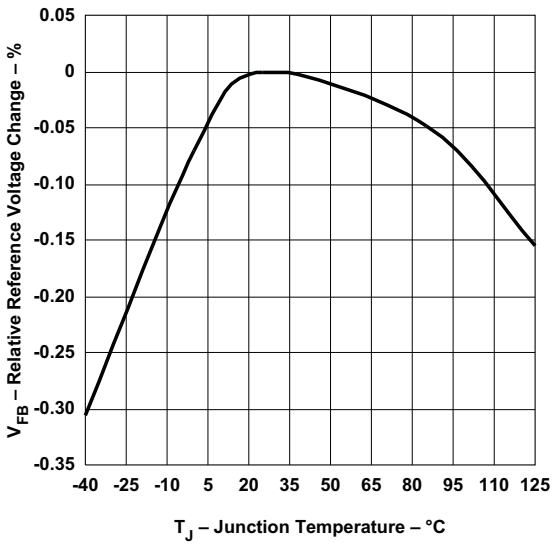


Figure 2. Relative Reference Voltage Change vs Junction Temperature

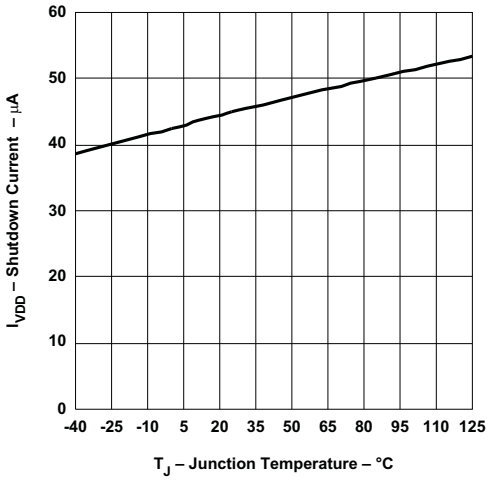


Figure 3. Shutdown Current vs Junction Temperature

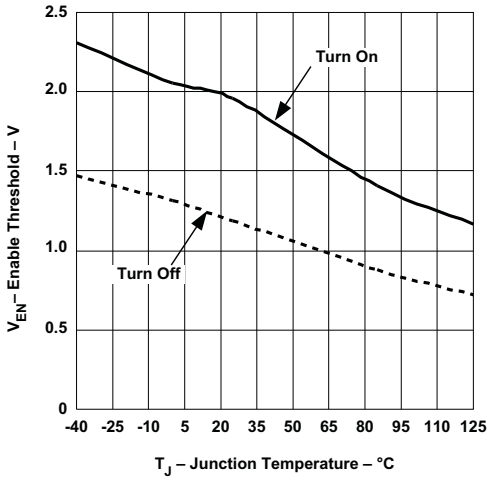


Figure 4. Enable Threshold vs Junction Temperature

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Typical Characteristics (continued)

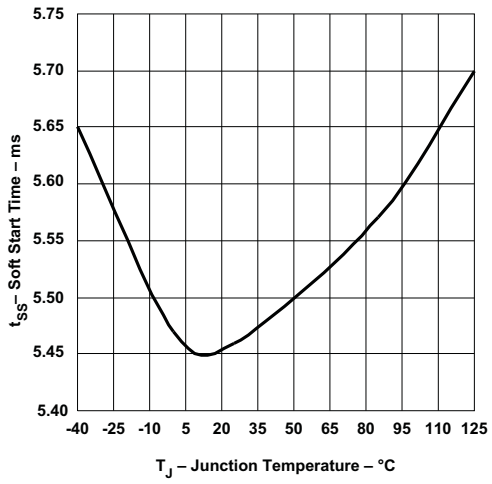


Figure 5. Soft-Start Time vs Junction Temperature

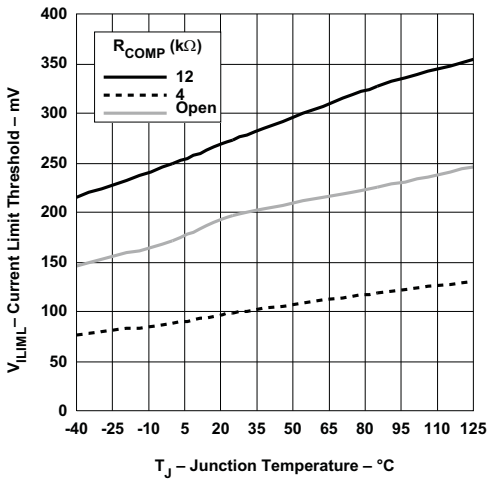


Figure 6. Low-Side MOSFET Current Limit Threshold vs Junction Temperature

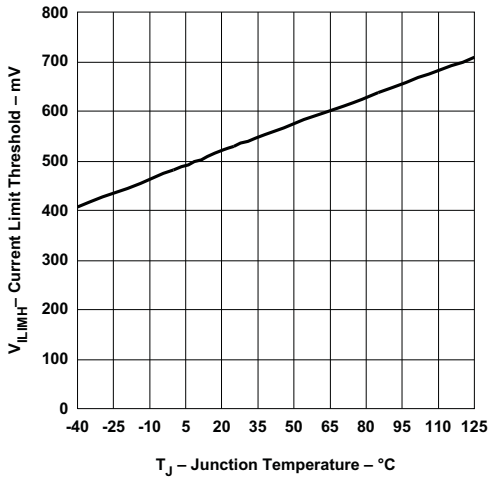


Figure 7. High-Side MOSFET Current Limit Threshold vs Junction Temperature

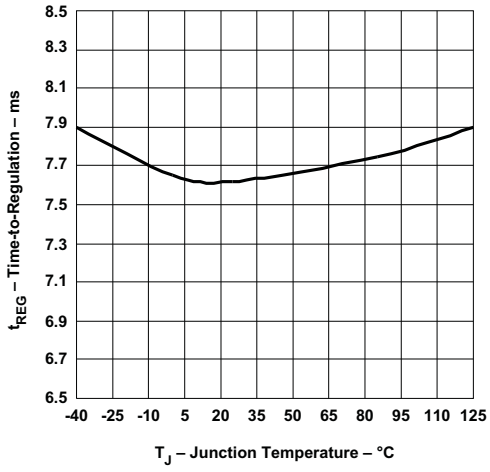


Figure 8. Total Time-To-Regulation vs Junction Temperature

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Typical Characteristics (continued)

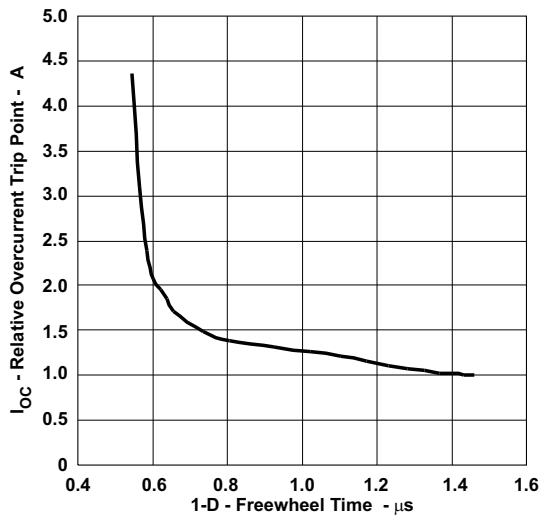


Figure 9. Relative Overcurrent Trip Point vs Freewheel Time

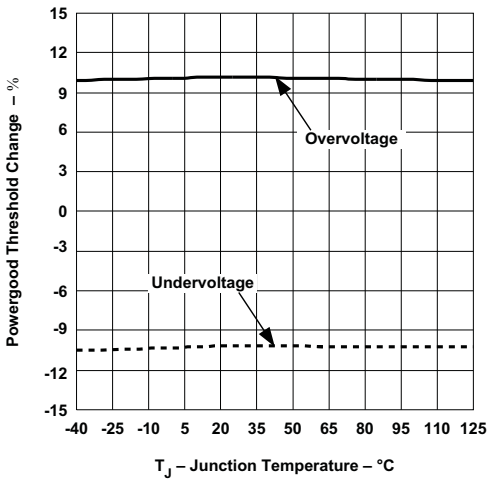


Figure 10. Relative Power Good Threshold vs Junction Temperature

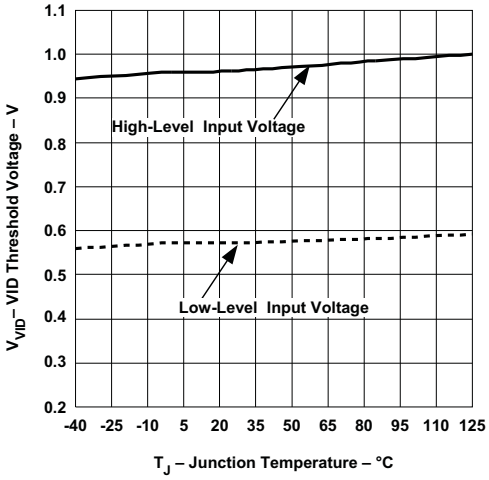


Figure 11. VID Threshold Voltage vs Junction Temperature

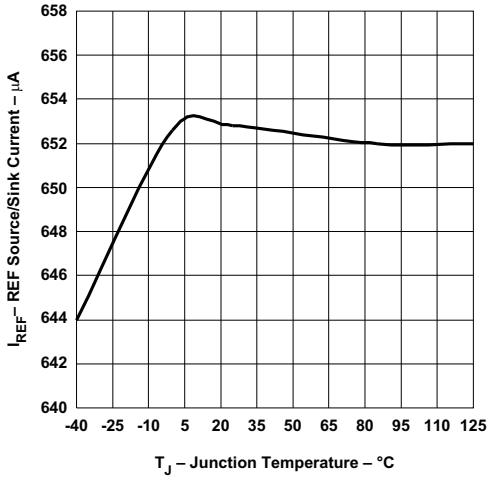


Figure 12. REF Source/Sink Current vs Junction Temperature

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Typical Characteristics (continued)

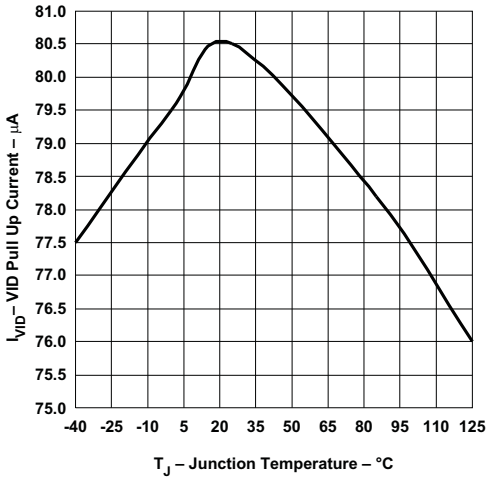


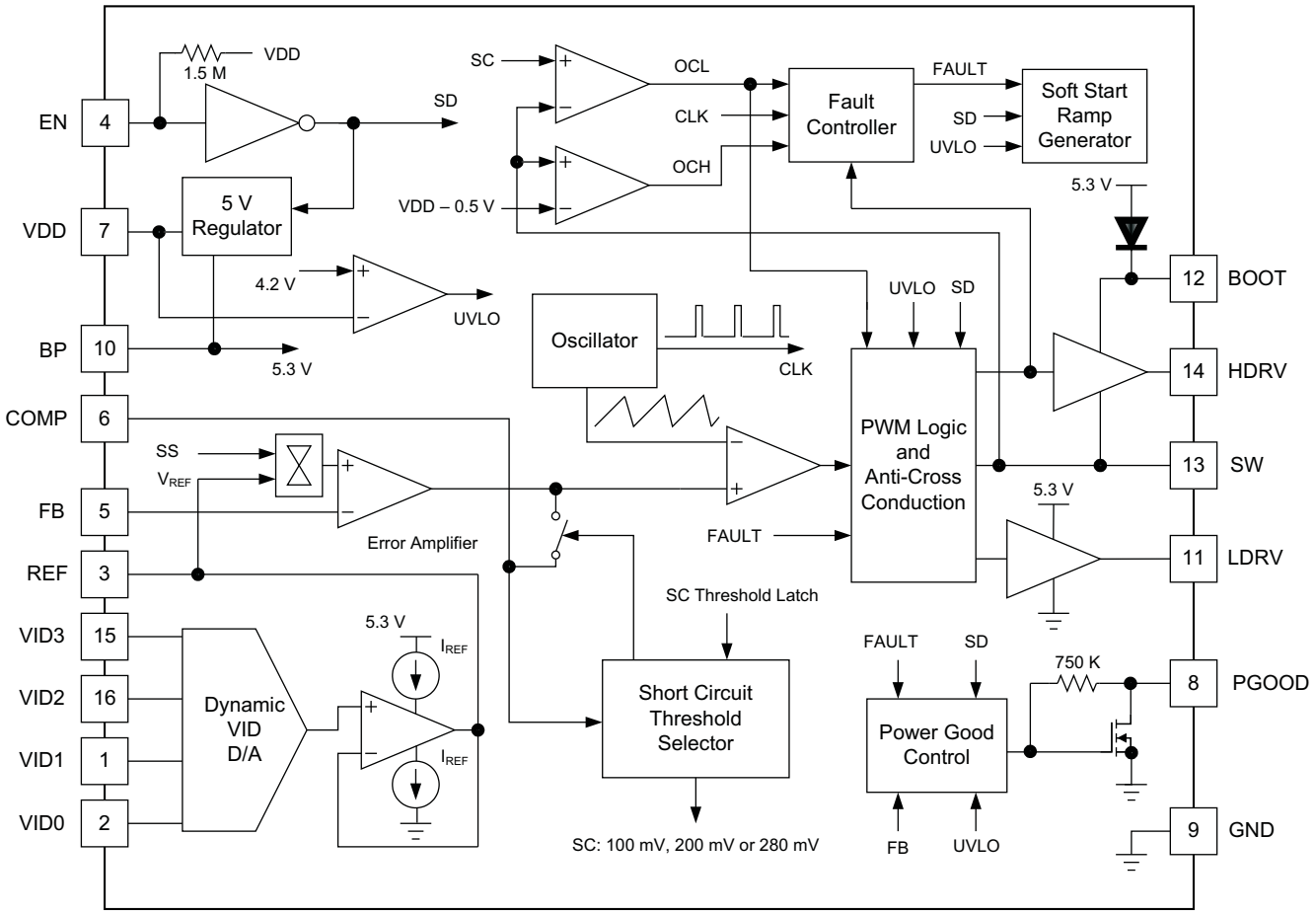
Figure 13. VID Pullup Current vs Junction Temperature

8 Detailed Description

8.1 Overview

The TPS40197 is a synchronous buck controller which provides all the necessary features to construct a high-performance DC/DC converter. Support for pre-biased outputs eliminates concerns about damaging sensitive loads during startup. Strong gate drivers for the high-side and rectifier MOSFETs decrease switching losses for increased efficiency. Adaptive gate drive timing prevents shoot through and minimizes body diode conduction in the rectifier MOSFET, also increasing efficiency. Selectable short-circuit protection thresholds and hiccup recovery from a short-circuit increase design flexibility and minimize power dissipation in the event of a prolonged output fault. A dedicated enable pin allows the converter to be placed in a very low quiescent current shutdown mode. Internally fixed switching frequency and soft-start time reduce external component count, simplifying design and layout, as well as reducing footprint and cost. The dynamic voltage identification (VID) circuitry is designed to provide Smart-Reflex™ power supply solution to DSPs with core voltage optimization.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Enable

The TPS40197 includes a dedicated EN pin. This simplifies user level interface design since no multiplexed functions exist. Another benefit is a true low-power shutdown mode of operation. When the EN pin is pulled to GND, all unnecessary functions, including the BP regulator, are turned off, reducing the I_{VDD} current to 45 μA. A functionally equivalent circuit of the enable circuitry is shown in Figure 14.

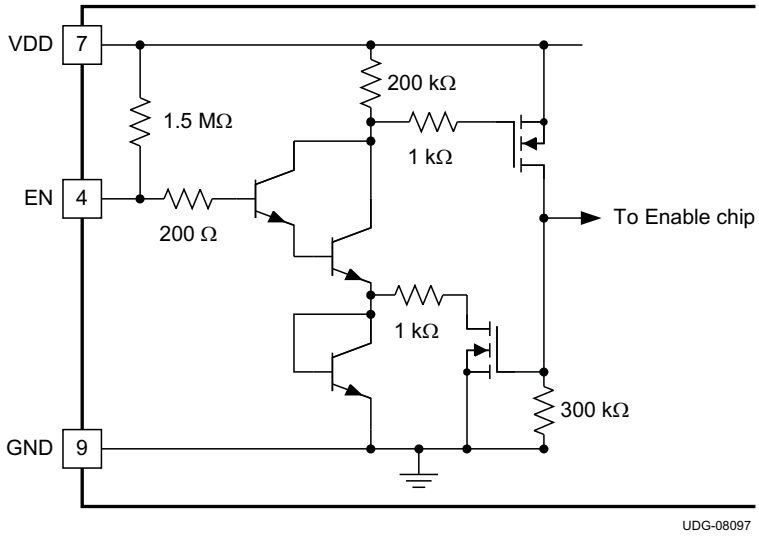


Figure 14. Tps40197 En Pin Internal Circuitry

If the EN pin is left floating, the device starts automatically. The pin must be pulled to less than 600 mV to specify that the TPS40197 is in shutdown mode. Note that the EN pin is relatively high impedance. In some situations, there could be enough noise nearby to cause the EN pin to swing below the 600-mV threshold and give erroneous shutdown commands to other components of the device. There are two solutions to this potential problem.

- Place a capacitor from EN to GND. A side-effect of this is to delay the start of the converter while the capacitor charges past the enable threshold.
- Place a resistor from VDD to EN. This causes more current to flow in the shutdown mode, but does not delay converter start-up. If a resistor is used, the total current into the EN pin must be limited to no more than 500 μA.

The ENABLE pin is self clamping. The clamp voltage can be as low as 1 V with a 1-kΩ ground impedance. Due to this self-clamping feature, the pull-up impedance on the ENABLE pin should be selected to limit the sink current to less than 500 μA. Driving the ENABLE pin with a low-impedance source voltage can result in damage to the device. Because of the self-clamping feature, it requires care when connecting multiple ENABLE pins together. For enabling multiple TPS4019x devices (TPS40190, TPS40192, TPS40193, TPS40195, TPS40197), see application report SLVA509.

8.3.2 Oscillator

The fixed internal switching frequency of the TPS40197 is 520 kHz.

8.3.3 UVLO

When the input voltage is below the UVLO threshold, the device holds all gate drive outputs in the low (OFF) state. When the input rises above the UVLO threshold, and the EN pin is above the turn ON threshold, the oscillator begins to operate and the start-up sequence is allowed to begin. The UVLO level is internally fixed at 4.2 V.

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Feature Description (continued)

8.3.4 Start-up Sequence and Timing

The TPS40197 startup sequence is as follows. After input power is applied, the 5-V onboard regulator initiates. Once this regulator comes up, the device goes through a period where it samples the impedance at the COMP pin and determines the short-circuit protection threshold voltage, by placing 400 mV on the COMP pin for approximately 1.15 ms. During this time, the current is measured and compared against internal thresholds to select the short circuit protection threshold. After this, the COMP pin is brought low for 1.15 ms. This ensures that the feedback loop is preconditioned at startup and no sudden output rise occurs at the output of the converter when the converter is allowed to start switching. After these initial 2.3 ms, the internal soft-start circuitry is engaged and the converter is allowed to start as shown in Figure 15.

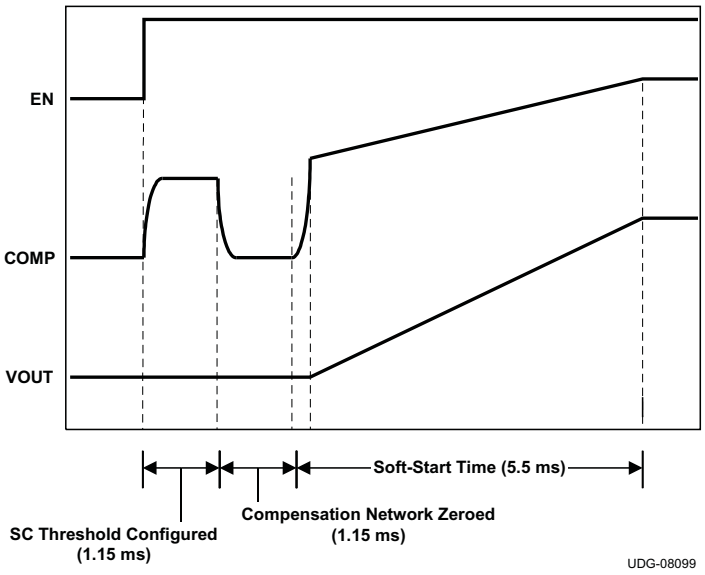


Figure 15. Start-up Sequence

8.3.5 Selecting the Short Circuit Current

A short circuit in the TPS40197 is detected by sensing the voltage drop across the low-side FET when it is on, and across the high-side FET when it is on. If the voltage drop across either FET exceeds the short-circuit threshold in any given switching cycle, a counter increments one count. If the voltage across the high-side FET was higher than the short circuit threshold, that FET is turned off early. If the voltage drop across either FET does not exceed the short circuit threshold during a cycle, the counter is decremented for that cycle. If the counter fills up (a count of 7) a fault condition is declared and the drivers turn off both MOSFETs. After a timeout of approximately 50 ms, the controller attempts to restart. If a short circuit continues at the output, the current quickly ramps up to the short-circuit threshold and another fault condition is declared and the process of waiting for the 50 ms and attempting to restart repeats. The low-side threshold increases as the low-side on time decreases due to blanking time and comparator response time. See Figure 9 for changes in the threshold as the low-side FET conduction time decreases.

The TPS40197 provides three selectable short-circuit protection thresholds for the low-side FET: 100 mV, 200 mV, and 280 mV. The particular threshold is selected by connecting a resistor from COMP to GND. Table 1 shows the short-circuit thresholds for corresponding resistors from COMP to GND. When designing the compensation for the feedback loop, remember that a low impedance compensation network combined with a long network time constant can cause the short-circuit threshold setting to not be as expected. The time constant and impedance of the network connected from COMP to FB must be as in Equation 1 to ensure no interaction with the short-circuit threshold setting.

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Feature Description (continued)

$$\left(\frac{0.4\,V}{R1}\right) \times e^{\left(\frac{-t}{(R1 \times C1)}\right)} \leq 10\,\mu A \quad (1)$$

where

- t is 1.15 ms, the sampling time of the short circuit threshold setting circuit
- R1 and C1 are the values of the components in Figure 16

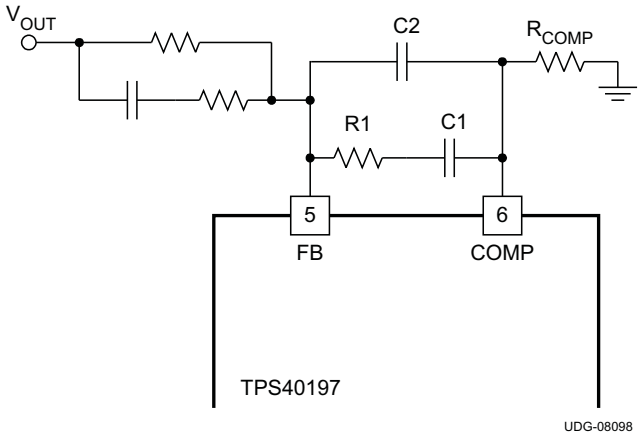


Figure 16. Short Circuit Threshold Feedback Network

Table 1. Circuit Threshold Voltage Selection

COMPARATOR RESISTANCE R_{COMP} (kΩ)	CURRENT LIMIT THRESHOLD VOLTAGE V_{ILIM} (mV)
12 ±10%	280
OPEN	200
4 ±10%	100

The range of expected short-circuit current thresholds is shown in Equation 2 and Equation 3.

$$I_{SCP(max)} = \frac{V_{ILIM(max)}}{R_{DS(on)min}} \quad (2)$$

$$I_{SCP(min)} = \frac{V_{ILIM(min)}}{R_{DS(on)max}}$$

where

- I_{SCP} is the short circuit current
- V_{ILIM} is the short-circuit threshold for the low-side MOSFET
- $R_{DS(on)}$ is the channel resistance of the low-side MOSFET (3)

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Note that due to blanking time considerations, overcurrent threshold accuracy may fall off for duty cycle greater than 75% because the overcurrent comparator has only a very short time to sample the SW pin voltage under these conditions and may not have time to respond to voltages very near the threshold.

The short-circuit protection threshold for the high-side MOSFET is fixed at 550 mV typical, 400 mV minimum. This threshold is in place to provide a maximum current output using pulse-by-pulse current limit in the case of a fault. The pulse terminates when the voltage drop across the high-side FET exceeds the short-circuit threshold. The maximum amount of current that can be specified to be sourced from a converter can be found by Equation 4.

$$I_{OUT(max)} = \frac{V_{ILIMH(min)}}{R_{DS(on)max}} \quad (4)$$

where

- $I_{OUT(max)}$ is the maximum current that the converter is specified to source
- $V_{ILIMH(min)}$ is the short-circuit threshold for the high-side MOSFET (400 mV)
- $R_{DS(on)max}$ is the maximum resistance of the high-side MOSFET

If the required current from the converter is greater than the calculated $I_{OUT(max)}$, a lower resistance high-side MOSFET must be chosen. Both the high-side and low-side thresholds use temperature compensation to approximate the change in resistance for a typical power MOSFET. This helps counteract shifts in overcurrent thresholds as temperature increases. For this to be effective, the MOSFETs and the device must be well coupled thermally.

8.3.6 Voltage Reference and Dynamic VID

To provide optimized voltage for Smart-Reflex™ DSP cores, the TPS40197 is designed to monitor the VID code at all times once soft-start is complete, and actively adjusts its output voltage if the VID code should change during normal operation. A digital-to-analog converter (DAC) generates a reference voltage based on the state of logical signals at pins VID0 through VID3. The DAC decodes the 4-bit logic signal into one of the discrete voltages shown in Table 2. The default setting for the output is 1.2 V (VID code 1111). The output voltage is 1.2 V during initial start or restart after cycling the input, toggling EN pin or recovering from a short circuit at the output.

To ensure that no erroneous output voltage is produced, the TPS40197 VID inputs have internal anti-skew circuit with approximately 550 ns of filtering time. Each VID input is pulled up to an internal 1.68-V source with 80-µA pullup current for use with open-drain outputs.

The output voltage can be programmed from 0.9 V to 1.2 V in 20 mV steps. Smooth upward and downward core voltage transition can be achieved by programming the transition rate with an external capacitor connected from REF pin to GND. The required capacitance can be calculated using Equation 5.

$$C_{REF} = \frac{(I_{REF} \times T_{TR})}{V_{VID-TR}} \quad (5)$$

where

- V_{VID-TR} is the total voltage transition through VID
- I_{REF} is the internal reference source/sink current
- T_{TR} is the intended total VID voltage transition time

C_{REF} must be limited to a maximum of 1.5 µF to avoid interfering with the soft start. A capacitor (C_{REF}) with a minimum capacitance of 100-nF is also recommended.

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Table 2. Voltage Identification Codes

VID TERMINALS (0 = LOW, 1 = HIGH)				V_{REF}
VID3	VID2	VID1	VID0	(Vdc)
0	0	0	0	0.90
0	0	0	1	0.92
0	0	1	0	0.94
0	0	1	1	0.96
0	1	0	0	0.98
0	1	0	1	1.00
0	1	1	0	1.02
0	1	1	1	1.04
1	0	0	0	1.06
1	0	0	1	1.08
1	0	1	0	1.10
1	0	1	1	1.12
1	1	0	0	1.14
1	1	0	1	1.16
1	1	1	0	1.18
1	1	1	1	1.20

8.3.7 Minimum On-Time Consideration

The TPS40197 has a minimum on-time of 110 ns (maximum). With the restriction of this minimum on-time, the device may begin to skip pulses to effectively lower the overall on-time to keep the output in regulation when operating at high input-to-output conversion ratio. If pulse skipping is undesirable for some reason, it is recommended that the maximum input voltage be limited to 13.5 V.

8.3.8 BP Regulator

The TPS40197 has an on board 5-V BP regulator that allows the parts to operate from a single voltage feed. No separate 5-V feed to the part is required. This regulator needs to have a minimum of 1-μF of capacitance on the BP pin for stability. A ceramic capacitor is suggested for this purpose.

This regulator can also be used to supply power to nearby circuitry, eliminating the need for a separate LDO in some cases. If this pin is used for external loads, be aware that this is the power supply for the internals of the TPS40197. While efforts have been made to reduce sensitivity, any noise induced on this line has an adverse effect on the overall performance of the internal circuitry and shows up as increased pulse jitter, or skewed reference voltage. Also, when the device is disabled by pulling the EN pin low, this regulator is turned off and will not be available to supply power.

The amount of power available from this pin varies with the size of the power MOSFETs that the drivers must operate. Larger MOSFETs require more gate drive current and reduce the amount of power available on this pin for other tasks. The total current that can be drawn from this pin by both the gate drive and external loads cannot exceed 50 mA. The device itself consumes up to 4 mA from the regulator and the total gate drive current can be found from Equation 6.

8.3.9 Prebias Start-up

The TPS40197 contains a unique circuit to prevent current from being pulled from the output during startup in the condition the output is prebiased. When the soft start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage [V_{FB}]), the controller slowly activates synchronous rectification by starting the first LDRV pulse with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensures that the output voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation with minimal disturbance to the output voltage. The amount of time from the start of switching until the low-side MOSFET is turned on for the full (1-D) interval is defined by 32 clock cycles.

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8.3.10 Drivers

The drivers for the external HDRV and LDRV MOSFETs are capable of driving a gate-to-source voltage of 5 V. The LDRV driver switches between BP and GND, while HDRV driver is referenced to SW and switches between BOOT and SW. The drivers have non-overlapping timing that is governed by an adaptive delay circuit to minimize body diode conduction in the synchronous rectifier. The drivers are capable of driving MOSFETS that are appropriate for a 15-A converter.

8.3.11 Power Good

The TPS40197 provides an indication that output power is good for the converter. This is an open drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- V_{FB} is more than 10% from the reference voltage based on VID codes
- soft-start is active
- an undervoltage condition exists for the device
- a short-circuit condition has been detected
- die temperature is over (140°C)

NOTE

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built in resistor connected from drain to gate on the PGOOD pull down device makes the PGOOD pin look approximately like a diode to GND.

8.3.12 Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 140°C, the PWM and the oscillator are turned off and HDRV and LDRV are driven low, turning off both FETs. When the junction cools to the required level (120°C nominal), the PWM initiates soft-start as during a normal power-up cycle.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS40197 is a synchronous buck controller that operates from 4.5-V to 14-V input supply nominally. The controller implements voltage-mode control architecture with the switching frequency fixed at 520 kHz. The higher switching frequency facilitates the use of smaller inductor and output capacitors, thereby providing a compact power-supply solution.

9.2 Typical Application

The schematic for the design is shown in Figure 17 and the list of materials is shown in Table 3.

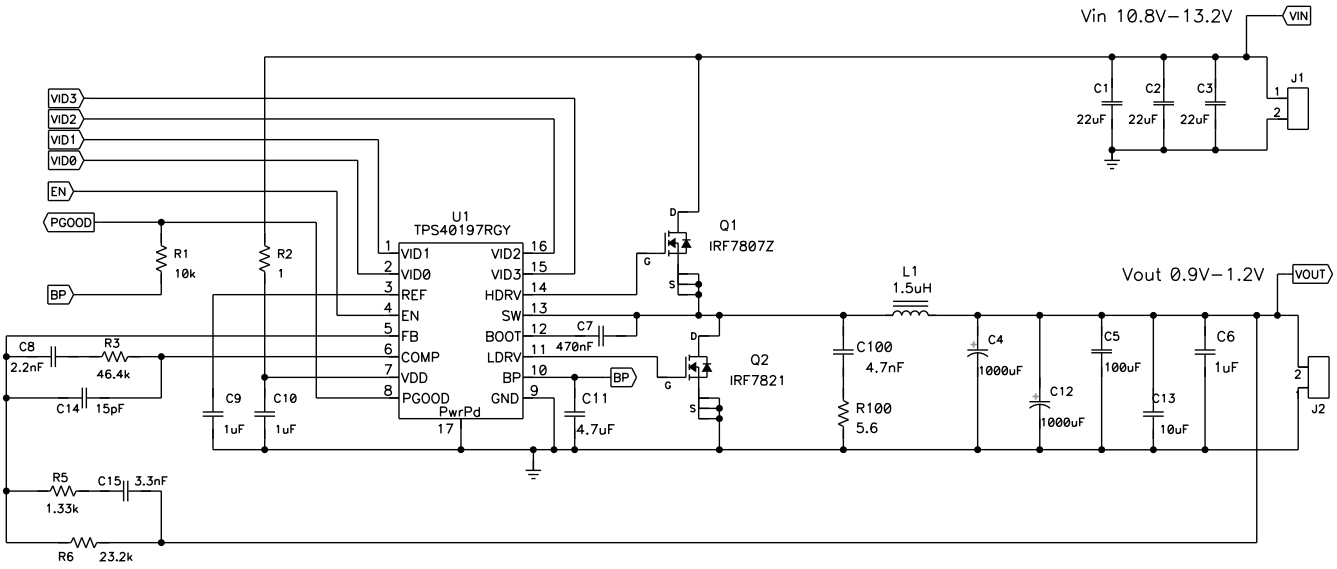


Figure 17. TPS40197 Sample Schematic

Typical Application (continued)

9.2.1 Design Requirements

Table 3. Design Example List Of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	MFR	PART NUMBER
C1, C2, C3	3	Capacitor, ceramic, 16 V, X7R, 20%, 22 μF, 1210	TDK	C3225X7R1C226K
C4, C12	2	Capacitor, POSCAP, 2.5 V, 20%, 1 mF, 5 mΩ, D4D	Sanyo	2R5TPD1000M5
C5	1	Capacitor, ceramic, 6.3 V, X5R, 20%, 100 μF, 1210	TDK	C3225X5R0J107K
C6, C9, C10	3	Capacitor, ceramic, 16 V, X7R, 20%, 1 μF, 0603	Std	Std
C7	1	Capacitor, ceramic, 10 V, X5R, 20%, 470 nF, 0603	Std	Std
C8	1	Capacitor, ceramic, 50 V, NPO, 10%, 2.2 nF, 0603	Std	Std
C11	1	Capacitor, ceramic, 6.3 V, X5R, 20%, 4.7 μF, 0603	TDK	C1608X5R0J475K
C13	1	Capacitor, ceramic, 6.3 V, X5R, 20%, 10 μF, 0603	TDK	C1608X5R0J106K
C14	1	Capacitor, ceramic, 50 V, NPO, 10%, 15 pF, 0603	Std	Std
C15	1	Capacitor, ceramic, 50 V, X7R, 20%, 3.3 nF, 0603	Std	Std
C100	1	Capacitor, ceramic, 50 V, X7R, 20%, 4.7 nF, 0603	Std	Std
L1	1	Inductor, SMT, 27 A, 1.5 μH, 2.5 mΩ, 0.508 x 0.520	Vishay	IHLP5050FDER1R5M01
Q1	1	MOSFET, N-channel, 30 V, 11A, 13.8 mΩ, SO-8	IR	IRF7807Z
Q2	1	MOSFET, N-channel, 30 V, 13.6 A, 9.1 mΩ, SO-8	IR	IRF7821
R1	1	Resistor, chip, 1/16 W, 5%, 10 kΩ, 0603	Std	Std
R2	1	Resistor, chip, 1/16 W, 5%, 1 Ω, 0603	Std	Std
R3	1	Resistor, chip, 1/16 W, 1%, 46.4 kΩ, 0603	Std	Std
R5	1	Resistor, chip, 1/16 W, 1%, 1.33 kΩ, 0603	Std	Std
R6	1	Resistor, chip, 1/16 W, 1%, 23.2 kΩ, 0603	Std	Std
R100	1	Resistor, chip, 1/4 W, 5%, 5.6 Ω, 1206	Std	Std
U1	1	IC, synchronous buck controller with 4-bit VID interface for Smart-Reflex DSPs, QFN-16	TI	TPS40197RGY

9.2.2 Detailed Design Procedure

For regulator stability, a 1-μF capacitor is required to be connected from BP to GND. In some applications using higher gate charge MOSFETs, a larger capacitor is required for noise suppression. For a total gate charge of both the high-side and low-side MOSFETs greater than 20 nC, a 2.2-μF or larger capacitor is recommended.

$$I_G = f_{SW} \times \left(Q_{G(high)} + Q_{G(low)}\right) \quad (6)$$

where

- I_G is the required gate drive current
- f_{SW} is the switching frequency
- $Q_{G(high)}$ is the gate charge requirement for the high-side FET when V_{GS} = 5 V
- $Q_{G(low)}$ is the gate charge requirement for the low-side FET when V_{GS} = 5 V

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Devices

The following devices have characteristics similar to the TPS40197 and may be of interest.

TI LITERATURE NUMBER	DEVICE	DESCRIPTION
SLUS719	TPS40192	4.5 V to 18 V Input Synchronous Buck Controller with Power Good
	TPS40193	

10.2.2 Related Documentation

TI LITERATURE NUMBER	DOCUMENT TYPE	DESCRIPTION
SPRAAW7	Application Report	TMS320C6474 Hardware Design Guide
SLVA057	Application Report	Understanding Buck Power Stages in Switchmode Power Supplies
SLUP206	Seminar Series	Under the Hood of Low-Voltage DC/DC Converters, SEM-1500, 2003
SLUP173	Seminar Series	Designing Stable Control Loops, SEM-1400, 2001
SLMA002	Application Report	PowerPAD™ Thermally Enhanced Package
SLMA004	Application Report	PowerPAD™ Made Easy

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.5 Trademarks

Smart-Reflex, PowerPAD, E2E are trademarks of Texas Instruments.

10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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10.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40197RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40197	Samples
TPS40197RGYT	ACTIVE	VQFN	RGY	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40197	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

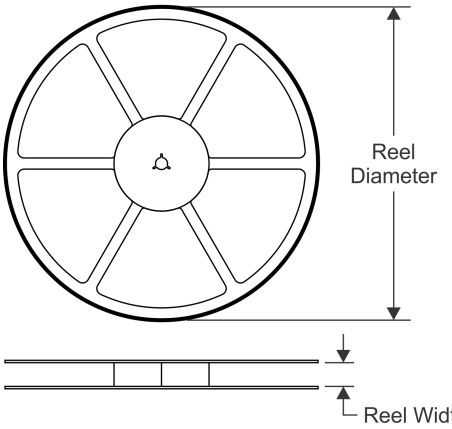
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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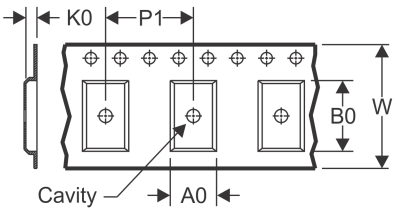
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

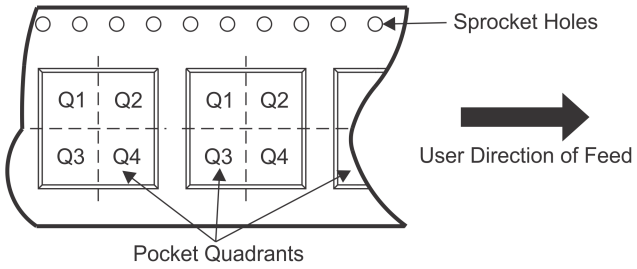


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

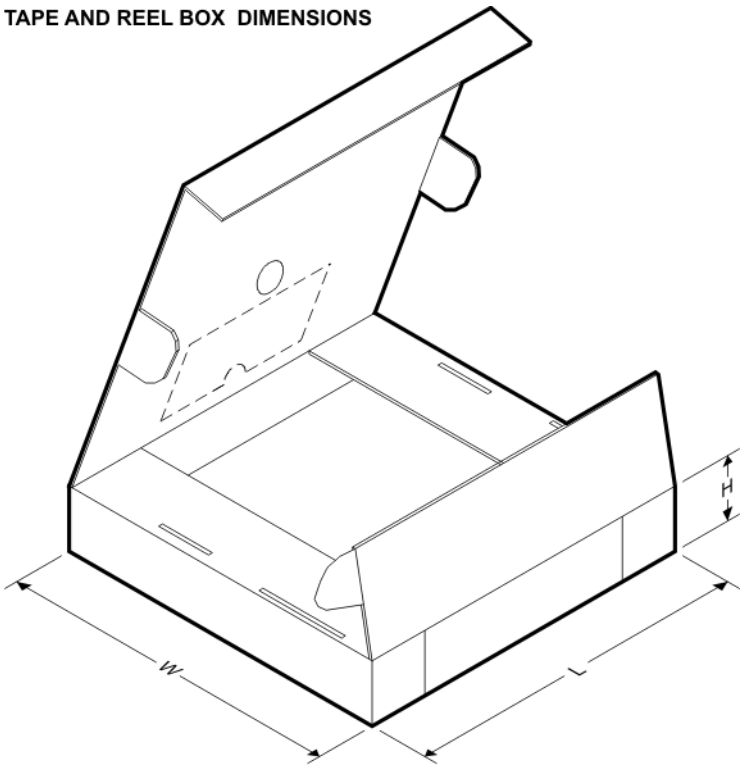
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40197RGYR	VQFN	RGY	16	3000	330.0	12.4	3.71	4.21	1.11	8.0	12.0	Q1
TPS40197RGYT	VQFN	RGY	16	250	180.0	12.5	3.71	4.21	1.11	8.0	12.0	Q1

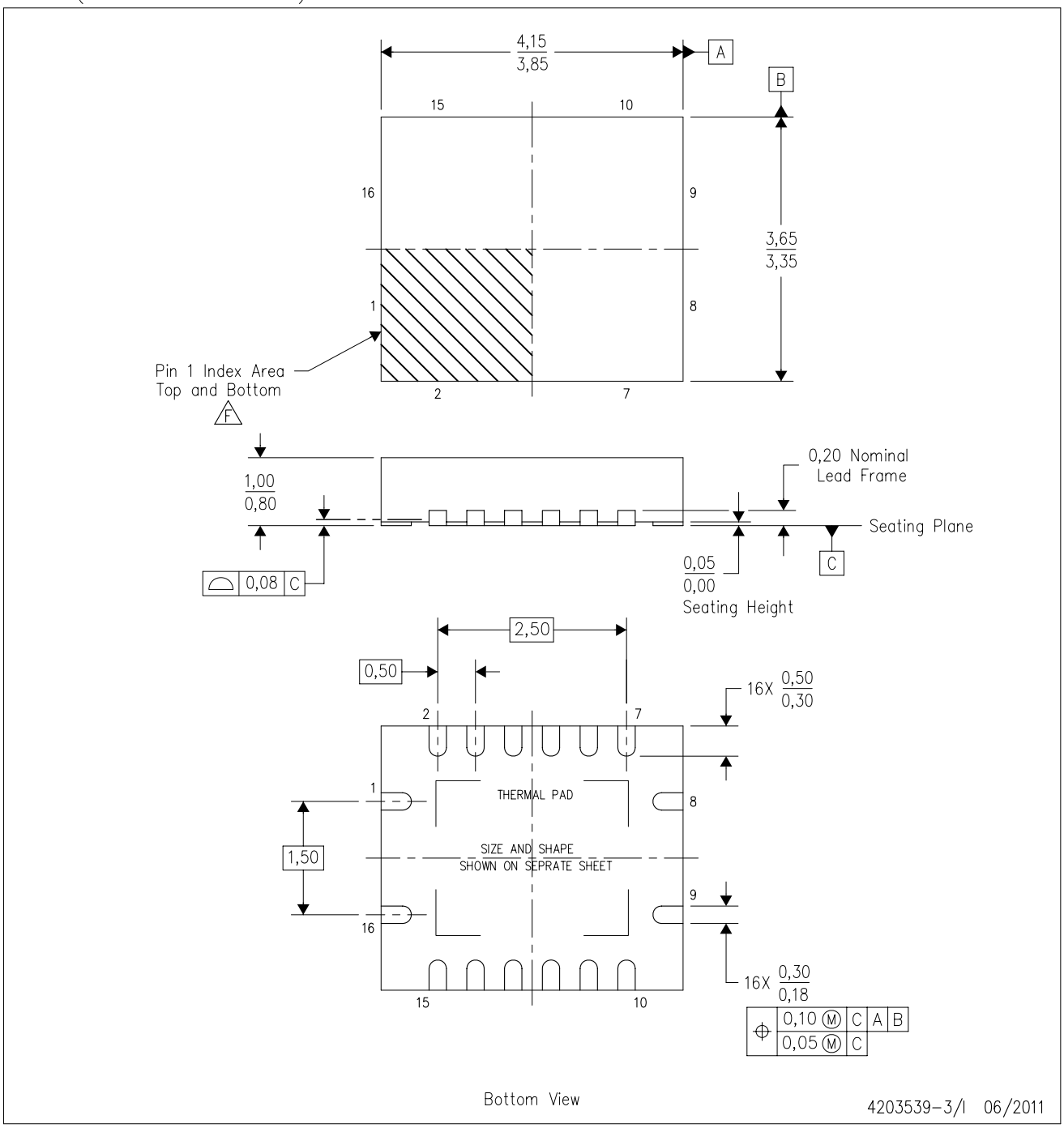
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40197RGYR	VQFN	RGY	16	3000	338.0	355.0	50.0
TPS40197RGYT	VQFN	RGY	16	250	338.0	355.0	50.0

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

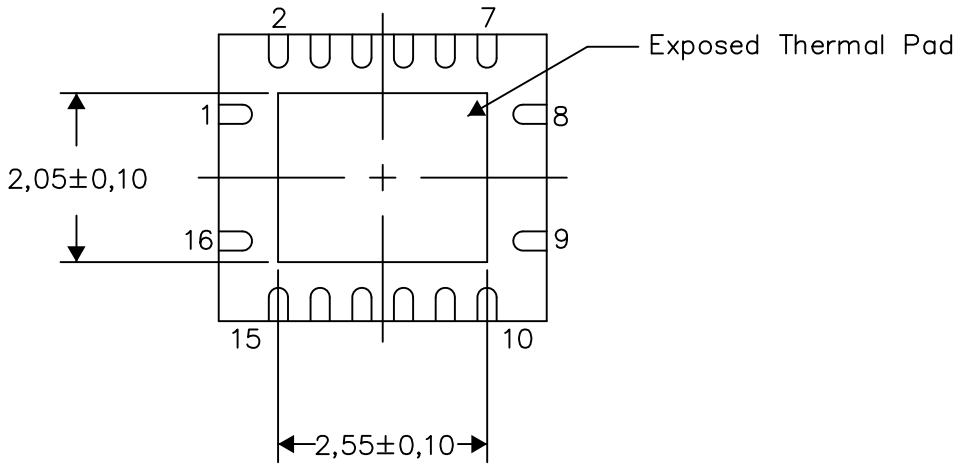
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



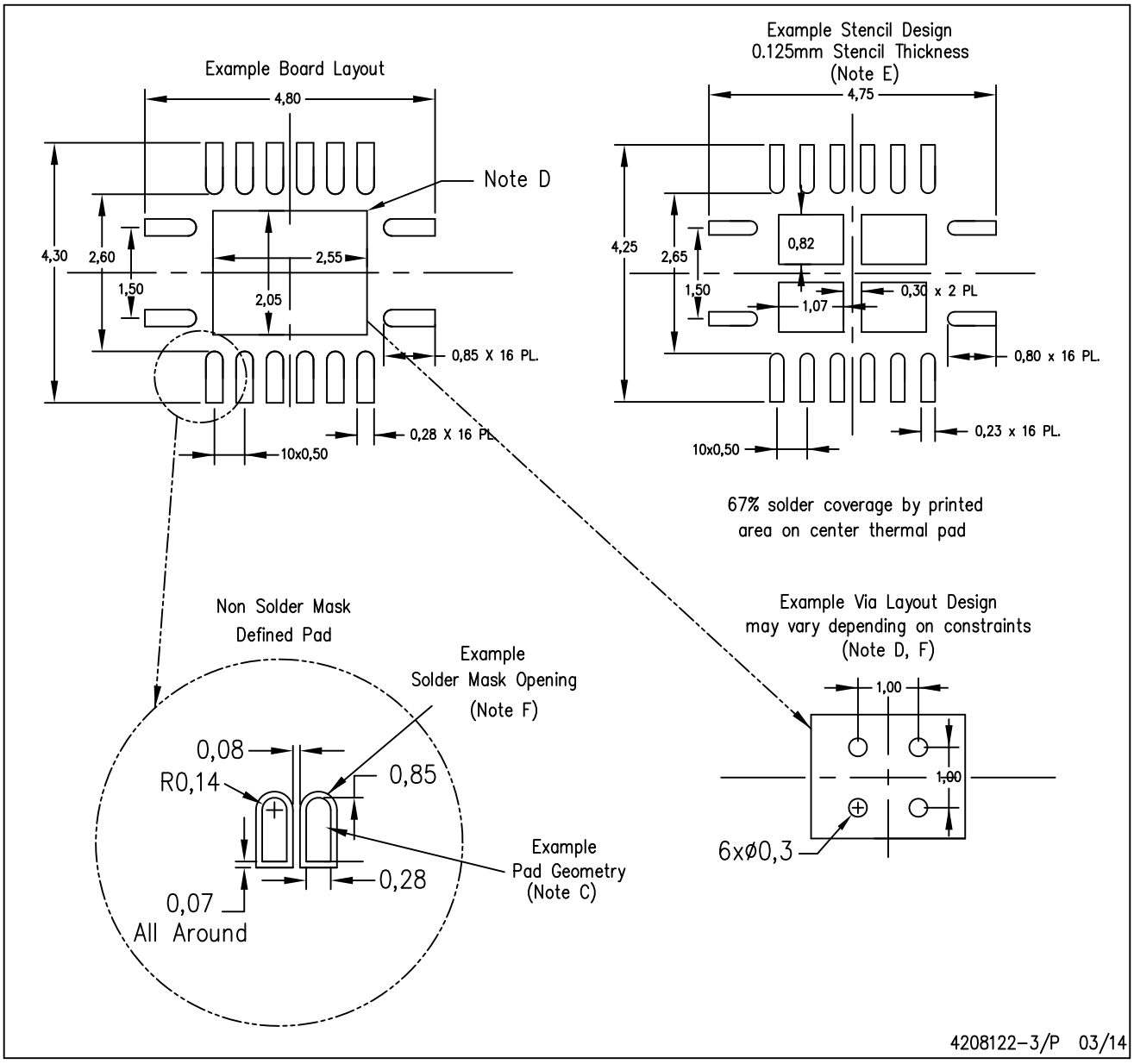
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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