Click here for production status of specific part numbers.

MAX17687

4.5V to 60V Input, Ultra-Small, High-Efficiency, Iso-Buck DC-DC Converter

General Description

The Rainier series of isolated DC-DC products enable small, efficient solutions with a lower BOM. The MAX17687 is a high-voltage, high-efficiency, iso-buck DC-DC converter designed to provide isolated power up to 10W. The device operates over a wide 4.5V to 60V input voltage range and uses primary-side feedback to regulate the output voltage. It delivers primary peak current up to 3.2A and regulates primary output voltage to within ±1.2%.

The device features peak-current-mode control with pulse-width modulation (PWM) scheme. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplify the layout.

A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input-voltage level. An open-drain $\overline{\text{RESET}}$ pin provides a delayed power-good signal to the system upon achieving successful regulation of the primary output voltage.

The device operates from -40°C to +125°C and is available in a compact 20-pin (4mm x 4mm) TQFN package. Simulation models are available.

Applications

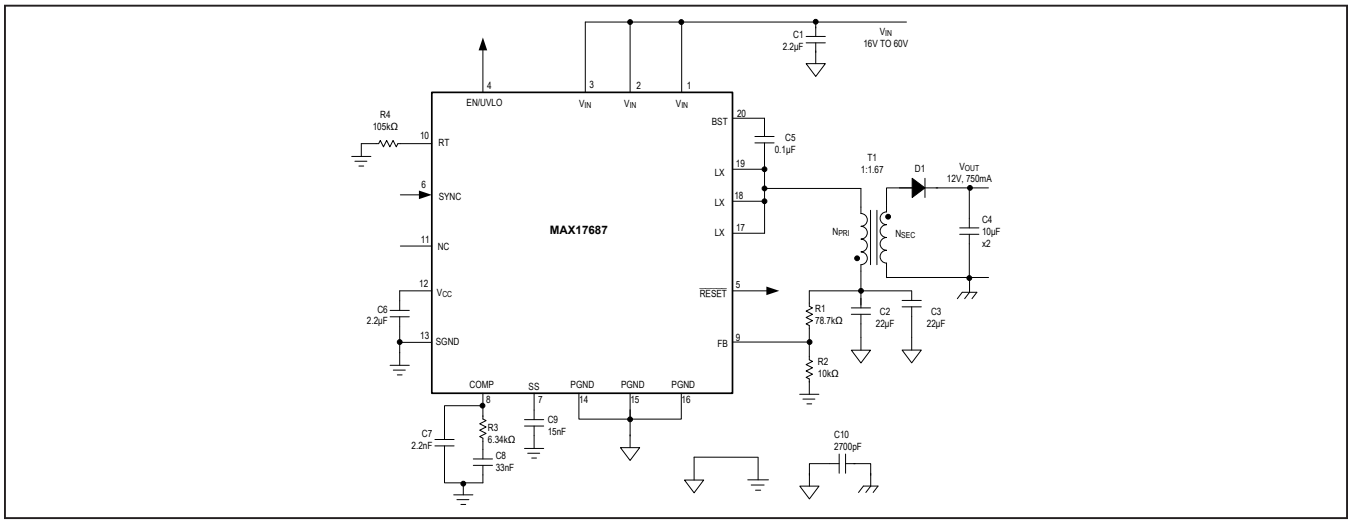
- Industrial Process Control
- Communication Hub in Smart Meters
- Isolated Power Supplies in Medical Equipment
- Floating Power Supply Generation

Benefits and Features

- Eliminates External Components and Reduces Total Cost
  - Synchronous Primary Operation for High Efficiency and Reduced Cost
  - All-Ceramic Capacitors, Ultra-Compact Layout
- Supports Numerous Isolated DC-DC Applications
  - Wide 4.5V to 60V Input Voltage Range
  - Delivers up to 3.2A Peak Current
  - 100kHz to 500kHz Adjustable Frequency with External Synchronization
  - Available in a 20-Pin, 4mm x 4mm TQFN Package
- Reduces Power Dissipation
  - Peak Efficiency > 90%
  - Shutdown Current = 2.8µA (typ)
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Current Limit, Sink Current Limit, and Auto-Retry Startup
  - Programmable EN/UVLO Threshold
  - Adjustable Soft-Start
  - -40°C to +125°C Ambient Operating Temperature Range
  - -40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



maxim integrated™

Absolute Maximum Ratings

V_{IN} to PGND .....-0.3V to +65V
EN/UVLO to PGND .....-0.3V to +65V
LX to PGND.....-0.3V to (V_{IN} + 0.3V)
BST to PGND .....-0.3V to (LX + 5V)
BST to LX.....-0.3V to +6.5V
BST to V_{CC} .....-0.3V to +65V
V_{CC}, SYNC, $\overline{RESET}$, COMP, SS, RT to SGND
.....-0.3V to +6.5V
FB to SGND .....-0.3V to +1.5V
SGND to PGND.....-0.3V to +0.3V
LX Total RMS Current .....±4A
Output Short-Circuit Duration.....Continuous
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Junction temperature greater than +125°C degrades operating lifetimes.

Package Information

PACKAGE TYPE: 20 TQFN	
Package Code	T2044+4
Outline Number	**21-0139**
Land Pattern Number	**90-0409**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Juntion to Ambient (θ_{JA})	33°C/W
Juntion to Case (θ_{JC})	2°C/W
Continuous Power Dissipation (T_A = +70°C) (derate 30.3mW/°C above +70°C) (multilayer board)	2424.2mW

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{IN} = V_{EN} = 24V, R_{RT} = 82.5kΩ (250kHz), V_{SGND} = V_{PGND} = V_{SYNC} = 0V, C_{VCC} = 2.2µF, V_{FB} = 1V, $V_{BST\ to\ LX}$ = 5V, LX = $\overline{RESET}$ = SS = COMP = unconnected. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		60	V
Input Quiescent Current	I_{IN-SH}	V_{EN} = 0V, shutdown mode		2.8	4.5	µA
Input Quiescent Current	I_Q			1.16	1.8	mA
Input Switching Current	I_{SW}	V_{FB} = 0.8V		6		mA
ENABLE/UVLO (EN/UVLO)						
EN Threshold	V_{ENR}	V_{EN} rising	1.19	1.215	1.26	V
	V_{ENF}	V_{EN} falling	1.068	1.09	1.131	
	$V_{EN-TRUESD}$	V_{EN} falling, true shutdown		0.8		
EN Input Leakage Current	I_{EN}	V_{EN} = V_{IN} = 60V, T_A = +25°C	-50	0	+50	nA
LDO						
V_{CC} Output Voltage Range	V_{CC}	6V < V_{IN} < 60V, I_{VCC} = 1mA	4.75	5	5.25	V
		1mA < I_{VCC} < 25mA				
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 6V	26.5	55	100	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 20mA	4.2			V
V_{CC} UVLO	V_{CC-UVR}	V_{CC} rising	4.05	4.2	4.3	V
	V_{CC-UVF}	V_{CC} falling	3.65	3.8	3.9	
POWER MOSFETs						
High-Side NMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A (sourcing)		165	325	mΩ
Low-Side NMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A (sinking)		80	150	mΩ
LX Leakage Current	I_{LX_LKG}	T_A = +25°C, V_{LX} = (V_{PGND} + 1V) to (V_{IN} – 1V)	-2		+2	µA
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0.5V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB_REG}		0.89	0.9	0.91	V
FB Input Bias Current	I_{FB}	V_{FB} = 1V, T_A = +25°C	-50		+50	nA
CURRENT LIMIT						
Peak Current Limit Threshold	$I_{PEAK-LIMIT}$		3.2	3.7	4.3	A
Runaway Current Limit Threshold	$I_{RUNAWAY-LIMIT}$		3.7	4.3	5	A
Valley Current Limit Threshold	$I_{SINK-LIMIT}$		5	6.5		A

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 24V, R_{RT} = 82.5kΩ (250kHz), V_{SGND} = V_{PGND} = V_{SYNC} = 0V, C_{VCC} = 2.2µF, V_{FB} = 1V, $V_{BST\ to\ LX}$ = 5V, LX = $\overline{RESET}$ = SS = COMP = unconnected. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RT AND SYNC						
Switching Frequency	f_{SW}	R_{RT} = OPEN		250		kHz
		R_{RT} = 210kΩ		100		
		R_{RT} = 102kΩ		200		
		R_{RT} = 82.5kΩ		250		
		R_{RT} = 40.2kΩ		500		
SYNC Frequency Capture Range		f_{SW} set by R_{RT}	1.1 x f_{SW}		1.4 x f_{SW}	kHz
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	
Feedback Undervoltage Trip Level to Cause Hiccup	$V_{FB-HICF}$	V_{SS} > 0.95V (soft-start is done)	0.56	0.58	0.65	V
HICCUP Timeout		(Note 2)		32768		Cycles
Minimum On-Time	t_{ON_MIN}			330	425	ns
Minimum Off-Time	t_{OFF_MIN}		140		160	ns
LX Dead Time		(Note 3)		5		ns
Number of ZX Events to Trigger HICCUP				16		Cycles
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			0.4	V
$\overline{RESET}$ Output Leakage Current High		T_A = T_J = 25°C			0.1	µA
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling	90.5	92	94.6	%V_{FB-REG}
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising	93.8	95	97.8	%V_{FB-REG}
$\overline{RESET}$ Delay After FB Reaches 95% Regulation		V_{FB} rising		1024		Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		165		°C
Thermal Shutdown Hysteresis				10		°C

Note 1: All limits are 100% tested at +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

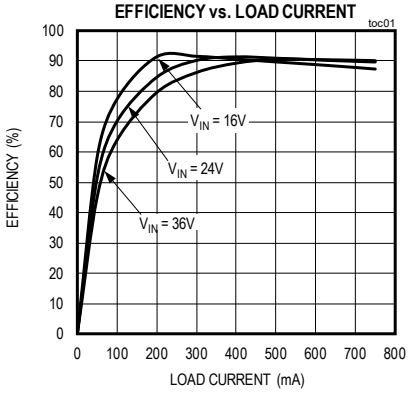
Note 2: See the *Overcurrent Protection/Hiccup Mode* section for more details.

Note 3: Guaranteed by design, not production tested.

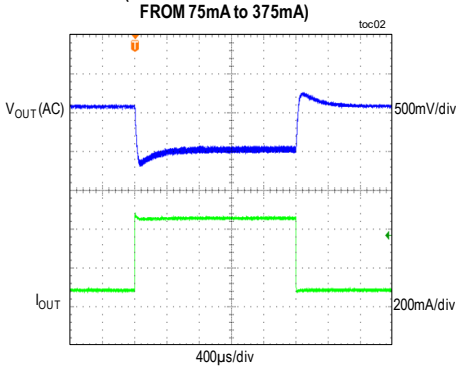
Typical Operating Characteristics

(V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 2.2µF, V_{EN} = 1.5V, C_{SS} = 15000pF, $\overline{RESET}$ = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

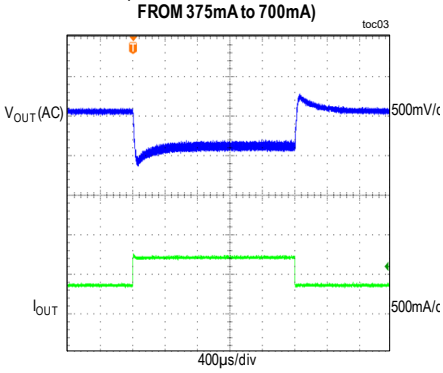
EFFICIENCY vs. LOAD CURRENT



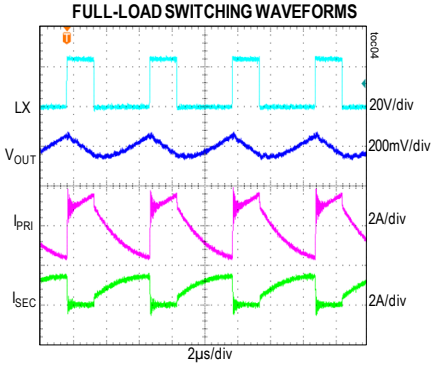
LOAD TRANSIENT RESPONSE, (LOAD CURRENT STEPPED FROM 75mA to 375mA)



LOAD TRANSIENT RESPONSE (LOAD CURRENT STEPPED FROM 375mA to 700mA)



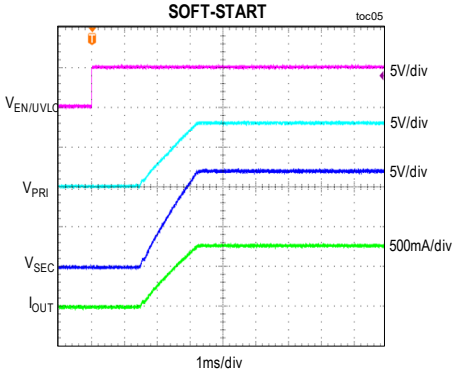
FULL-LOAD SWITCHING WAVEFORMS



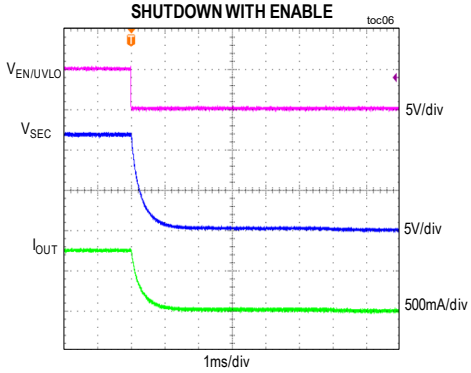
Typical Operating Characteristics (continued)

(V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 2.2µF, V_{EN} = 1.5V, C_{SS} = 15000pF, $\overline{RESET}$ = unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

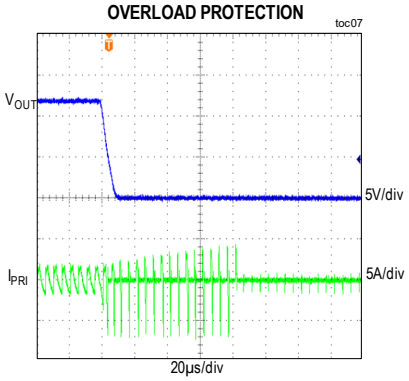
SOFT-START



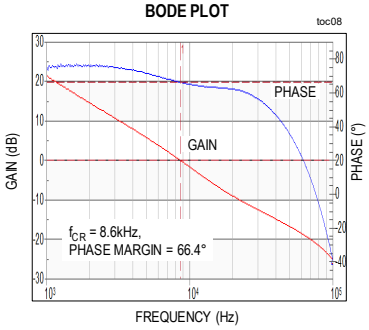
SHUTDOWN WITH ENABLE



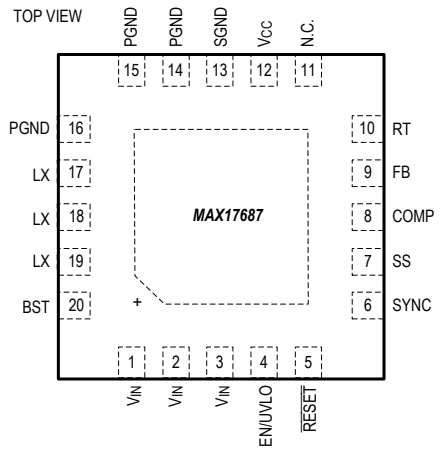
OVERLOAD PROTECTION



BODE PLOT



Pin Configuration

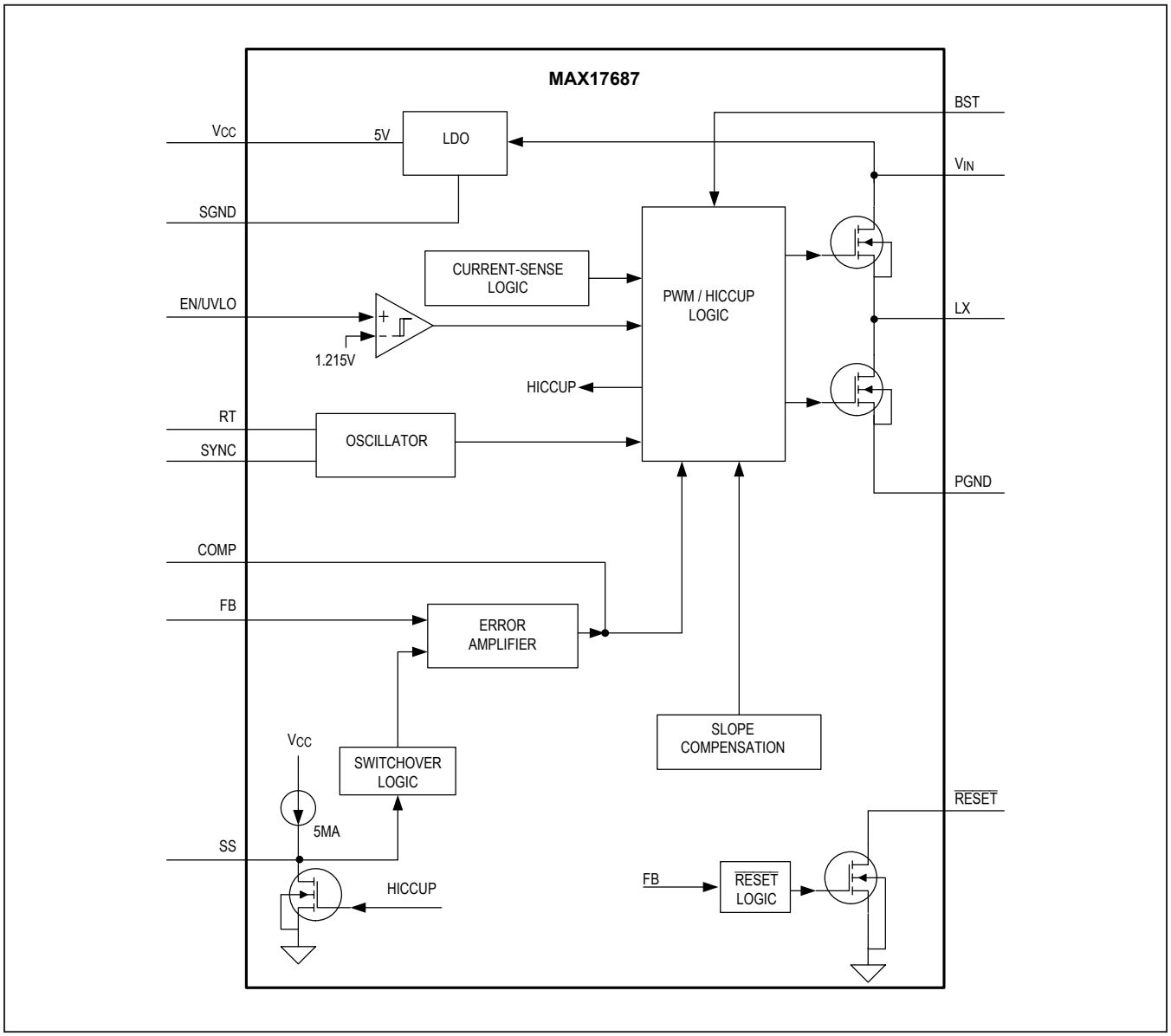


20-PIN TQFN 4mm × 4mm
*EXPOSED PAD (CONNECT TO GROUND).

Pin Description

PIN	NAME	FUNCTION
1-3	V_{IN}	Power-Supply Input. 4.5V to 60V input supply range. Connect the V_{IN} pins together. Decouple to PGND with a 2.2µF capacitor; place the capacitor close to the V_{IN} and PGND pins. Refer to the MAX17687EV kit data sheet for a layout example.
4	EN/UVLO	Enable/Undervoltage Lockout Input. Drive EN/UVLO high to enable the output voltage. Connect to the center of resistive divider between V_{IN} and GND to set the input voltage (undervoltage threshold) at which the device turns on. Pull up to V_{IN} for always on.
5	$\overline{RESET}$	Open-Drain $\overline{RESET}$ Output. $\overline{RESET}$ output is driven low if FB drops below 92.5% of its set value. $\overline{RESET}$ goes high 1024 clock cycles after FB rises above 95.5% of its set value.
6	SYNC	The device can be synchronized to an external clock using this pin. See the External Frequency Synchronization section for more details.
7	SS	Soft-Start Input. Connect a capacitor from SS to GND to set the soft-start time.
8	COMP	Compensation Input. Connect an RC network from COMP to GND
9	FB	Feedback Input. Connect FB to the center of resistive divider between VOUT and GND. See the *Adjusting Output Voltage* section for more details.
10	RT	Connect a resistor from RT to SGND to set the regulator's switching frequency. Leave RT open for the default 250kHz frequency. See the *Setting the Switching Frequency (RT)* section for more details.
11	NC	No Connection. Do not connect any voltage to this pin.
12	V_{CC}	5V LDO Output. Bypass V_{CC} with 2.2µF ceramic capacitance to GND.
13	SGND	Analog Ground.
14-16	PGND	Power Ground. Connect PGND externally to the power ground plane. Connect GND and PGND pins together at the ground return path of the V_{CC} bypass capacitor.
17-19	LX	Switching Node. Connect LX to the switching side of the transformer. LX is high impedance when the device is in shutdown mode.
20	BST	Boost Flying Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX.
	EP	Exposed pad. Connect to the SGND pin. Connect to a large copper plane below the IC to improve heat dissipation capability. Add thermal vias below the exposed pad.

Functional (or Block) Diagram



Detailed Description

The MAX17687 a high-voltage, high-efficiency, Iso-Buck DC-DC converter designed to operate over a wide 4.5V to 60V input voltage range. It delivers primary peak current up to 3.2A and regulates primary output voltage to within ±1.2% over -40°C to +125°C.

The device features peak-current-mode control with pulse-width modulation (PWM) scheme. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplify the layout.

A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input-voltage level. An open-drain $\overline{RESET}$ pin provides a delayed power-good signal to the system upon achieving successful regulation of the primary output voltage.

The device operates from -40°C to +125°C and is available in a compact 20-pin (4mm x 4mm) TQFN package.

Linear Regulator (V_{CC})

An internal linear regulator (V_{CC}) provides a 5V nominal supply to power the internal blocks and the low-side MOSFET driver. The output of the V_{CC} linear regulator should be bypassed with a 2.2µF ceramic capacitor to GND. The device employs an undervoltage-lockout circuit that disables the internal linear regulator when V_{CC} falls below 3.8V (typ). The internal V_{CC} linear regulator can source up to 20mA to supply the device and to power the low-side gate driver.

Setting the Switching Frequency (RT)

The switching frequency of the device can be programmed from 100kHz to 500kHz by using a resistor connected from the RT pin to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} \cong \frac{21 \times 10^3}{f_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the R_{RT} pin open causes the device to operate at the default switching frequency of 250 kHz. See Table 1 for R_{RT} resistor values for a few common switching frequencies.

Table 1. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
100	210
200	102
250	82.5
500	40.2

External Frequency Synchronization (SYNC)

The internal oscillator of the device can be synchronized to an external clock signal on the SYNC pin. The external synchronization clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the frequency programmed by the R_{RT} resistor. The minimum external clock pulse-width high should be greater than 50ns. See the *RT AND SYNC* section in the *Electrical Characteristics* table for details.

Enable Input (EN/UVLO) and Soft-Start (SS)

When EN/UVLO voltage increases above 1.215V (typ), the device initiates a soft-start sequence and duration of the soft-start depends on the value of the capacitor connected from SS to GND. A 5µA current source charges the capacitor and ramps up the SS pin voltage. The SS pin voltage is used as reference for the internal error amplifier. Such a reference ramp up allows the output voltage to increase monotonically from zero to the final set value independent of the load current.

EN/UVLO can be used as an input voltage UVLO-adjustment input. An external voltage divider between IN and EN/UVLO to GND adjusts the input voltage at which the device turns on or turns off. See the *Setting the Input Undervoltage Lockout Level* section for details. If input UVLO programming is not desired, connect EN/UVLO to VIN (see the *Electrical Characteristics* table for EN/UVLO rising and falling-threshold voltages). Driving EN/UVLO low disables the high-side FET and part enters into primary output discharge mode (explained in the *Overcurrent Protection/ Hiccup Mode* section). Once hiccup timeout period expires, other internal circuitry is disabled and SS capacitor is discharged with an internal pull-down resistor. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the signal source output and the EN/UVLO pin, to reduce voltage ringing on the line.

Overcurrent Protection/Hiccup Mode

The MAX17687 enters hiccup mode, either on one occurrence of the runaway current limit, or when the feedback voltage drops to 0.58V (typ) after the soft-start is completed, or when EN/UVLO < 1.09V with V_{CC} > 3.8V or when 16 consecutive negative current limit events occur. When the hiccup mode is triggered, the converter enters a hiccup timeout period of 32,768 clock cycles. During this period, the high side switch is kept off and the low side switch is turned on each cycle with a maximum possible duty cycle of 98% till the negative current limit reaches 0.6A. This mode of operation effectively produces a negative current in the primary capacitor and discharges the primary voltage towards zero. Once the hiccup timeout period expires, soft-start is attempted again. For cases where the amount of output capacitance is such that it is discharged to zero within one hiccup timeout period, the MAX17687 executes a normal soft-start operation upon exit from the Hiccup timeout period. For cases, where the capacitor is sized such that it does not discharge to zero in one hiccup timeout period, during the next soft-start attempt the converter may re-enter the hiccup time period due to one of the event which triggers hiccup mode. Eventually the primary capacitor is completely discharged and the smooth output voltage recovery is ensured.

$\overline{\text{RESET}}$ Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the primary output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pull-up resistor. $\overline{\text{RESET}}$ can sink 2mA of current while low. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the primary output increases above 95.5% of the nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the primary output voltage drops to below 92.5% of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown. $\overline{\text{RESET}}$ is valid when the device is enabled and V_{IN} is above 4.5V.

Thermal-Shutdown Protection

Thermal-shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown in normal operation.

Applications Information

Operation of the Iso-Buck Converter

Iso-buck is a synchronous buck converter based topology, useful for generating isolated outputs at low power level without using an optocoupler. Figure 1 shows basic circuit of an Iso-buck converter, consists of a Half bridge transformer driver and secondary side filter.

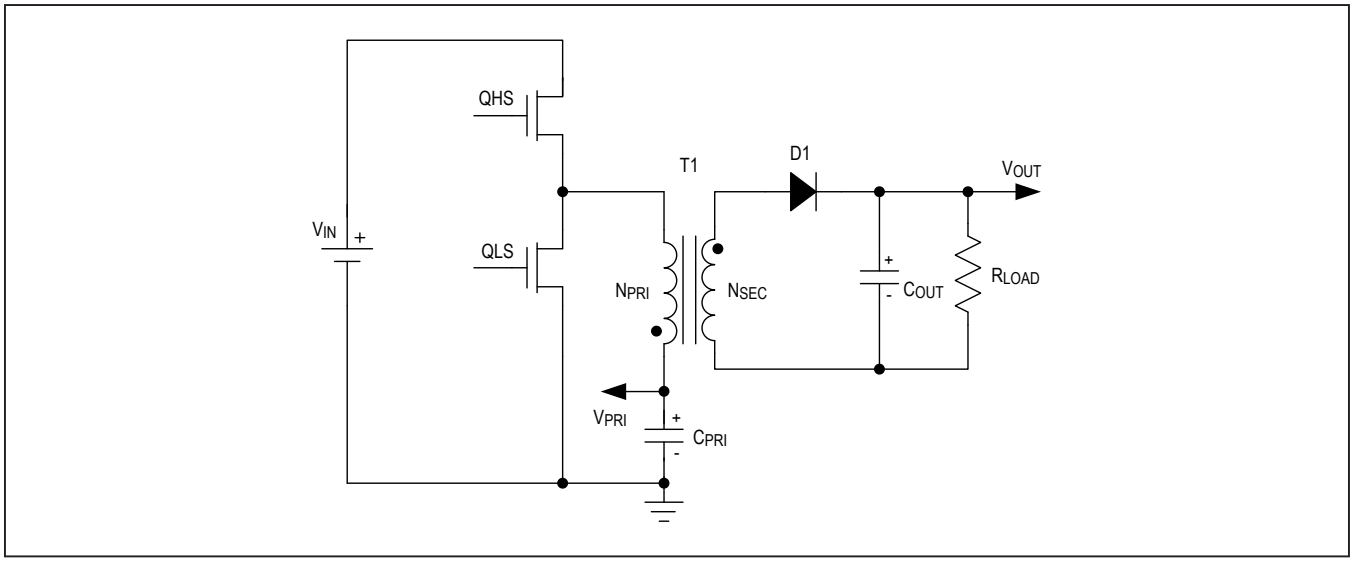


Figure 1. Iso-Buck Topology

Figure 2 shows the equivalent circuit when high side switch (QHS) is on. During this time, primary current ramps up and stores energy in transformer magnetizing inductance LPRI and primary capacitor C_{PRI}. Secondary side diode is reverse-biased by (V_{IN} - V_{PRI}) voltage and load current is supplied by secondary filter capacitor C_{OUT}.

Figure 3 shows the equivalent circuit when low side switch (QLS) is on. During this time, secondary diode gets forward biased by primary output voltage V_{PRI}. Primary current ramps down and releases stored energy in transformer magnetizing inductance and primary capacitor to the load. Operating waveforms of the converter are shown in Figure 4. Neglecting diode drop VD and transformer resistances, output voltage V_{OUT} is proportional to the primary output voltage V_{PRI} and is regulated by MAX17687 current mode control loop.

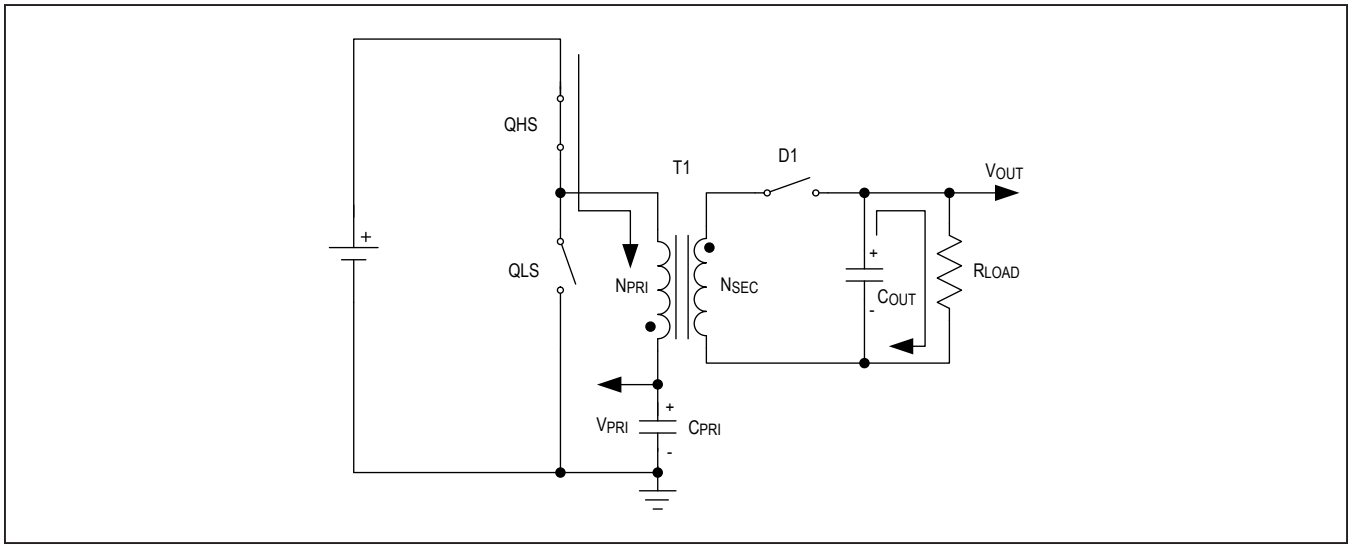


Figure 2. On Period Equivalent Circuit

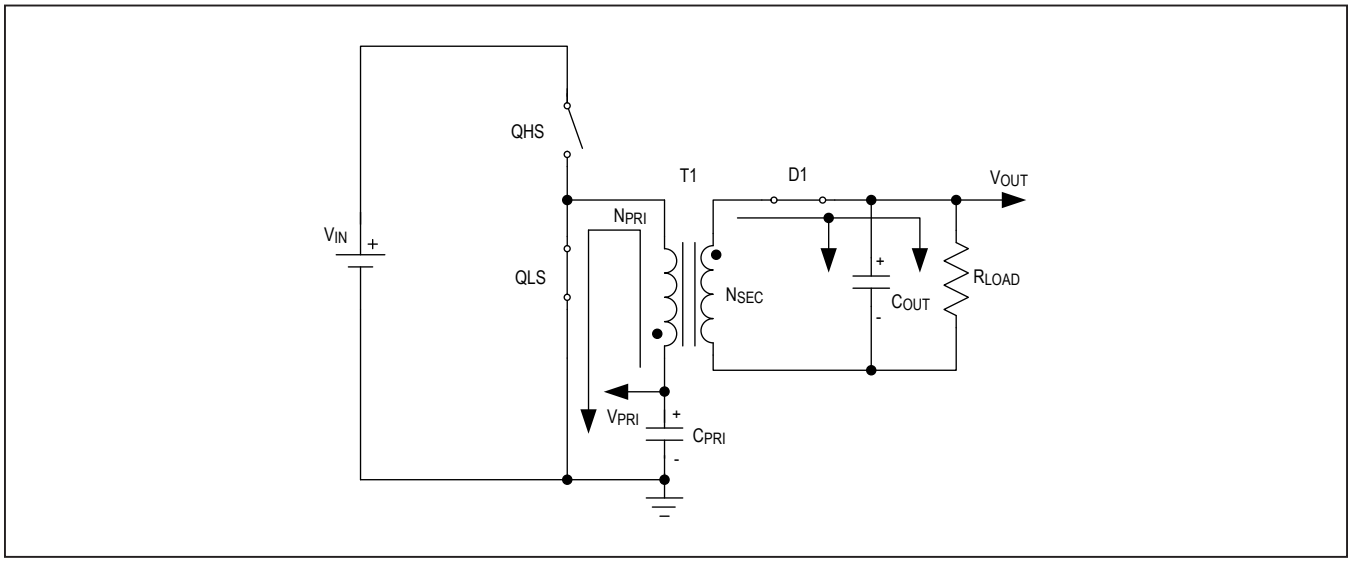


Figure 3. Off Period Equivalent Circuit

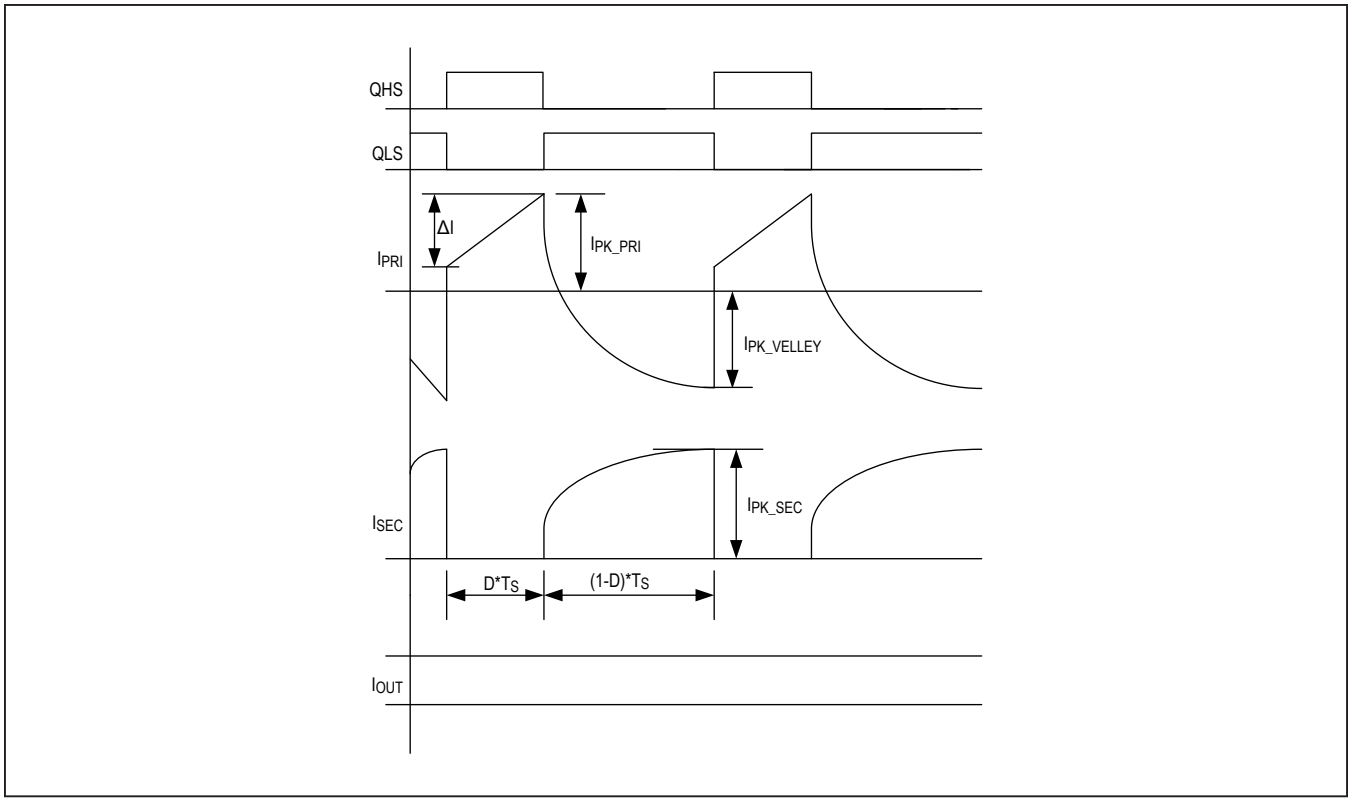


Figure 4. Iso-Buck Operating Waveforms

Primary Output Voltage Selection

Primary output voltage is regulated by the MAX17687 control loop. The primary output voltage can be calculated by using the equation:

$$V_{PRI} = D_{MAX} \times V_{IN_MIN}$$

where D_{MAX} is the maximum duty cycle of the converter and V_{IN_MIN} is the minimum input voltage. Maximum duty cycle should be in the range of 0.4 to 0.6 for ideal iso-buck operation.

Adjusting Primary Output Voltage

Set the primary output voltage by connecting a resistor-divider from primary output to FB to GND (see Figure 5). Choose R2 in the range of 10kΩ to 100kΩ and calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{PRI}}{0.9} - 1 \right)$$

Turns Ratio Selection

Neglecting parasitic resistances, Iso-buck output voltage V_{OUT} is proportional to the primary output voltage V_{PRI}. Select the turns ratio (K) using the equation:

$$\frac{N_{SEC}}{N_{PRI}} = \frac{V_{OUT} + V_D}{V_{PRI}}$$

$$K = \frac{N_{SEC}}{N_{PRI}}$$

where, V_D is the diode forward voltage drop.

Turns ratio can be adjusted to match with the readily available off-the-shelf transformer turns ratio by adjusting the primary output voltage.

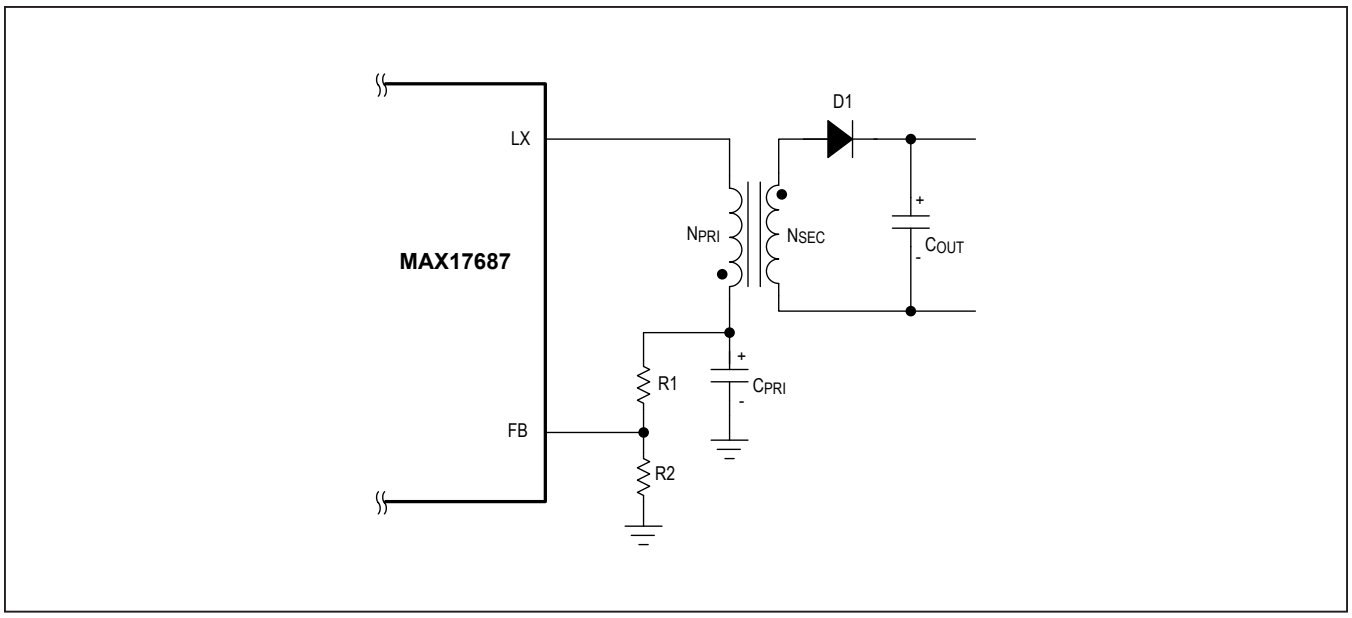


Figure 5. Adjusting Primary Output Voltage

Primary Inductance Selection

Primary inductance value determines ripple current in the transformer. Calculate required primary inductance using the equation:

$$L_{PRI} = \frac{V_{PRI}}{f_{SW}}$$

where V_{PRI} and f_{SW} are nominal values.

Calculate the primary ripple current using the equation:

$$\Delta I = \frac{V_{PRI} \times \left(1 - \frac{V_{PRI}}{V_{IN}}\right)}{f_{SW} \times L_{PRI}}$$

where:

L_{PRI} = Primary inductance in H

f_{SW} = Switching frequency in Hz

V_{PRI} = Primary output voltage

V_{IN} = Input voltage.

Winding Peak and RMS Currents

Windings peak and RMS current ratings should be specified for selecting the Iso-buck transformer.

Primary and secondary winding peak currents are given by the equations:

$$I_{PK_PRI} = (I_{OUT} \times K) + \left(\frac{\Delta I}{2}\right)$$

$$I_{PK_SEC} = \frac{2 \times I_{OUT}}{(1 - D)}$$

$$D = \frac{V_{PRI}}{V_{IN}}$$

where I_{OUT} is load current, K is turns ratio and D is duty cycle.

Primary RMS current is sum of the high-side and low-side switch RMS currents.

High-side switch RMS current:

$$I_{HS_RMS} = \sqrt{D \times \left((I_{OUT} \times K)^2 + \frac{\Delta I^2}{12} \right)}$$

Low-side switch RMS current:

$$I_{LS_RMS} = \sqrt{(1-D)} \times \sqrt{\left\{ (I_{OUT} \times K)^2 + \frac{\Delta I^2}{12} + \left(\frac{4 \times (I_{OUT} \times K)^2}{3 \times (1-D)} \right) \times \left(\frac{(3D-1)}{2 \times (1-D)} + \frac{\Delta I}{4 \times (I_{OUT} \times K)} \right) \right\}}$$

Primary winding RMS current:

$$I_{PRI_RMS} = \sqrt{I_{HS_RMS}^2 + I_{LS_RMS}^2}$$

Secondary winding RMS current is given by the equation:

$$I_{SEC_RMS} = 2 \times I_{OUT} \times \sqrt{\frac{1}{3 \times (1-D)}}$$

Leakage Inductance

Transformer leakage inductance (L_LEAK) plays a key role in determining the output voltage regulation. For better output voltage regulation, leakage inductance should be reduced to less than 1% of the primary inductance value. Higher leakage inductance also limits the amount of power delivered to the output.

Primary Negative Peak Current

The primary current can go negative when the low-side switch is turned on. The primary negative peak current can be calculated using the equation:

$I_NEGPK_PRI = (-I_{OUT} \times K \times (1 + D)/(1 - D)) - \Delta I/2$

Specifying the Iso-Buck Transformer

Off-the-shelf transformer or coupled inductor can be used as Iso-buck transformer. If readily not available, use the table below to specify the Iso-buck transformer parameters to transformer vendor.

Primary Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. Calculate the minimum required output capacitance from the equation:

$$D_{MAX} = \frac{V_{PRI}}{V_{IN_MIN}}$$

Table 2. Switching Frequency vs. RT Resistor

PARAMETER	SYMBOL
Primary Inductance	L_{PRI}
Leakage Inductance	L_{LEAK}
Primary Ripple Current	ΔI
Primary Peak Current	I_{PK_PRI}
Primary RMS Current	I_{PRI_RMS}
Secondary Peak Current	I_{PK_SEC}
Secondary RMS Current	I_{SEC_RMS}
Working Voltage	VAC, VDC
Insulation Level	VAC, VDC

$$C_{PRI} = \frac{K \times I_{OUT} \times D_{MAX}}{f_{SW} \times 0.01 \times V_{PRI}}$$

where:

I_{OUT} = Load current

K = Turns ratio

f_{SW} = Switching frequency

V_{PRI} = Primary output voltage

V_{IN_MIN} = Minimum input voltage.

Secondary Output Capacitor Selection

Secondary side capacitor supplies load current when high-side switch is on. Calculate the required output capacitance to support 1% steady state ripple using the equation:

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times 0.01 \times V_{OUT}}$$

It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in the application.

Input Capacitor Selection

Ceramic input capacitors are recommended for the IC. The input capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the input ceramic capacitor to provide necessary damping for potential oscillations caused by the longer input power path and input ceramic capacitor. Calculate required input capacitance using the equation:

$$C_{IN} = \frac{K \times I_{OUT} \times D_{MAX} \times (1 - D_{MAX})}{f_{SW} \times \Delta V_{IN}}$$

$$D_{MAX} = \frac{V_{PRI}}{V_{IN_MIN}}$$

ΔV_{IN} is input voltage ripple, normally 2% of the minimum input voltage, D_{MAX} is maximum duty cycle, f_{SW} switching frequency of operation.

Secondary Diode Selection

Secondary rectifier diode should be rated to carry peak secondary current and to withstand reverse voltage when high side switch is on. Schottky diode with less forward voltage drop should be selected for better output regulation.

Calculate peak current rating of the diode using the equation:

$$I_{PK_DIODE} = \frac{2 \times I_{OUT}}{(1 - D)}$$

Calculate peak reverse voltage rating of the diode using the equation:

$$V_{DIODE} = 2 \times \left(\left(V_{IN_MAX} - V_{PRI} \right) \times K + V_{OUT} \right)$$

Power dissipated in the diode can be calculated using the equation:

$$P_{DIODE} = V_D \times I_{OUT}$$

Minimum Load Requirements

Under light-load conditions, the iso-buck converter output voltage increases excessively due to the transformer leakage inductance and parasitic capacitance. Normally, a minimum load of 10% to 20% of the full load is sufficient to keep the converter output voltage regulation within ±5%. The output voltage regulation should be verified after testing prototype.

A resistor connected in series with a Zener diode can be used as an overvoltage protection circuit to limit the overvoltage under absolute no load conditions. The Zener diode threshold can be selected as 15% higher than the nominal regulated output voltage V_{OUT}. The series resistor (R1) value can be in the range of 30Ω to 60Ω.

Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{PRI}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to SGND.

Setting the Input Undervoltage Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage divider connected from V_{IN} to SGND (see Figure 6). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.3MΩ max and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the device is required to turn on.

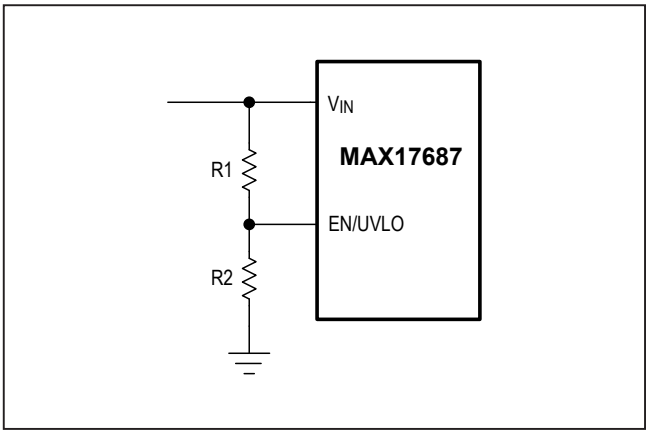


Figure 6. Setting the Input Undervoltage Lockout

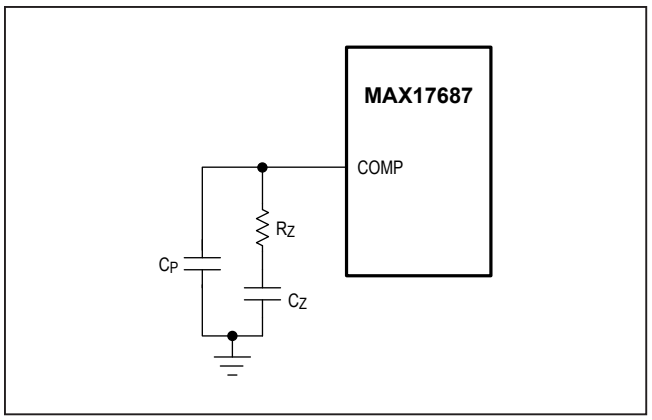


Figure 7. External Compensation Network

External Loop Compensation

The MAX17687 uses peak current-mode control scheme and needs only a simple RC network to have a stable, control loop. The compensation network is shown in Figure 7. Use the following equations for calculating the compensation components:

$$R_Z = 1100 \times f_C \times \left[C_{OUT} \times (1\text{-}D) \times K^2 + C_{PRI}\right] \times V_{PRI}$$

where R_Z is in Ω and f_C is bandwidth of the converter in Hz. Choose f_C to be $1/20^{th}$ of the switching frequency.

$$C_Z = \frac{5}{\pi \times f_C \times R_Z}$$

$$C_P = \frac{1}{\pi \times f_{SW} \times R_Z}$$

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the device can be estimated as follows:

$$P_{LOSS} = P_{OUT} \times \left(\frac{1}{\eta} - 1\right) - \left(I_{PRI_RMS}^2 \times R_{PRI}\right) - \left(I_{SEC_RMS}^2 \times R_{SEC}\right) - \left(V_D \times I_{OUT}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

P_{OUT} = Output power

η = Efficiency of power conversion

R_{PRI} = Primary resistance of the transformer

R_{SEC} = Secondary resistance of the transformer

V_D = Diode drop.

The junction temperature of the device can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the equation below:

$$T_{J_MAX} = T_{A_MAX} + (\theta_{JA} \times P_{LOSS})$$

if the application has a thermal management system that ensures that the exposed pad of the device is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature from the equation below:

$$T_{J_MAX} = T_{EP_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperature greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the V_{IN} pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum, typically the return terminal of the V_{CC} bypass capacitor. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation. For a sample layout that ensures first pass success, refer to the MAX17687 evaluation kit layout available at **www.maximintegrated.com**.

Typical Application Circuit

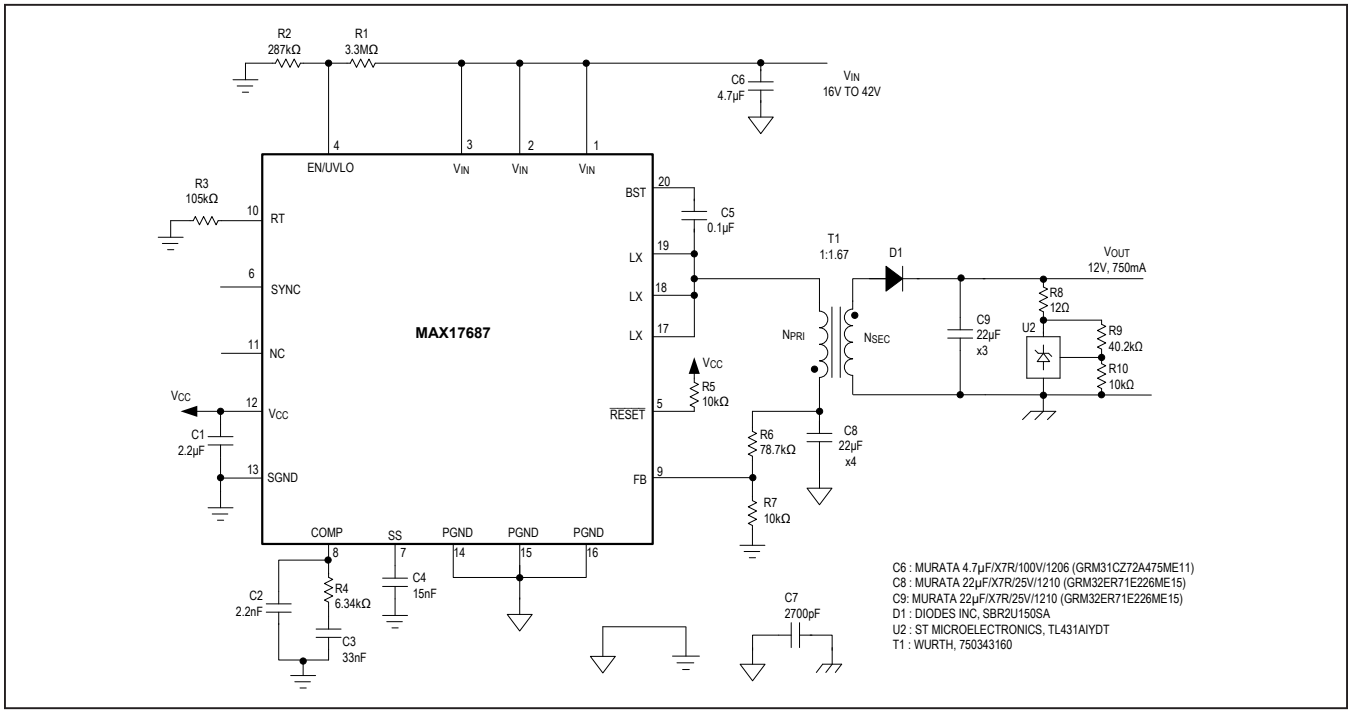


Figure 8: 12V, 750mA Isolated Output Application Circuit -1

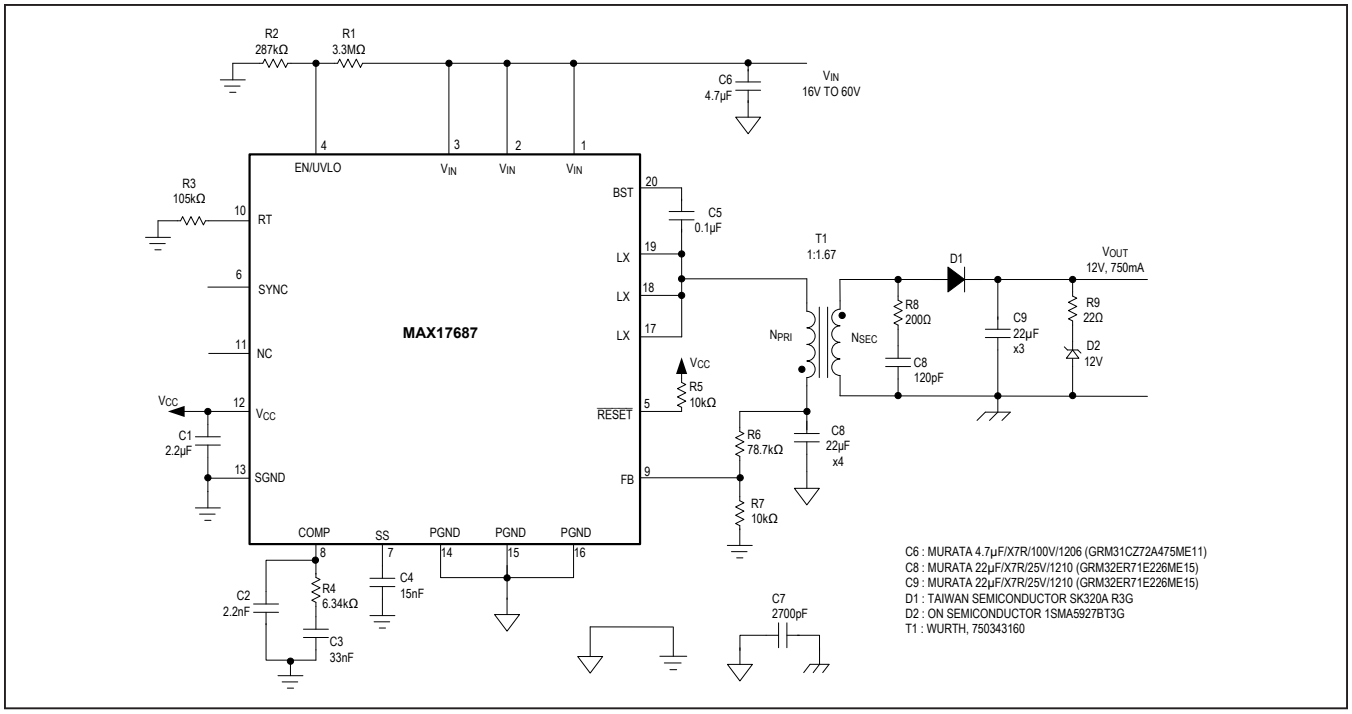


Figure 9: 12V, 750mA Isolated Output Application Circuit -2

Ordering Information

PART	PIN-PACKAGE
MAX17687ATP+	20 TQFN-EP*

Note: *All devices operate over the -40ºC to +125ºC temperature range, unless otherwise noted.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/18	Initial release	—

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