Complete, High Resolution 16-Bit A/D Converter

ADADC71

FEATURES

16-bit converter with reference and clock
±0.003% maximum nonlinearity
No missing codes to 14 bits
Fast conversion: 35 µs (14 bit)
Short cycle capability
Parallel logic outputs
Low power: 645 mW typical
Industry standard pinout

APPLICATIONS

Medical and analytic instrumentation
Precision measurement for industrial robots
Automatic test equipment
Multi-channel data acquisition systems
Servo-control systems

FUNCTIONAL BLOCK DIAGRAM

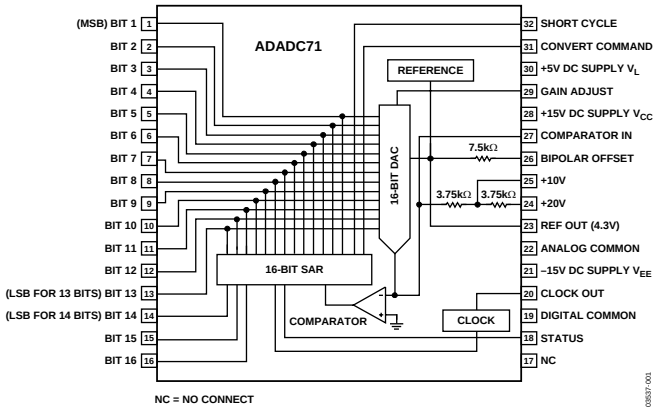


Figure 1.

GENERAL DESCRIPTION

The ADADC71 is a high resolution 16-bit hybrid IC analog-to-digital converter including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin hermetic ceramic DIP. The thin-film scaling resistors allow analog input ranges of ±2.5 V, ±5 V, ±10 V, 0 to +5 V, 0 to +10 V, and 0 to +20 V.

Important performance characteristics of the device are maximum linearity error of ±0.003% of FSR, and maximum conversion time of 50 µs. This performance is due to innovative design and the use of proprietary monolithic DAC chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The ADADC71 provides data in parallel format with corresponding clock and status outputs. All digital inputs and outputs are TTL-compatible. The ADADC71 used to provide data in a serial format. The serial output function is no longer available after date code 0120.

PRODUCT HIGHLIGHTS

1. The ADADC71 provides 16-bit resolution with a maximum linearity error less than ±0.003% (±0.006% for J grades) at 25°C.
2. Conversion time is 35 µs typical (50 µs max) to 14 bits with short cycle capability.
3. Two binary codes are available on the ADADC71 output: complementary straight binary (CSB) for unipolar input voltage ranges, and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature, and lower chip count for improved reliability.

Rev. C

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REVISION HISTORY

6/05—Rev. B to Rev. C

Updated Format ..... Universal
Removed ADADC72 ..... Universal
Updated Outline Dimensions 12
Changes to Ordering Guide 12

SPECIFICATIONS

Typical at T_A =+25°C, V_S = ±15 V, +5 V unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Units	Comment
RESOLUTION			16	Bits	
ANALOG INPUTS					
Voltage Ranges					
Bipolar		±2.5		V	
		±5		V	
		±10		V	
Unipolar		0 to +5		V	
		0 to +10		V	
		0 to +20		V	
Impedance (Direct Input)					
0 to ±5 V, ±2.5 V		1.88		KΩ	
0 to ±10 V, ±5.0 V		3.75		KΩ	
0 to ±20 V, ±10 V		7.50		KΩ	
DIGITAL INPUTS[1]					
Convert command					Trailing edge of positive 50 ns (min) pulse initiates conversion
Logic Loading			1	LSTTL Load	
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error		±0.1[2]	±0.2	%	
Offset Error					
Unipolar		±0.05[2]	±0.1	% of FSR[3]	
Bipolar		±0.1[2]	±0.2	% of FSR	
Linearity Error			±0.006	% of FSR	J Grade
			±0.003	% of FSR	K Grade
Inherent Quantization Error		±1/2		LSB	
Differential Linearity Error		±0.003		% of FSR	
No Missing Codes @ 25°C[4]		to 14 bits		Guaranteed	K Grade
POWER SUPPLY SENSITIVITY					
±15 V dc		0.003		% of FSR/%ΔV_S	
+5 V dc		0.001		% of FSR/%ΔV_S	
CONVERSION TIME[5] (14 BITS)		35	50	µs	
WARM-UP TIME	5			Minutes	
DRIFT					
Gain			±15	ppm/°C	
Offset					
Unipolar		±2	±4	ppm of FSR/°C	
Bipolar			±10	ppm of FSR/°C	
Linearity		±2	±3	ppm of FSR/°C	
Guaranteed No Missing Code Temperature Range[4]		0 to 70		°C	JD (13 bits), KD (14 bits)

Parameter	Min	Typ	Max	Units	Comment
DIGITAL OUTPUT[1]					All codes complementary
Parallel Output Codes[6]					
Unipolar		CSB			
Bipolar		COB, CTC[7]			
Output Drive		5		LSTTL Loads	
Status					Logic 1 during conversion
Status Output Drive			5	LSTTL Loads	
Internal Clock					
Clock Output Drive			5	LSTTL Loads	
Frequency		400		kHz	
INTERNAL REFERENCE VOLTAGE		6.3		V dc	
Error			±5	%	
Max External Current Drain with No Degradation of Specifications			±200	µA	
Temperature Coefficient			±10	ppm/°C	
POWER SUPPLY REQUIREMENTS					
Power Consumption		645	850	mW	
Rated Voltage, Analog		±15	±0.5	V dc	
Rated Voltage, Digital		±5	±0.25	V dc	
Supply Drain +15 V dc		+16		mA	
Supply Drain −15 V dc		−21		mA	
Supply Drain +5 V dc		+18		mA	
TEMPERATURE RANGE					
Specification		0 to +70		°C	
Operating (Derated Specs)		−25 to +85		°C	
Storage		−55 to +125		°C	

[1] For inputs Logic 0 = 0.8 V, max. Logic 1 = 2.0 V, min. For digital outputs Logic 0 = 0.4 V max. Logic 1 = 2.4 V min.
[2] Adjustable to 0.
[3] Full scale range.
[4] For definition of "No Missing Codes," refer to the Theory of Operation section.
[5] Conversion time may be shortened with short cycle set for lower resolution.
[6] CSB—Complementary straight binary. COB— Complementary offset binary, CTC—Complementary twos complement.
[7] CTC coding obtained by inverting MSB (Pin 1).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Logic Supply Voltage	7 V
Analog Ground to Digital Ground	±0.3 V
Analog Inputs (Pin 25, Pin 24)	$\pm V_S$
Digital Input	−0.3 V to V_{DD} + 0.3 V
Junction Temperature	175°C
Storage Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



THEORY OF OPERATION

The analog continuum is partitioned into 2^{16} discrete ranges for 16-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. An inherent quantization uncertainty of ±1/2 LSB is associated with the resolution, in addition to the actual conversion errors.

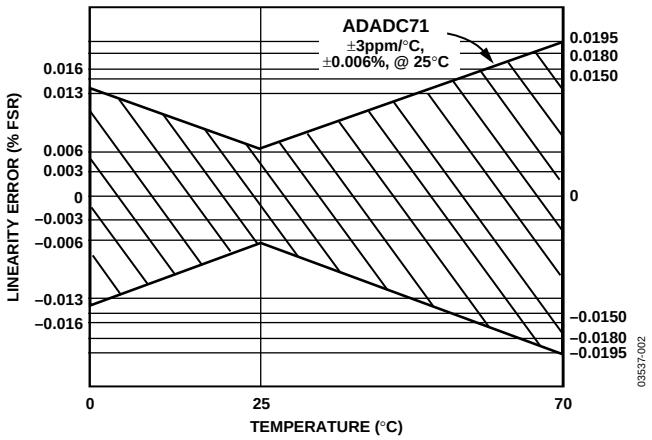


Figure 2. Linearity Error vs. Temperature

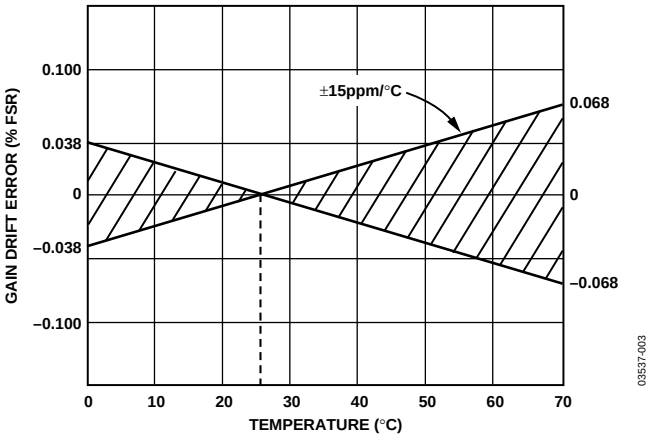


Figure 3. Gain Drift Error vs. Temperature

The actual conversion errors associated with ADCs are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error, and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.2% FSR for gain and ±0.1% FSR for offset. These errors may be trimmed to 0 by using external trim circuits as shown in Figure 5 and Figure 6. Linearity error is defined for unipolar ranges as the deviation from a true straight-line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point that is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of ADC accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

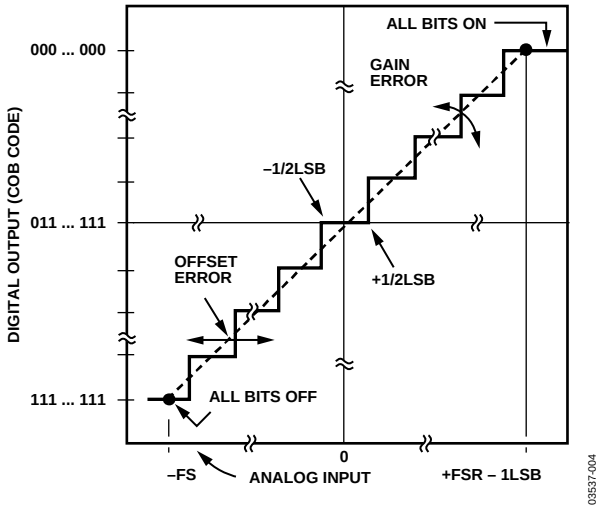


Figure 4. Transfer Characteristics for an Ideal Bipolar ADC

Monotonic behavior requires that the differential linearity error be less than 1 LSB. However, a monotonic converter can have missing codes. The ADADC71 is specified as having no missing codes over temperature ranges noted in the Specifications section.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero point for unipolar ranges or the negative full-scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-square (RSS) and can be shown as

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

where:

ϵ_G = *gain drift error* (*ppm*/°*C*).

ϵ_O = *offset drift error* (*ppm of FSR*/°*C*).

ϵ_L = *linearity error* (*ppm of FSR*/°*C*).

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the ADADC71 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjustment circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 510 kΩ resistor to Pin 29 (GAIN ADJUST), as shown in Figure 5.

If no external trim adjustment is desired, Pin 27 (COMPARATOR IN) and Pin 29 may be left open.

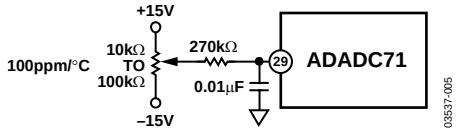


Figure 5. Gain Adjustment Circuit

ZERO OFFSET ADJUSTMENT

The zero offset adjustment circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8 MΩ resistor to Pin 27 for all ranges. As shown in Figure 6, the tolerance of this fixed resistor is not critical; a carbon composition type is generally adequate. Using a carbon composition resistor with a −1200 ppm/°C temperature coefficient contributes a worst-case offset temperature coefficient of 32 $LSB_{14} \times 61$ ppm/ $LSB_{14} \times 1200$ ppm/°C = 2.3 ppm/°C of FSR, if the offset adjustment potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±16 LSB_{14}, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset temperature coefficient.

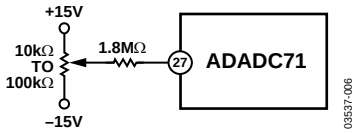


Figure 6. Zero Offset Adjustment Circuit

An alternate offset adjustment circuit, which contributes negligible offset temperature coefficient if metal film resistors (temperature coefficient < 100 ppm/°C) are used, is shown in Figure 7.

In either adjustment circuit, the fixed resistor connected to Pin 27 should be located close to this pin to keep the pin connection runs short. Pin 27 is quite sensitive to external noise pick-up.

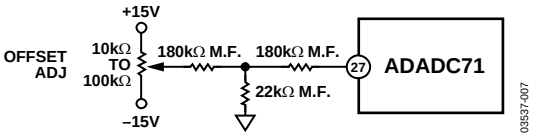


Figure 7. Low Temperature Coefficient Zero Adjustment Circuit

TIMING

The timing diagram is shown in Figure 8. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This in turn removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 to B_{16} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic 0 state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

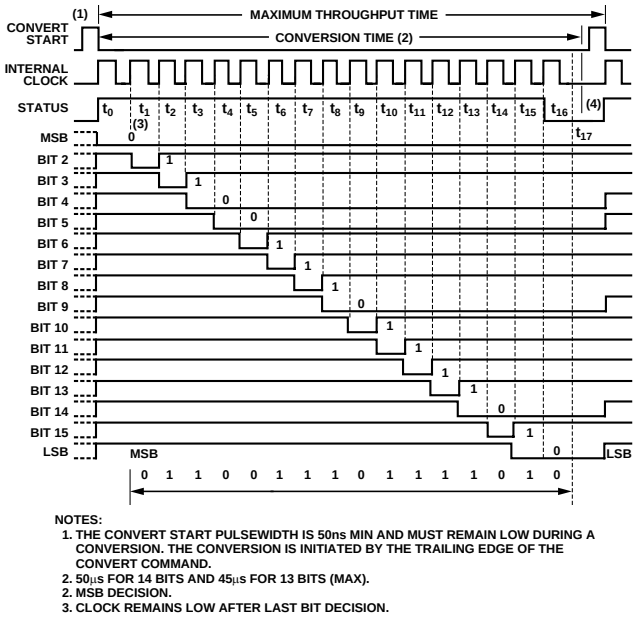


Figure 8. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Parallel data from TTL storage registers is in negative true form (Logic 1 = 0 V and Logic 0 = 2.4 V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20 ns before the STATUS flag returns to Logic 0, permitting parallel data transfer to be clocked on the 1 to 0 transition of the STATUS flag (see Figure 9). Parallel data outputs change state on positive-going clock edges.

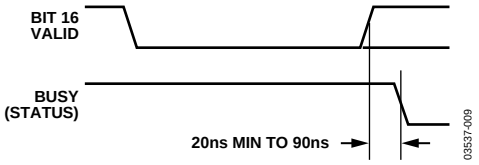


Figure 9. LSB Valid to Status Low

Short Cycle Input: Pin 32 (SHORT CYCLE) permits the timing cycle shown in Figure 8 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, Pin 32 is connected to Bit 11 output Pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (t_{10} + 40 ns in the timing diagram of Figure 8). Short cycle connections and associated maximum 8-, 10-, 12-, 13-, 14-, and 15-bit conversion times are summarized in Table 3.

Table 3. Short Cycle Connections

Connect Short Cycle Pin 32 to	Resolution		Maximum Conversion Time	Status Flag Reset
	Bits	% FSR		
N/C (Open)	16	0.0015	57.0	t_{16} + 40 ns
Pin 16	15	0.003	53.5	t_{15} + 40 ns
Pin 15	14	0.006	50.0	t_{14} + 40 ns
Pin 14	13	0.012	46.5	t_{13} + 40 ns
Pin 13	12	0.024	42.8	t_{12} + 40 ns
Pin 11	10	0.100	35.6	t_{10} + 40 ns
Pin 9	8	0.390	28.5	t_8 + 40 ns

INPUT SCALING

The ADADC71 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the ADC. Connect the input signal as shown in Table 4. See Figure 10 for circuit details.

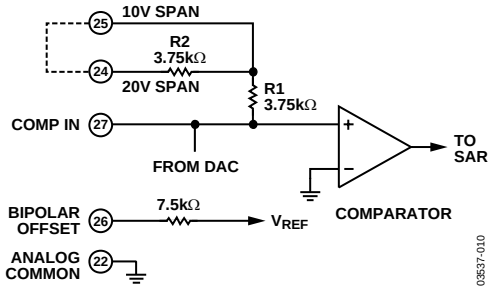


Figure 10. ADADC71 Input Scaling Circuit

Table 4. Input Scaling Connections

Input Signal Line	Output Code	Connect Pin 26 to	Connect Pin 24 to	For Direct Input, Connect Input Signal to
±10 V	COB	Pin 27[1]	Input Signal	Pin 24
±5 V	COB	Pin 27[1]	Open	Pin 25
±2.5 V	COB	Pin 27[1]	Pin 27[1]	Pin 25
0 V to +5 V	CSB	Pin 22	Pin 27[1]	Pin 25
0 V to +10 V	CSB	Pin 22	Open	Pin 25
0 V to +20 V	CSB	Pin 22	Input Signal	Pin 24

[1] Pin 27 is extremely sensitive to noise and should be guarded by analog common

Table 5. Transition Values vs. Calibration Codes

Output Code MSB LSB[1]	Range	±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V
000. . . .000[2]	+Full Scale	+10 V −3/2 LSB	+5 V −3/2 LSB	+2.5 V −3/2 LSB	+10 V −3/2 LSB	+5 V −3/2 LSB
011 . . . 111	Mid Scale	0 −1/2 LSB	0 −1/2 LSB	0 −1/2 LSB	+5 V −1/2 LSB	+2.5 V −1/2 LSB
111 . . . 110	−Full Scale	−10 V +1/2 LSB	−5 V +1/2 LSB	−2.5 V +1/2 LSB	0 V +1/2 LSB	0 V +1/2 LSB

[1] For LSB value for range and resolution used, see Table 6.
[2] Voltages given are the nominal value for transition to the code specified.

Table 6. Input Voltage Range and LSB Values

Analog Input Voltage Range		±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV
	n = 13	2.44 mV	1.22 mV	0.61 mV	1.22 mV	0.61 mV
	n = 14	1.22 mV	0.61 mV	0.31 mV	0.61 mV	0.31 mV
	n = 15	0.61 mV	0.31 mV	0.15 mV	0.31 mV	0.15 mV

[1] COB = complementary offset binary.
[2] CTC = complementary twos complement—achieved by using an inverter to complement the most significant bit to produce (MSB).
[3] CSB = complementary straight binary.

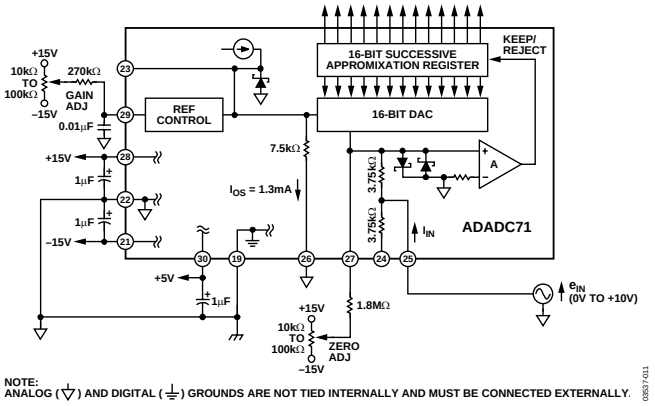


Figure 11. Analog and Power Connections for Unipolar 0 V to +10 V Input Range

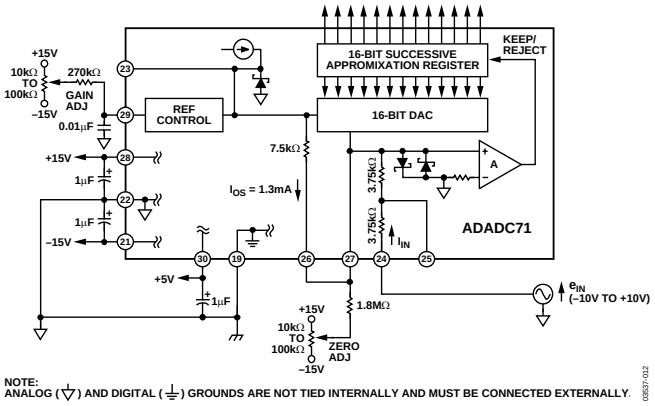


Figure 12. Analog and Power Connections for Bipolar –10 V to +10 V Input Range

CALIBRATION (14-BIT RESOLUTION EXAMPLES)

External zero adjustment and gain adjustment potentiometers, connected as shown in Figure 5 and Figure 6, are used for device calibration. To prevent interaction of these two adjustments, zero is always adjusted first and then gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and –FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 V to +10 V Range

Set the analog input to +1 LSB_{14} = 0.00061 V. Adjust zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR – 2 LSB = +9.9987 V. Adjust gain for 00000000000001 digital output code; full-scale (gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000 V; digital output code should be 01111111111111.

–10 V to +10 V Range

Set the analog input to –9.99878 V; adjust zero for 11111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756 V; adjust gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000 V; digital output (complementary offset binary) code should be 01111111111111.

Other Ranges

Representative digital coding for 0 to +10 V and –10 V to +10 V ranges is given above. Coding relationships and calibration points for 0 to +5 V, –2.5 V to +2.5 V and –5 V to +5 V ranges can be found by proportionally halving the corresponding code equivalents listed for the 0 to +10 V and –10 V to +10 V ranges, respectively, as indicated in Table 5.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2 LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end point) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *A/D Conversion Handbook*, D. Sheingold, Analog Devices, Inc., 1986 Part II, Chapter 4.

GROUNDING, DECOUPLING, AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins, which are not connected together within the device. These grounds are usually referred to as the DIGITAL COMMON (logic power return), ANALOG COMMON (analog power return), or analog signal ground. These grounds (Pin 19 and Pin 22) must be tied together at one point as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit card, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the ADADC71. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way the ADADC71 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the ADADC71's supply terminals should be capacitively decoupled as close to the ADADC71 as possible. A large value, such as 1 μF, capacitor in parallel with a 0.1 μF capacitor is usually sufficient. Analog supplies are to be bypassed to the ANALOG COMMON (analog power return) Pin 22 and the logic supply is bypassed to DIGITAL COMMON (logic power return) Pin 19.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

T/H REQUIREMENTS FOR HIGH RESOLUTION APPLICATIONS

The characteristics required for high resolution track-and-hold amplifiers are low feedthrough, low pedestal shifts with changes of input signal or temperature, high linearity, low temperature coefficients, and minimal droop rate.

The aperture jitter is a result of noise within the switching network that modulates the phase of the hold command, and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The T/H amplifier slew rate determines the maximum frequency tracking rate and part of the settling time when sampling pulses and square waves. The feedthrough from input to output while in the hold mode should be less than 1 LSB. The amplitude of 1 LSB of the companion ADC for a given input range will vary from 610 μV for a 14-bit ADC using a 0 V to +10 V input range to 4.88 mV for a 12-bit ADC using a ±10 V input range. The hold mode droop rate should produce less than 1 LSB of droop in the output during the conversion time of the ADC. For 610 μV/LSB, as noted in the example above, for a 50 μs 14-bit ADC, the maximum droop rate is 610 μV/50 μs or 12 μV/μs during the 50 μs conversion period.

Minimal thermal tail effects are another requirement of high resolution applications. The self-heating errors induced by the changing current levels in the output stages of T/H amps may cause more than 1 LSB of error due to thermal tail effects.

The linearity error should be less than 1 LSB over the transfer function, as set by the resolution of the ADC. The T/H acquisition time and T/H settling time along with the conversion time of the ADC determines the highest sampling rate. This in turn determines the highest input signal frequency that can be sampled at twice a cycle.

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in under sampling or aliasing errors of the input signal.

The pedestal shift due to input signal changes should either be linear, to be seen as a gain error, or negligible, as with the feedthrough specification. The temperature coefficients for drift would be low enough such that full accuracy is maintained over some minimum temperature range. The droop rate and pedestal shift increases above +70°C (+158°F). For commercial and industrial users, these shifts only appear above the highest temperatures their equipment might expect to experience. Most precision instrumentation is installed only in human inhabitable work spaces or in controlled enclosures if the area has a hostile environment. Thus, the ADADC71 used with a sample-and-hold amplifier offers high accuracy sampling in high precision applications.

USING THE ADADC71 AT SLOWER CONVERSION TIMES

The user may wish to run the ADADC71 at slower conversion times in order to synchronize the ADC with an external clock. This is accomplished by running a slower clock that the internal clock into the START CONVERT input. This clock must consist of narrow negative-going clock pulses, as seen in Figure 13. The pulse must be a minimum of 100 ns wide, but not greater than 700 ns. Having a raising edge immediately after a falling edge inhibits the internal clock pulse. This enables the ADADC71 to function normally and complete a conversion after 16 clock pulses. The STATUS command functions normally and switches high after the first clock pulse and falls low after the 17th clock pulse. In this way an external clock can be used to control the ADADC71 at slower conversion times.

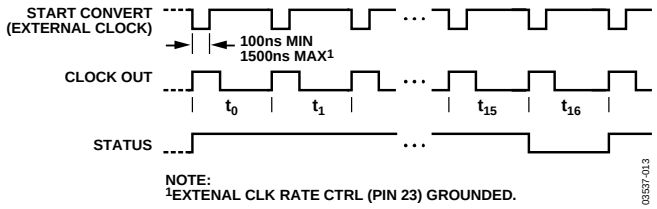
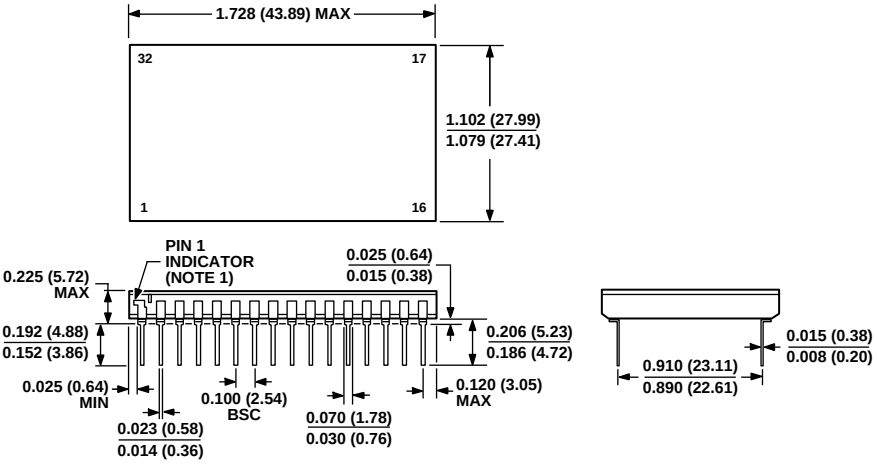


Figure 13. Timing Diagram for Use with an External Clock

OUTLINE DIMENSIONS



NOTES:
1. INDEX AREA IS INDICATED BY A NOTCH OR LEAD ONE IDENTIFICATION MARK LOCATED ADJACENT TO LEAD ONE.
2. CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 14. 32-Lead Bottom-Brazed Ceramic Dip for Hybrid [BBDIP_H] (DH-32E)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Linearity Error (Max)	Specification Temp Range	Package Option
AD ADC71JD	±0.006% of FSR	0°C to +70°C	Ceramic (DH-32E)
AD ADC71KD	±0.003% of FSR	0°C to +70°C	Ceramic (DH-32E)

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