19-1574; Rev 0; 1/00

MAXIM

Fan Controller and Remote Temperature Sensor with SMBus Serial Interface

MAX1669

General Description

The MAX1669 fan controller includes a precise digital thermometer that reports the temperature of a remote sensor. The remote sensor is a diode-connected transistor—typically a low-cost, easily mounted 2N3906 PNP type—replacing conventional thermistors or thermocouples. Remote accuracy is ±3°C for transistors from multiple manufacturers, with no calibration needed. The MAX1669 has an independent fan controller with a low-current logic output requiring external power components to interface to a DC brushless fan. The fan controller has two modes of operation: a low-frequency (20Hz to 160Hz) PWM mode intended for driving the fan motor, or a high-impedance DAC output that generates a variable DC control voltage. In PWM mode, the FAN frequency can be synchronized to an external clock.

Other key features include general-purpose inputs/outputs (GPIOs) for fan presence detection and a thermostat output intended as a fan override signal in case the host system loses the ability to communicate. The internal ADC has a wide input voltage range and gives overrange readings when too large an input voltage is applied. Other error-checking includes temperature out-of-range indication and diode open/short faults.

The MAX1669 is available in a space-saving 16-pin QSOP package that allows it to fit adjacent to the SLOT1 connector.

Applications

Pentium® CPU Cooling

Desktop Computers

Notebook Computers

Servers

Workstations

Typical Operating Circuit appears at end of data sheet.

Pentium is a registered trademark of Intel Corp.

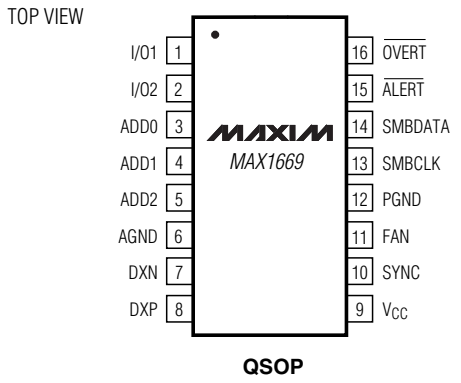
Features

- ♦ **Measures Remote CPU Temperature**
- ♦ **No Calibration Required**
- ♦ **20Hz to 160Hz PWM Output for Fan**
- ♦ **PWM Frequency Sync Input (260kHz)**
- ♦ **Flexible Fan Interface: Linear or PWM**
- ♦ **SMBus 2-Wire Serial Interface**
- ♦ **Programmable Under/Overtemperature Alarms**
- ♦ **$\overline{\text{ALERT}}$ Latched Interrupt Output**
- ♦ **$\overline{\text{OVERT}}$ Thermostat Output**
- ♦ **Two GPIO Pins**
- ♦ **Write-Once Configuration Protection**
- ♦ **Supports SMBus Alert Response**
- ♦ **±3°C Temperature Accuracy (-40°C to +125°C, remote)**
- ♦ **3µA Standby Supply Current**
- ♦ **+3V to +5.5V Supply Range**
- ♦ **Small 16-Pin QSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1669EEE	-40°C to +85°C	16 QSOP

Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 1-800-835-8769.

Fan Controller and Remote Temperature Sensor with SMBus Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{CC} to AGND.....-0.3V to +6V
DXP, ADD_ to AGND.....-0.3V to (V_{CC} + 0.3V)
DXN to AGND.....-0.3V to +0.8V
SMBCLK, SMBDATA, $\overline{\text{ALERT}}$, SYNC,
I/O1, I/O2, $\overline{\text{OVERT}}$, FAN to AGND.....-0.3V to +6V
FAN to PGND.....-0.3V to (V_{CC} + 0.3V)
PGND to AGND.....-0.3V to +0.3V
PWM Current.....-50mA to +50mA
SMBDATA Current.....-1mA to +50mA
I/O1, I/O2 Current.....-1mA to +25mA
DXN Current.....±1mA
ESD Protection (all pins, Human Body Model).....2000V
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.30mW/°C above +70°C).....667mW
Operating Temperature Range (extended).....-55°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC AND POWER SUPPLY						
Resolution (Note 1)	Monotonicity guaranteed		8			Bits
Temperature Error, Remote Diode (Note 2)	T_R = 0°C to +100°C, diode ideality factor = 1.013		-3		3	°C
Supply Voltage Range			3		5.5	V
Undervoltage Lockout Threshold	V_{CC} input, disables A/D conversion, rising edge		2.6	2.8	2.95	V
Undervoltage Lockout Hysteresis				50		mV
Power-On Reset Threshold	V_{CC}, falling edge		1	1.9	2.5	V
POR Threshold Hysteresis				50		mV
Standby Supply Current	SMBus static			3	10	µA
	SMBCLK at 10kHz			3		
Average Operating Supply Current	Autoconvert mode, average measured over 1s	FAN output set to 150Hz mode		75	150	µA
		FAN output set to DAC mode		360		µA
Conversion Time	From stop bit to conversion complete		47	62	78	ms
Conversion Rate	Autoconvert mode		1.6	2	2.4	Hz
Remote-Diode Source Current	V_{DXP} forced to V_{DXN} + 0.65V	High level	80	100	120	µA
		Low level	8	10	12	
DXN Source Voltage				0.7		V
FAN OUTPUT						
FAN Output Source Current	PWM mode, V_{FAN} forced to 2.9V		10			mA
FAN Output Sink Current	PWM mode, V_{FAN} forced to 0.4V				-10	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.3V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FAN PWM Frequency Error	PWM mode, any setting	-20		+20	%
FAN Total Unadjusted Error	DAC mode, any setting, R_L = 10kΩ to GND	-4		4	%FS
FAN Output Voltage High	DAC mode, FAN duty factor = 1111b, I_{OUT} = 5mA	2.96	3.06		V
FAN Output Voltage Low	DAC mode, FAN duty factor = 0000b, I_{OUT} = -5mA		0.05	0.2	V
SYNC Capture Range		140	260	400	kHz
SYNC Input High Period		500			ns
SYNC Input Low Period		500			ns
SMBus INTERFACE (Figures 7, 8)					
Logic Input High Voltage	ADD_, I/O1, I/O2, SYNC, SMBCLK, SMBDATA; V_{CC} = 3V to 5.5V	2.1			V
Logic Input Low Voltage	ADD_, I/O1, I/O2, SYNC, SMBCLK, SMBDATA; V_{CC} = 3V to 5.5V			0.8	V
SMBDATA, $\overline{ALERT}$, $\overline{OVERT}$, I/O1, I/O2 Output Low Sink Current	Pin forced to 0.4V	6			mA
$\overline{ALERT}$, $\overline{OVERT}$, I/O1, I/O2 Output High Leakage Current	Pin forced to 5.5V			1	µA
Logic Input Current	Logic inputs forced to V_{CC} or GND	-1		1	µA
SMBus Input Capacitance	SMBCLK, SMBDATA		5		pF
SMBus Clock Frequency	(Note 3)	DC		100	kHz
SMBCLK Clock Low Time (t_{LOW})	10% to 10% points	4.7			µs
SMBCLK Clock High Time (t_{HIGH})	90% to 90% points	4			µs
SMBus Rise Time	SMBCLK, SMBDATA, 10% to 90% points			1	µs
SMBus Fall Time	SMBCLK, SMBDATA, 90% to 10% points			300	ns
SMBus Start Condition Setup Time		4.7			µs
SMBus Repeated Start Condition Setup Time ($t_{SU:STA}$)	90% to 90% points	500			ns
SMBus Start Condition Hold Time ($t_{HD:STA}$)	10% of SMBDATA to 90% of SMBCLK	4			µs
SMBus Stop Condition Setup Time ($t_{SU:STO}$)	90% of SMBCLK to 10% of SMBDATA	4			µs
SMBus Data Valid to SMBCLK Rising-Edge Time ($t_{SU:DAT}$)	10% or 90% of SMBDATA to 10% of SMBCLK	250			ns
SMBus Data-Hold Time ($t_{HD:DAT}$)	(Note 4)	0			µs
SMBus Bus-Free Time (t_{BUF})	Between start/stop conditions	4.7			µs
SMBCLK Falling Edge to SMBus Data-Valid Time	Master clocking-in data			1	µs

Fan Controller and Remote Temperature Sensor with SMBus Serial Interface

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
ADC AND POWER SUPPLY				
Temperature Resolution (Note 1)	Monotonicity guaranteed	8		Bits
Temperature Error, Remote Diode (Note 2)	T_R = -55°C to +125°C, diode ideality factor = 1.013	-5	5	°C
Supply Voltage Range		3	5.5	V
Average Operating Supply Current	Autoconvert mode, average measured over 1sec, FAN output set to 150Hz mode		100	µA
Conversion Time	From stop bit to conversion complete	47		ms
Conversion Rate	Autoconvert mode	1.6	2.4	Hz
FAN OUTPUT				
FAN Output Source Current	PWM mode, V_{FAN} forced to 2.9V	10		mA
FAN Output Sink Current	PWM mode, V_{FAN} forced to 0.4V		-10	mA
FAN PWM Frequency Error	PWM mode, any setting	-25	+25	%
FAN Total Unadjusted Error	DAC mode, any setting, R_L = 10kΩ to GND	-5	5	%FS
FAN Output Voltage High	DAC mode, FAN duty factor = 1111b, I_{OUT} = 5mA	2.94		V
FAN Output Voltage Low	DAC mode, FAN duty factor = 0000b, I_{OUT} = -5mA		0.2	V
SMBus INTERFACE				
Logic Input High Voltage	ADD_, I/O1, I/O2, SYNC, SMBCLK, SMBDATA; V_{CC} = 3V to 5.5V	2.1		V
Logic Input Low Voltage	ADD_, I/O1, I/O2, SYNC, SMBCLK, SMBDATA; V_{CC} = 3V to 5.5V		0.8	V
SMBDATA, $\overline{ALERT}$, $\overline{OVERT}$, I/O1, I/O2 Output Low Sink Current	Pin forced to 0.4V	6		mA
$\overline{ALERT}$, $\overline{OVERT}$, I/O1, I/O2 Output High Leakage Current	Pin forced to 5.5V		1	µA
Logic Input Current	Logic inputs forced to V_{CC} or GND	-1	1	µA

Note 1: Guaranteed but not 100% tested.

Note 2: T_R is the junction temperature of the remote diode. The temperature error specification is optimized to and guaranteed for a diode-connected 2N3906 transistor with ideality factor = 1.013. Variations in the ideality factor "m" of the actual transistor used will increase the temperature error by *. See the Temperature Error vs. Remote Diode Temperature graph in the *Typical Operating Characteristics* for typical temperature errors using several random 2N3906s. See *Remote Diode Selection* for remote diode forward-voltage requirements.

Note 3: The SMBus logic block is a static design that works with clock frequencies down to DC. While slow operation is possible, it violates the 10kHz minimum clock frequency and SMBus specifications, and may monopolize the bus.

Note 4: Note that a transition must internally provide at least a hold time in order to bridge the undefined region (300ns max) of SMBCLK's falling edge.

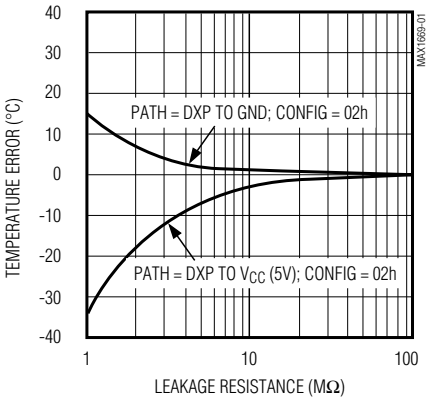
Note 5: Specifications to -40°C are guaranteed by design and not production tested.

$$^*\Delta T = \left(\frac{1.013}{m} - 1\right)\left(273.15k + T_R\right)\left(^\circ C\right)$$

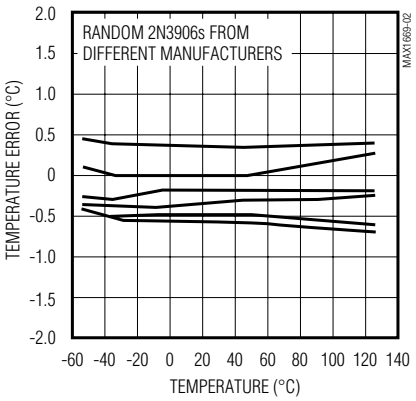
Typical Operating Characteristics

(Temperature error = measured - actual, T_A = +25°C, unless otherwise noted.)

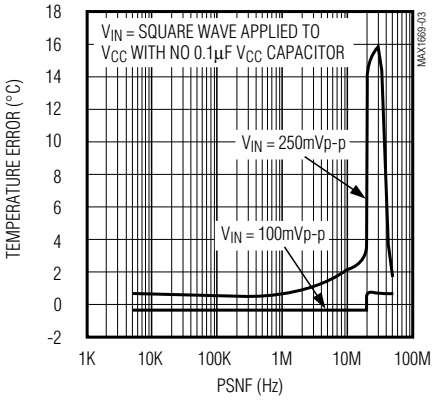
TEMPERATURE ERROR vs. LEAKAGE RESISTANCE



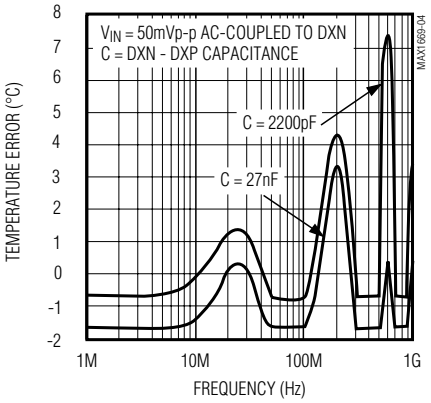
TEMPERATURE ERROR vs. REMOTE DIODE TEMPERATURE



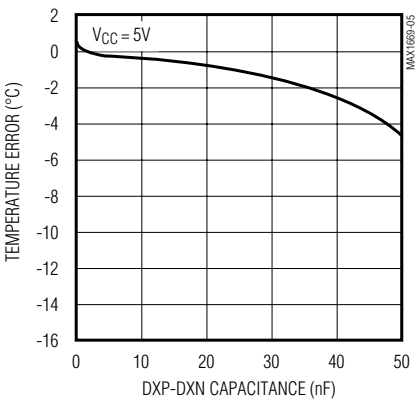
TEMPERATURE ERROR vs. POWER-SUPPLY NOISE FREQUENCY



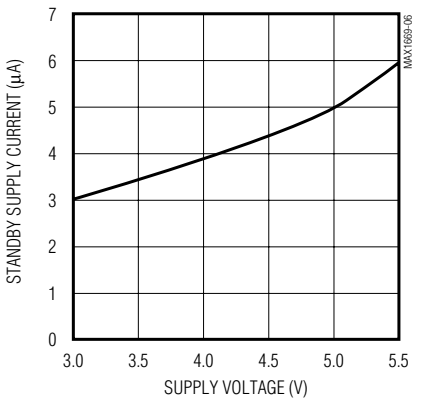
TEMPERATURE ERROR vs. COMMON-MODE NOISE FREQUENCY



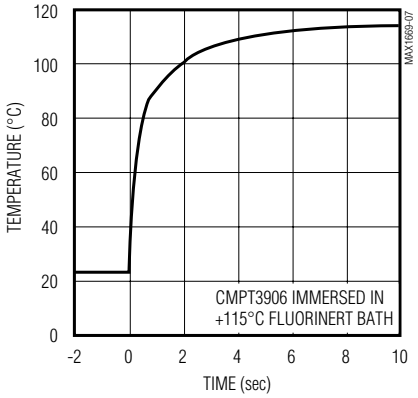
TEMPERATURE ERROR vs. DXP - DXN CAPACITANCE



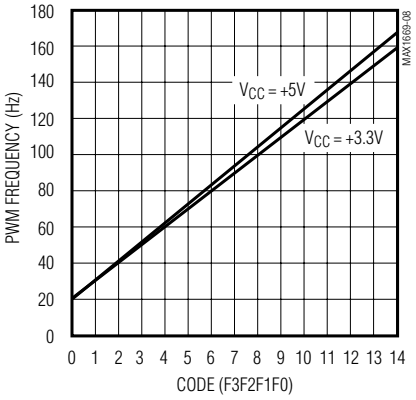
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



RESPONSE TO THERMAL SHOCK



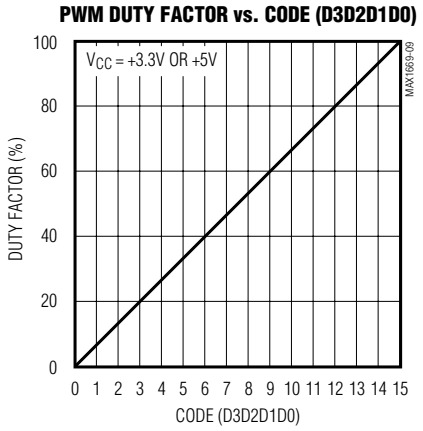
PWM FREQUENCY vs. CODE (F3F2F1F0)

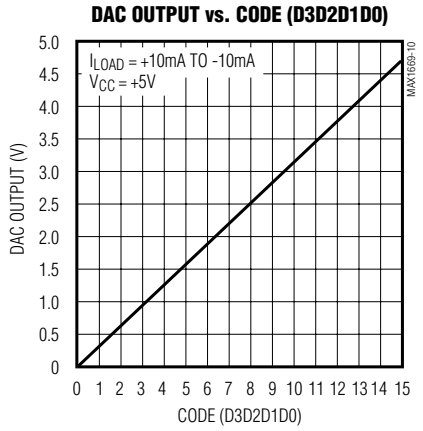


Fan Controller and Remote Temperature Sensor with SMBus Serial Interface

Typical Operating Characteristics (continued)

(Temperature error = measured - actual, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN	NAME	FUNCTION
1	I/O1	General-Purpose Open-Drain Logic Input/Output 1. I/O1 is intended for driving LEDs, driving power-plane switching MOSFETs, or detecting fan presence or chassis intrusion.
2	I/O2	General-Purpose Open-Drain Logic Input/Output 2. I/O2 is intended for driving LEDs, driving power-plane switching MOSFETs, or detecting fan presence or chassis intrusion.
3	ADD0	SMBus Address Select Pin 0. See Table 11.
4	ADD1	SMBus Address Select Pin 1. See Table 11.
5	ADD2	SMBus Address Select Pin 2. See Table 11.
6	AGND	Analog Ground
7	DXN	Combined Current Sink and ADC Negative Input from Remote Diode. DXN is normally biased to a diode voltage above ground.
8	DXP	Combined Current Source and ADC Positive Input from Remote Diode. Place a 2200pF capacitor between DXP and DXN for noise filtering.
9	V_{CC}	Supply Voltage Input, +3V to +5.5V. Bypass to AGND with a 0.1µF capacitor.
10	SYNC	Oscillator Synchronization Input. Connect to AGND to use internal clock. Capture range is 140kHz to 400kHz. The synchronization signal is internally applied to the FAN PWM clock. See Table 5 for synchronized frequencies.
11	FAN	Fan-Control Logic Output. Swings from PGND to V_{CC} in PWM mode, or PGND to 0.94 • V_{CC} in DAC mode.
12	PGND	Power Ground
13	SMBCLK	SMBus Serial-Clock Input
14	SMBDATA	Open-Drain SMBus Serial-Data Input/Output
15	$\overline{\text{ALERT}}$	Active-Low, Open-Drain SMBus Alert (interrupt) Output
16	$\overline{\text{OVERT}}$	Active-Low, Open-Drain Thermostat Output. Activated by T_{CRIT} threshold

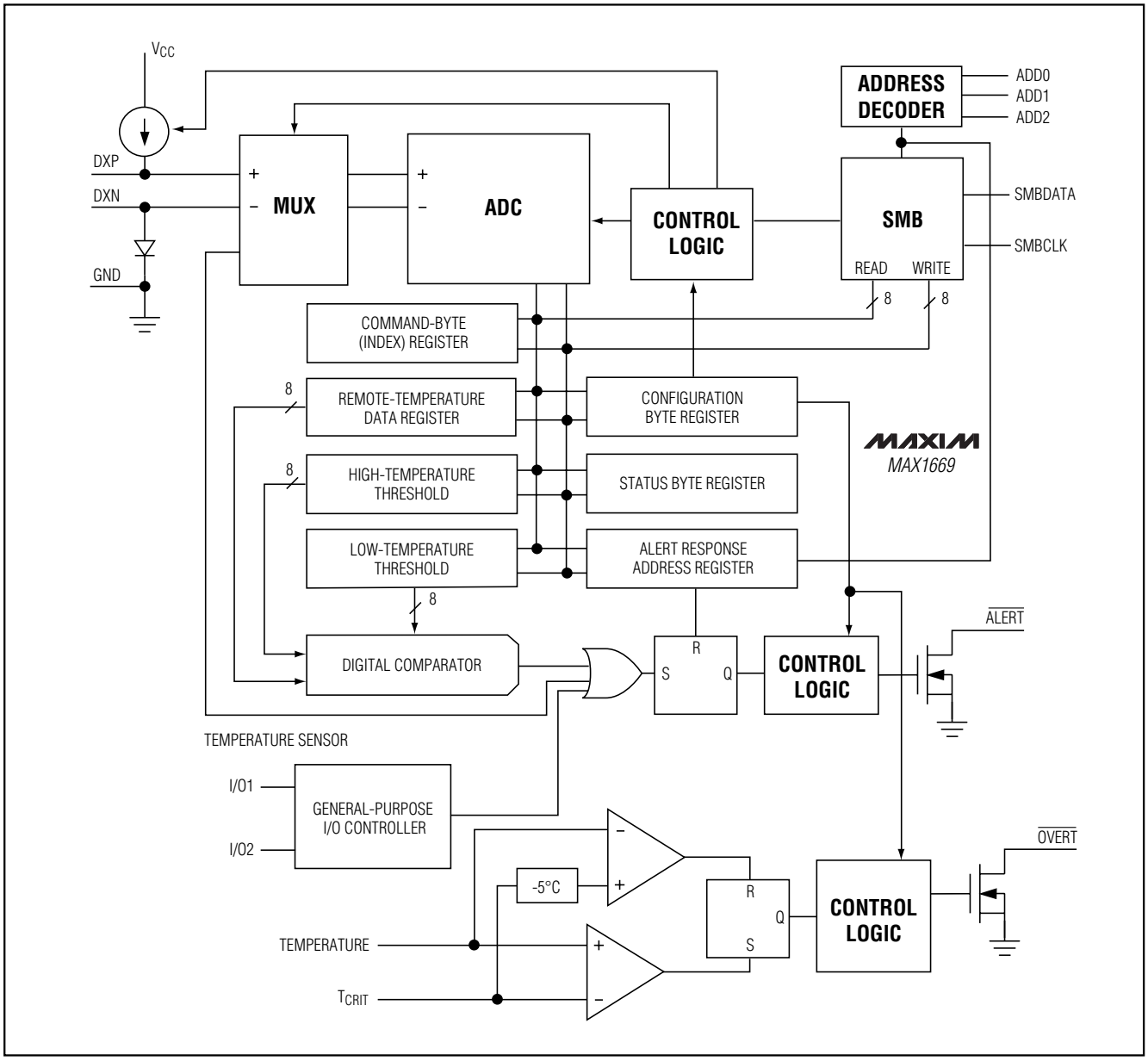


Figure 1. MAX1669 Temperature Sensor Functional Diagram

Detailed Description

The MAX1669 temperature sensor is designed to work with an external microcontroller (µC) or other intelligent devices in computer fan-control applications. The µC is typically a power-management or keyboard controller, generating SMBus serial commands by "bit-banging" general-purpose input/output (GPIO) pins or through a dedicated SMBus interface block.

Essentially an 8-bit serial analog-to-digital converter (ADC) with a sophisticated front end, the temperature measurement channel contains a switched-current source, a multiplexer, and an integrating ADC. Temperature data from the ADC is loaded into a data register, where it is automatically compared with data previously stored in over/undertemperature alarm registers and the critical register (Figure 1).

Fan Controller and Remote Temperature Sensor with SMBus Serial Interface

The PWM or DAC fan control circuitry is completely independent from the temperature measurement, and software closes the temperature-control feedback loop (Figure 2).

ADC and Multiplexer

The ADC is an averaging type that integrates over a 62ms period (typ), with excellent noise rejection. The multiplexer automatically steers bias currents through the remote diode, measures the forward voltage, and calculates the temperature.

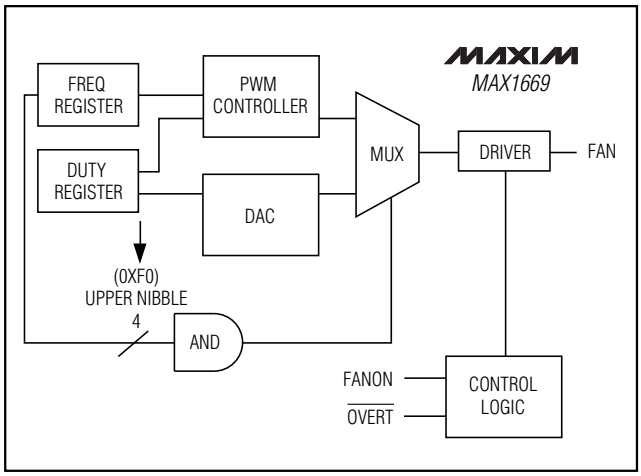


Figure 2. MAX1669 Fan-Control Functional Diagram

The DXN input is biased at 0.7V above ground by an internal diode to set up the analog-to-digital (A/D) inputs for a differential measurement. The worst-case DXP-DXN differential input voltage range is 0.21V to 0.95V. Diode voltages that are outside the ADC input range cause overrange indications rather than non-monotonic readings. Overrange readings will return +127°C. Excess resistance in series with the remote diode causes approximately +1/2°C error/Ω. Likewise, 200µV of offset voltage forced on DXP-DXN causes approximately +1°C error.

A/D Conversion Sequence

When the device is taken out of standby mode, the result of the measurement is available one conversion time later (78ms max). If the ADC is busy, the results of the previous conversion are always available. Toggling the standby mode on and off is a good way to initiate a new conversion since this action resets the rate timer.

Low-Power Standby Mode

Supply-current drain during the 62ms conversion period is 500µA. Between conversions, the instantaneous supply current is 18µA. In standby mode, supply current drops to 3µA and the fan output is disabled.

SMBus Digital Interface

From a software perspective, the MAX1669 appears as a set of byte-wide registers that contain temperature data, alarm threshold values, or control bits. A standard SMBus 2-wire serial interface is used to read temperature data and write control bits and alarm threshold data.

The MAX1669 employs four standard SMBus protocols: write byte, read byte, send byte, and receive byte (Figure 3). The two shorter protocols (receive and send) allow quicker transfers, provided that the correct data register was previously selected by a write or read byte instruction. Use caution with the shorter protocols in multimaster systems since a second master could overwrite the command byte without informing the first master.

The temperature data format is 7 bits plus sign in two's complement form for each channel, with the LSB representing +1°C (Table 1), MSB transmitted first. Measurements are offset by +1/2°C to minimize internal rounding errors; for example, +99.5°C to +100.4°C is reported as +100°C.

Alarm Threshold Registers

Three registers store alarm threshold data, with high-temperature (T_{HIGH}) and low-temperature (T_{LOW}) registers that activate the $\overline{ALERT}$ output, and a critical overtemperature register (T_{CRIT}) that activates the $\overline{OVERT}$ output. If a measured temperature equals or exceeds the T_{HIGH} or T_{LOW} threshold value, an $\overline{ALERT}$ interrupt is asserted. Do not set the T_{CRIT} register to values outside of the temperatures in Table 1.

The power-on-reset (POR) state of the T_{HIGH} register is full scale (0111 1111b or +127°C). The POR state of the T_{LOW} register is 1100 1001b or -55°C. The POR state of the T_{CRIT} register is 0110 0100b or +100°C.

$\overline{OVERT}$ Thermostat Output

The $\overline{OVERT}$ output is a self-clearing interrupt output that is activated when the temperature equals or exceeds T_{CRIT}. $\overline{OVERT}$ normally goes low when active, but this polarity can be changed through the configuration register. The latch is cleared when the temperature reading is equal to or less than T_{CRIT} minus 5°C, which provides for 5°C of hysteresis.

The $\overline{ALERT}$ and $\overline{OVERT}$ comparisons are made after each conversion, and at the end of a write command to their respective temperature limit registers. For example, if the limit is changed while the device is in standby

Write Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
1	7 bits	1	1	8 bits	1	8 bits	1	1

7-bit slave address: equivalent to chip-select line

Command byte: selects which register you are writing to

Data byte: data goes into the register set by the command byte (to set thresholds, configuration masks, and sampling rate)

Read Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	RD	ACK	DATA	$\overline{A}$	P
1	7 bits	1	1	8 bits	1	1	7 bits	1	1	8 bits	1	1

Slave address: equivalent to chip-select line

Command byte: selects which register you are reading from

Slave address: repeated due to change in data-flow direction

Data byte: reads from the register set by the command byte

S = Start condition *Shaded = Slave transmission*
P = Stop condition *$\overline{A}$ = Not acknowledged*

Figure 3. SMBus Protocols

Table 1. Data Format (Two's Complement)

TEMP (°C)	ROUNDED TEMP (°C)	DIGITAL OUTPUT DATA BITS		
		SIGN	MSBs	LSBs
+130.00	+127	0	111	1111
+127.00	+127	0	111	1111
+126.50	+127	0	111	1111
+126.00	+126	0	111	1110
+25.25	+25	0	001	1001
+0.50	+1	0	000	0001
+0.25	+0	0	000	0000
+0.00	+0	0	000	0000
-0.25	+0	0	000	0000
-0.50	+0	0	000	0000
-0.75	-1	1	111	1111
-1.00	-1	1	111	1111
-25.00	-25	1	110	0111
-25.50	-26	1	110	0110
-54.75	-55	1	100	1001
-55.00	-55	1	100	1001
-65.00	-65	1	011	1111
-70.00	-65	1	011	1111

mode, the $\overline{ALERT}$ and $\overline{OVERT}$ outputs respond correctly according to the last valid A/D result.

Note that the $\overline{ALERT}$ output does not respond to T_{CRIT} ($\overline{OVERT}$) comparisons.

The $\overline{OVERT}$ latch can implement an override control to the FAN output, which forces the fan to V_{CC} whenever the T_{CRIT} threshold is crossed. This override switch is the backup fan control loop, and is enabled through the FAN ON bit in the configuration register (bit 2). Note that changing the duty to 100% in this way doesn't affect the contents of the DUTY register, and the FAN output reverts to the preprogrammed duty factor (or DAC voltage) when the $\overline{OVERT}$ latch is reset.

Diode Fault Alarm

A continuity fault detector at DXP detects whether the remote diode has an open-circuit condition, short-circuit to GND, or short-circuit DXP-to-DXN condition. At the beginning of each conversion, the diode fault is checked and the status byte updated. This fault detector is a simple voltage detector; DXP rising above V_{CC} - 1V or falling below DXN + 40mV constitutes a fault condition. Also, if the ADC has an extremely low differential input voltage, the diode is assumed to be shorted and a fault occurs. Note that the diode fault isn't checked until a conversion is initiated, so immediately after power-on reset the status byte indicates no fault is present even if the diode path is broken. Any diode fault will return a +127°C fault reading and cause $\overline{ALERT}$ to go low.

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$\overline{\text{ALERT}}$ Interrupts

The $\overline{\text{ALERT}}$ interrupt output signal is latched and can only be cleared by reading the Alert Response address. Interrupts are generated in response to T_{HIGH} and T_{LOW} comparisons, when there is a fault with the remote diode, or when a high-to-low or low-to-high transition at I/O1 or I/O2 is detected.

The interrupt does not halt automatic conversions; new temperature data continues to be available over the SMBus interface after $\overline{\text{ALERT}}$ is asserted. The interrupt output is open-drain so that devices can share a common interrupt line. The interface responds to the SMBus Alert Response address, an interrupt pointer return-address feature (see the *Alert Response Address* section).

The $\overline{\text{ALERT}}$ interrupt latch is set when the temperature exceeds an ALARM threshold. $\overline{\text{ALERT}}$ will not be set again until the threshold is reprogrammed. This prevents the $\overline{\text{ALERT}}$ latch from being set again during the interval between reading the Alert Response address and updating the offending alarm threshold. Note that this behavior is identical to the MAX1618 but is slightly different from the MAX1617, which continues to interrupt until the temperature no longer exceeds the alarm threshold. Note also that if some new alarm condition occurs, such as crossing the other alarm threshold or having a GPIO transition, a new interrupt is generated.

ALERT Response Address

The SMBus Alert Response interrupt pointer provides quick fault identification for simple slave devices that lack the complex, expensive logic needed to be a bus master. Upon receiving an $\overline{\text{ALERT}}$ interrupt signal, the host master can broadcast a receive byte transmission to the Alert Response slave address (0001100b). Then any slave device that generated an interrupt attempts to identify itself by putting its own address on the bus (Table 2).

The Alert Response can activate several different slave devices simultaneously, similar to the I^2C General Call. If more than one slave attempts to respond, bus arbitration rules apply, and the device with the lower address code wins. The losing device does not generate an acknowledge and continues to hold the $\overline{\text{ALERT}}$ line low until serviced. Successful reading of the alert response address clears the interrupt latch.

Command Byte Functions

The 8-bit command byte register (Table 3) is the master index that points to the MAX1669's other registers. The register's POR state is 00000001b, so a receive byte transmission (a protocol that lacks the command byte) that occurs immediately after POR returns the current remote temperature data.

Table 2. Read Format for the Alert Response Address (0001100b)

BIT	NAME	FUNCTION
7 (MSB)	ADD7	Provide the MAX1669 slave address
6	ADD6	
5	ADD5	
4	ADD4	
3	ADD3	
2	ADD2	
1	ADD1	
0 (LSB)	1	Logic 1

One-Shot Conversion

The one-shot command immediately forces a new conversion cycle to begin. In software standby mode (STBY bit = 1), a new conversion starts, after which the device returns to standby mode. If a conversion is in progress when a one-shot command is received, the command is ignored. If a one-shot command is received in autoconvert mode (STBY bit = 0) between conversions, a new conversion begins, the conversion rate timer is reset, and the next automatic conversion takes place after a full period.

Configuration Byte Functions

The configuration byte register (Table 4) is used to mask (disable) interrupts, set the $\overline{\text{OVERT}}$ output polarity, and put the device in software standby mode. Bit 1 of the configuration byte in Table 4 is for factory use only and must be set to 1 (value at POR). This register's contents can be read back over the serial interface.

FAN PWM Frequency and Duty Factor Control

The fan speed is controlled by the average voltage applied to the fan. The average voltage is equal to the product of the motor power-supply voltage and the duty factor. The duty factor is equal to zero upon start-up and it is software controlled. The FAN output frequency is controlled by the PWM frequency register unless this register's code is set to 1111b (Table 5). A PWM frequency code of 1111b puts the FAN output in DAC mode. For all other codes, the FAN frequency is in the 20Hz to 160Hz range as shown in Table 5. For the possible synchronized frequencies, also see Table 5. The FAN output duty factor is controlled by the FAN duty factor register unless the PWM frequency code is

Table 3. Command Byte Bit Assignments

REGISTER	COMMAND	POR STATE	FUNCTION
	00h	N/A	Reserved for future use
RTEMP	01h	N/A	Read latest temperature
RSTAT	02h	N/A	Read status byte (temp flags, I/O_ states)
RCFG	03h	0000 0010b	Read configuration byte
	04h	N/A	Reserved for future use
	05h	N/A	Reserved for future use
	06h	N/A	Reserved for future use
RHI	07h	0111 1111b	Read T_{HIGH} limit
RLOW	08h	1100 1001b	Read T_{LOW} limit
WCFG	09h	N/A	Write configuration byte
	0Ah	N/A	Reserved for future use
	0Bh	N/A	Reserved for future use
	0Ch	N/A	Reserved for future use
WHI	0Dh	N/A	Write T_{HIGH} limit
WLOW	0Eh	N/A	Write T_{LOW} limit
OSHT	0Fh	N/A	One-shot command. Will execute a single conversion even if the device is in software standby.
RCRIT	10h	0110 0100b	Read T_{CRIT} limit
RPROT	11h	0000 0000b	Read write-once protection byte
RFREQ	12h	0000 0000b	Read PWM frequency
RDUTY	13h	0000 0000b	Read FAN duty factor
RGPIO	14h	1100 0000b	Read GPIO data
	15h	N/A	Reserved for future use
	16h	N/A	Reserved for future use
	17h	N/A	Reserved for future use
WCRIT	18h	N/A	Write T_{CRIT} limit
WPROT	19h	N/A	Write write-once protection byte
WFREQ	1Ah	N/A	Write PWM frequency
WDUTY	1Bh	N/A	Write FAN duty factor
WGPIO	1Ch	N/A	Write GPIO data
RFU	1Dh-FDh	N/A	Reserved for future use
ID Codes			
MFG ID	FEh	Least Sig Byte 0100 1101b	Manufacturing ID code = 4Dh, ASCII code for “M” (for Maxim)
DEV ID	FFh	Least Sig Byte 0000 0101b	Device ID code, specific to MAX1669

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Table 4. Configuration Byte Bit Assignments

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	MASK0	0	Masks T_{HIGH}, T_{LOW}, and diode fault $\overline{ALERT}$ interrupts when high. If all three MASK_ bits are set high, $\overline{ALERT}$ interrupts are totally masked.
6	STBY	0	Standby mode control bit. If high, the device immediately stops converting, forces FAN low, and enters standby mode. If low, the device continuously autoconverts at a 2Hz rate.
5	POL	0	$\overline{OVERT}$ pin polarity control: 0 = active low (low when T_{CRIT} is crossed) 1 = active high
4	MASK1	0	Masks I/O1 $\overline{ALERT}$ interrupts when high. Set MASK1 = 1 and connect a 10k to 100k pull-up resistor on I/O1 to configure I/O1 as an output.
3	MASK2	0	Masks I/O2 $\overline{ALERT}$ interrupts when high. Set MASK2 = 1 and connect a 10k to 100k pull-up resistor on I/O2 to configure I/O2 as an output.
2	FAN ON	0	Enables FAN duty factor override when high.
1		1	Must be “1”
0	RFU	0	Reserved for future use

Table 5. PWM Frequency Data Byte Bit Assignments (Write Command = 1Ah)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	F3	0	Frequency control bit. F3–F0 are decoded as follows: **F3–F0 / Frequency (SYNC = GND) / Synchronized Frequency (SYNC Clocked)** 0000b / 20Hz / f_{SYNC}/13100 0001b / 30Hz / f_{SYNC}/8730 0010b / 40Hz / f_{SYNC}/6550 0011b / 50Hz / f_{SYNC}/5240 0100b / 60Hz / f_{SYNC}/4370 0101b / 70Hz / f_{SYNC}/3740 0110b / 80Hz / f_{SYNC}/3270 0111b / 90Hz / f_{SYNC}/2910 1000b / 100Hz / f_{SYNC}/2620 1001b / 110Hz / f_{SYNC}/2380 1010b / 120Hz / f_{SYNC}/2180 1011b / 130Hz / f_{SYNC}/2020 1100b / 140Hz / f_{SYNC}/1870 1101b / 150Hz / f_{SYNC}/1750 1110b / 160Hz / f_{SYNC}/1640 1111b / DAC Mode
6	F2	0	Frequency control bit
5	F1	0	Frequency control bit
4	F0	0	Frequency control bit
3–0	RFU	0	Reserved for future use

set to 1111b. The FAN duty factor can be selected from 0% to 100% in increments of 6.67%.

FAN Output in DAC Mode

If the PWM frequency register is set to code 1111b, the DAC is multiplexed to the FAN output and the FAN duty factor register (Table 6) now controls the DAC output voltage rather than the duty factor. In DAC mode, the output swing is 0 to 0.94 • V_{CC} (out of 4 bits of resolution). To ensure a smooth transition, make sure that the FAN duty factor code is 0000b prior to setting the PWM frequency code for DAC mode (1111b). External circuitry must accept an initial FAN DAC voltage of 0.

Table 6. Fan Duty-Factor Data Byte Bit Assignments (Write Command = 1Bh)

BIT	NAME	NAME	FUNCTION
7 (MSB)	D3	0	FAN duty-factor control bit. D3–D0 are decoded as follows: **D3–D0 / Duty / V_{OUT} (nominal)** 0000b / 0% / 0V 0001b / 6.67% / 0.0625 • V_{CC} 0010b / 13.33% / 0.125 • V_{CC} 0011b / 20% / 0.1875 • V_{CC} 0100b / 26.67% / 0.25 • V_{CC} 0101b / 33.33% / 0.3125 • V_{CC} 0110b / 40% / 0.375 • V_{CC} 0111b / 46.67% / 0.4375 • V_{CC} 1000b / 53.33% / 0.5 • V_{CC} 1001b / 60% / 0.5625 • V_{CC} 1010b / 66.67% / 0.625 • V_{CC} 1011b / 73.33% / 0.6875 • V_{CC} 1100b / 80% / 0.75 • V_{CC} 1101b / 86.67% / 0.8125 • V_{CC} 1110b / 93.33% / 0.875 • V_{CC} 1111b / 100% / 0.9375 • V_{CC}
6	D2	0	FAN duty-factor control bit
5	D1	0	FAN duty-factor control bit
4	D0	0	FAN duty-factor control bit
3–0	RFU	0	Reserved for future use

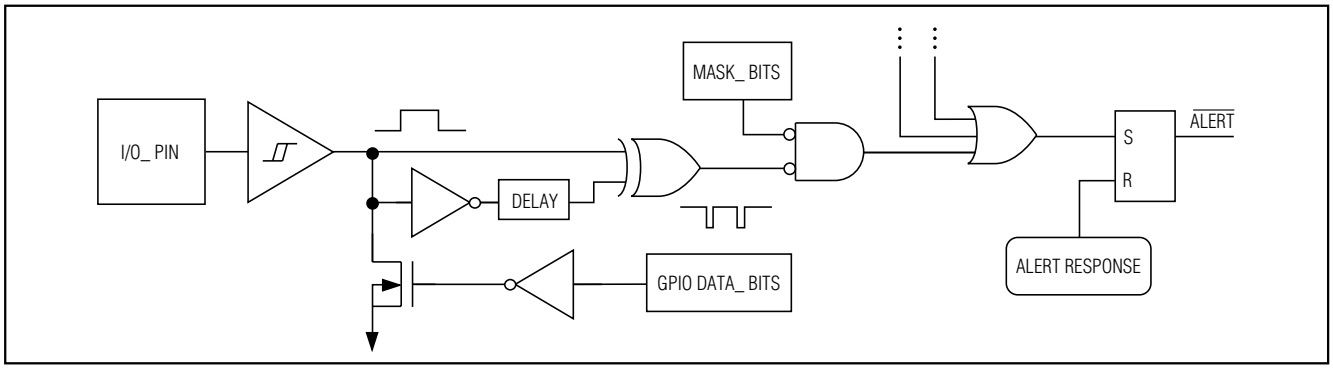

Figure 4. GPIO Logic Diagram

GPIO Data Register

I/O1 and I/O2 are configured through the GPIO data register and CONFIG byte register (Table 7 and Table 3). Upon power-up, the GPIOs are set as inputs. To ensure the I/Os are configured as inputs, set the state of the DATA1 and DATA2 bits high within the GPIO data register for I/O1 and I/O2, respectively. Figure 4 shows that by setting the GPIO DATA_ bits high, the open-drain FET connected to the I/O_ pins goes high impedance. Next, clear the MASK1 and MASK2 bits low within the CONFIG byte register to remove the masks on the $\overline{\text{ALERT}}$ interrupts for I/O1 and I/O2, respectively.

To use I/O1 or I/O2 as an output, first set the MASK1 and MASK2 bits high, respectively. Setting the MASK_ bits high within the CONFIG byte register masks out the corresponding I/O $\overline{\text{ALERT}}$ interrupts. Since the internal FETs are open-drain, a pull-up resistor is required from I/O_ to V_{CC}. The DATA1 and DATA2 bits within the GPIO data register directly control the state of the outputs of I/O1 and I/O2, respectively (Figure 4).

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Table 7. GPIO Input/Output Data Byte Bit Assignments

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	DATA1	1	For I/O1 configured as an output (MASK1 bit set high and a pull-up resistor on I/O1), this bit corresponds to the GPIO DATA1 block in Figure 4 and controls the output state of I/O1. To configure I/O1 as an input, set this bit high and clear the MASK1 bit low (Figure 4).
6	DATA2	1	For I/O2 configured as an output (MASK2 bit set high and a pull-up resistor on I/O2), this bit corresponds to the GPIO DATA2 block in Figure 4 and controls the output state of I/O2. To configure I/O2 as an input, set this bit high and clear the MASK2 bit low (Figure 4).
5–0	RFU	0	Reserved for future use

Table 8. Write-Once Protection Byte Bit Assignments

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	PROT1	0	Write-protects the T_{CRIT} limit threshold register when high.
6	PROT2	0	Write-protects certain bits in the configuration register when high: - STBY standby-mode control (bit 6) - POL polarity control (bit 5) - FAN ON control (bit 2)
5	PROT3	0	Write-protects bit 7 in the GPIO register when high (DATA1).
4	PROT4	0	Write-protects bit 6 in the GPIO register when high (DATA2).
3–0	RFU	0	Reserved for future use

Write-Once Protection

Write-once protection allows the host BIOS code to configure the MAX1669 and protect against data corruption in the host that might cause spurious writes to the MAX1669. In particular, write protection allows a foolproof overtemperature override that forces the fan on, independent of the host system whether in DAC mode or PWM mode. The bits in the write-protection register (Table 8), once set high, cannot be reset low except by power-on reset.

Having a separate write-protect master register rather than making the actual registers themselves write once allows the host to read back and verify each register's contents before applying final write protection. Having individual write-protect control over different registers allows flexibility in application; for example, the T_{CRIT} and configuration register could be protected while leaving one or both GPIO outputs free to be used as actuators.

Status Byte Functions

The status byte register (Table 9) indicates which (if any) temperature thresholds have been exceeded. The status byte also indicates changes in GPIO states and transitions and whether there is a fault in the remote diode DXP-DXN path. After POR, the normal state of all the flag bits is 0, assuming none of the alarm conditions are present. Bits 2 to 5 of the status byte are cleared by *any* successful read of the status byte. Note that the $\overline{\text{ALERT}}$ interrupt latch is not automatically cleared when the status flag bit is cleared.

Manufacturer and Device ID Codes

This code identifies the functional capabilities of a particular device. New devices having enhanced or reduced software or hardware capabilities must be assigned a new code. The device ID allows the host system to interrogate the device to determine its capabilities, and use extra features if they're available. The device ID code is 2 bytes, for a total of 256X256 possible combinations. The device ID codes are located at command code 1111 1111b (FFh). If a read-byte operation (as opposed to a read-word) is applied to the device, it returns the least-significant byte correctly without the most-significant byte. Table 10 shows the device ID code for the MAX1669.

Table 9. Status Byte Bit Assignments

BIT	NAME	FUNCTION
7 (MSB)	I/O1	This bit indicates the current state of I/O1 (unlatched).
6	I/O2	This bit indicates the current state of I/O2 (unlatched).
5	TRAN1*	This bit is set if a low-to-high or high-to-low transition has occurred at I/O1 (regardless of the state of the mask bits).
4	TRAN2*	This bit is set if a low-to-high or high-to-low transition has occurred at I/O2 (regardless of the state of the mask bits).
3	RHIGH*	A high indicates that the high-temperature alarm has activated
2	RLOW*	A high indicates that the low-temperature alarm has activated.
1	DIODE	A high indicates a remote-diode fault (open-circuit, shorted diode, or DXP short to GND).
0 (LSB)	OVERT	When the T_{CRIT} threshold is crossed, this bit goes high. The polarity of this bit does not depend on the POL bit (bit 5 in configuration byte).

**TRAN1 and TRAN2 alarm flags stay high until cleared by POR or until the status byte register is read. RHIGH and RLOW alarm flags stay high until cleared by POR or the temperature fault is removed and the status byte is read.*

Table 10. Device ID Code

MAX1669 ID CODE	
LS BYTE LSBs MSBs	MS BYTE LSBs MSBs
0000 0101	0000 0000

Table 11. Slave Address Decoding (ADD_ Pins)

ADD0	ADD1	ADD2	ADDRESS
GND	GND	GND	0011 000b
GND	GND	V_{CC}	0011 001b
GND	V_{CC}	GND	0011 010b
GND	V_{CC}	V_{CC}	0101 001b
V_{CC}	GND	GND	0101 010b
V_{CC}	GND	V_{CC}	0101 011b
V_{CC}	V_{CC}	GND	1001 100b
V_{CC}	V_{CC}	V_{CC}	1001 101b

Slave Addresses

The MAX1669 appears to the SMBus as one device having a common address for the temperature sensor section, GPIO section, and fan-control section. The device address can be set to one of eight different values by pin-strapping ADD_ pins so that more than one MAX1669 can reside on the same bus without address conflicts (Table 11).

The MAX1669 also responds to the SMBus Alert Response slave address (see the *Alert Response Address* section).

POR and UVLO

The MAX1669's memory is volatile. To prevent ambiguous power-supply conditions from corrupting the data in memory and causing erratic behavior, a POR voltage detector monitors V_{CC} and clears the memory if V_{CC} falls below 1.85V (typical, see the *Electrical Characteristics* table). When power is first applied and V_{CC} rises above 1.9V (typ), the logic blocks begin operating; although reads and writes at V_{CC} levels below 3V are not recommended. A second V_{CC} comparator, the ADC UVLO comparator, prevents the ADC from converting until there is sufficient headroom (V_{CC} = 2.8V typ).

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Power-Up Defaults

- Interrupt latch is cleared.
- ADC begins autoconverting at a 2Hz rate.
- Command byte is set to 01h to facilitate quick remote receive-byte queries.
- T_{HIGH} and T_{LOW} registers are set to +127°C and -55°C limits, respectively.
- T_{CRIT} register is set to +100°C.
- $\overline{ALERT}$ and $\overline{OVERT}$ are reset to high-Z state.
- Device is in low-frequency PWM mode, 20Hz setting.
- PWM output is off (duty factor set to 0%).
- I/O1, I/O2 are high-Z (configured as inputs).

Applications Information

Remote Diode Selection

Temperature accuracy depends on having a good-quality, diode-connected, small-signal transistor. Accuracy has been experimentally verified for all of the devices listed in Table 12. The MAX1669 can also directly measure the die temperature of CPUs and other ICs having on-board temperature-sensing diodes, such as the Intel Pentium II.

The transistor must be a small-signal type having a relatively high forward voltage; otherwise, the A/D input voltage range can be violated. The forward voltage must be greater than 0.25V at 10µA; check to ensure this is true at the highest expected temperature. The forward voltage must be <0.95V at 100µA; check to ensure this is true at the lowest expected temperature. Do not use large power transistors. Also, ensure that the base resistance is <100Ω. Tight specifications for forward-current gain (+50 to +150, for example) indicate that the manufacturer has good process controls and the devices have consistent V_{BE} characteristics.

Series resistance causes +1/2°C error per ohm. When monitoring the temperature of a remote unit's internal diode, ensure that trace series resistance does not introduce significant error.

ADC Noise Filtering

The ADC is an integrating type with inherently good noise rejection, especially of low-frequency signals such as 60Hz/120Hz power-supply hum. Micropower operation places constraints on high-frequency noise rejection; therefore, careful PC board layout and proper external noise filtering is required for high-accuracy remote measurements in electrically noisy environments.

High-frequency EMI is best filtered at DXP and DXN with an external 2200pF capacitor. This value can be increased to about 3300pF (max), including cable capacitance. Capacitance higher than 3300pF introduces errors due to the rise time of the switched-current source.

Nearly all noise sources tested cause the ADC measurements to be higher than the actual temperature, typically by +1°C to +10°C, depending on frequency and amplitude (see *Typical Operating Characteristics*).

FAN Application Circuits

In PWM mode, the output impedance at FAN is <50Ω, enabling it to drive an N-channel MOSFET as shown in the *Typical Operating Circuit*. Return the source of the N-channel MOSFET to the system power ground, away from the ground of the MAX1669. For 3.3V applications, use low-threshold N-channel MOSFETs (Table 1).

In DAC mode, the FAN output can be linearly controlled (Figure 5). Upon power-up, the fan is off. The N-channel MOSFET is biased at the threshold of turning on. As V_{FAN} rises, the fan turns on linearly. To have the fan turned on at power-up, use the circuit shown in Figure 6.

Table 12. Component Manufacturers

MANUFACTURER	MODEL NUMBER
SOT23 BJT	
Central Semiconductor (USA)	CMPT3906
Fairchild Semiconductor (USA)	MMBT3906
Motorola (USA)	MMBT3906
Rohm Semiconductor (Japan)	SST3906
Samsung (Korea)	KST3906
MOSFET N-CHANNEL	
International Rectifier (USA)	IRF7201
Fairchild Semiconductor (USA)	FDN359AN
MOSFET P-CHANNEL	
International Rectifier (USA)	IRF7205

Note: *Transistors must be diode-connected (base shorted to collector).*

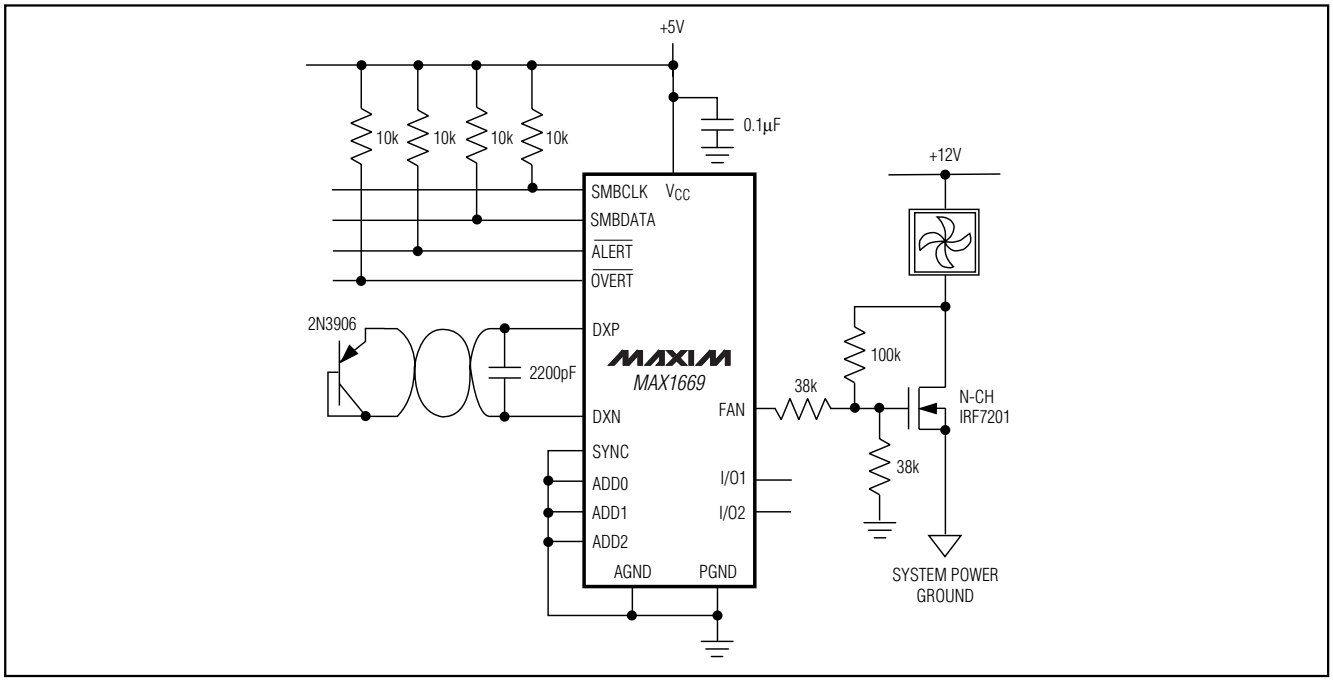


Figure 5. Linear Fan Control (DAC Mode) with Fan "Off" at Power-Up

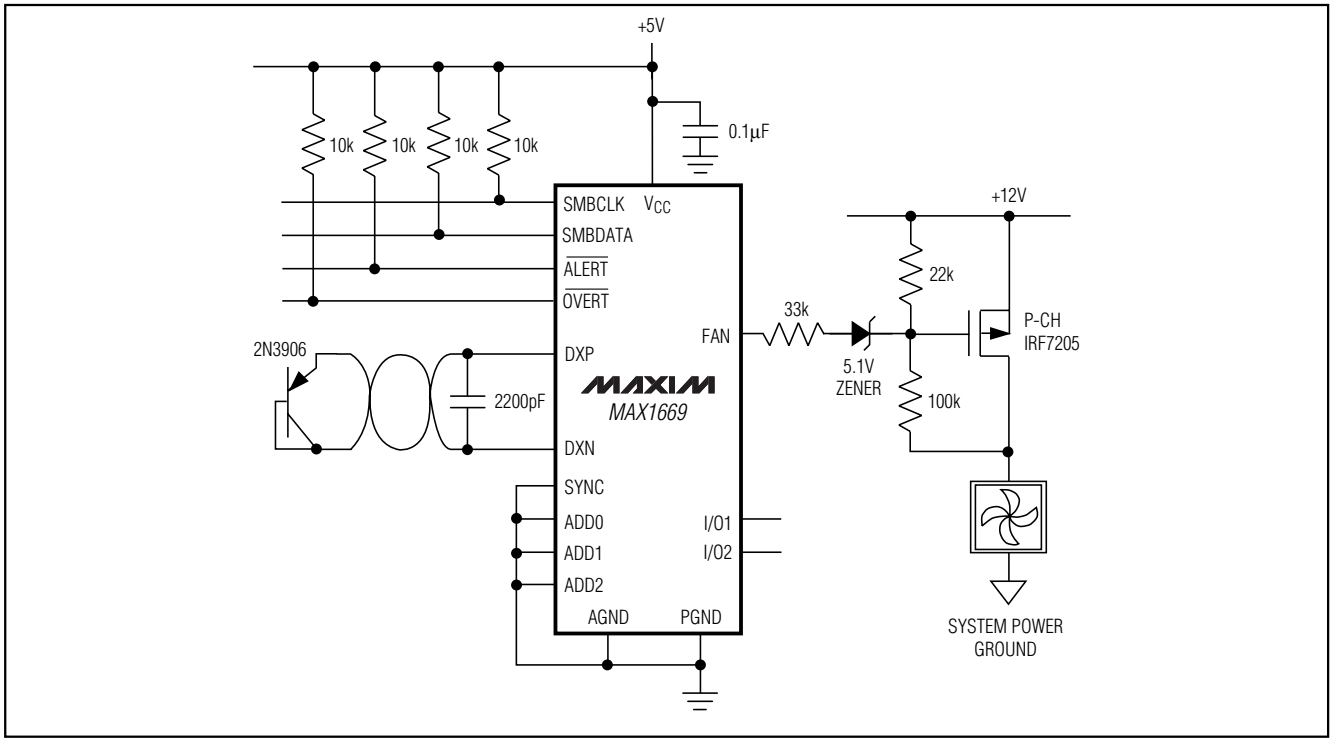
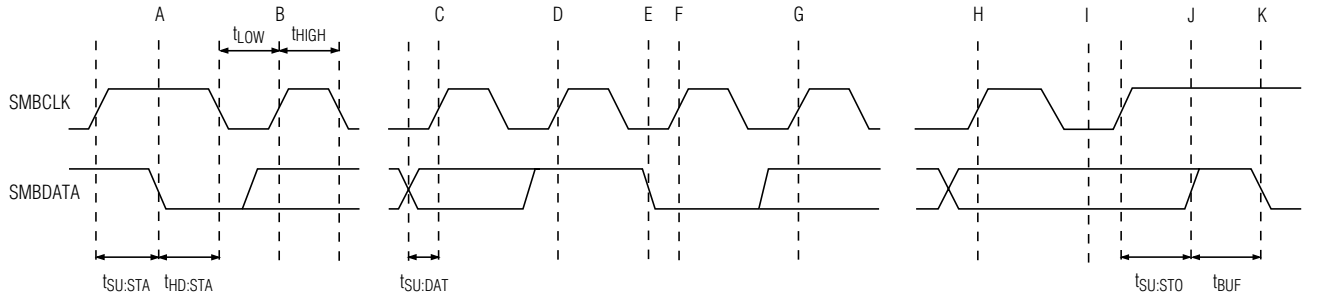


Figure 6. Linear Fan Control (DAC Mode) with Fan "On" at Power-Up

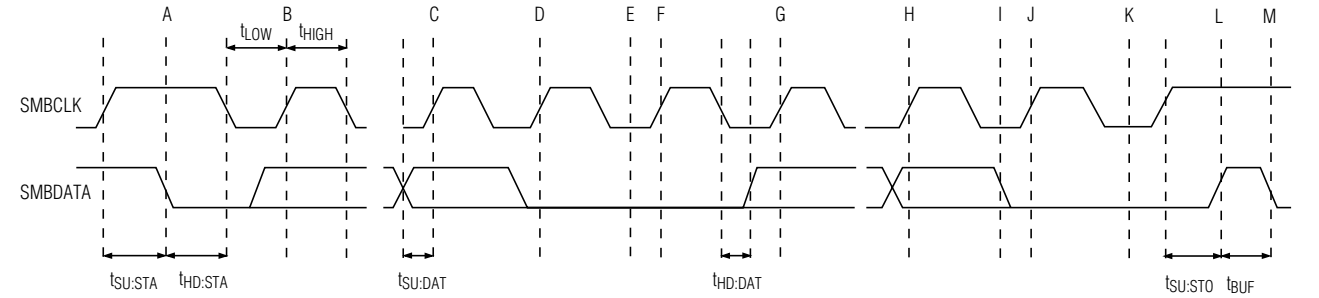


A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/$\overline{W}$ BIT CLOCKED INTO SLAVE

E = SLAVE PULLS SMBDATA LINE LOW
F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO MASTER
H = LSB OF DATA CLOCKED INTO MASTER

I = ACKNOWLEDGE CLOCK PULSE
J = STOP CONDITION
K = NEW START CONDITION

Figure 7. SMBus Write Timing Diagram



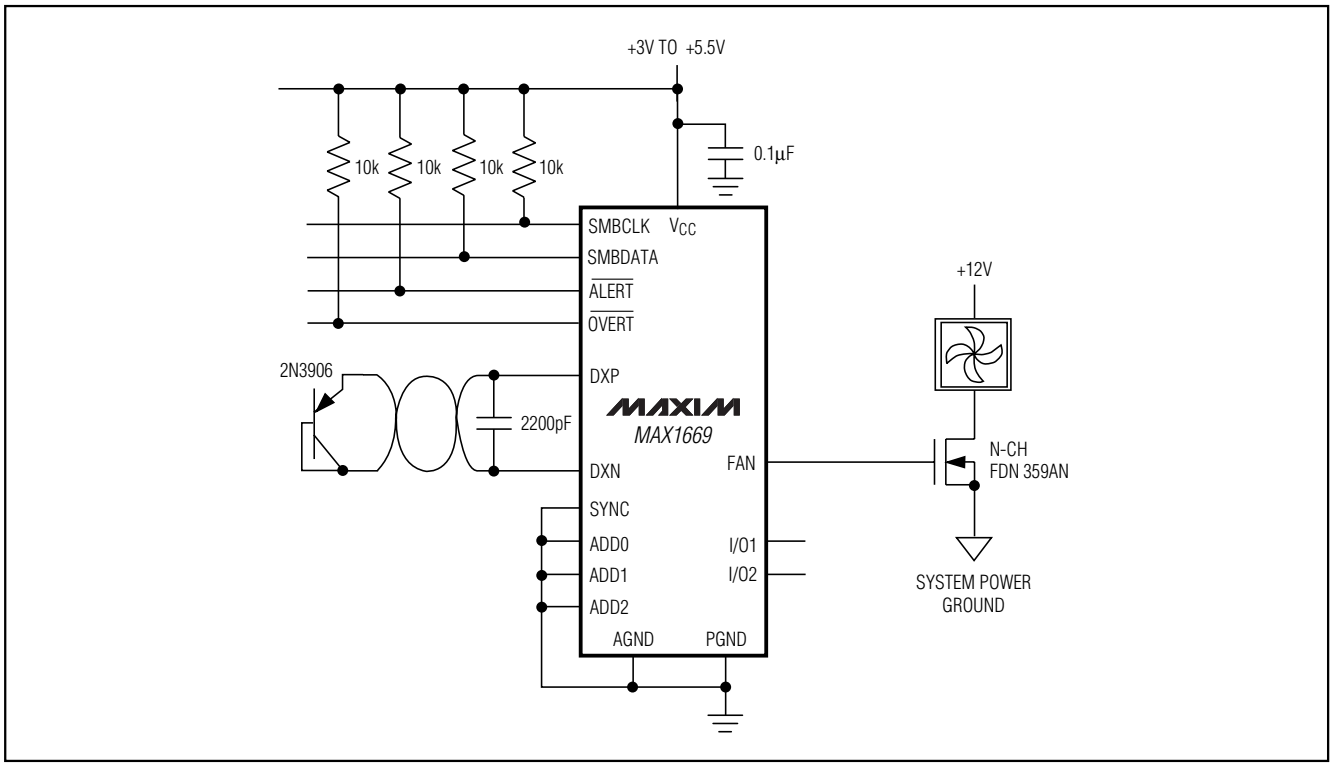
A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/$\overline{W}$ BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW

F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO SLAVE
H = LSB OF DATA CLOCKED INTO SLAVE
I = SLAVE PULLS SMBDATA LINE LOW

J = ACKNOWLEDGE CLOCKED INTO MASTER
K = ACKNOWLEDGE CLOCK PULSE
L = STOP CONDITION, DATA EXECUTED BY SLAVE
M = NEW START CONDITION

Figure 8. SMBus Read Timing Diagram

Typical Operating Circuit



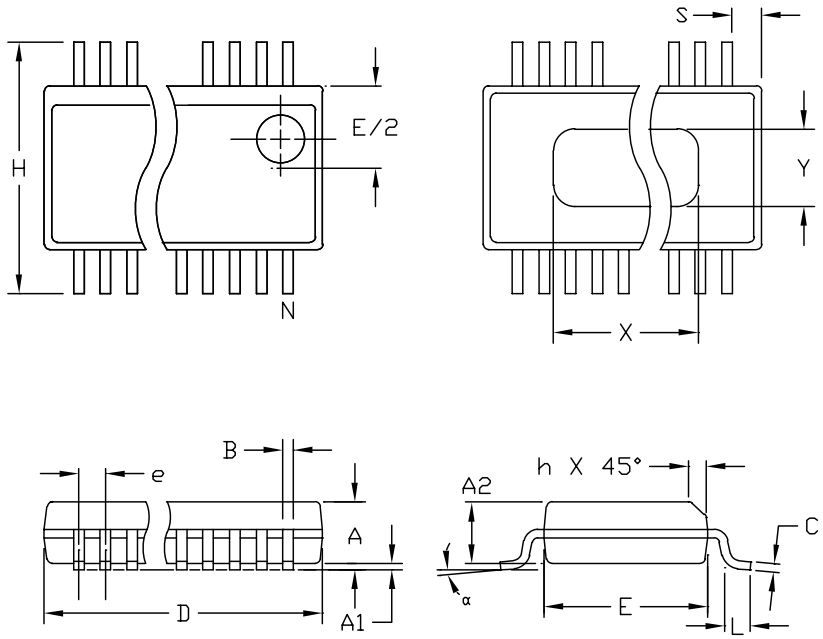
Chip Information

TRANSISTOR COUNT: 12,924

Fan Controller and Remote Temperature Sensor with SMBus Serial Interface

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1

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