

SN54LS846 THRU SN54LS649 SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS190A - DECEMBER 1982 - REVISED MAY 2004

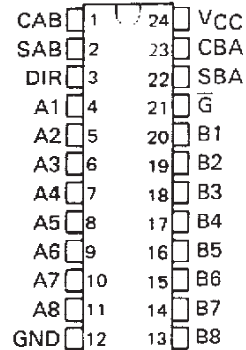
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Included Among the Package Options Are Compact 24-pin 300-mil-Wide Plastic and Ceramic DIPs, Ceramic Chip Carriers, and Plastic "Small Outline" Packages
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'LS646	3-State	True
'LS647	Open-Collector	True
'LS648	3-State	Inverting
'LS649	Open-Collector	Inverting

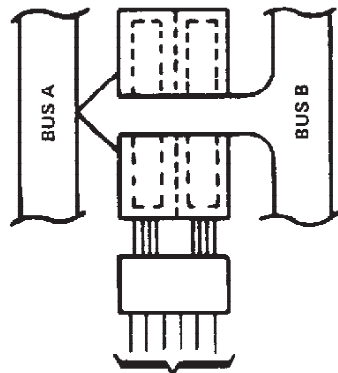
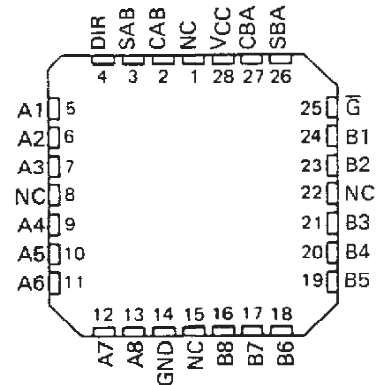
description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

SN54LS'...JT PACKAGE
SN74LS'...DW OR NT PACKAGE
(TOP VIEW)

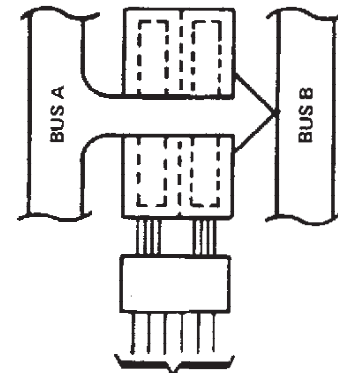


SN54LS'...FK PACKAGE
(TOP VIEW)



(21)	(3)	(1)	(23)	(2)	(22)
$\bar{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



(21)	(3)	(1)	(23)	(2)	(22)
$\bar{G}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

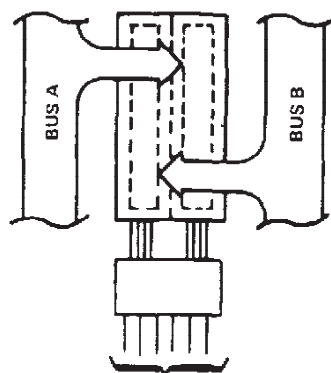
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649

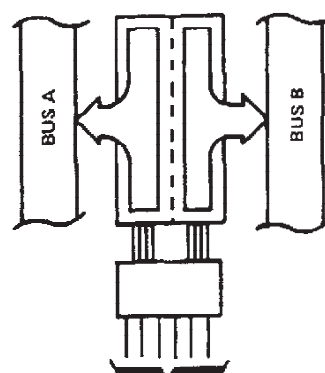
OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS190A – DECEMBER 1982 – REVISED MAY 2004



(21)	(3)	(1)	(23)	(2)	(22)
$\bar{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21)	(3)	(1)	(23)	(2)	(22)
$\bar{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	Hor L	X	H
L	H	Hor L	X	H	X

TRANSFER
STORED DATA
TO A OR B

Enable ($\bar{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\bar{G}$ is active (low). In the isolation mode (control $\bar{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0° to 70°C .

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	LS646, LS647	LS648, LS649
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\bar{B}$ Data to A Bus
L	L	X	Hor L	X	H	Output	Input	Stored B Data to A Bus	Stored $\bar{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\bar{A}$ Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus	Stored $\bar{A}$ Data to B Bus

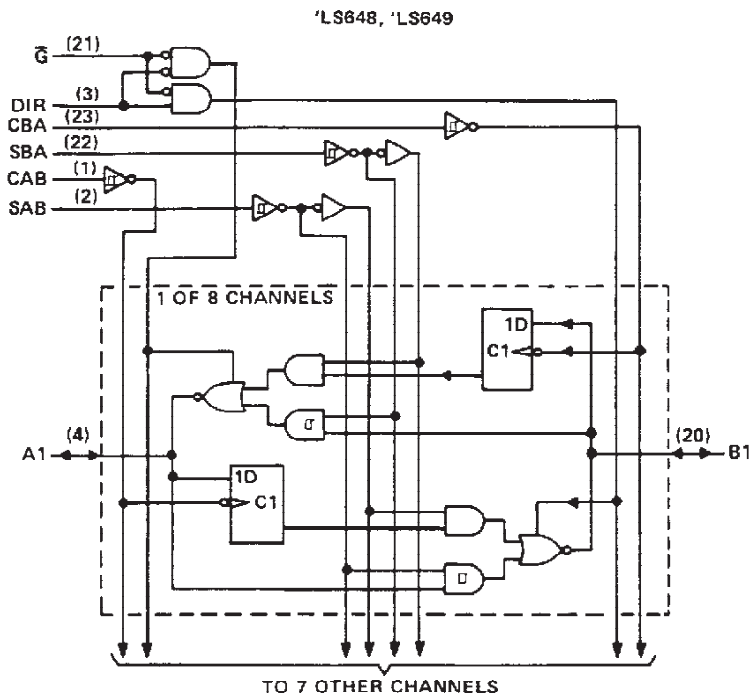
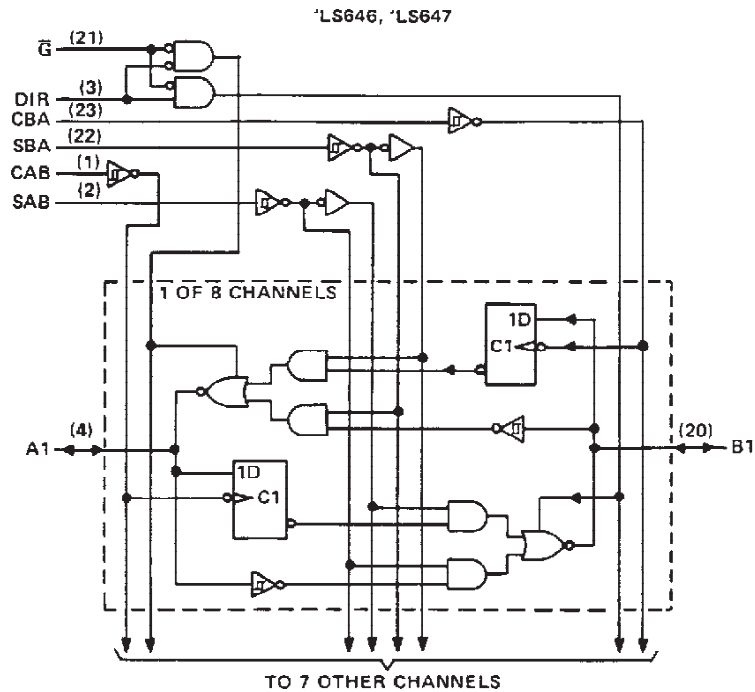
† The data output functions may be enabled or disabled by various signals at the $\bar{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649

OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS190A - DECEMBER 1982 - REVISED MAY 2004

logic diagrams (positive logic)



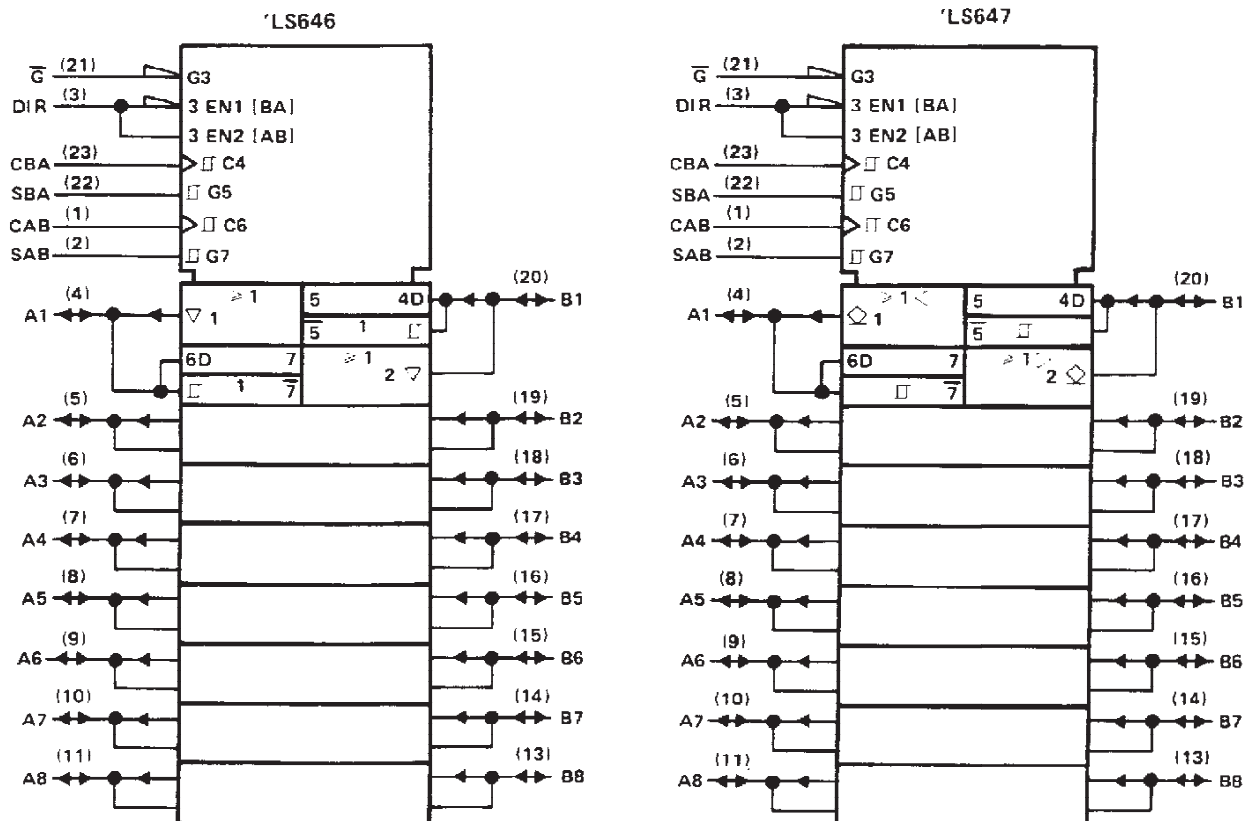
Pin numbers shown are for DW, JT, and NT packages.

SN54LS646, SN54LS647, SN74LS646, SN74LS647

OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS190A – DECEMBER 1982 – REVISED MAY 2004

logic symbols[†]



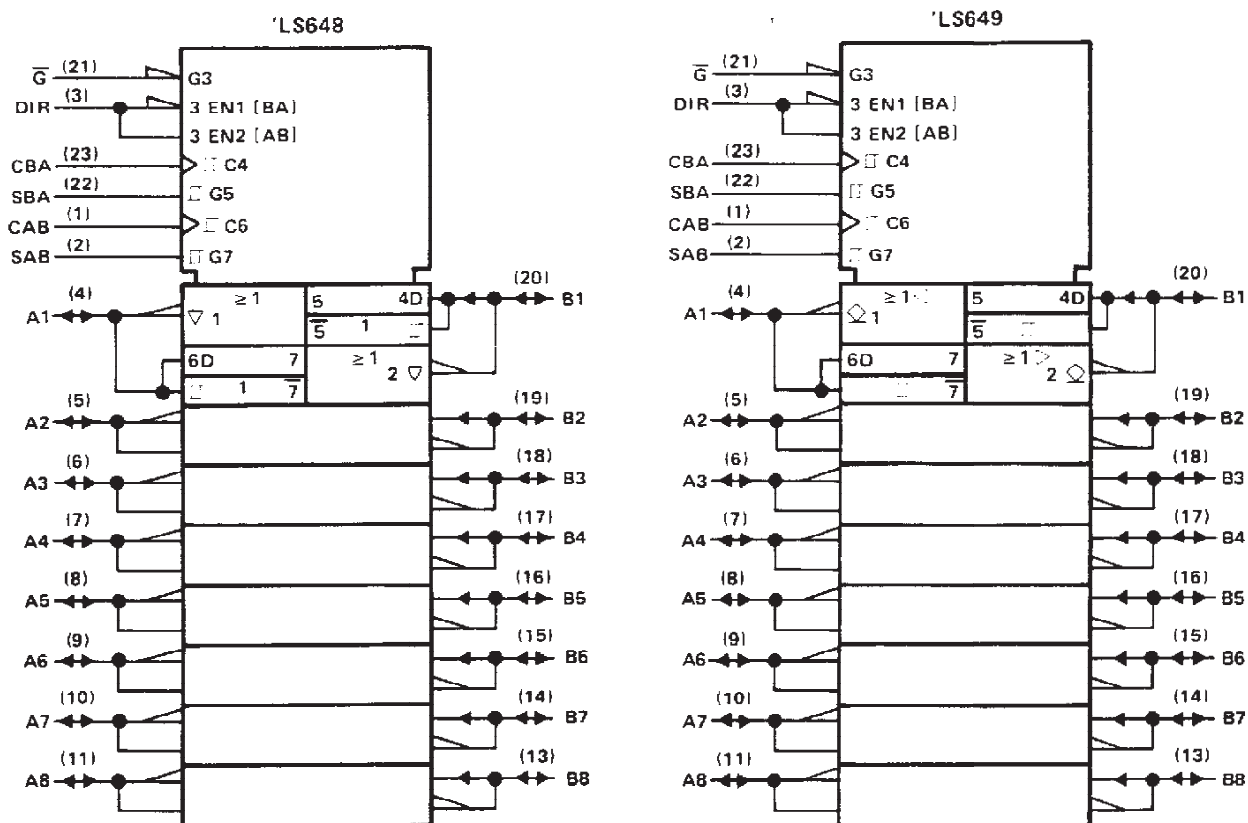
[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

SN54LS648, SN54LS649, SN74LS648, SN74LS649

OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS190A - DECEMBER 1982 - REVISED MAY 2004

logic symbols[†] (continued)

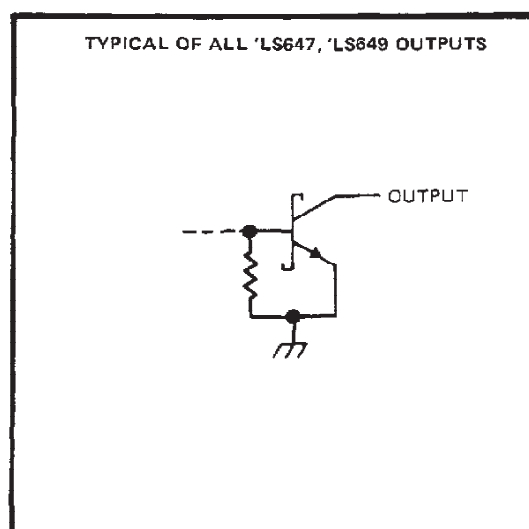
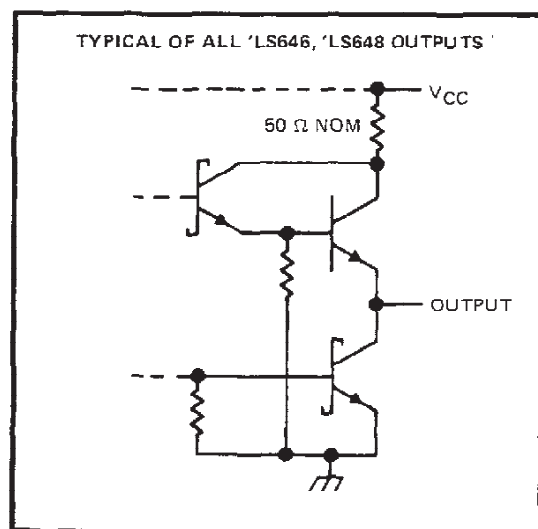
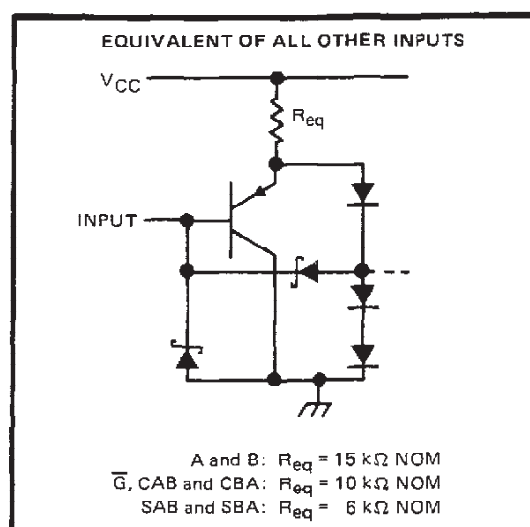
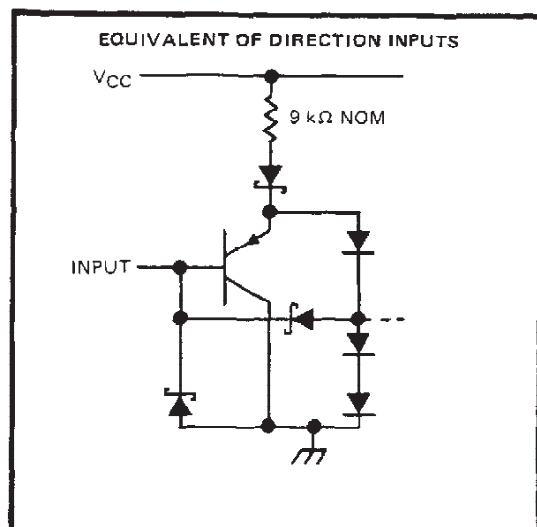


[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

SN54LS646 THRU SN54LS649 SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

SDLS190A - DECEMBER 1982 - REVISED MAY 2004

schematics of inputs and outputs



SN54LS646, SN54LS648, SN74LS646, SN74LS648

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDLS190A - DECEMBER 1982 - REVISED MAY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54LS646, SN54LS648	-55°C to 125°C
SN74LS646, SN74LS648	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			SN54LS646/648			SN74LS646/648			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage				0.5			0.6	V		
I _{OH}	High-level output current				− 12			− 15	mA		
I _{OL}	Low-level output current				12			24	mA		
t _w	Pulse duration	CBA or CAB high	15			15			ns		
		CBA or CAB low	30			30					
		Data high or low	30			30					
t _{su}	Setup time before CAB↑ or CBA↑	A or B	15			15			ns		
t _h	Hold time after CAB↑ or CBA↑	A or B	0			0			ns		
T _A	Operating free-air temperature		− 55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS646/648		SN74LS646/648		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN, I _I = - 18 mA		- 1.5		- 1.5		V
Hysteresis (V _{T+} - V _{T-})	A or B input	V _{CC} = MIN		0.1	0.4	0.2	0.4	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX		I _{OH} = - 3 mA		2.4 3.4		V
				I _{OH} = - 12 mA		2		
				I _{OH} = - 15 mA		2		
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX		I _{OL} = 12 mA		0.25	0.4	V
				I _{OL} = 24 mA		0.35 0.5		
I _I	Control inputs	V _{CC} = MAX, V _I = 7 V		0.1		0.1		mA
	A or B ports	V _{CC} = MAX, V _I = 5.5 V		0.1		0.1		
I _{IH}	Control inputs	V _{CC} = MAX, V _I = 2.7 V		20		20		μA
	A or B ports‡			20		20		
I _{IL}	Control inputs	V _{CC} = MAX, V _I = 0.4 V		- 0.4		- 0.4		mA
	A or B ports‡			- 0.4		- 0.4		
I _{OS} §		V _{CC} = MAX, V _O = 0 V		- 40	- 225	- 40	- 225	mA
I _{CC}	LS646	V _{CC} = MAX	Outputs high	91	145	91	145	mA
			Outputs low	103	165	103	165	
			Outputs disabled	103	165	103	165	
	LS648		Outputs high	91	145	91	145	
			Outputs low	103	165	103	165	
			Outputs disabled	120	180	120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LS646, SN54LS648, SN74LS646, SN74LS648

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDLS190A – DECEMBER 1982 – REVISED MAY 2004

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646			'LS648			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
tPLH	CAB or CBA	A or B	RL = 667 Ω, CL = 45 pF, See Note 2	15	25		15	25	ns	
tPHL				23	35		24	40	ns	
tPLH	A or B	B or A		12	18		12	18	ns	
tPHL				13	20		15	25	ns	
tPLH	SAB or SBA† with Bus input high	A or B		26	40		37	55	ns	
tPHL				21	35		24	40	ns	
tPLH	SAB or SBA† with Bus input low	A or B		33	50		26	40	ns	
tPHL				14	25		23	40	ns	
tPZH	G	A or B	33	55		30	50	ns		
tPZL			42	65		37	55	ns		
tPZH	DIR	A or B	28	45		23	40	ns		
tPZL			39	60		30	45	ns		
tPHZ	G	A or B	23	35		28	45	ns		
tPLZ			22	35		22	35	ns		
tPHZ	DIR	A or B	20	30		24	35	ns		
tPLZ			19	30		19	30	ns		

† These parameters are measured with the internal output state of the storage register opposite to that of the input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN54LS647, SN54LS649, SN74LS647, SN74LS649

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

SDLS190A – DECEMBER 1982 – REVISED MAY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (control inputs)	7 V
Off-state output voltage (A and B ports)	5.5 V
Operating free-air temperature range: SN54LS647, SN54LS649	– 55°C to 125°C
SN74LS647, SN74LS649	– 0°C to 70°C
Storage temperature range	– 65°C to 150°C

recommended operating conditions

		SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage			0.5			0.6	V		
V _{OH}	High-level output voltage			5.5			5.5	V		
I _{OL}	Low-level output voltage			12			24	mA		
t _w	Pulse duration	CBA or CAB high			15			ns		
		CBA or CAB low			30					
		Data high or low			30					
t _{su}	Setup time before CAB ↑ or CBA ↑	A or B			15			ns		
t _h	Hold time after CAB ↑ or CBA ↑	A or B			0			ns		
T _A	Operating free-air temperature	− 55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS647 SN54LS649		SN74LS647 SN74LS649		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN, I _I = – 18 mA		– 1.5		– 1.5		V
Hysteresis (V _{T+} – V _{T–})	A or B input	V _{CC} = MIN		0.1	0.4	0.2	0.4	V
I _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V		0.1		0.1		mA
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX		0.25 0.4		0.25 0.4 0.35 0.5		V
I _I	A or B	V _{CC} = MAX		0.1		0.1		mA
	All others			0.1		0.1		
I _{IH}		V _{CC} = MAX, V _I = 2.7 V		20		20		μA
I _{IL}		V _{CC} = MAX, V _I = 0.4 V		– 0.4		– 0.4		mA
I _{CC}	'LS647	V _{CC} = MAX, Outputs open	Outputs high	79	130	79	130	mA
			Outputs low	94	150	94	150	
	'LS649	V _{CC} = MAX, Outputs open	Outputs high	79	130	79	130	
			Outputs low	94	150	94	150	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.



SN54LS647, SN54LS649, SN74LS647, SN74LS649

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

SDLS190A – DECEMBER 1982 – REVISED MAY 2004

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS647			'LS649			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	CAB or CBA	A or B	R _L = 667 Ω, C _L = 45 pF, See Note 2	22		35	17		30	ns
t _{PHL}				28		45	28		45	ns
t _{PLH}	A or B	B or A		17		26	15		25	ns
t _{PHL}				18		27	20		30	ns
t _{PLH}	SAB or SBA† with Bus input high	A or B		33		50	37		55	ns
t _{PHL}				29		45	28		45	ns
t _{PLH}	SAB or SBA† with Bus input low			39		60	30		45	ns
t _{PHL}				19		30	26		40	ns
t _{PLH}	G	A or B		25		40	21		40	ns
t _{PHL}				33		50	34		50	ns
t _{PLH}	DIR			23		35	19		30	ns
t _{PHL}				25		40	27		45	ns

† These parameters are measured with the internal outputs state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS646DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS646	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

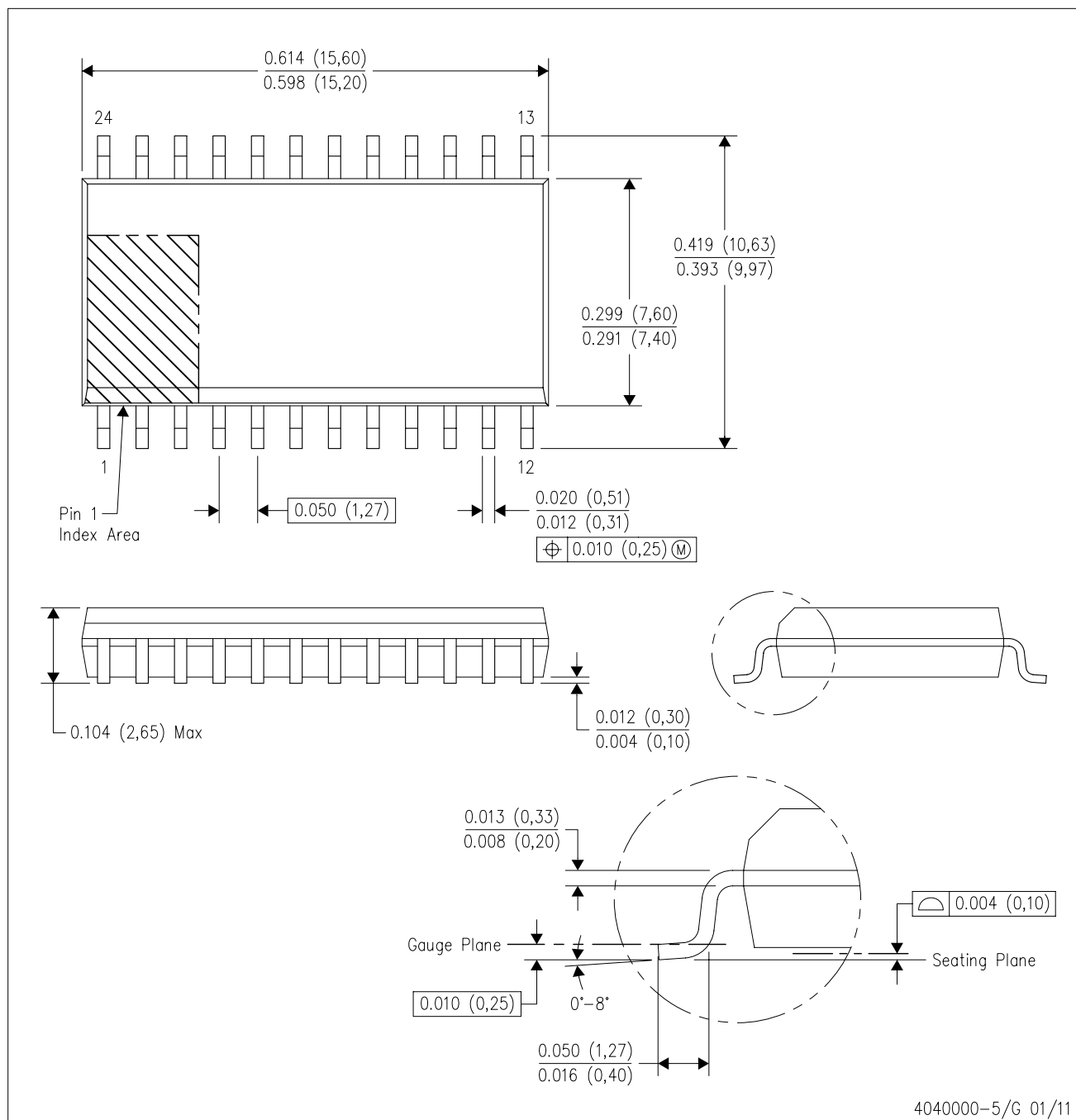
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated