OPAx145 High-Precision, Low-Noise, Rail-to-Rail Output, 5.5-MHz JFET Operational Amplifiers

1 Features

- Best bandwidth and slew-rate-to-power ratio:
  - Gain-bandwidth Product: 5.5 MHz
  - Slew rate: 20 V/μs
  - Low supply current: 475 μA (maximum)
- High precision:
  - Very low offset: 150 μV (maximum)
  - Very low offset drift: 1 μV/°C (maximum)
- Low input bias current: 2 pA
- Excellent noise performance:
  - Very low voltage noise: 7 nV/√Hz
  - Very low current noise: 0.8 fA/√Hz
- Input-voltage range includes V– supply
- Single-supply operation: 4.5 V to 36 V
- Dual-supply operation: ±2.25 V to ±18 V

2 Applications

- Semiconductor test
- Lab and field instrumentation
- Source measurement unit (SMU)
- Weigh scale
- Intra-DC interconnect (metro)
- Merchant network and server PSU
- DC power supply, ac source, electronic load
- Data acquisition (DAQ)

3 Description

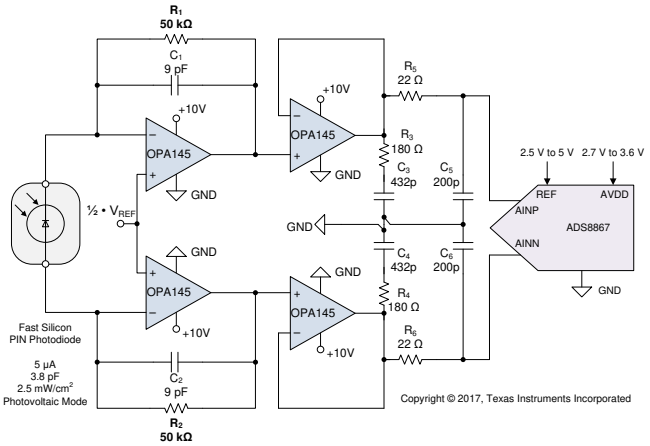
The OPA145 and OPA2145 (OPAx145) devices are part of a family of low-power JFET input amplifiers that have excellent drift, low current noise, and pico-ampere input bias current. These features make the OPAx145 an excellent choice for amplifying small signals from high-impedance sensors. The rail-to-rail output swing interfaces to modern, single-supply, precision, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). In addition, the input range that includes V– allows designers to simplify power management and take advantage of the single-supply, low-noise JFET architecture.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA145	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
OPA2145	SOIC (8) (Preview)	4.90 mm × 3.91 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

OPA145 Excels in 16-Bit, 100-kSPS Fully Differential Transimpedance Imaging Application



OPA145 Precision JFET Technology Offers Excellent Linear Input Impedance

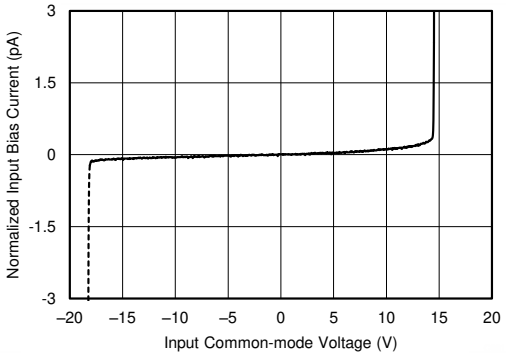


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information: OPA145 ... 5
6.5 Thermal Information: OPA2145 ... 5
6.6 Electrical Characteristics: V_S = 4.5 V to 36 V; ±2.25 V to ±18 V ... 6
6.7 Typical Characteristics ... 8
7 Detailed Description ... 16
7.1 Overview ... 16
7.2 Functional Block Diagram ... 16
7.3 Feature Description ... 17
7.4 Device Functional Modes ... 23
8 Application and Implementation ... 24
8.1 Application Information ... 24
8.2 Typical Application ... 24
8.3 System Examples ... 25
9 Power Supply Recommendations ... 27
10 Layout ... 27
10.1 Layout Guidelines ... 27
10.2 Layout Example ... 28
11 Device and Documentation Support ... 29
11.1 Device Support ... 29
11.2 Documentation Support ... 29
11.3 Related Links ... 30
11.4 Receiving Notification of Documentation Updates 30
11.5 Support Resources ... 30
11.6 Trademarks ... 30
11.7 Electrostatic Discharge Caution ... 30
11.8 Glossary ... 30
12 Mechanical, Packaging, and Orderable Information ... 30

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2018) to Revision D — **Page**

- Added OPA2145 advanced information (preview) device and associated content to data sheet ... 1

Changes from Revision B (May 2018) to Revision C — **Page**

- Deleted "preview" from information re: DBV (SOT-23) package, now released ... 1
- Changed status of data sheet to "Production Data" ... 1

Changes from Revision A (March 2018) to Revision B — **Page**

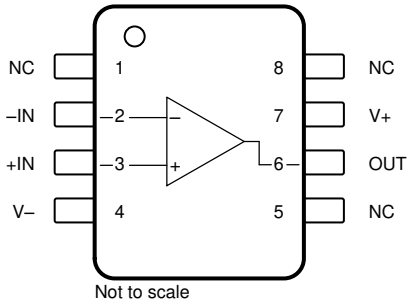
- Deleted "preview" from information re: DGK (VSSOP) package, now released ... 1

Changes from Original (June 2017) to Revision A — **Page**

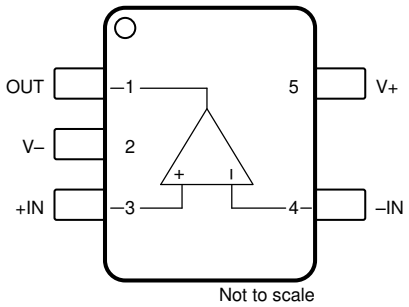
- Added preview of DBV and DGK packages; removed content regarding future device releases ... 1

5 Pin Configuration and Functions

OPA145: D and DGK Packages
8-Pin SOIC, 8-Pin VSSOP
Top View



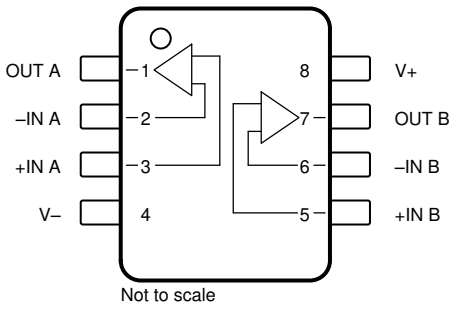
OPA145: DBV Package
5-Pin SOT-23
Top View



Pin Functions: OPA145

PIN			I/O	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK (VSSOP),	DBV (SOT-23)		
–IN	2	4	I	Inverting input
+IN	3	3	I	Noninverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

OPA2145: D Package
8-Pin SOIC
Top View



Pin Functions: OPA2145

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V–	4	—	Negative supply
V+	8	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply		±20	V
		Single supply		40	
	Signal input pins(2)	Voltage	(V–) – 0.5	(V+) + 0.5	
		Current		±10	mA
I_{SC}	Output short-circuit(3)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	
T_{STG}	Storage temperature		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to V_S / 2 (ground in symmetrical dual-supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply	±2.25	±15	±18	V
		Single supply	4.5	30	36	
T_A	Ambient temperature		–40	25	125	°C

6.4 Thermal Information: OPA145

THERMAL METRIC (1)		OPA145			UNIT
		D (SOIC)	DGK (VSSOP)	DBV (SOT)	
		8 PINS	8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136	143	205	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74	47	200	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	64	113	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	5.3	38.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.8	62.8	104.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2145

THERMAL METRIC (1)		OPA2145	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, seethe *Semiconductorand IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics: V_S = 4.5 V to 36 V; ±2.25 V to ±18 V

at T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Offset voltage, RTI	V_S = ±18 V		±40	±150	µV
		V_S = ±18 V, T_A = 0°C to +85°C			±280	
		V_S = ±18 V, T_A = –40°C to +125°C			±350	
dV_{OS}/dT	Drift	V_S = ±18 V, T_A = 0°C to +85°C D and DGK Packages		±0.4	±1	µV/°C
		V_S = ±18 V, T_A = 0°C to +85°C DBV Package		±0.4	±1.2	
		V_S = ±18 V, T_A = –40°C to +125°C D and DGK Packages		±0.5	±1.4	
		V_S = ±18 V, T_A = –40°C to +125°C DBV Package		±0.5	±1.5	
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V D Package Only		±0.06	±0.3	µV/V
		V_S = ±2.25 V to ±18 V DGK and DBV Packages		±0.06	±0.5	
		V_S = ±2.25 V to ±18 V, T_A = –40°C to +125°C			±2	
INPUT BIAS CURRENT						
I_B	Input bias current			±2	±10	pA
		T_A = 0°C to +85°C			±600	
		T_A = –40°C to +125°C			±10	nA
I_{OS}	Input offset current			±2	±10	pA
		T_A = 0°C to +85°C			±600	
		T_A = –40°C to +125°C			±10	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		320		nV_{PP}
		f = 0.1 Hz to 10 Hz		60		nV_{RMS}
e_n	Input voltage noise density	f = 10 Hz		9		nV/√Hz
		f = 100 Hz		7.2		
		f = 1 kHz		7		
I_n	Input current noise density	f = 1 kHz		0.8		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C	(V–) –0.1		(V+)–3.5	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, V_{CM} = (V–) –0.1 V to (V+) – 3.5 V	126	140		dB
		V_S = ±18 V, V_{CM} = (V–) –0.1 V to (V+) – 3.5 V, T_A = –40°C to +125°C	118			
INPUT IMPEDANCE						
	Differential			10^{13} || 5		Ω || pF
	Common-mode	V_{CM} = (V–) –0.1 V to (V+) –3.5 V		10^{13} || 4.3		

Electrical Characteristics: V_S = 4.5 V to 36 V; ±2.25 V to ±18 V (continued)

at T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 10 kΩ D Package Only	118	123		dB
			V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 10 kΩ DGK and DBV Packages	110	123		dB
			V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 2 kΩ	106	110		
			V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 2 kΩ, T_A = –40°C to +125°C	104			
FREQUENCY RESPONSE							
BW	Gain bandwidth product				5.5		MHz
SR	Slew rate				20		V/µs
	Settling time	12 bits	10-V Step, G = +1		1.6		µs
		16 bits	10-V Step, G = +1		6		
THD+N	Total harmonic distortion and noise		1 kHz, G = +1, V_O = 3.5 V_{RMS}		0.0001%		
	Overload recovery time				600		ns
OUTPUT							
	Linear output voltage swing range		R_L = 10 kΩ, A_{OL} ≥ 108 dB, T_A = –40°C to +125°C See Figure 24 and Figure 25	(V–) + 0.1		(V+) – 0.1	V
			R_L = 2 kΩ, A_{OL} ≥ 108 dB, T_A = –40°C to +125°C See Figure 24 and Figure 25	(V–) + 0.3		(V+) – 0.3	
V_O	Voltage output swing from rail		R_L = 10 kΩ			75	mV
			R_L = 10 kΩ, T_A = –40°C to +125°C			90	
			R_L = 2 kΩ			210	
			R_L = 2 kΩ,T_A = –40°C to +125°C D Package Only			250	
			R_L = 2 kΩ,T_A = –40°C to +125°C DGK and DBV Packages			350	
I_{SC}	Short-circuit current				±20		mA
C_{LOAD}	Capacitive load drive				See Figure 27		
R_O	Open-loop output impedance		f = 1 MHz, I_O = 0 (See Figure 26)		150		Ω
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)		I_O = 0 mA		445	475	µA
			T_A = 0°C to +85°C			590	
			T_A = –40°C to +125°C			655	

6.7 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution From –40°C to +125°C	Figure 2
Input Bias Current Production Distribution	Figure 3
Input Offset Current Production Distribution	Figure 4
Offset Voltage vs Temperature	Figure 5
Offset Voltage vs Common-Mode Voltage	Figure 6
Offset Voltage vs Power Supply	Figure 7
Open-Loop Gain and Phase vs Frequency	Figure 8
Closed-Loop Gain vs Frequency	Figure 9
Input Bias Current vs Common-Mode Voltage	Figure 10
Input Bias Current and Offset vs Temperature	Figure 11
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 12
CMRR and PSRR vs Frequency	Figure 13
CMRR vs Temperature	Figure 14
PSRR vs Temperature	Figure 15
0.1-Hz to 10-Hz Voltage Noise	Figure 16
Input Voltage Noise Spectral Density vs Frequency	Figure 17
THD+N Ratio vs Frequency	Figure 18
THD+N vs Output Amplitude	Figure 19
Quiescent Current vs Supply Voltage	Figure 20
Quiescent Current vs Temperature	Figure 21
Open-Loop Gain vs Temperature (10-kΩ)	Figure 22
Open-Loop Gain vs Temperature (2-kΩ)	Figure 23
DC Open-Loop Gain vs Output Voltage Swing Relative to Supply	Figure 24, Figure 25
Open-Loop Output Impedance vs Frequency	Figure 26
Small-Signal Overshoot vs Capacitive Load (10-mV Step)	Figure 27
No Phase Reversal	Figure 28
Positive Overload Recovery	Figure 29
Negative Overload Recovery	Figure 30
Small-Signal Step Response (10-mV Step)	Figure 31, Figure 32
Large-Signal Step Response (10-V Step)	Figure 33, Figure 34
Settling Time	Figure 35
Short-Circuit Current vs Temperature	Figure 36
Maximum Output Voltage vs Frequency	Figure 37
EMIRR vs Frequency	Figure 38

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

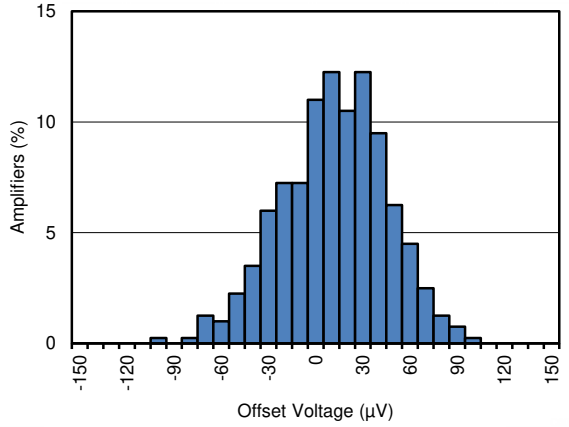


Figure 1. Offset Voltage Production Distribution

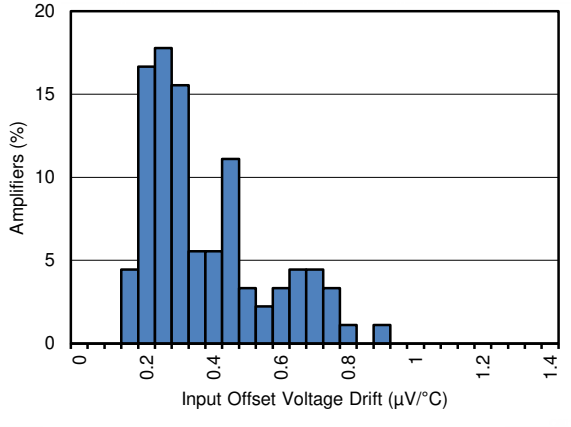


Figure 2. Offset Voltage Drift Distribution From –40°C to +125°C

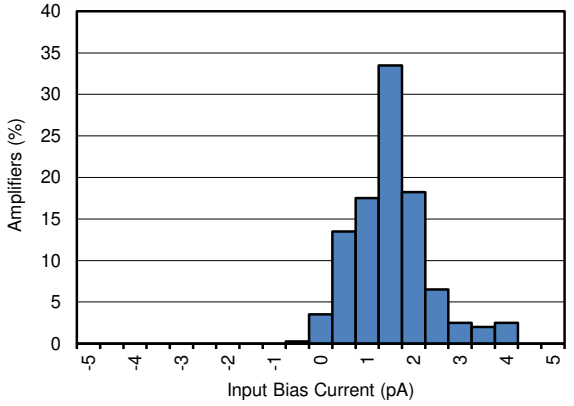


Figure 3. Input Bias Current Production Distribution

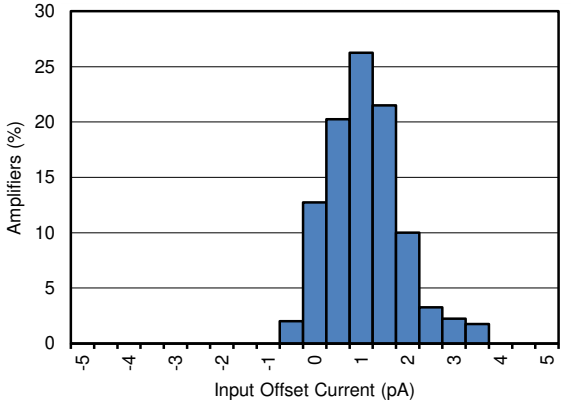


Figure 4. Input Offset Current Production Distribution

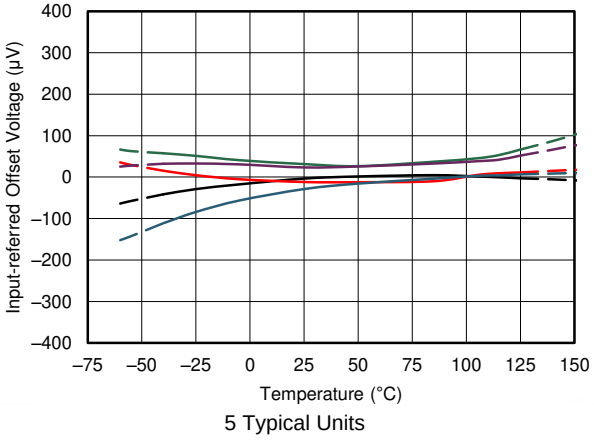


Figure 5. Offset Voltage vs Temperature

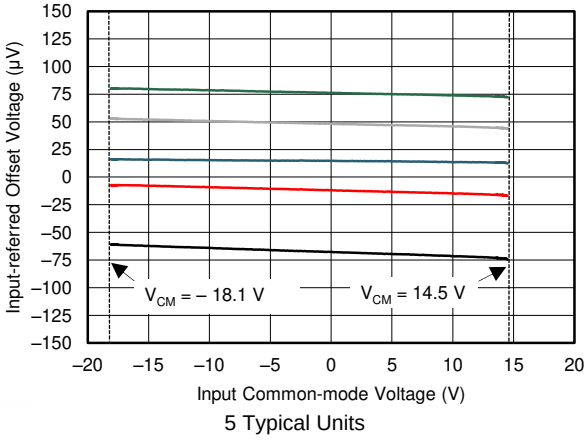


Figure 6. Offset Voltage vs Common-Mode Voltage

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

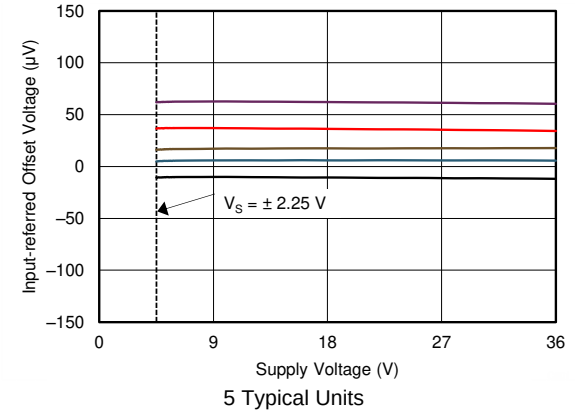


Figure 7. Offset Voltage vs Supply Voltage

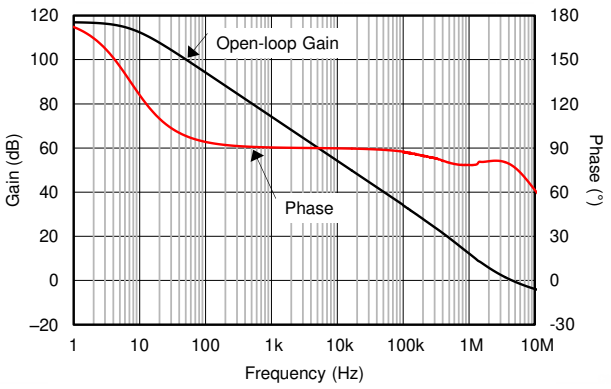


Figure 8. Open-Loop Gain and Phase vs Frequency

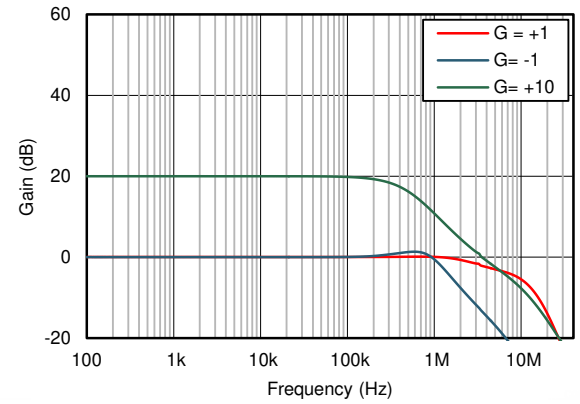


Figure 9. Closed-Loop Gain vs Frequency

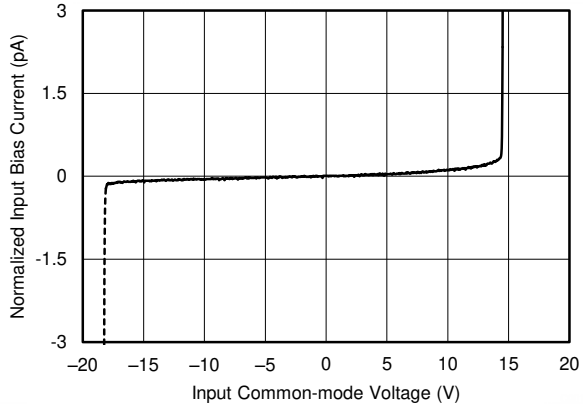


Figure 10. Input Bias Current vs Common-Mode Voltage

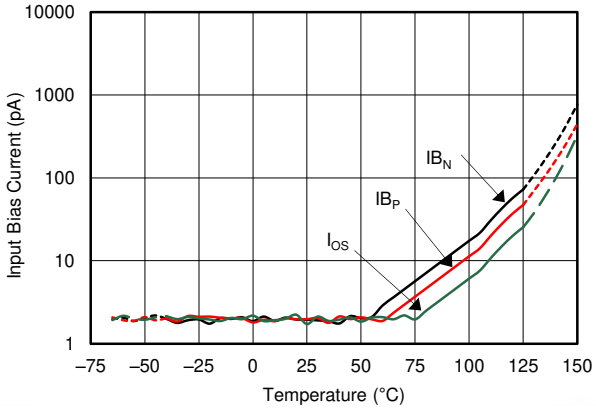


Figure 11. Input Bias Current and Offset vs Temperature

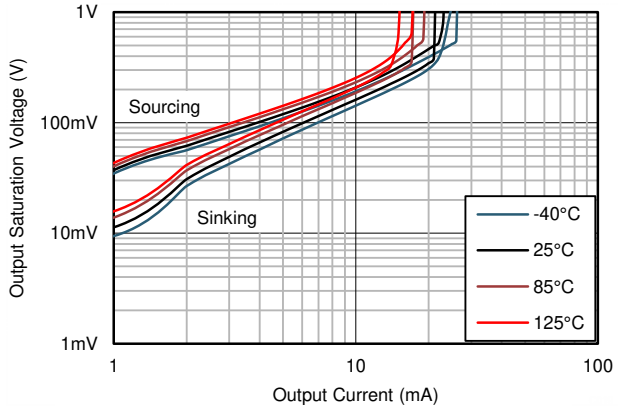


Figure 12. Output Voltage Swing vs Output Current (Maximum Supply)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

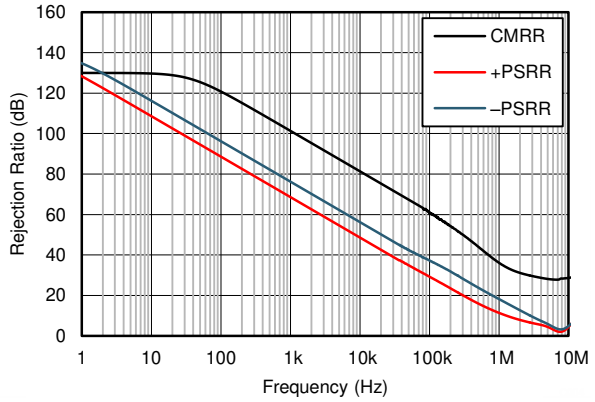


Figure 13. CMRR and PSRR vs Frequency

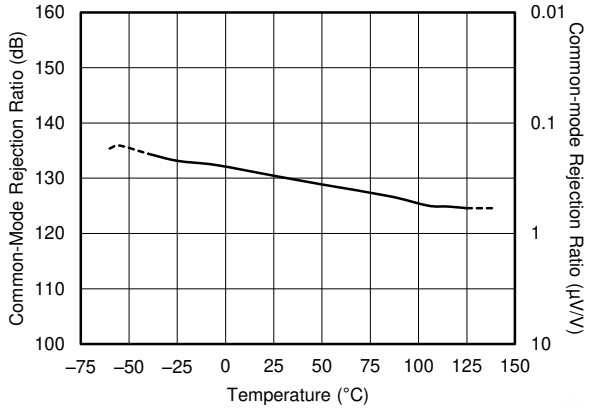


Figure 14. CMRR vs Temperature

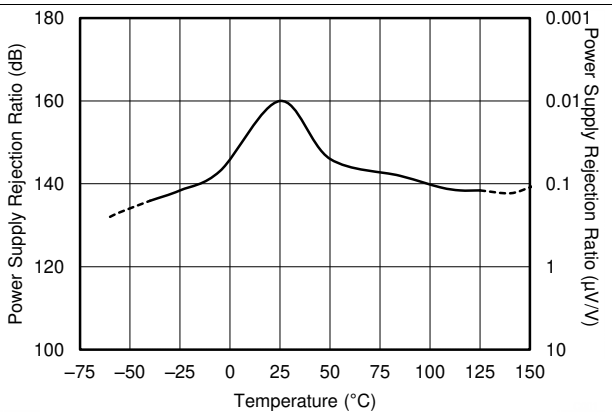


Figure 15. PSRR vs Temperature

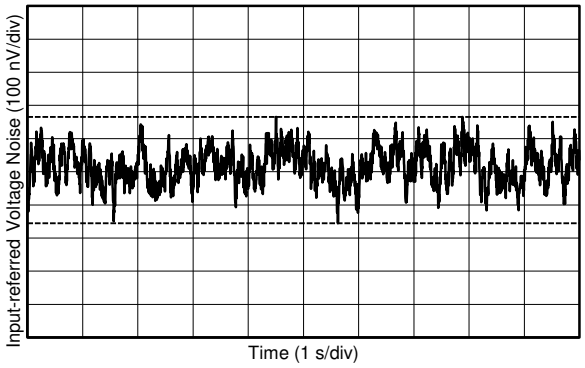


Figure 16. 0.1-Hz to 10-Hz Voltage Noise

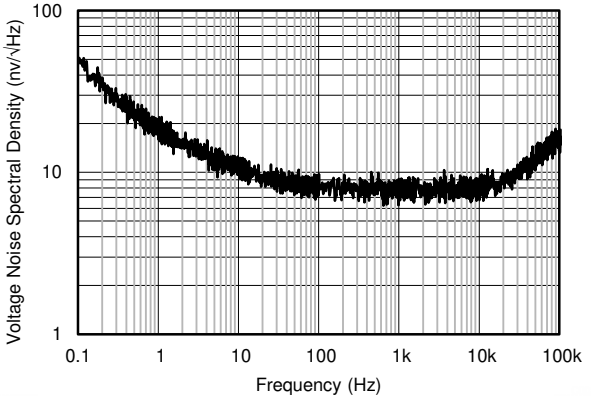
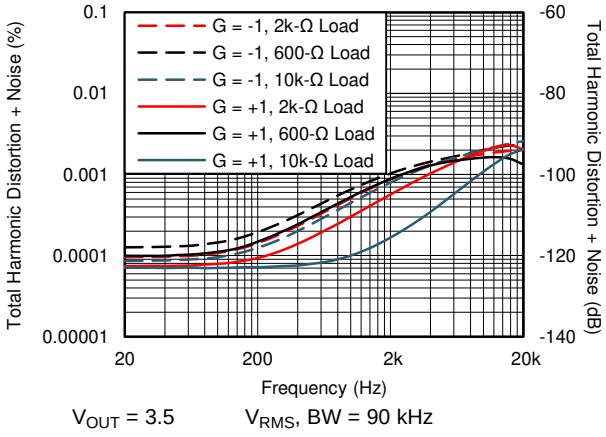


Figure 17. Input Voltage Noise Spectral Density vs Frequency



V_{OUT} = 3.5 V_{RMS}, BW = 90 kHz

Figure 18. THD+N Ratio vs Frequency

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

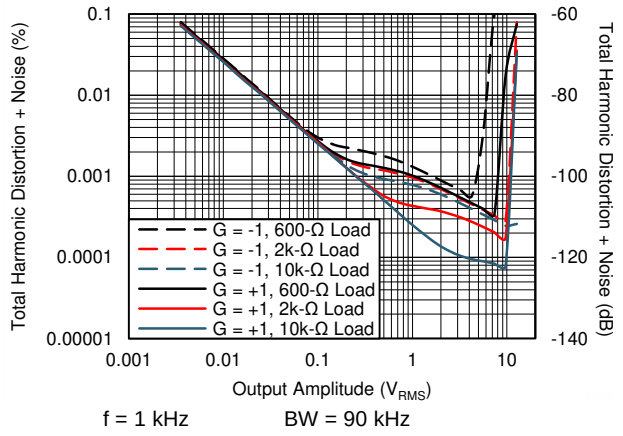


Figure 19. THD+N vs Output Amplitude

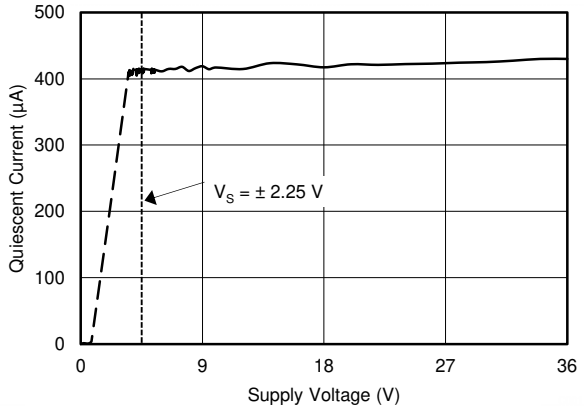


Figure 20. Quiescent Current vs Supply Voltage

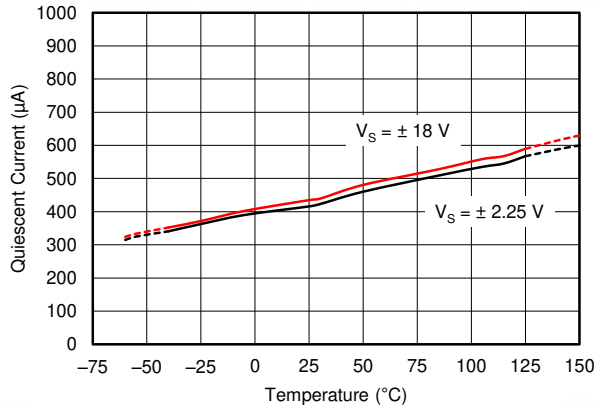


Figure 21. Quiescent Current vs Temperature

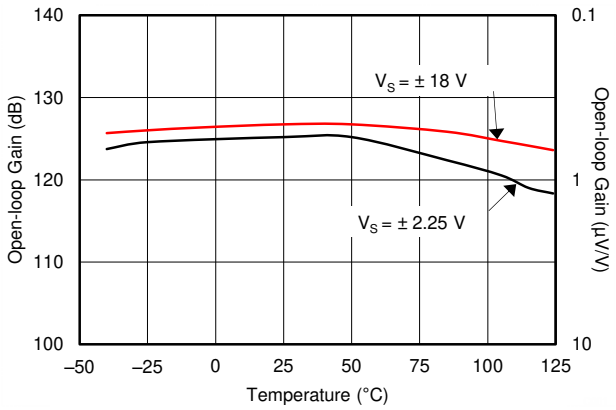


Figure 22. Open-Loop Gain vs Temperature

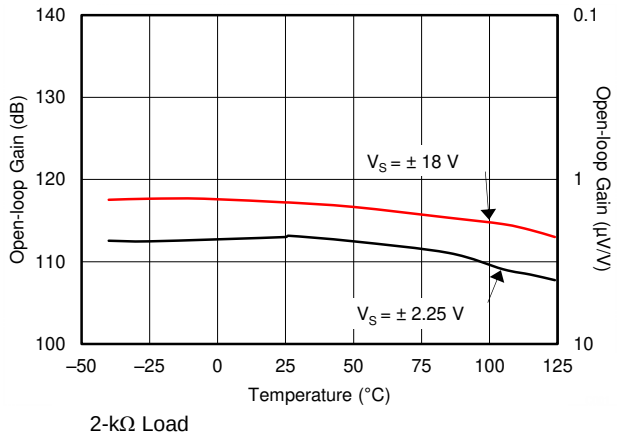


Figure 23. Open-Loop Gain vs Temperature)

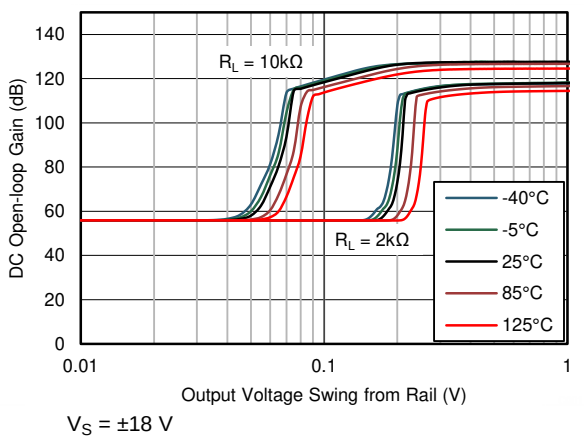


Figure 24. Open-Loop Gain vs Output Voltage Swing to Supply

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

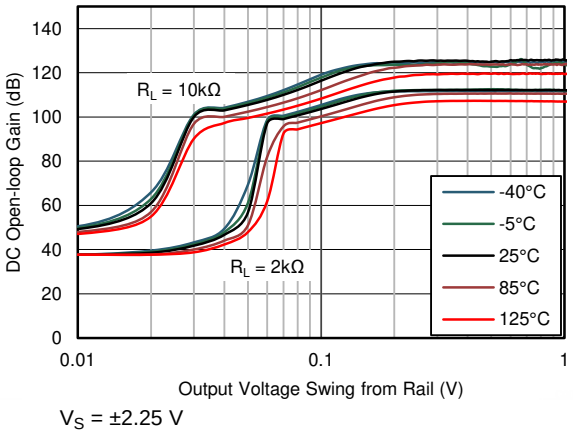


Figure 25. Open-Loop Gain vs Output Voltage Swing to Supply

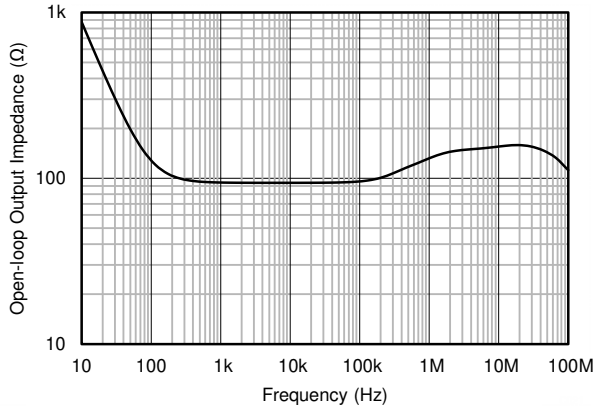


Figure 26. Open-Loop Output Impedance vs Frequency

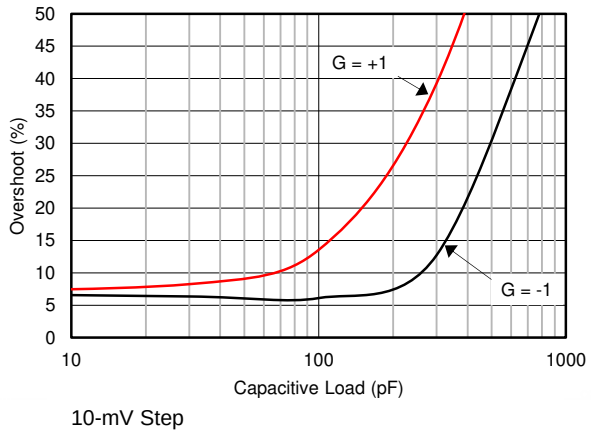


Figure 27. Small-Signal Overshoot vs Capacitive Load

Figure 28. No Phase Reversal

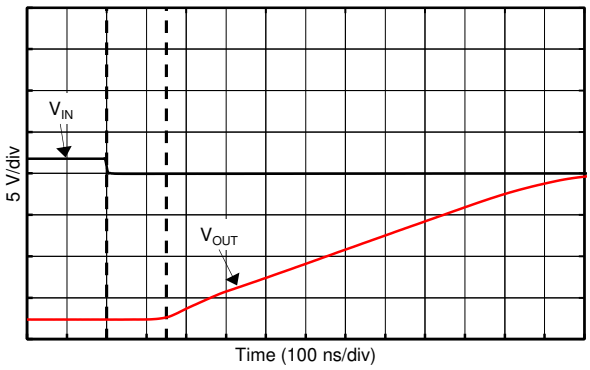


Figure 29. Positive Overload Recovery

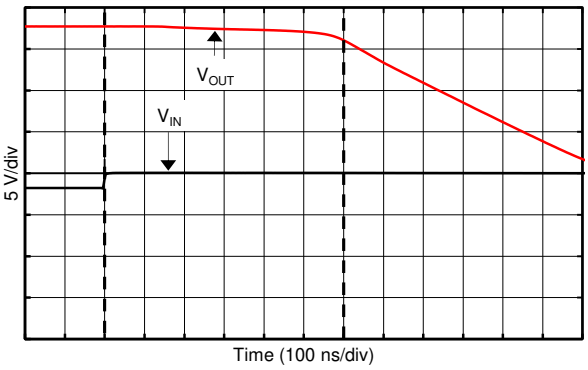
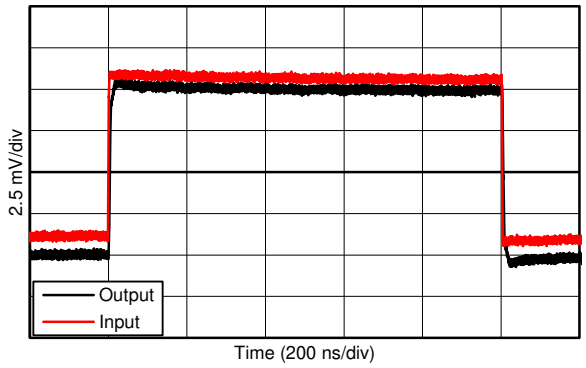


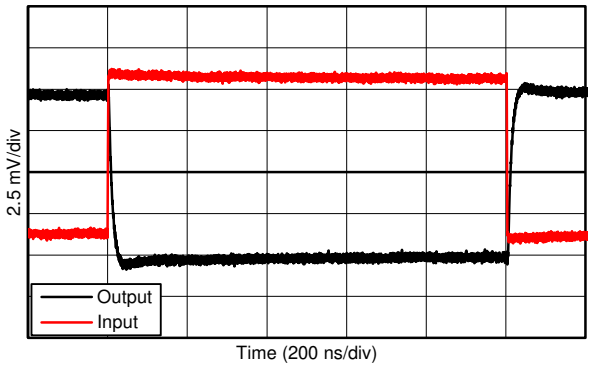
Figure 30. Negative Overload Recovery

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



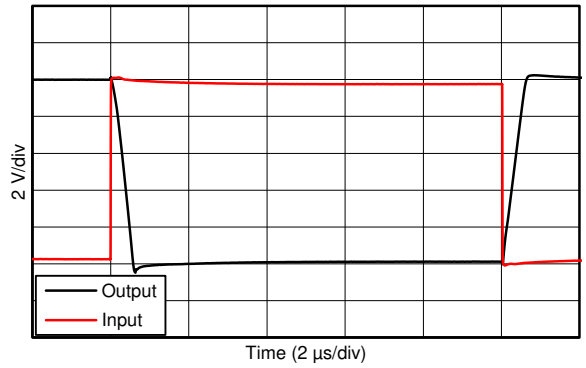
G = +1

Figure 31. Small-Signal Step Response (10-mV Step)



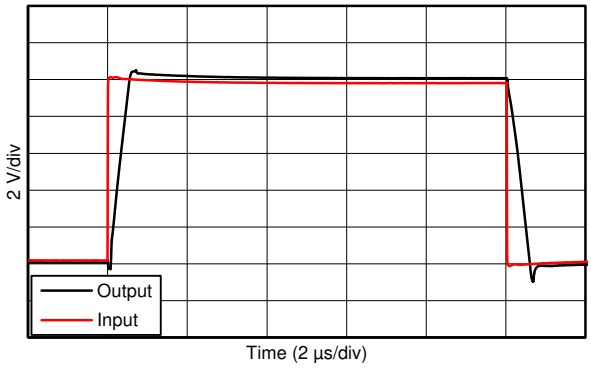
10-mV Step G = –1

Figure 32. Small-Signal Step Response



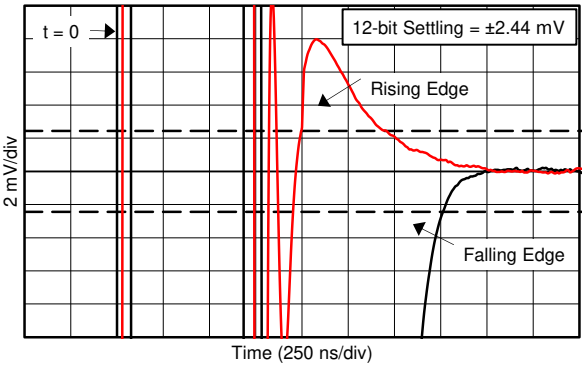
10-V Step G = –1

Figure 33. Large-Signal Step Response



10-V Step G = +1

Figure 34. Large-Signal Step Response



12-bit settling on 10-V step = ±2.44 mV

Figure 35. Settling Time (10-V Step)

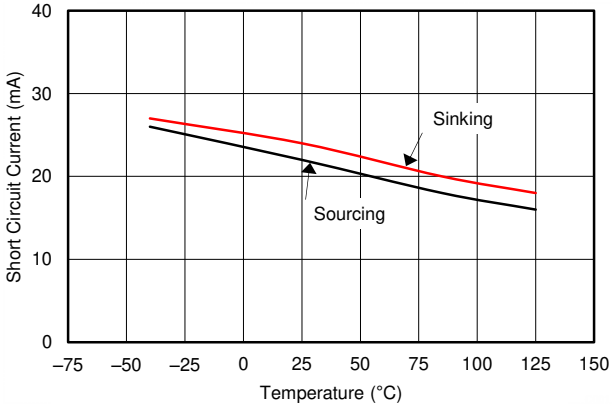


Figure 36. Short-Circuit Current vs Temperature

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

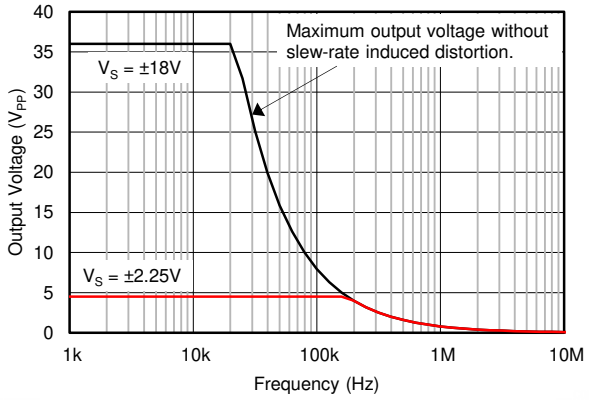
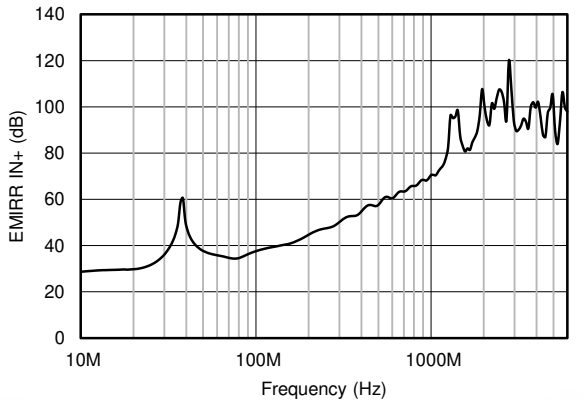


Figure 37. Maximum Output Voltage Amplitude vs Frequency



P_{RF} = –10 dBm

Figure 38. EMIRR vs Frequency

7 Detailed Description

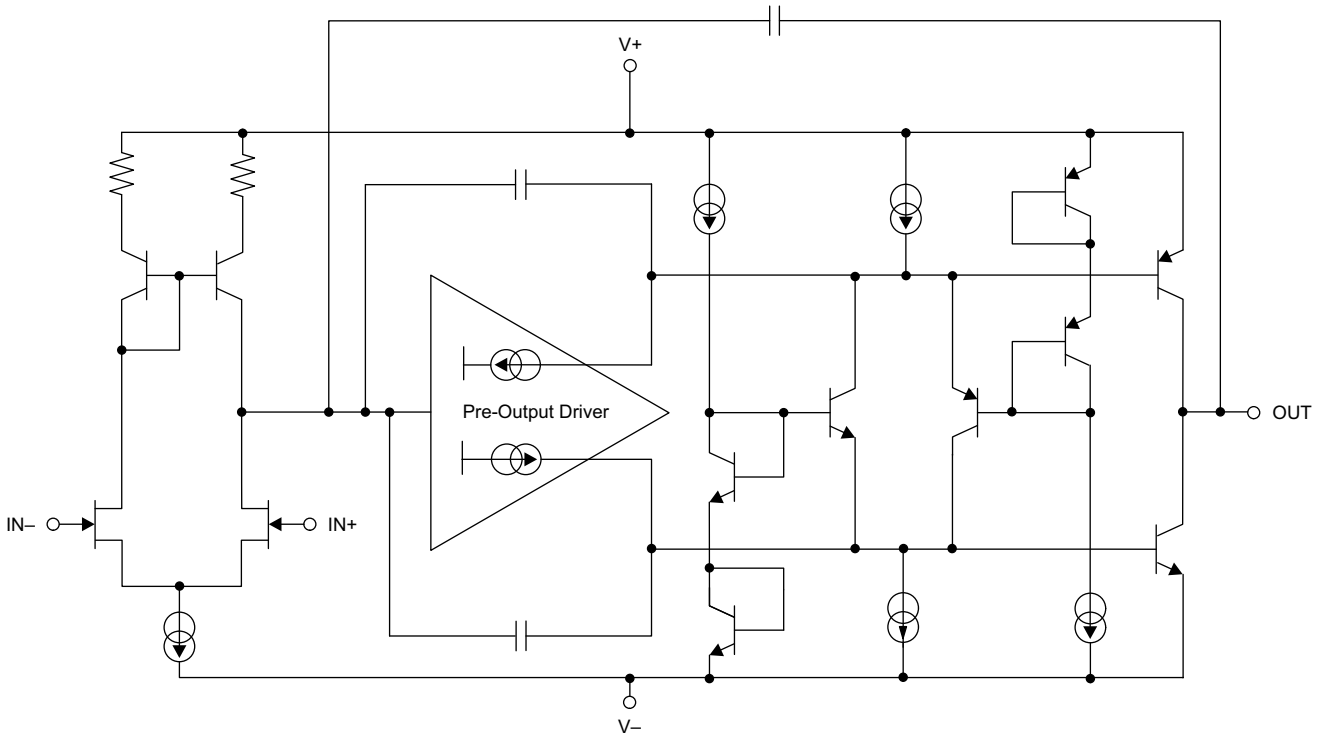
7.1 Overview

The OPA145 and OPA2145 (OPAx145) operational amplifiers are part of a family of low-power JFET input amplifiers that feature superior drift performance and low input bias current. The rail-to-rail output swing and input range that includes V– allow designers to use the low-noise characteristics of JFET amplifier while also interfacing to modern, single-supply, precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The OPAx145 achieve 5.5-MHz gain-bandwidth product and 20-V/μs slew rate and consumes only 445 μA (typical) of quiescent current, making these devices an excellent choice for low-power applications. These devices operate on a single 4.5-V to 36-V supply or dual ±2.25-V to ±18-V supplies.

The OPAx145 are fully specified from –40°C to +125°C for use in the most challenging environments. The OPA145 is available in 5-pin SOT-23, 8-pin SOIC, and 8-pin VSSOP packages. The dual-channel OPA2145 is available in an 8-pin SOIC package.

The *Functional Block Diagram* shows the simplified diagram of the OPAx145.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

CAUTION

Supply voltages greater than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

The OPA145 and OPA2145 series of op amps can be used with single or dual supplies from an operating range of V_S = 4.5 V (±2.25 V) up to V_S = 36 V (±18 V). These devices do not require symmetrical supplies; only a minimum supply voltage of 4.5 V (±2.25 V) is required. For V_S less than ±3.5 V, the common-mode input range does not include midsupply. Key parameters are specified over the operating temperature range, T_A = –40°C to +125°C. Key parameters that vary over the supply voltage, temperature range, or frequency are shown in *Typical Characteristics*.

7.3.2 Capacitive Load and Stability

The dynamic characteristics of the OPAx145 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50 Ω, for example) in series with the output.

Figure 27 illustrates the effects on small-signal overshoot for several capacitive loads. Also, see the *Feedback Plots Define Op Amp AC Performance* application bulletin, available for download from www.ti.com, for details of analysis techniques and application circuits.

7.3.3 Output Current Limit

The output current of the OPAx145 device is limited by internal circuitry to +20 mA/–20 mA (sinking/sourcing) to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature, as shown in Figure 36.

Feature Description (continued)

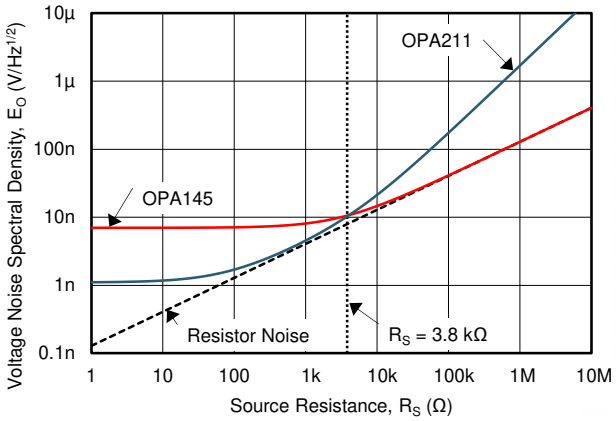
7.3.4 Noise Performance

Figure 39 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network, and therefore, no additional noise contributions). The OPAx145 and OPAx211 are shown with total circuit noise calculated. The op amp contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current, and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPAx145 have both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPAx145 are negligible for any practical source impedance, which makes this device the better choice for applications with high source impedance.

The equation in Figure 39 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in kelvins (K)

For more details on calculating noise, see the *Basic Noise Calculations* section.



NOTE: R_S = 3.8 kΩ is indicated in Figure 39.

NOTE: This is the source impedance above which OPA145 is a lower noise option than the OPA211.

Figure 39. Noise Performance of the OPA145 and OPA211 in Unity-Gain Buffer Configuration

Feature Description (continued)

7.3.5 Basic Noise Calculations

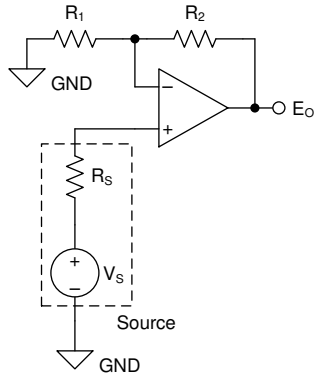
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 39. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 40 illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx145 means that ithe current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1+\frac{R_2}{R_1}\right)\cdot\sqrt{(e_S)^2+(e_N)^2+\left(e_{R_1\|R_2}\right)^2+(i_N\cdot R_S)^2+\left(i_N\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]\right)^2}\quad [\,V_{RMS}\,]$$

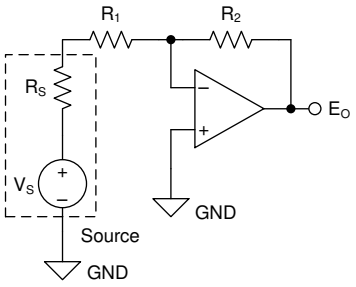
$$(2)\quad e_S = \sqrt{4\cdot k_B\cdot T(K)\cdot R_S}\quad \left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of R_S

$$(3)\quad e_{R_1\|R_2} = \sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]}\quad \left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of $R_1 \| R_2$

$$(4)\quad k_B = 1.38065\cdot 10^{-23}\quad \left[\frac{J}{K}\right]$$ Boltzmann Constant

$$(5)\quad T(K) = 237.15 + T(°C)\quad [\,K\,]$$ Temperature in kelvins

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O = \left(1+\frac{R_2}{R_S+R_1}\right)\cdot\sqrt{(e_N)^2+\left(e_{R_1+R_S\|R_2}\right)^2+\left(i_N\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]\right)^2}\quad [\,V_{RMS}\,]$$

$$(7)\quad e_{R_1+R_S\|R_2} = \sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]}\quad \left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of $(R_1 + R_S) \| R_2$

$$(8)\quad k_B = 1.38065\cdot 10^{-23}\quad \left[\frac{J}{K}\right]$$ Boltzmann Constant

$$(9)\quad T(K) = 237.15 + T(°C)\quad [\,K\,]$$ Temperature in kelvins

Where: e_N is the voltage noise of the amplifier. For the OPAx145 operational amplifiers, e_N = 7 nV/√Hz at 1 kHz.
i_N is the current noise of the amplifier. For the OPAx145 operational amplifiers, i_N = 0.8 fA/√Hz at 1 kHz.

NOTE: For additional resources on noise calculations visit *TI's Precision Labs Series*.

Figure 40. Noise Calculation in Gain Configurations

Feature Description (continued)

7.3.6 Phase-Reversal Protection

The OPAx145 have internal phase-reversal protection. Many FET-input and bipolar-input op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPAx145 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see Figure 28).

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See Figure 41 for an illustration of the ESD circuits contained in the OPAx145 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the power supply is connected to an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse that discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent the amplifier from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is greater than the normal operating voltage of the OPAx145 but less than the device breakdown voltage level. After this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit, such as the one Figure 41 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

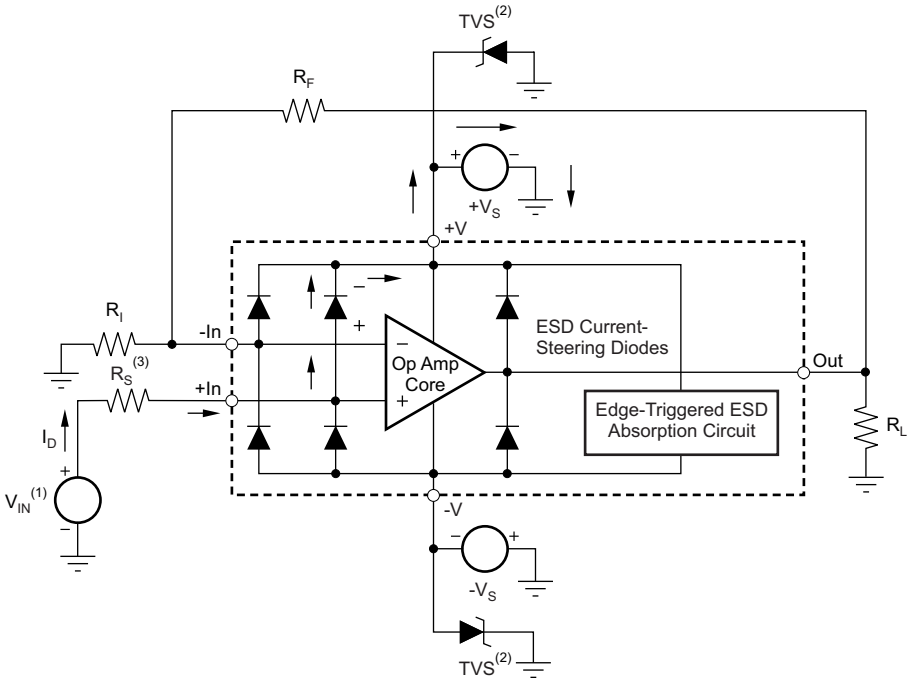
Figure 41 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. The answer depends on the supply characteristic while at 0 V, or at a level less than the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

Feature Description (continued)

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins as shown in Figure 41. The Zener voltage must be selected so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) V_{IN} = $+V_S$ + 500 mV.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value approximately 1 kΩ.

Figure 41. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

Feature Description (continued)

7.3.8 EMI Rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR, and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

  High-frequency signals conducted or radiated to any pin of the operational amplifier result in adverse effects, as the amplifier would not have sufficient loop gain to correct for signals with spectral content outside the amplifier bandwidth. Conducted or radiated EMI on inputs, power supply, or output may result in unexpected dc offsets, transient voltages, or other unknown behavior. Be sure to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces. Figure 43 shows the effect of conducted EMI to the power supplies on the input offset voltage of OPAx145.

  The EMIRR IN+ of the OPAx145 is plotted versus frequency, as shown in Figure 42. The OPAx145 unity-gain bandwidth is 5.5 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth.

See the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

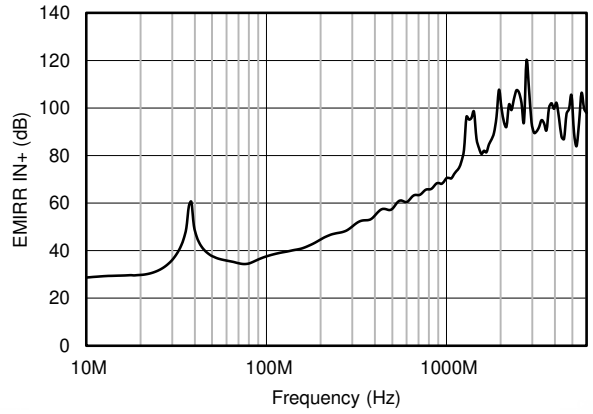


Figure 42. OPAx145 EMIRR IN+

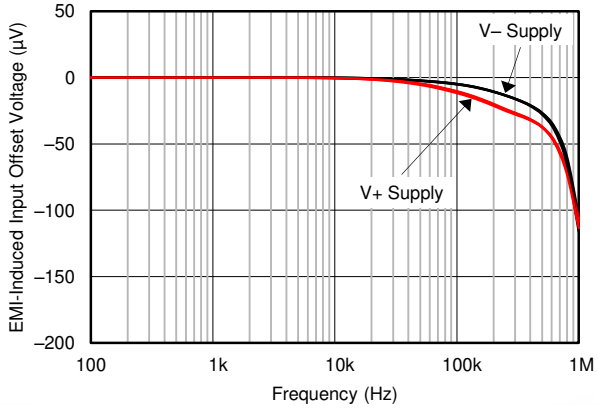


Figure 43. OPAx145 EMI-Induced Input Offset Voltage (Power Supplies)

Table 2 lists the EMIRR IN+ values for the OPAx145 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 2. OPAx145 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	54 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	86 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	107 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	100 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105 dB

7.3.9 EMIRR +IN Test Configuration

Figure 44 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the op amp noninverting input terminal using a transmission line. The op amp is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.

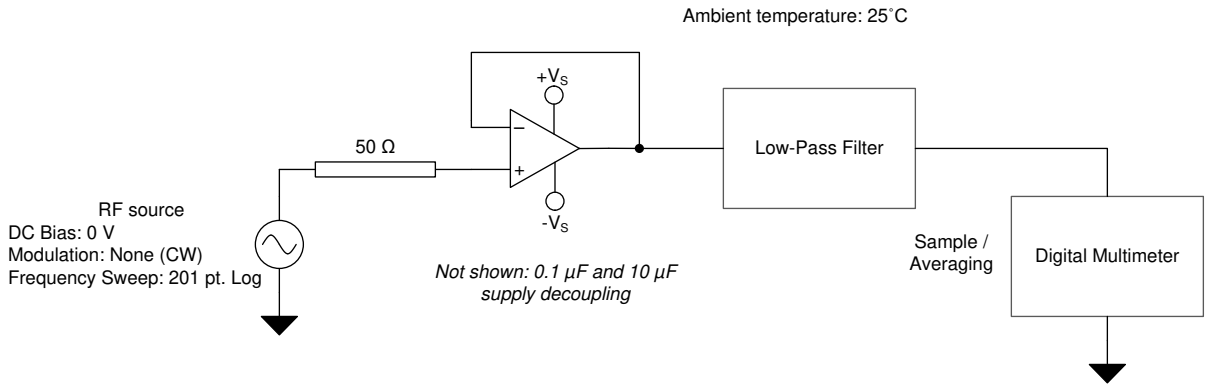


Figure 44. EMIRR +IN Test Configuration

7.4 Device Functional Modes

The OPAx145 have a single functional mode and are operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx145 is 36 V (±18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx145 is a unity-gain stable operational amplifier with low noise, low input-bias current, and low input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-μF capacitors are adequate. Designers can easily use the rail-to-rail output swing and input range that includes V– to take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision data converters.

8.2 Typical Application

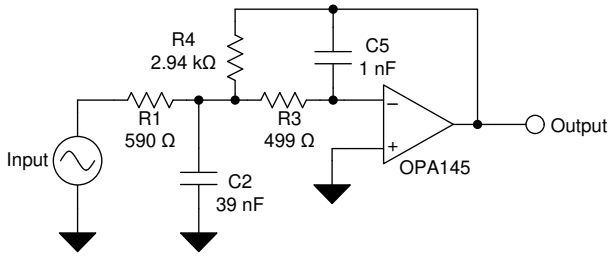


Figure 45. 25-kHz Low-Pass Filter

8.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx145 are designed to construct high-speed, high-precision active filters. Figure 45 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 45. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Typical Application (continued)

For systems that have different filter parameters or require specific system optimization, such as minimizing the system noise, an alternative device may be desired. A list of recommended alternatives can be found in Table 3.

Table 3. Alternative Devices

FEATURES	PRODUCT
Low-power, 10-MHz FET input industrial op amp	OPA140
2.2-nV/√Hz, low-power, 36-V op amp in SOT-23 package	OPA209
Low-noise, high-precision, 22-MHz, 4-nV/√Hz JFET-input op amp	OPA827
Low-noise, low I_Q precision CMOS op amp	OPA376
Low-power, precision, CMOS, rail-to-rail input/output, low-offset, low-bias op amp	OPA191

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets designers create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows designers to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.2.3 Application Curve

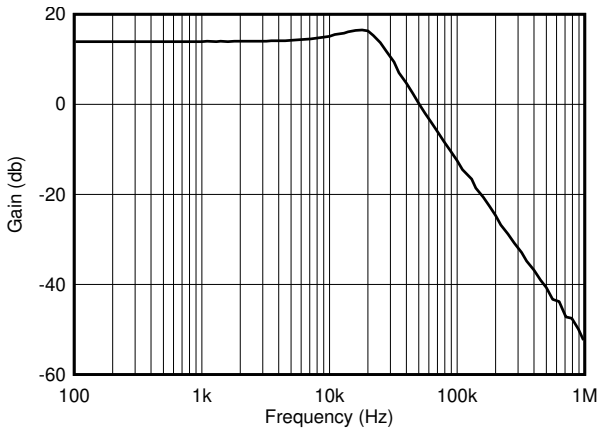


Figure 46. OPA145 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

8.3 System Examples

8.3.1 16-Bit, 100-kSPS, Fully Differential Transimpedance Imaging and Measurement

The OPAx145 are used in a differential transimpedance (I-V) measurement application capable of driving the ADS8867, a 16-bit, microPower, truly-differential ADC, at a maximum conversion rate of 100 kSPS, with an acquisition time of 1200 ns, and a conversion time of 8800 ns. The first stage supports a forward bandwidth of 493.5 kHz with 100 kΩ of transimpedance gain, enabling the photodiode to fully charge and settle to ±38 µV (±1/2 LSB on 5-V ADC reference voltage) within the conversion time of the ADC. The differential nature of the system provides several advantages, such as double the transimpedance gain compared to a single-ended system, improved signal-to-noise ratio, easy interfacing to high-precision, fully-differential ADCs, and additional protection against inductively-coupled noise and interference. Additionally, capacitively coupled common-mode transients can be minimized using low-impedance termination resistors R_{TERM1} and R_{TERM2}.

System Examples (continued)

The second stage provides the reverse bandwidth required for settling to 16-bit accuracy after the internal sampling capacitor of the successive-approximation-register (SAR) ADC is connected to the second stage. The two OPAx145 amplifiers in the second stage are configured as buffers for maximum closed-loop bandwidth, and stability is optimized using R3, C3 and R4, C4 by creating a snubber that reduces the open-loop output impedance (see Figure 26). C5 and C6 are provided as a charge reservoir for the internal sampling capacitor of the ADC, and R5 and R6 are tuned to optimize the phase margin of the second stage to drive the output capacitance. This two-stage approach enables compatibility with a wide selection of high output-impedance sensors while still maintaining 16-bit settling performance. Furthermore, the first stage can be designed with sufficient phase margin to drive twisted-pair transmission lines in remote measurement systems. Proper design of the transmission line reduces the interference of other signals over long distances. Figure 48 shows the settling performance of the system described previously and in Figure 47 — the settling time during the acquisition cycle is shown for settling successfully to 0 µA from 5 µs to 6.2 µs. At 6.3 µs, the photodiode current is changed to 5 µA (full-scale) and settles during the conversion cycle of the ADC (6.2 µs to 15 µs), and is then acquired successfully from 15 µs to 16.2 µs.

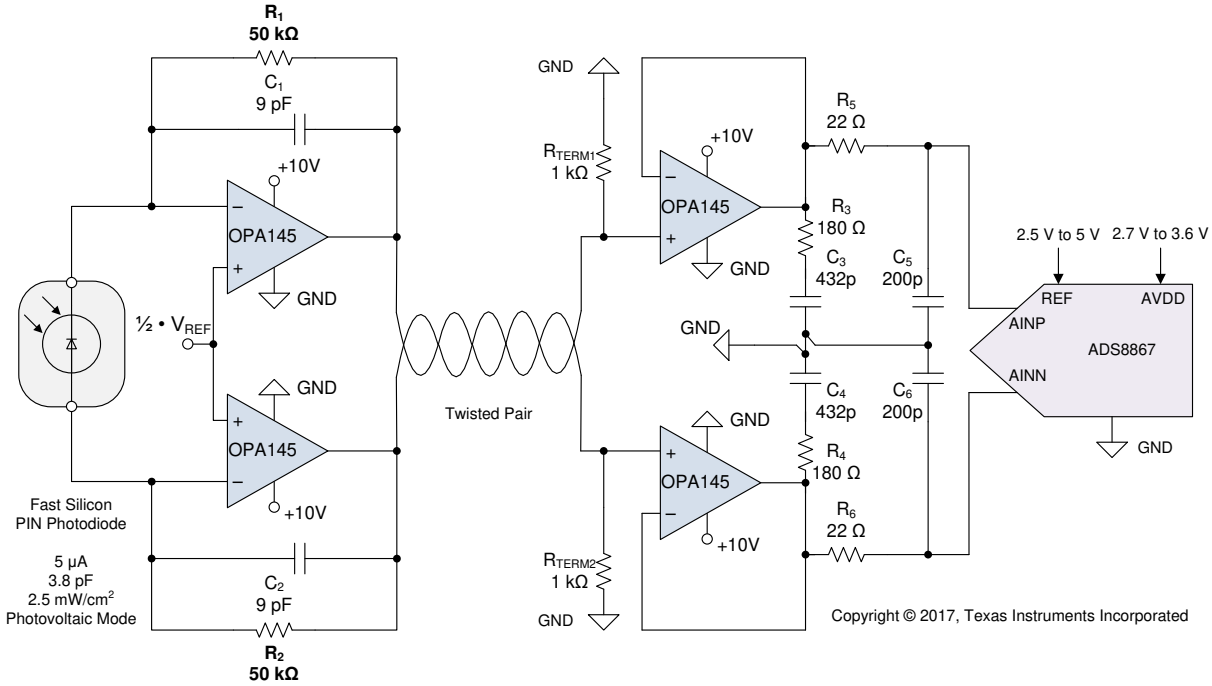


Figure 47. 16-Bit, 100-kSPS, Fully Differential Transimpedance Schematic

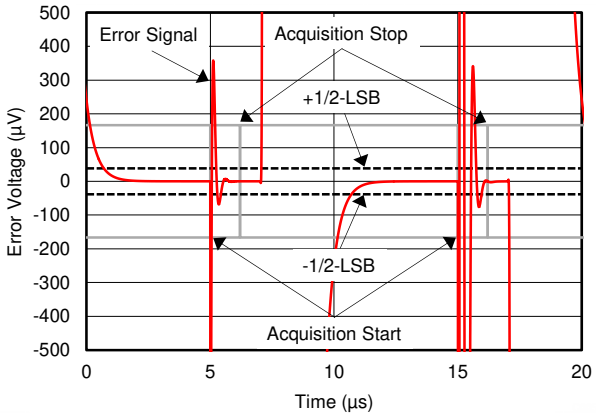


Figure 48. 16-bit, 100-kSPS, Fully Differential Transimpedance Settling Performance

9 Power Supply Recommendations

The OPAx145 are specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

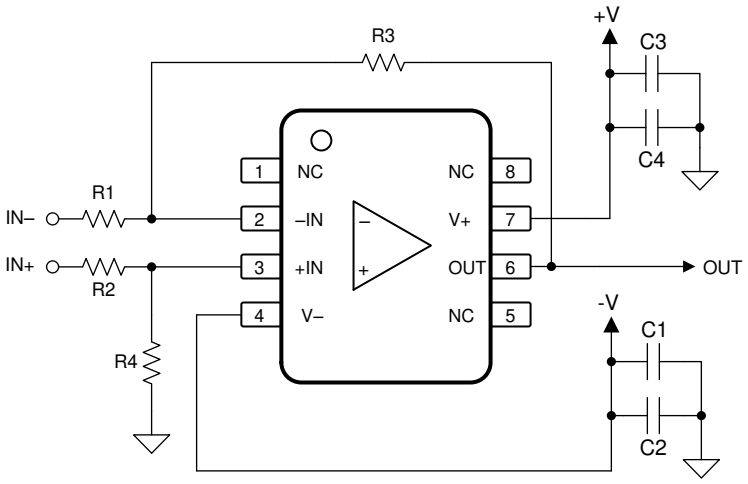
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *App note: 'The PCB is a component of op amp design"*.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in Figure 49, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example



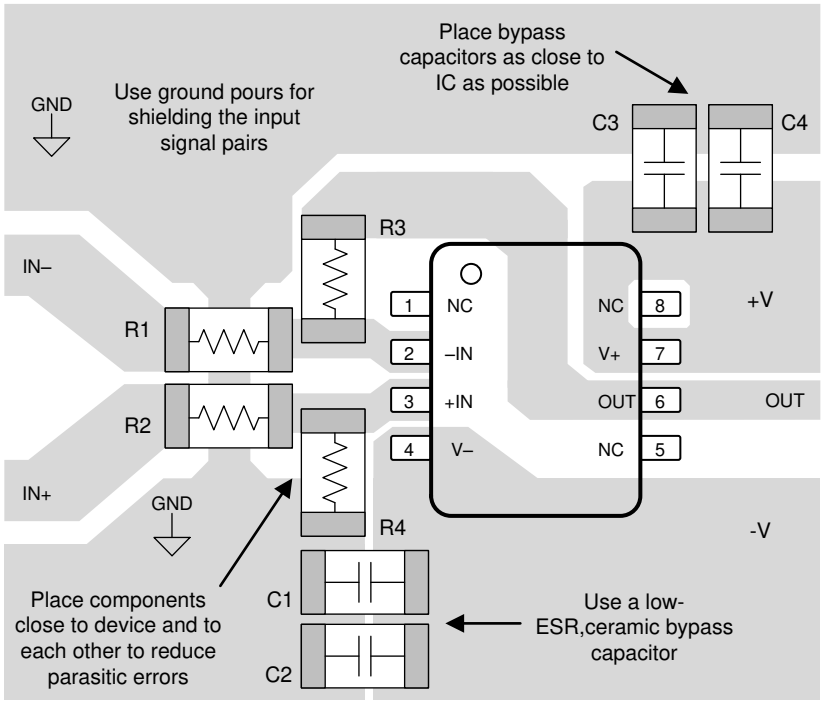


Figure 49. Operational Amplifier Board Layout for Difference Amplifier Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 WEBENCH Filter Designer Tool

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

11.1.1.3 TI Precision Designs

TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *The PCB is a component of op amp design*
- Texas Instruments, *OPA140, OPA2140, OPA4140 EMI Immunity Performance*
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively*
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis*
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis*
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters*
- Texas Instruments, *Op Amp Performance Analysis*
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers*
- Texas Instruments, *Tuning in Amplifiers*
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes*
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance*
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*

11.3 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA145	Click here	Click here	Click here	Click here	Click here
OPA2145	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
WEBENCH is a registered trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA145ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA145	Samples
OPA145IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1IB2	Samples
OPA145IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1IB2	Samples
OPA145IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1I4Q	Samples
OPA145IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1I4Q	Samples
OPA145IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA145	Samples
OPA2145ID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		
POPA2145ID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

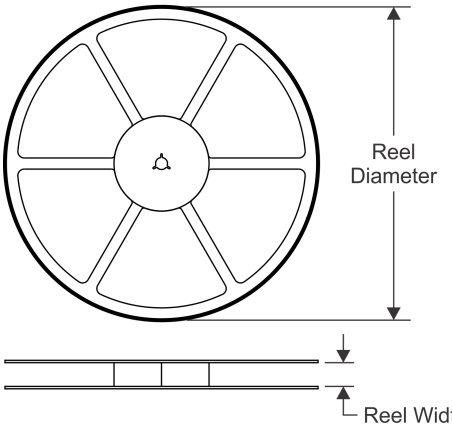
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

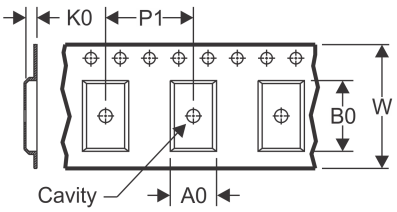
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

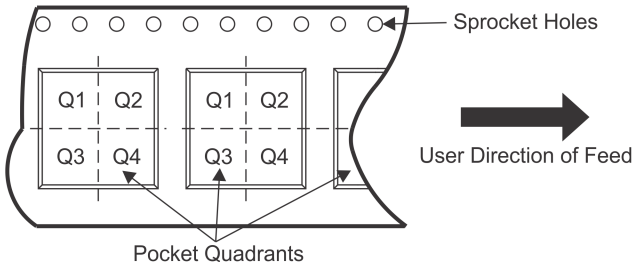


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

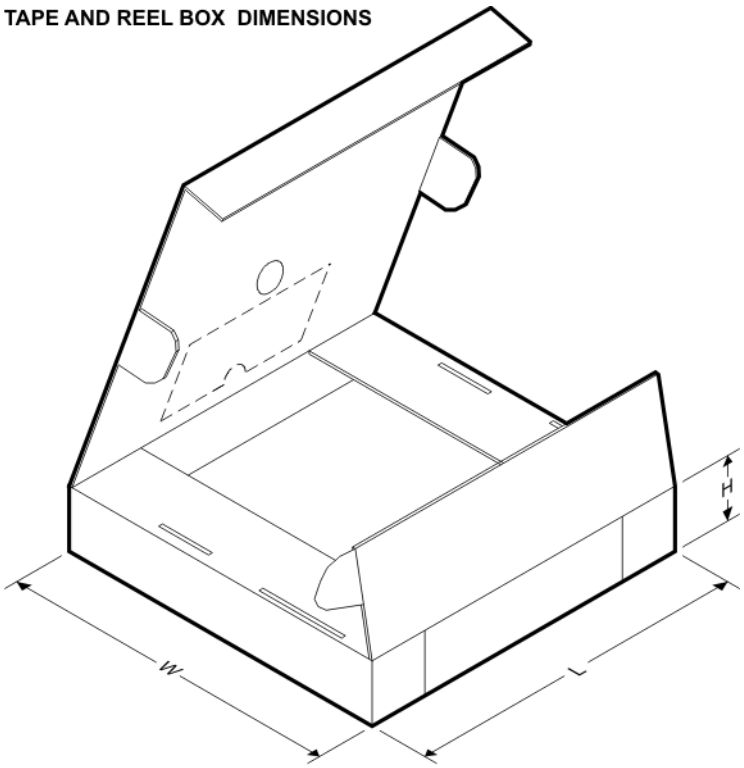
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA145IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA145IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA145IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA145IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA145IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

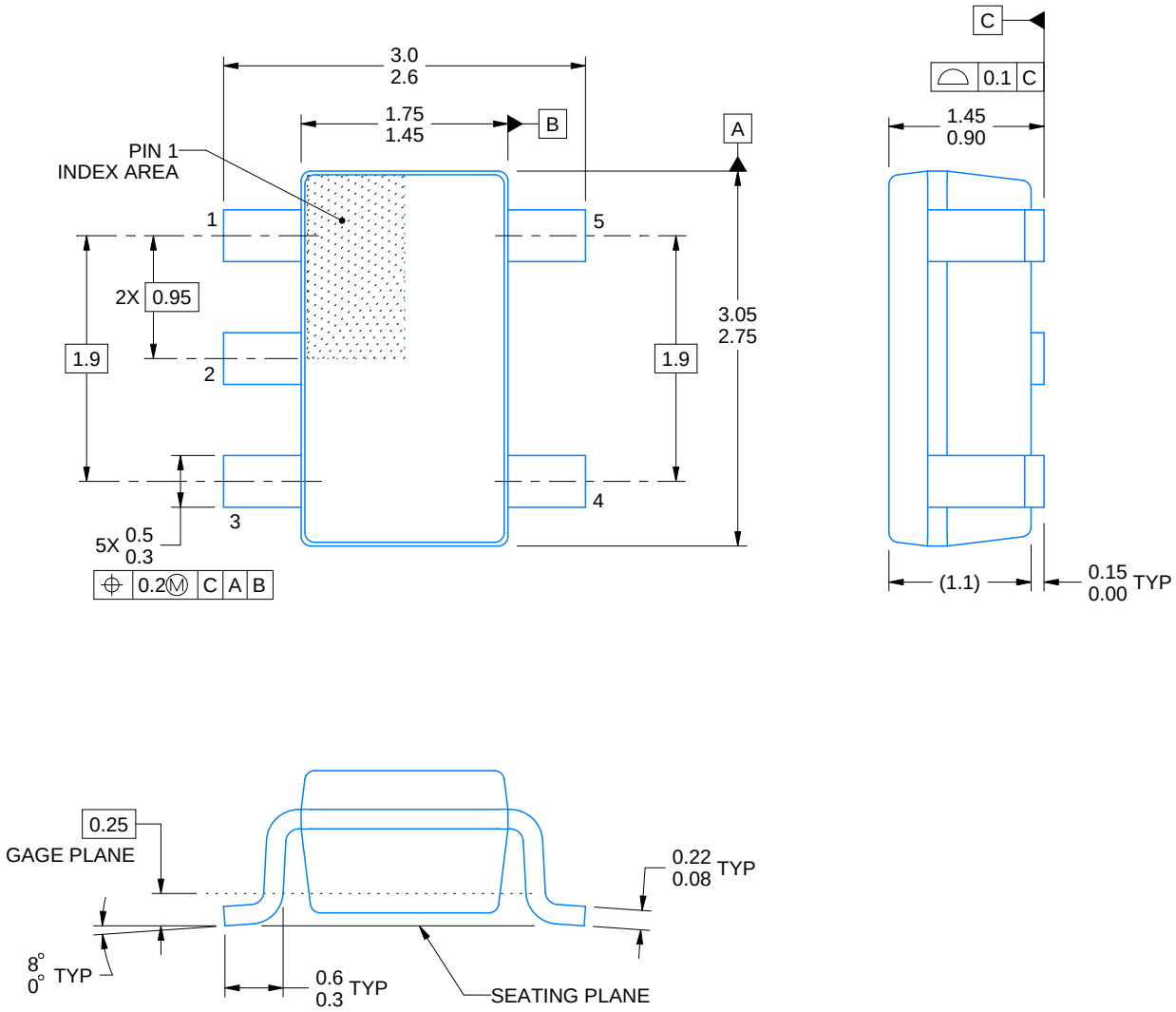
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA145IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA145IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA145IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA145IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA145IDR	SOIC	D	8	2500	367.0	367.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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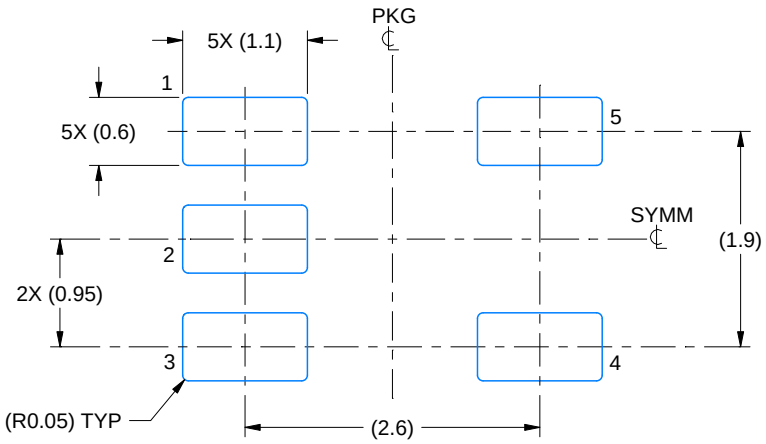
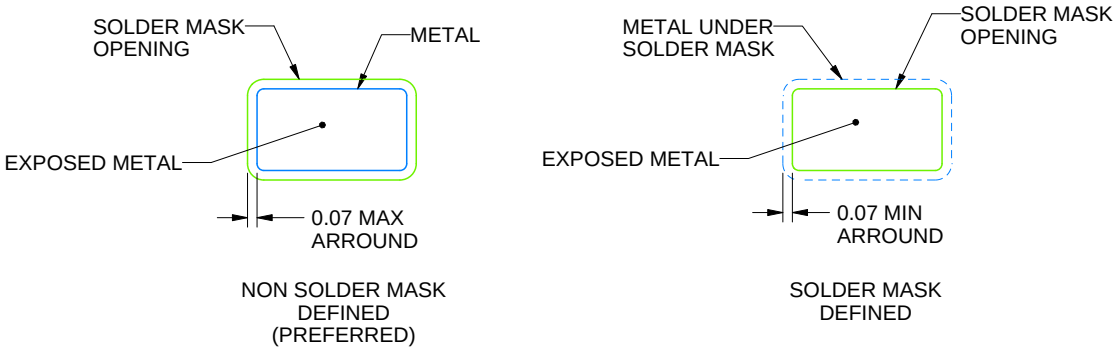
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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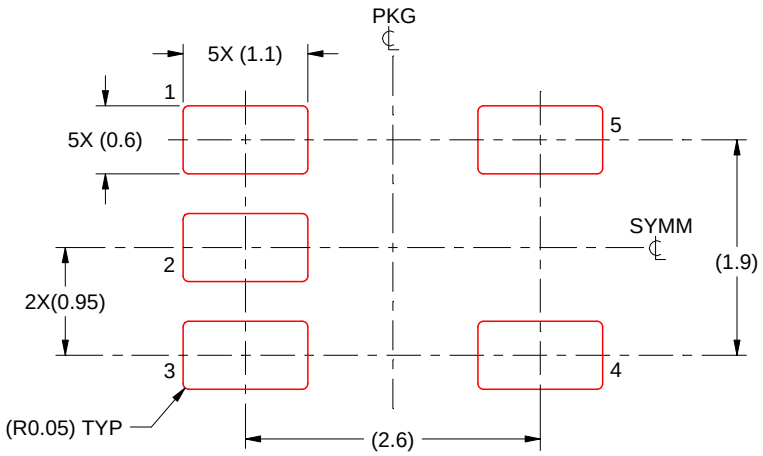
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

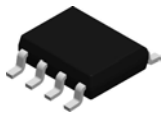


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

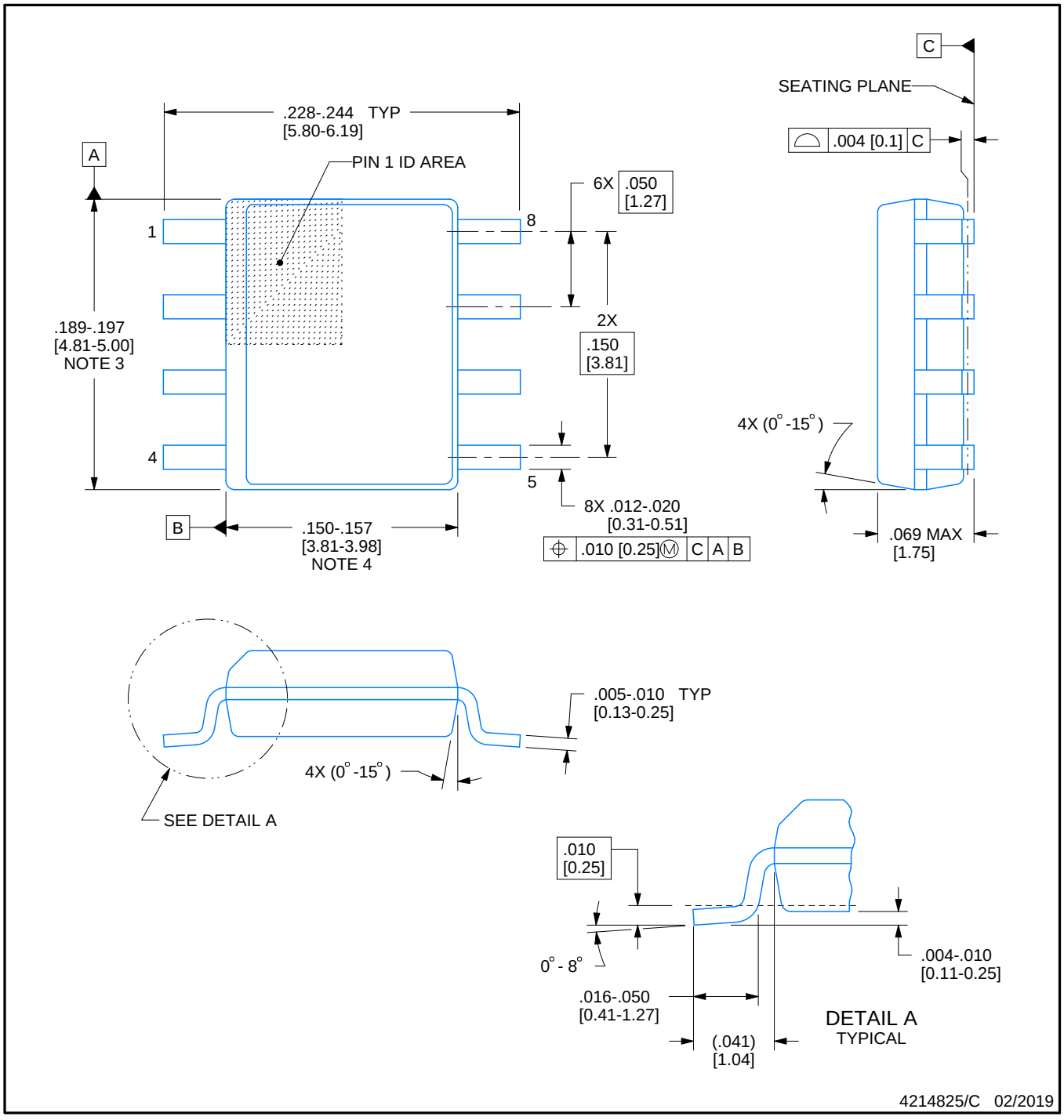


PACKAGE OUTLINE

D0008A

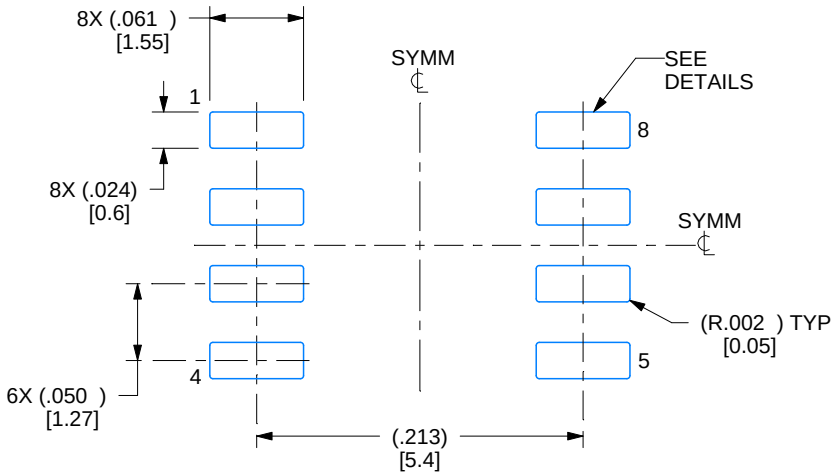
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

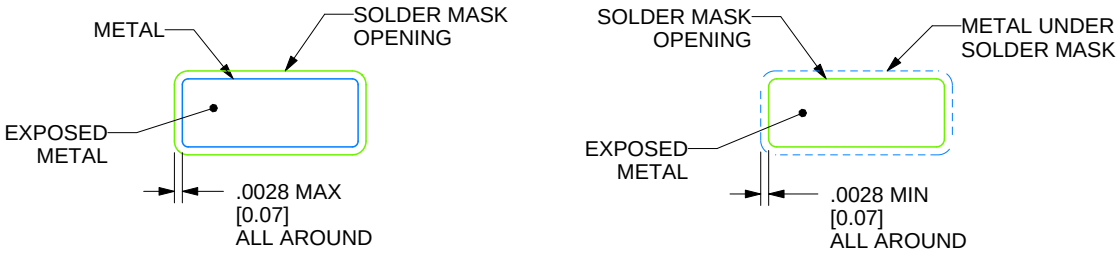


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

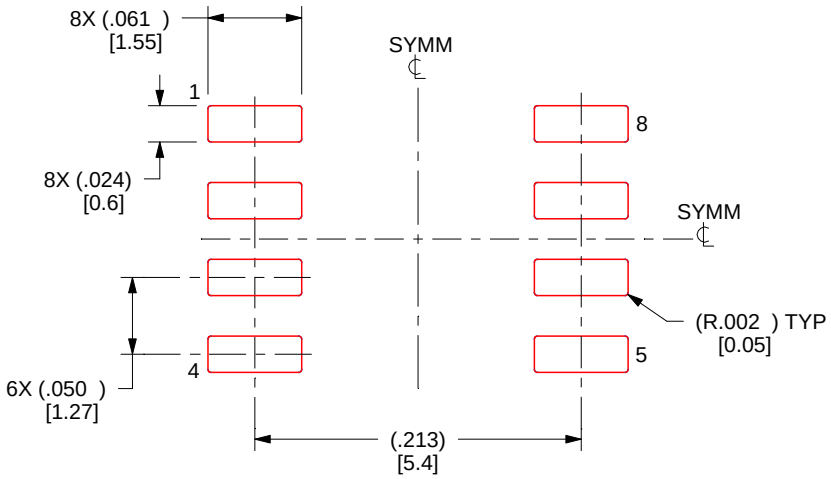
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



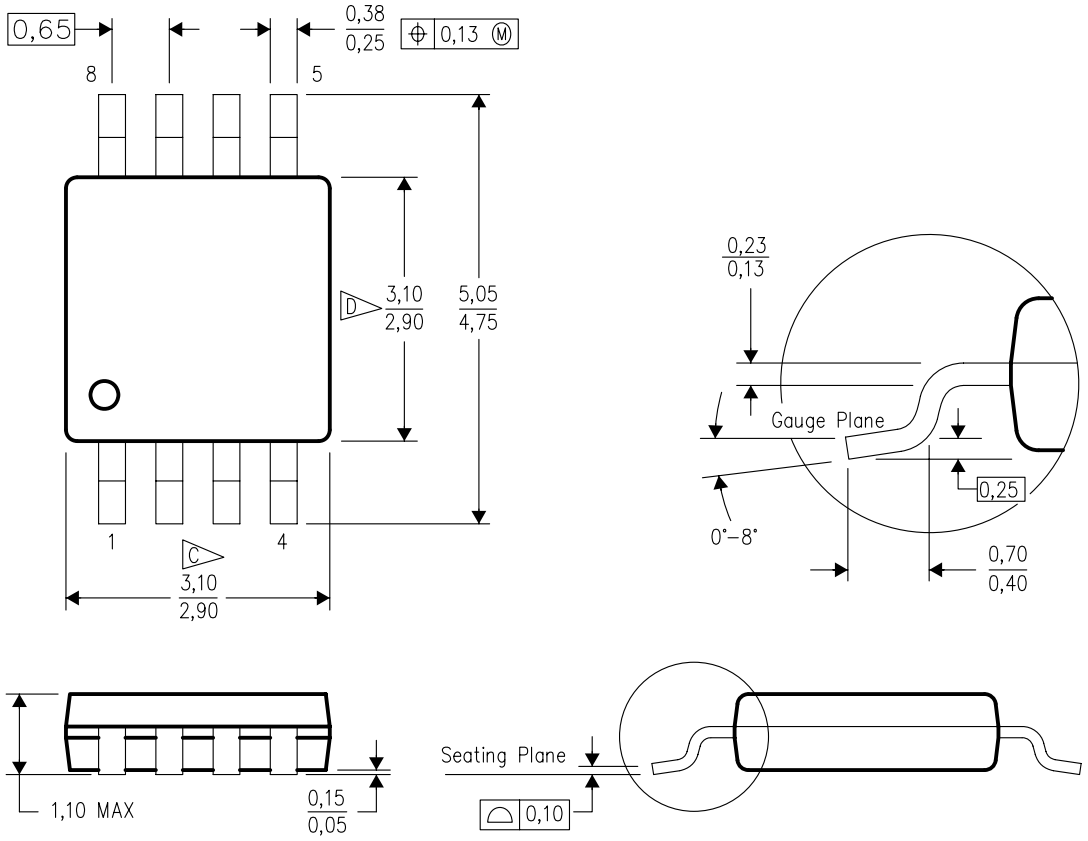
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

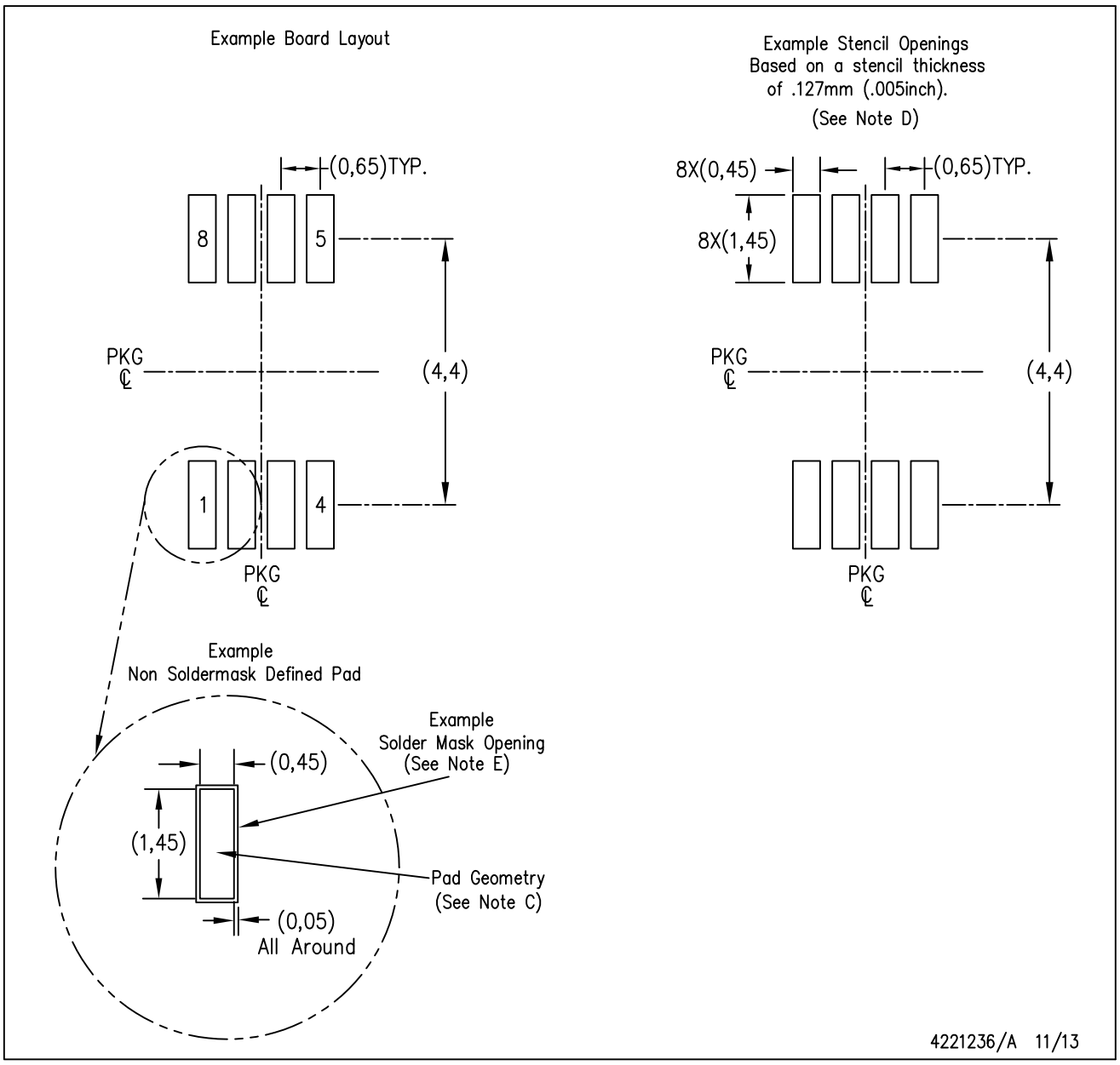
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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