LMH1983 3G/HD/SD Video Clock Generator with Audio Clock

1 Features

- Four PLLs for Simultaneous A/V Clock Generation
  - PLL1: 27 or 13.5 MHz
  - PLL2: 148.5 or 74.25 MHz
  - PLL3: 148.5/1.001 or 74.25/1.001 MHz
  - PLL4: 98.304 MHz / 2^X (X = 0 to 15)
- 3 x 2 Video Clock Crosspoint
- Flexible PLL Bandwidth to Optimize Jitter Performance and Lock Time
- Soft Resynchronization to New Reference
- Digital Holdover or Free-run on Loss of Reference
- Status Flags for Loss of Reference and Loss of PLL Lock
- 3.3 V Single Supply Operation
- I^2C Interface with Address Select Pin (3 States)

2 Applications

- Triple Rate (3G/HD/SD) SDI SerDes
- FPGA Reference Clock Generation/Cleaning
- Audio Embed or De-embed
- Video Cameras
- Frame Synchronizers (Genlock, DARS)
- A-D or D-A Conversion, Editing, Processing Cards
- Keyers and Logo Inserters
- Format or Standards Converters
- Video Displays and Projectors
- A/V Test and Measurement Equipment

3 Description

The LMH1983 is a highly-integrated programmable audio/video (A/V) clock generator intended for broadcast and professional applications. It can replace multiple PLLs and VCXOs used in applications supporting SMPTE serial digital video (SDI) and digital audio AES3/EBU standards. It offers low-jitter reference clocks for any SDI transmitter to meet stringent output jitter specifications without additional clock cleaning circuits.

The LMH1983 features automatic input format detection, simple programming of multiple A/V output formats, genlock or digital free-run modes, and override programmability of various automatic functions. The recognized input formats include HVF syncs for the major video standards, 27 MHz, 10 MHz, and 32/44.1/48/96 kHz audio word clocks.

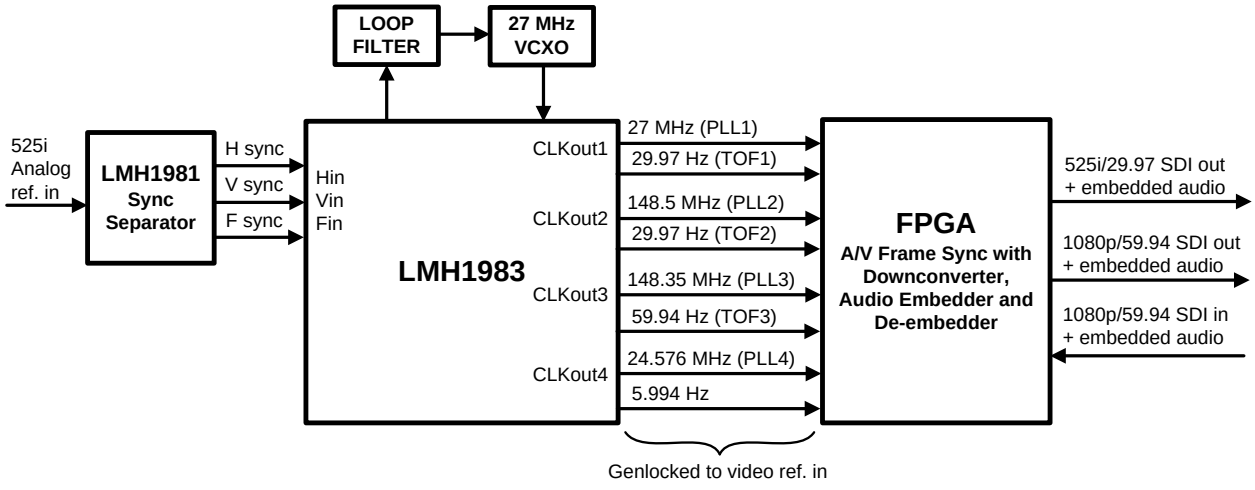
The dual-stage PLL architecture integrates four PLLs with three on-chip VCOs. The first stage (PLL1) uses an external low-noise 27 MHz VCXO with narrow loop bandwidth to provide a clean reference clock for the next stage. The second stage (PLL2, 3, 4) consists of three parallel VCO PLLs for simultaneous generation of the major digital A/V clock fundamental rates, including 148.5 MHz, 148.5/1.001 MHz, and 98.304 MHz (4 × 24.576 MHz). Each PLL can generate a clock and a timing pulse to indicate top of frame (TOF).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH1983	WQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (October 2014) to Revision I — **Page**

- Updated ESD Ratings table ... 5
- Updated formatting for *Typical Characteristics* graphs ... 9

Changes from Revision G (Nov 2012) to Revision H — **Page**

- Added Added, updated, or renamed the following sections: Device Information Table, *Pin Configuration and Functions*, *Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* ... 1
- Changed typical value of low output sink current to match simulation value of 1.25 mA. ... 6
- Added clarification about PLL4 behavior. ... 15
- Added clarification section for LOR Determination ... 17
- Changed appearance of Reg 0x11 mode description for clarity. ... 18
- Changed register initialization procedure to prevent device from exhibiting poor duty cycle performance on CLKout3 ... 19
- Added clarification note about 480i/29.97, 480p/59.94, 576i/25 and 576p/50 resolutions. ... 23
- Changed default value for Reg 0x11[3:2] bits. ... 28
- Changed Reg 0x11[3:2] description for clarification of TOF1_Sync behavior dependent on LOA window ... 28

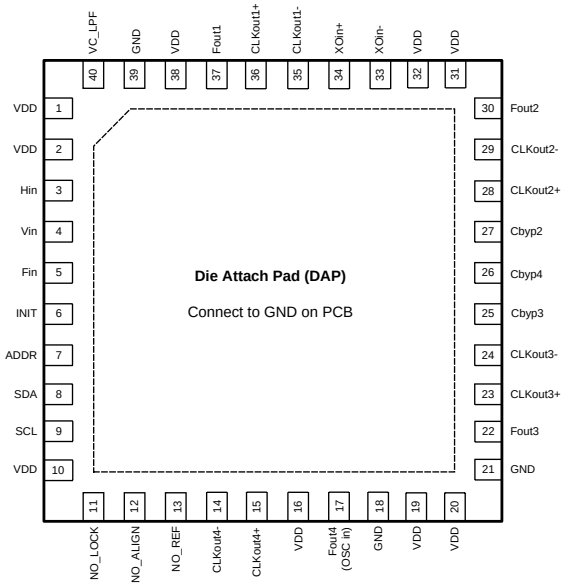
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5 Description (continued)

When locked to reference, an internal 10-bit ADC will track the loop filter control voltage. When a loss of reference (LOR) occurs, the LMH1983 can be programmed to hold the control voltage to maintain output accuracy within ±0.5 ppm (typical) of the previous reference. The LMH1983 can be configured to re-synchronize to a previous reference with glitch-less operation.

6 Pin Configurations and Functions

RTA40A Package
40-Pin WQFN Package with Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	SIGNAL LEVEL	DESCRIPTION
NO.	NAME			
1	VDD	–	Power	3.3-V supply for PLL1
2	VDD	–	Power	3.3-V supply for logic I/O
3	Hin	I	LVCMOS	Horizontal sync reference signal Auto polarity correction for HVF will be based off Hin polarity. Recognized clock inputs can be applied to Hin.
4	Vin	I	LVCMOS	Vertical sync reference signal
5	Fin	I	LVCMOS	Field sync (odd/even) reference signal
6	INIT	I	LVCMOS	Reset signal for audio-video phase alignment (rising edge triggered)
7	ADDR	I	LVCMOS	I^2C address select Pin settings: – Tie low: 0x65 (7-bit slave address in hex) – Float: 0x66 – Tie high: 0x67
8	SDA (1)	I/O	I^2C	I^2C Data signal
9	SCL (1)	I	I^2C	I^2C Clock signal
10	VDD	–	Power	3.3-V supply for logic I/O
11	NO_LOCK (2)	O	LVCMOS	Loss of lock status flag for PLLs 1-4 (active high)
12	NO_ALIGN	O	LVCMOS	Loss of alignment status flag for OUTs 1–4 (active high)

(1) SDA and SCL pins each require a pull-up resistor of 4.7 kΩ to the VDD supply.
(2) The NO_LOCK status flag is derived from the Lock Status register bits (LOCK1-4) for each PLL. Each lock status bit can be masked from the NO_LOCK flag by setting their respective mask bits.

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Pin Functions (continued)

PIN		I/O	SIGNAL LEVEL	DESCRIPTION
NO.	NAME			
13	NO_REF	O	LVCMOS	Loss of reference status flag (active high)
14 15	CLKout4– CLKout4+	O	LVDS	Audio clock from PLL4 (fundamental rate is 98.304 MHz). The output is 24.576 MHz by default and is selectable via the host.
16	VDD	–	Power	3.3 V supply for CLKout4
17	Fout4 (OSCin)	I/O	LVCMOS	Audio frame timing signal for OUT4 (active low.) Timing Generator fixed to PLL4 clock. The output is the audio-video-frame (AVF) pulse by default and is programmable via the host. **Optional** OSCin function can be used to apply a 27 MHz external clock for PLL4 to generate an audio clock independent of the video input reference; this function must be enabled via the host.
18	GND	–	GND	Ground
19	VDD	–	Power	3.3 V supply for PLL3 and PLL4
20	VDD	–	Power	3.3 V supply for CLKout3
21	GND	–	GND	Ground
22	Fout3	O	LVCMOS	Video frame timing signal for OUT3 (active low). Timing generator assignable to PLL1, PLL2, or PLL3. OUT3 format is selectable via the host.
23 24	CLKout3+ CLKout3–	O	LVDS	Video clock from PLL1, PLL2, or PLL3 depending on output crosspoint mode. The output is 148.35 MHz by default and is selectable via the host.
25	Cbyp3	–	Analog	Bias bypass for on-chip LDO for PLL3 Connect to 1.0 µF and 0.1 µF bypass capacitors.
26	Cbyp4	–	Analog	Bias bypass for on-chip LDO for PLL4 Connect to 1.0 µF and 0.1 µF bypass capacitors.
27	Cbyp2	–	Analog	Bias bypass for on-chip LDO for PLL2 Connect to 1.0 µF and 0.1 µF bypass capacitors.
28 29	CLKout2+ CLKout2–	O	LVDS	Video clock from PLL1, PLL2, or PLL3 depending on output crosspoint mode. The output is 148.5 MHz by default and is selectable via the host.
30	Fout2	O	LVCMOS	Video frame timing signal for OUT2 (active low). Timing generator assignable to PLL1, PLL2, or PLL3. OUT2 format is selectable via the host.
31	VDD	–	Power	3.3-V supply for CLKout2
32	VDD	–	Power	3.3-V supply for PLL2
33 34	XOin– (3) XOin+	I	LVCMOS/LVDS	27 MHz VCXO clock signal for PLL1. – LVCMOS: Directly connect clock signal to XOin+ and bias XOin- to mid-supply with 0.1µF bypass capacitor. – LVDS: Directly connect LVDS clock signals to XOin+ and XOin-. (4)
35 36	CLKout1– CLKout1+	O	LVDS	Video clock from PLL1. The output is 27 MHz by default and is selectable via the host.
37	Fout1	O	LVCMOS	Reference frame timing signal for OUT1 (active Low). Timing generator fixed to PLL1 OUT1 Format follows the reference input format.
38	VDD	–	Power	3.3 V supply for CLKout1
39	GND	–	GND	Ground
40	VC_LPF	O	Analog	Loop filter for PLL1 charge pump output with VCXO Voltage Control (VC) sensing. If free-run and holdover mode, PLL1 is disabled and an internal DAC outputs a control voltage to the VCXO.
–	DAP	–	GND	Die Attach Pad (Connect to ground on PCB)

(3) XOin must be driven by a 27 MHz clock in order to read or write registers via I^2C.
(4) A TCXO or other clean 27 MHz oscillator can be applied for standalone clock generation using PLLs 2-4 (bypass PLL1).

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

		MIN	MAX	UNIT
V_{DD}	Supply voltage		3.6	V
V_I	Input voltage (any input)	-0.3	V_{DD} + 0.3	V
V_O	Output voltage (any output)	-0.3	V_{DD} + 0.3	V
T_{JMAX}	Junction temperature		150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering information, see SNOA549.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2500	V
		Machine model (MM) (2)	250	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2500 V may actually have higher performance.
(2) Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC).
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input Voltage	0		V_{DD}	V
Temperature Range, T_A	-40		85	°C

7.4 Thermal Information

THERMAL METRIC (1)		RTA	UNIT
		40 PINS	
T_{JMAX}	Junction Temperature, V_{DD}	3.3 ± 5%	°C/W
$R_{\theta JA}$	Thermal Resistance (2)	33	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $PD = (T_{J(MAX)} – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC Board.

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7.5 Electrical Characteristics(1)

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{DD} = 3.3 V, R_{L_CLK} = 100 Ω (CLKout differential load).

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
I_{DD}	Total supply current	Default register settings, no load on logic outputs. V_{DD} = 3.465 V		170	212	mA
I_{DD}	Total supply current	PLL2, PLL3 and PLL4 disabled, no load on logic outputs. V_{DD} = 3.465 V		60	100	mA
REFERENCE INPUTS (Hin, Vin, Fin)						
V_{IL}	Low input voltage	I_{IN} = ±10 µA	0		0.3 V_{DD}	V
V_{IH}	High input voltage	I_{IN} = ±10 µA	0.7 V_{DD}		V_{DD}	V
T_{AFD}	Auto-format detection time	Time from when reference input first presented to when detected as indicated by NO_REF going low. Reference timing must be stable and accurate (no missing pulses).		2	4	Input Frames
OSCin LOGIC INPUTS						
V_{IL}	Low input voltage	I_{IN} = ±10 µA	0		0.3 V_{DD}	V
V_{IH}	High input voltage	I_{IN} = ±10 µA	0.7 V_{DD}		V_{DD}	V
I²C INTERFACE (SDA, SCL)						
V_{IL}	Low input voltage		0		0.3 V_{DD}	V
V_{IH}	High input voltage		0.7 V_{DD}		V_{DD}	V
I_{IN}	Input current	V_{IN} between 0.1 V_{DD} and 0.9 V_{DD}	−10		+10	µA
I_{OL}	Low output sink current	V_{OL} = 0V or 0.4V		1.25		mA
STATUS FLAG OUTPUTS (NO_REF, NO_ALIGN,NO_LOCK)						
V_{OL}	Low output voltage	I_{OUT} = +10 mA			0.4	V
V_{OH}	High output voltage	I_{OUT} = −10 mA	V_{DD}-0.4V			V
FRAME TIMING OUTPUTS						
V_{OL}	Low output voltage	I_{OUT} = +10 mA Fout1, Fout2, Fout3(4)			0.4	
V_{OH}	High output voltage	I_{OUT} = -10mA Fout1, Fout2, Fout3(4)	V_{DD}-0.4 V			
I_{OZ}	Output shutdown leakage current	Output buffer shutdown, pin connected to V_{DD} or GND V_{DD} = 3.465V		0.4	10	|µA|
VIDEO and AUDIO CLOCK OUTPUTS (CLKout1, CLKout2 and CLKout3)						
t_{DJ}	27 MHz TIE deterministic Jitter	Measured at CLKout1 all other CLKouts shutdown		250		fs
		Measured at CLKout1, other CLKouts output default PLL		250		fs
	148.5 MHz TIE deterministic Jitter	Measured at CLKout2 all other CLKouts shutdown		8		ps
		Measured at CLKout2, other CLKouts output default PLL		8		ps
	148.35 MHz TIE deterministic Jitter	Measured at CLKout3 all other CLKouts shutdown		4		ps
		Measured at CLKout3, other CLKouts output default PLL		4		ps
	24.576 MHz TIE deterministic Jitter	Measured at CLKout4 all other CLKouts shutdown		15		ps
		Measured at CLKout4, other CLKouts output default PLL		15		ps

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using statistical analysis methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) t_D for FoutX is measured from the positive clock edge of CLKout to the negative edge of FoutX at the 50% levels.

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Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{DD} = 3.3 V, R_{L_CLK} = 100 Ω (CLKout differential load).

PARAMETER		TEST CONDITIONS	MIN[2]	TYP[3]	MAX[2]	UNIT
t_{RJ}	27 MHz TIE random Output Jitter[5]	Measured at CLKout1, other CLKouts shutdown		2.7		ps
		Measured at CLKout1, other CLKouts output default PLL		2.7		ps
	148.5 MHz TIE Random Output Jitter[5]	Measured at CLKout2, other CLKouts shutdown		3.0		ps
		Measured at CLKout2, other CLKouts output default PLL		3.0		ps
	148.35 MHz TIE Random Output Jitter [5]	Measured at CLKout3, other CLKouts shutdown		3.5		ps
		Measured at CLKout3, other CLKouts output default PLL		3.5		ps
	24.576 MHz TIE Random Output Jitter[5]	Measured at CLKout4, other CLKouts shutdown		3.4		ps
		Measured at CLKout4, other CLKouts output default PLL		3.4		ps
T_D	Duty cycle	Measured at 50% level of clock amplitude, any output clock		50%		
t_R	Rise time 20% to 80%	15 pF load		400		ps
t_F	Fall time 80% to 20%	15 pF load		400		ps
V_{OD}	Differential signal output voltage	100 Ω differential load, CLKout1, CLKout2 or CLKout3[6]	247	350	454	mV
V_{OS}	Common signal output voltage	100 Ω differential load, CLKout1, CLKout2 or CLKout3[6]	1.125	1.25	1.375	V
$\lvert V_{OD} \rvert$	|Change to V_{OD}| for complementary output states	100 Ω differential load, CLKout1, CLKout2 or CLKout3[6]			50	|mV|
$\lvert V_{OS} \rvert$	|Change to V_{OS}| for complementary output states	100 Ω differential load, CLKout1, CLKout2 or CLKout3[6]			50	|mV|
I_{OS}	Output short circuit current	Differential clock output pins connected to GND for CLKout1, CLKout2, or CLKout3			24	|mA|
I_{OZ}	Output shutdown leakage current	Output buffer in shutdown mode, differential clock output pins connected to V_{DD} or GND		1	10	|µA|
VCXO INPUT (XOin)						
f_{OFF}	Maximum relative frequency offset between VCXO input and H input	Assumes H input jitter of ±15 ns		±150		ppm
V_{XOin_SE}	Single-ended signal input voltage range	Single-ended input buffer mode	0		V_{DD}	V
V_{XOin_DIFF}	Differential signal input voltage range	Differential input buffer mode, V_{CM} = 1.2 V	247	350	454	mV
DIGITAL HOLDOVER and FREE-RUN SPECIFICATIONS						
V_{VCout_RNG}	DAC output voltage range	Digital Free-run Mode	0.5		V_{DD} - 0.5V	V

(5) The SD and HD clock output jitter is based on XO input clock with 20 ps peak-to-peak using a time interval error (TIE) jitter measurement. The typical TIE peak-to-peak jitter was measured on the LMH1983 evaluation bench board using TDSJIT3 jitter analysis software on a Tektronix DSA71604 oscilloscope and 1 GHz active differential probe. TDSJIT3 Clock TIE Measurement Setup: 10^{-12} bit error rate (BER), >100K samples recorded using multiple acquisitions. Oscilloscope Setup: 20 mV/div vertical scale, 10 µs/div horizontal scale, and 25 GS/s sampling rate

(6) The differential output swing and common mode voltage may be adjusted via the I^2C interface. Testing is done with a value of 0x3E loaded into Register 0x3A.

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7.6 Frame Timing Outputs Timing Requirements

			MIN	NOM	MAX	UNIT
t_R	Rise time 20% to 80%	15 pF load		1		ns
t_F	Fall time 20% to 80%	15 pF load		1		ns

7.7 Frame Timing Outputs Switching Characteristics

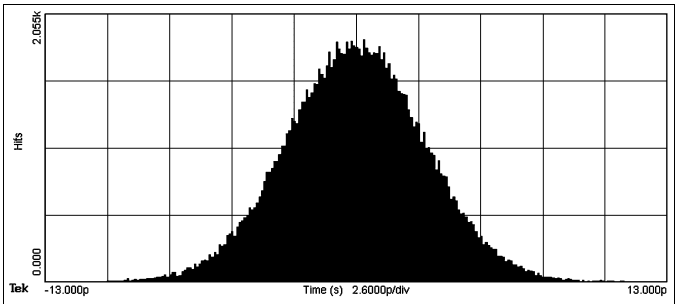
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{D1} (1)	Timing output delay time	TOF1 delay measured from the CLKout1 clock reset edge. Delay spec applies for all output clock and format supported by the output pair following output initialization. 15 pF load.		22		ns
t_{D2}	Timing output delay time	TOF2 delay measured from the CLKout2 clock reset edge. Delay spec applies for all output clock and format supported by the output pair following output initialization. 15 pF load.		2		ns
t_{D3}	Timing output delay time	TOF3 delay measured from the CLKout3 clock reset edge. Delay spec applies for all output clock and format supported by the output pair following output initialization. 15 pF load.		2		ns
t_{D4}	Timing output delay time	TOF4 delay measured from the CLKout4 clock reset edge. Delay spec applies for all output clock and format supported by the output pair following output initialization. 15 pF load.		22		ns

(1) t_D for CLKoutX is measured from the positive clock edge of XOin to the positive clock edge of CLKoutX using 50% levels. The measurement is taken at the clock cycle where the input and output clocks are phase aligned.

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7.8 Typical Characteristics



Horizontal Scale: 2.6ps / Division

Figure 1. CLKout1 Jitter Histogram

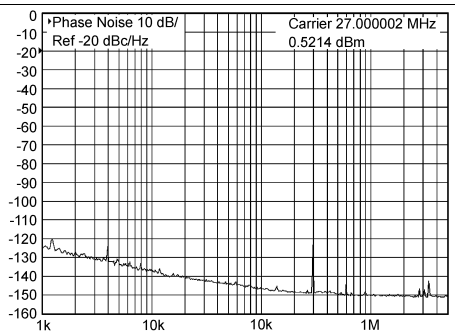
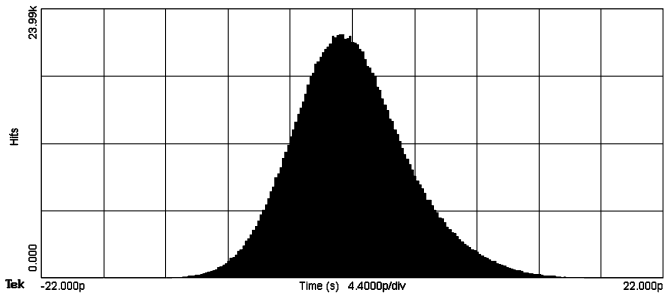


Figure 2. CLKout1 Phase Noise



Horizontal Scale: 4.4ps / Division

Figure 3. CLKout2 Jitter Histogram

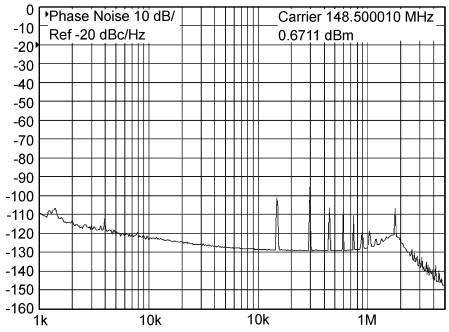
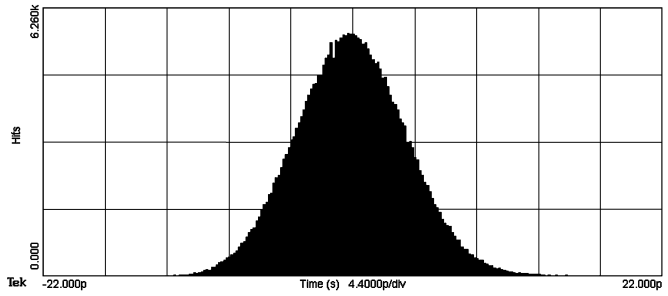


Figure 4. CLKout2 Phase Noise



Horizontal Scale: 4.4ps / Div

Figure 5. CLKout3 Jitter Histogram

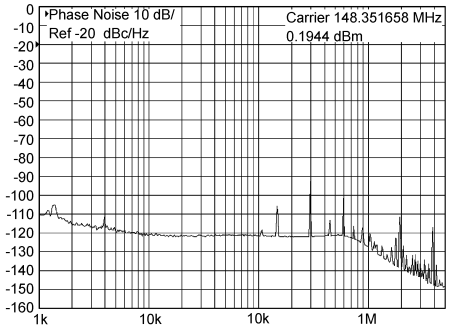
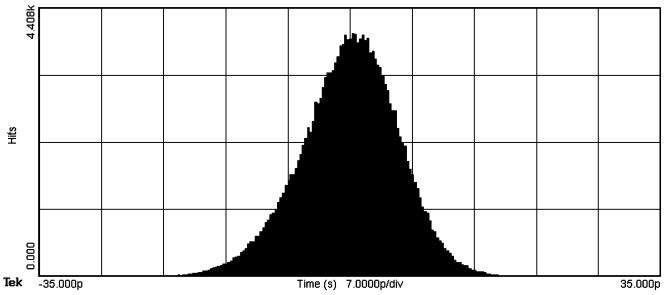


Figure 6. CLKout3 Phase Noise

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Typical Characteristics (continued)



Horizontal Scale: 7 ps / Div

Figure 7. CLKout4 Jitter Histogram

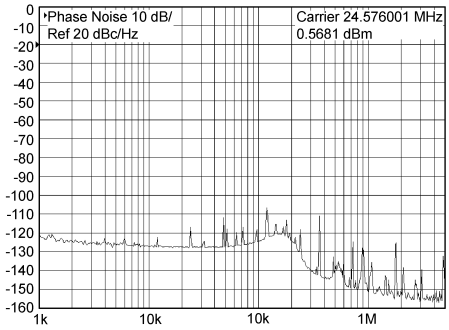


Figure 8. CLKout4 Phase Noise

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8 Detailed Description

8.1 Overview

The LMH1983 is an analog phase locked loop (PLL) clock generator that can output simultaneous clocks at a variety of video and audio rates, synchronized or “genlocked” to Hsync and Vsync input reference timing. The LMH1983 features an output Top of Frame (TOF) pulse generator for each of its four channels, each with programmable timing that can also be synchronized to the reference frame. The clock generator uses a two-stage PLL architecture. The first stage is a VCXO-based PLL (PLL1) that requires an external 27 MHz VCXO and loop filter. In Genlock mode, PLL1 can phase lock a low loop bandwidth VCXO clock to the input reference. The VCXO provides a low phase noise clock source to attenuate input timing jitter for minimum jitter transfer. The combination of the external VCXO, external loop filter, and programmable PLL parameters provide flexibility for the system designer to optimize the loop bandwidth and loop response for the application.

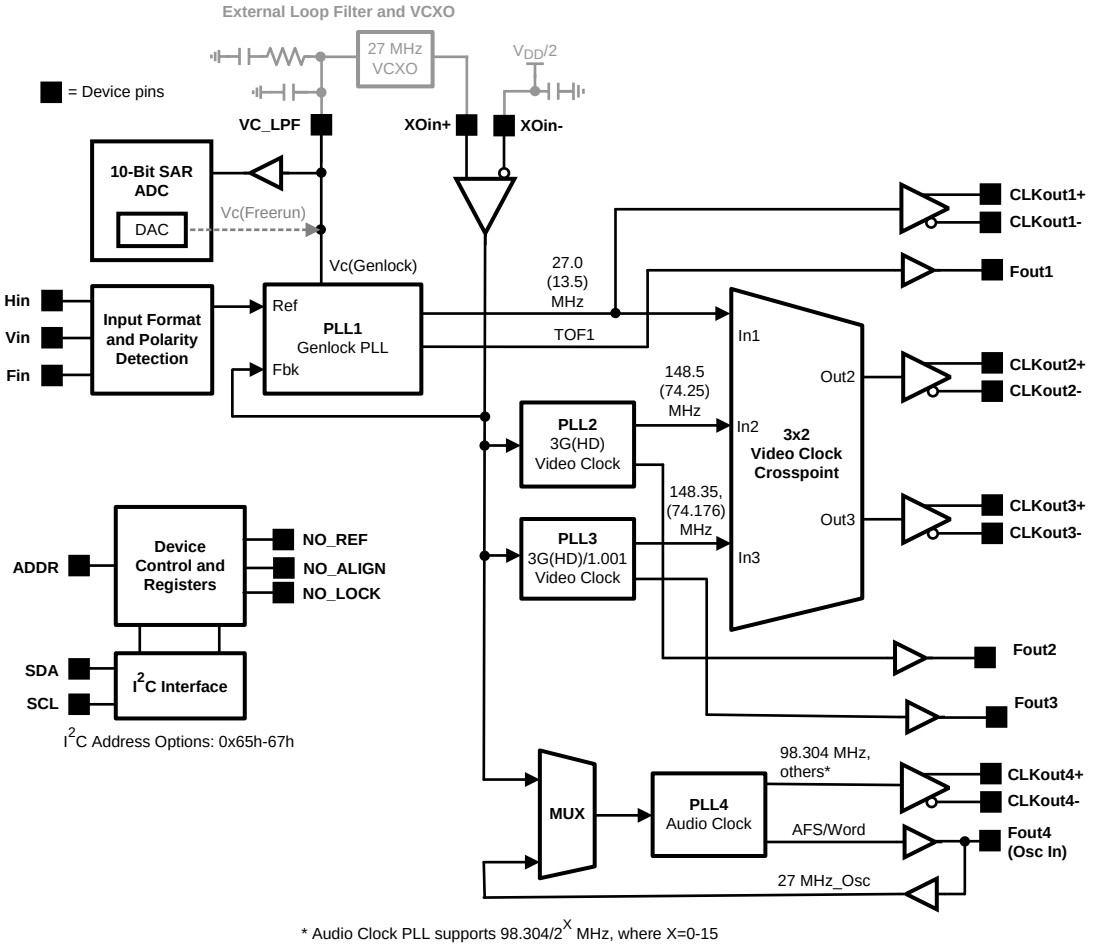
The second stage consists of three PLLs (PLL2, PLL3, PLL4) with integrated VCOs and loop filters. These PLLs continually track the reference VCXO clock phase from PLL1 regardless of the device mode. The PLL2 and PLL3 have pre-configured divider ratios to provide frequency multiplication or translation from the VCXO clock frequency to generate the two common HD clock rates (148.5 MHz and 148.35 MHz). PLL4 is pre-configured to generate an audio clock that defaults to a 24.576 MHz output, although PLL4 has several registers that allow it to be re-configured for a variety of applications.

The VCO PLLs use a high loop bandwidth to assure PLL stability, so the VCXO of PLL1 must provide a stable low-jitter clock reference to ensure optimal output jitter performance. Any unused clock or TOF output can be placed in Hi-Z mode. This may be useful for reducing power dissipation as well as reducing jitter or phase noise on the active clock output. The TOF pulse can be programmed to indicate the start (top) of frame and even provide format cross-locking. The output format registers should be programmed to specify the output timing (output clocks and TOF pulse), the output timing offset relative to the reference, and the output initialization (alignment) to the reference frame.

When a loss of reference occurs during genlock, PLL1 can default to either Free-run or Holdover operation. When Free-run is selected, the output frequency accuracy will be determined by the external bias on the free-run control voltage input pin, VC_LPF. When Holdover is selected, the loop filter can hold the control voltage to maintain short-term output phase accuracy for a brief period in order to allow the application to select the secondary input reference and re-lock the outputs. These options in combination with a proper PLL1 loop response design can provide flexibility to manage output clock behavior during loss and re-acquisition of the reference. The reference status and PLL lock status flags can provide real-time status indication to the application system. The loss of reference and lock detection thresholds can also be configured.

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8.2 Functional Block Diagram



8.3 Feature Description

The following subsections provide information about the various control mechanisms and features that are fundamental to the LMH1983 clock generator.

8.3.1 Control of PLL1

PLL1 generates a 27 MHz reference that is used as the primary frequency reference for all of the other PLLs in the device. PLL1 has a dual loop architecture with the primary loop locking the external 27 MHz VCXO to a harmonic of the H_{IN} signal. In addition to this loop, there is a secondary loop that may be used in genlock operations. This second loop compares the phase of the TOF1 output signal from the LMH1983 to the F_{IN} signal. In order to bring the frame alignment of the output signals into sync with the input reference, the second loop may override the primary loop. Detailed information about controlling this functionality is described in *TOF1 Alignment*.

To illustrate the dual loop architecture of PLL1, refer to the PLL1 block diagram in Figure 9. The primary loop takes the reference applied to the H_{IN} input and divides that by R (stored in Registers 0x29 and 0x2A). The dividend is then compared in phase and frequency to the output of the external 27 MHz VCXO divided by N (stored in Registers 0x2B and 0x2C). The PFD (phase frequency detector) then generates output pulses that are integrated via an external loop filter that drives the control voltage of the external VCXO.

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Feature Description (continued)

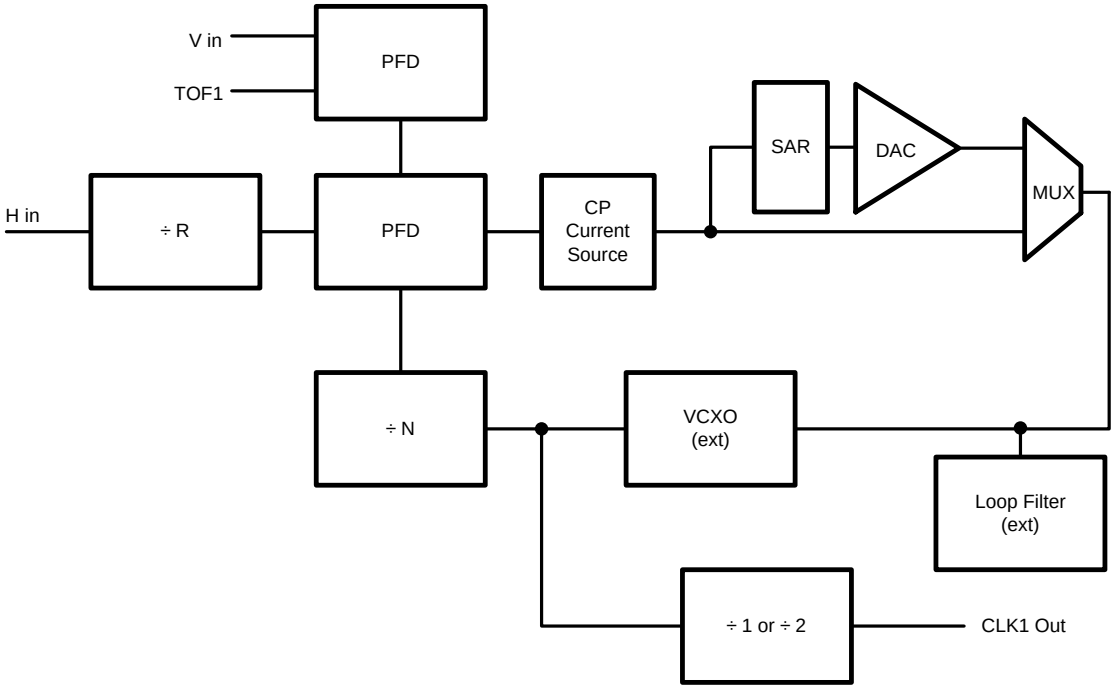


Figure 9. PLL1 Block Diagram

Since PLL2, PLL3, and PLL4 all use PLL1 as their input reference, the performance of PLL1 affects the performance of all four clock outputs. The loop filters for the other three PLLs are internal, and the bandwidths are set significantly higher than that of PLL1, so the low frequency jitter characteristics of all four clock outputs are determined by the loop response of PLL1. Accordingly, special attention should be paid to the PLL1's loop bandwidth and damping factor.

8.3.2 PLL1 Loop Response Design Equations

The loop response is primarily determined by the loop filter components and the loop gain. A passive second order loop filter consisting of R_S, C_S, and C_P components can provide sufficient input jitter attenuation for most applications. In some cases, a higher order filter may be used to shape the low frequency response of PLL1 further. Assuming a topology for the loop filter similar to that shown in the Figure 9, the bandwidth of the PLL is determined by:

$$BW_{PLL1} = R_S x\ K_{VCO}\ x\ I_{CP1}/(2*\pi*FB_DIV) \quad (1)$$

where

- R_S is the series resistor value in the external loop filter.
- K_{VCO} is the nominal 27 MHz VCXO gain in Hz/V. K_{VCO}= Pull_range*27 MHz/Vin_Range. For the VCXO used in the typical interface circuit (Mfgr: CTS, P/N 357LB3C027M0000): L_{VCO}=100 ppm*27 MHz / (3.0V-0.3V) = 1000 Hz/V
- I_{CP1} is the current from the PLL1 charge pump.
- FB_DIV is the divide ratio of the PLL, which is set by the R and N register values, this will be equal to the number of 27 MHz clock pulses in one H_{IN} period. For NTSC, this value will be 1716.

Under normal operation, several of these parameters are set by the device automatically, for example the charge pump current and the value of 'FB_DIV'. When the input reference format changes, both N and the charge pump current are updated, N is changed to allow for lock to the new reference, and the charge pump current is adjusted to maintain constant loop bandwidth.

It should be noted that this bandwidth calculation is an approximation and does not take into account the effects of the damping factor or the second pole introduced by C_P.

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Feature Description (continued)

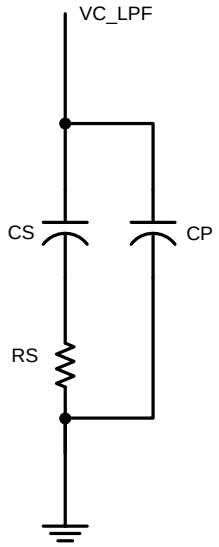


Figure 10. External Loop Filter Schematic Detail

At frequencies far above the –3dB loop bandwidth, the closed-loop frequency response of PLL1 will roll off at about –40dB/decade, which is useful for attenuating input jitter at frequencies above the loop bandwidth. Near the –3dB corner frequency, the roll-off characteristic depends on other factors, such as damping factor and filter order.

To prevent output jitter due to the modulation of the VCXO by the PLL's phase comparison frequency, the bandwidth needs to meet the following criterion:

$$BW \leq (27\ MHz / FB_DIV) / 20 \quad (2)$$

PLL1's damping factor can be approximated by:

$$DF = (R_S/2)\sqrt{(I_{CP1} \times C_S \times K_{VCO}/FB_DIV)}$$

where

- C_S is the value of the series capacitor (in Farads) (3)

Typically, DF is targeted to be between $1/\sqrt{2}$ and 1, which will yield a good trade-off between lock time and reference spur attenuation. DF is related to the phase margin, a measure of the PLL stability.

There is a second parallel capacitor, C_P, which is needed to filter the reference spurs introduced by the PLL. The spurs may modulate the VCXO control voltage, leading to jitter. The following relationship should be used to determine C_P:

$$C_P \approx C_S/20 \quad (4)$$

The PLL loop gain, K, can be calculated as:

$$K = I_{CP1} \times K_{VCO}/FB_DIV \quad (5)$$

Therefore, Bandwidth and Damping Factor can be expressed in terms of K:

$$BW = R_S \times K \quad (6)$$

$$DF = (R_S/2) \times \sqrt{(C_S \times K)} \quad (7)$$

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Feature Description (continued)

8.3.3 Control of PLL2 and PLL3

PLL2 and PLL3 have the least amount of flexibility of the four PLLs in the LMH1983. They are pre-programmed to run at 148.5 MHz and 148.35 MHz respectively. There is a divide-by-two option available to allow the output to be 74.25 MHz or 74.18 MHz, should these frequencies be required. These two PLLs can also be disabled – disabling PLL2 or PLL3 can save significant amounts of power if that particular clock is not required. Figure 11 shows a simplified functional block diagram of PLL2 and PLL3.

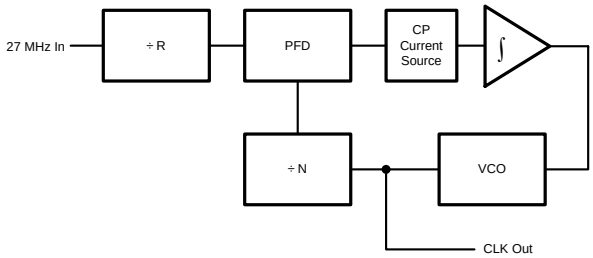


Figure 11. PLL2 / PLL3 Block Diagram

8.3.4 Control of PLL4

Although originally intended to generate only a clock for audio use, PLL4 features much greater versatility. Several registers may be used to configure PLL4 to generate a broad selection of frequencies. The default state for PLL4 is to generate 24.576 MHz (48 kHz x 512) on the output of CLK4 and a 5.996 Hz output from TOF4. This is done by taking CLK1 (27 MHz), and dividing by 75, resulting in a signal of 360 kHz. This frequency is compared to the internal PLL4 VCO, nominally 1.2 GHz, divided by 4096. The VCO frequency is adjusted via register control until the resulting frequency yields 360 kHz. The final VCO frequency is then divided by 12 to generate a 98.304 MHz signal (48 kHz x 2048). Any power of two multiple of 48 kHz can be generated by changing the contents of the PLL4_DIV component of Register 0x34. Note that the divider here is in powers of 2, so the default value of 2 results in the 98.304 MHz signal being divided by 2^2 or 4. The final CLKout4 frequency is therefore 24.576 MHz. PLL4_DIV is a 4-bit value, so values up to 15 may be programmed, resulting in a divide by 2^{15} or 32,768. If audio clocks based on a 44.1 kHz sampling clock are desired, refer to Application Note AN–2108, *Generating 44.1 kHz Based Clocks with the LMH1983*, (SNLA129) for detailed instructions.

TOF4 has two different operation modes. When the AFS_mode bit (Register 0x09) is set to a 0, then TOF4 is derived by dividing CLKout4 by a value of 2^{TOF4_ACLK} (Register 0x4A). if the AFS_mode bit is set to 1, then TOF4 is derived from TOF1 — divided by AFS_div (Register 0x49). When AutoFormatDetect is true, then the AFS_div register is read only and is internally set depending upon the format detected.

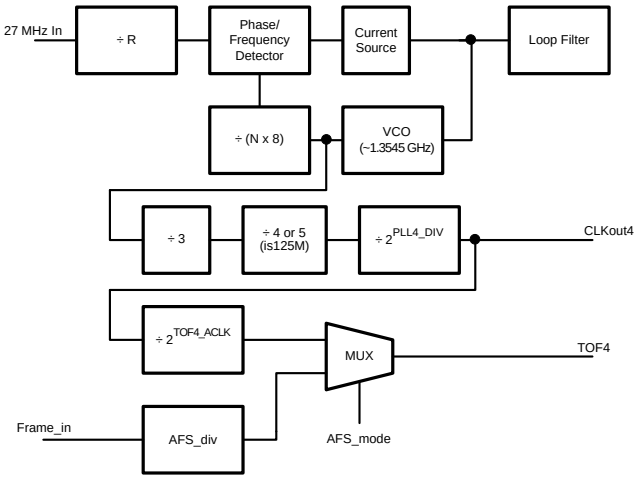


Figure 12. PLL4 Block Diagram

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Feature Description (continued)

8.3.5 Clock Output Jitter

Many circuits that require video clocks, such as the embedded Serializers and Deserializers found in FPGAs, are sensitive to jitter. In all real world applications, jitter has a random component, so it is best specified in statistical terms. The SMPTE serial standards (SMPTE 259M, SMPTE 292M and SMPTE 424M) use a frequency domain method of specifying jitter where they refer to the peak-to-peak jitter of a signal after the jitter has been bandpass filtered. Jitter at frequencies below 10 Hz is ignored, and the jitter in a band from 10 Hz to an intermediate frequency (1 kHz for the 270 Mbps standard, 100 kHz for the 1.5 Gbps and 3 Gbps standards) is referred to as timing jitter. Jitter from the intermediate frequency up to 1/10 of the serial rate is referred to as alignment jitter. The limits that the SMPTE standards place are peak-to-peak limits, but especially at the higher rates, random processes have a significant impact, and it is not possible to consider peak-to-peak jitter without a corresponding confidence level. The methodology used to specify the jitter on the LMH1983 decomposes the jitter into a deterministic component (t_{DJ}) plus a random component (t_{RJ}). This is the methodology used by the jitter analysis tools supported on high bandwidth oscilloscopes and timing analysis tools from major instrumentation manufacturers.

To convert between RMS jitter and peak-to-peak jitter, the Bit Error Rate (BER) must be specified. Since jitter is a random event, without a known BER, the peak-to-peak jitter will be dependent upon the observation time and can be arbitrarily large. The equation that links peak-to-peak jitter to RMS jitter is:

$$t_{P-P} = t_{DJ} + \alpha * t_{RJ} \quad (8)$$

where α is determined by the BER according to the equation:

$$1/2\text{erfc}(\sqrt{2}*\alpha) = \text{BER} \quad (9)$$

The erfc (error function) can be found in several mathematics references and is also a function in both Excel and MATLAB. A fairly common BER used for these calculations is 10^{-12}, which yields a value of α = 14.

Another common method for evaluating the jitter of a clock output is to look at the phase noise as a function of frequency. Plots showing the phase noise for each of the four CLKout outputs can be found in Figure 1 through Figure 8.

8.3.6 Lock Determination

There are four bits in Register 0x02 that indicate the lock status of the four PLLs. Lock determination for PLL1 can be controlled through two registers: LockStepSize (Register 0x2D) and Loss of Lock Threshold (Register 0x1C). The LockStepSize register sets the amount of variation that is permitted on the VC_LPF pin while still considering the device to be locked. If the reference to the LMH1983 has a large amount of jitter, then the device may be unable to declare lock because the LockStepSize is set too low. The second register, the Loss of Lock Threshold register, controls the lock state declaration of PLL1. This register sets a number of cycles on the H_{IN} input that must be seen before loss of lock is declared. For some reference signals, there can be several missing H_{IN} pulses during vertical refresh. Therefore, it is suggested that this register be loaded with a value greater than six (Loss of Lock Threshold > 6). Pin 11, NO_LOCK, gives the lock status of the LMH1983. Note that the status of the NO_LOCK pin can also be read from Register 0x01, and it is a logical OR of the four individual NO_LOCK status bits of the four PLLs. The NO_LOCK status pin is masked by the bits in the PLL Lock mask (Register 0x1D), and the status is also masked if an individual PLL is powered down.

8.3.7 Lock Time Considerations

The lock time of the LMH1983 is dominated by the lock time of PLL1. The other PLLs have much higher loop bandwidths, and as a result, they lock more quickly than PLL1 does. Therefore, lock time considerations mainly rely on PLL1. The lock time for a PLL is dependent upon the loop bandwidth (see Equation 1). A small loop bandwidth typically increases the time required to achieve lock. To counter this issue, the LMH1983 also allows a Fastlock mode. In this mode, the bandwidth is increased by increasing the charge pump current when the loop is unlocked. Then, at a time programmed by the user after lock is declared, I_{CP1} is throttled back to drop the bandwidth to the desired set point. The result is both fast lock time and very low residual jitter.

Another factor when considering lock time is whether 'drift lock' has been enabled or not (see *TOF1 Alignment*). If drift lock is enabled and there is a significant difference in the phase of TOF1 relative to the F_{IN} signal, the VCXO is slewed to ramp the clock rate up or down until the two framing signals are brought into alignment. It is possible that this process may take a long time (tens of seconds).

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Feature Description (continued)

Aside from the time required for the PLL to lock, there is a circuit that determines how to set the NO_LOCK output pin. The LMH1983 PLL operates by adjusting the voltage that is applied to the VCXO control pin to lock the VCXO to a harmonic of the incoming reference. When the device is not locked, the PLL pulls the VCXO control voltage to one extreme of its range to slew the voltage into lock. Once the phase differences between the VCXO and the reference are small, the device begins to nudge the control voltage back and forth to maintain the phase difference. An adjustment might be necessary either due to VCXO drift or due to jitter on the reference. To determine the status of NO_LOCK, the LMH1983 establishes a window to view the amount of adjustment that is required over a period of time. Two parameters are set via register control to determine NO_LOCK status. LockStepSize (Register 0x2D) sets the amount of time in which to observe the signal, and Loss of Lock Threshold (Register 0x1C) sets the amount of variation in the control voltage that can be seen over this time frame while still considering the device to be locked.

To minimize the amount of time necessary to assert lock, load LockStepSize (Register 0x2D) with a value of 0x01 and the Loss of Lock Threshold (Register 0x1C) with a value of 0x1F. The effect of this change can be seen in Figure 13:

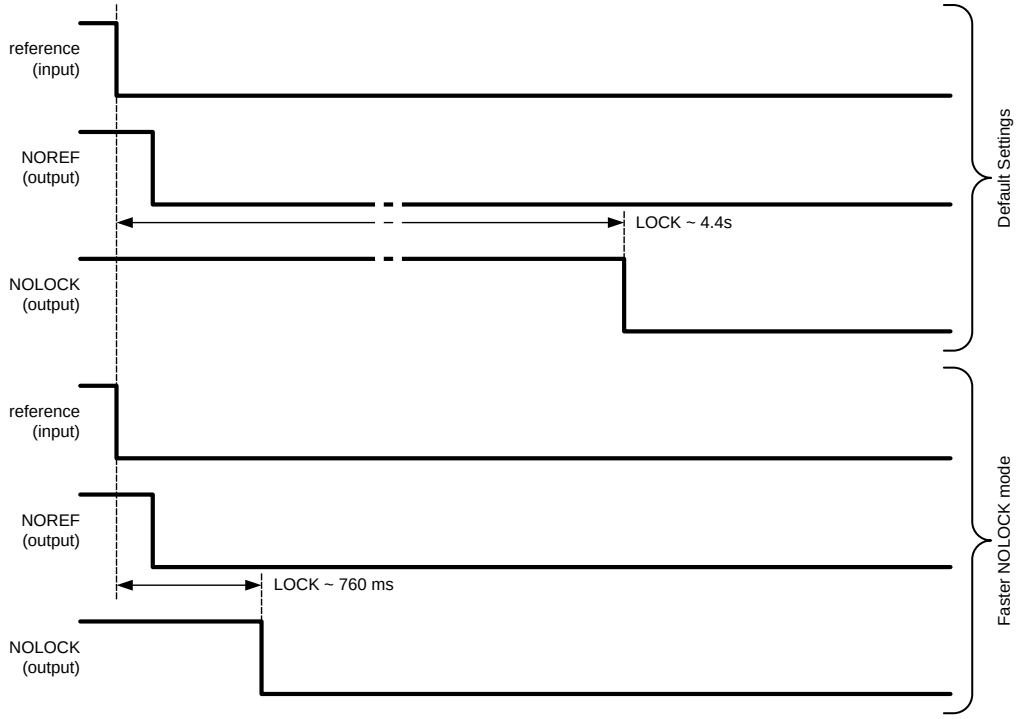


Figure 13. Faster NO_LOCK Reaction Mode Timing

8.3.8 LOR Determination

When the PLL is not locked, there is an internal counter that counts the number of 27 MHz clock pulses between consecutive HSync pulses divide-by-two. This counter saturates at 0x7FFF (or 32767 decimal). Once this counter saturates, LOR is declared. Given this is a divide-by-two counter, the time to declare LOR is: (2 x 32767) / (27E6) = 2.4 ms. On the other hand, when the PLL is locked and there are missing HSync pulses, LOR is set when the internal counter is greater than the following: (Number of 27 MHz clocks in one Hsync pulse + 3) x (LOR_THRES + 1).

8.3.9 Output Driver Adjustments

The LVDS output drivers can be adjusted via the I^2C interface to change the differential output voltage swing, the common mode voltage, and the amount of pre-emphasis applied to the LVDS output:

- Register 0x3A, Bit 7 turns on the pre-emphasis, which may be used to extend the reach between the LMH1983 and the load. It is recommended that the trace length is kept short, as longer traces have more opportunity to couple with hostile signals and degrade jitter performance.

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Feature Description (continued)

- The differential output swing of the CLKout pins is adjusted through Register 0x3A, Bits [6:4]. A larger value loaded into Bits [6:4] correspond to an increase in the output swing.
- The common mode output voltage can be adjusted via Register 0x3A, Bits [3:0].

8.3.10 TOF1 Alignment

Each of the four clock outputs has a corresponding Top Of Frame (TOF) output signal. The LMH1983 is programmed with a video format for each of the three video clocks (CLKout 1-3), and the TOF signal provides a digital indication when the start of a new frame occurs for that particular format. As an example, if PLL1 is programmed with a video format corresponding to NTSC, CLK1 is 27 MHz, and TOF1 outputs a pulse once per frame, or once every 900,900 clock cycles. In its default state, the LMH1983 detects the input reference format and programs this format as the output format for CLKout1. Therefore, if the input reference is an NTSC reference, then TOF1 will default to a 29.97 Hz signal.

If the H_{IN}, V_{IN}, and F_{IN} inputs to the LMH1983 are coming from the LMH1981 Sync Separator, then the rising edge of the F_{IN} input will come in the middle of a line (between H_{IN} pulses). The TOF pulse, if aligned, will be a pulse with a width of 1 x H period and transitions aligned with the leading edges of the H_{IN} pulses. When set for zero offset, the TOF pulse will be high during the H period where the F_{IN} input transitions, as seen in Figure 14.

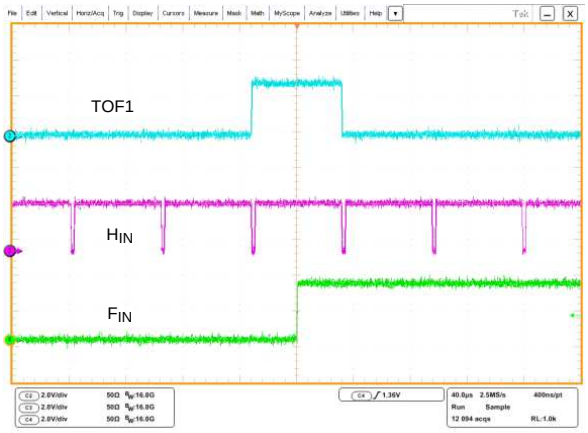


Figure 14. TOF1 Timing

The alignment between the incoming F_{IN} and the TOF1 output may be controlled in a number of ways. There are three different alignment modes in which TOF1 may operate as selected via Register 0x11:

1. 11'b (default): PLL1 never attempts to align.
2. 10'b: PLL1 always forces alignment to F_{IN}.
3. 00'b: Automatically force alignment to F_{IN} when they are misaligned.

Misalignment can be defined by the user via Register 0x15. In Register 0x15, a time window is defined to specify the amount of mismatch permitted between F_{IN} and TOF1 while still considering them to be aligned. If the input reference signal has a significant amount of low frequency jitter or wander, it may be possible for the relative alignment between TOF1 and F_{IN} to vary over time. Selecting "Always Align" mode may lead to undesirable timing jumps on the output of CLKout1/TOF1.

Once the device decides that it needs to align TOF1 and F_{IN}, there are two ways that it can be done. Crash lock involves simply resetting the counter that keeps track of where the TOF1 output transition happens, resulting in an instantaneous shift of TOF1 to align with F_{IN}. Drift lock involves using the second loop in PLL1 and skewing the VCXO to make the frequency of CLKout1 either speed up or slow down. The VCXO skewing slowly pulls TOF1 and F_{IN} into alignment. If a new reference is applied that is not in alignment with TOF1, but the output is currently in use, it may be better to slew TOF1 into alignment rather than to cause a major disruption in the timing with a crash lock. The LMH1983 allows the user to select either crash lock or drift lock, controllable via Register 0x11. The option of crash lock or drift lock is available when the difference in phase is small (Output <

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Feature Description (continued)

2^{LOA_window} x 27 MHz Clock) and when the difference in phase is large (Output > 2^{LOA_window} x 27 MHz Clock). Furthermore, if the difference is large, the user can tell the device to achieve alignment either by advancing or retarding the phase of PLL1. Note that if the difference in alignment is large, achieving alignment via drift lock may take a very long time (tens of seconds), during which the output clock will not be phase locked to the input H_{IN}.

8.3.11 TOF2 and TOF3 Alignment

Similar to TOF1, CLKout2 and CLKout3 have associated video formats. The format is determined by programming Register 0x07 and 0x08, respectively. Once the format is programmed and the TOF outputs are enabled, a TOF pulse is generated at the appropriate rate for each of the outputs. There are four different alignment modes that may be selected for TOF2 and TOF3:

Table 1. TOF2/TOF3 Alignment Modes

TOF2/TOF3 ALIGNMENT MODE	DESCRIPTION
0	Auto Align when Misaligned
1	One Shot Manual Align
2	Always Align
3	Never Align

TOF2 and TOF3 are generally aligned with TOF1. The alignment status bit will only be set if the frame rates are the same as one another. Another option for alignment is via software, where the TOFX_INIT bit is set. For example, the LSB of Register 0x12 is the TOF2_INIT bit. Writing a 1 to this bit while also setting TOF2 alignment mode to anything other than 3 (Never Align) will cause TOF2 to reset its phase immediately. Note that this bit is a self-clearing bit, so it will always return a zero.

8.3.11.1 TOF3 Initialization Set Up

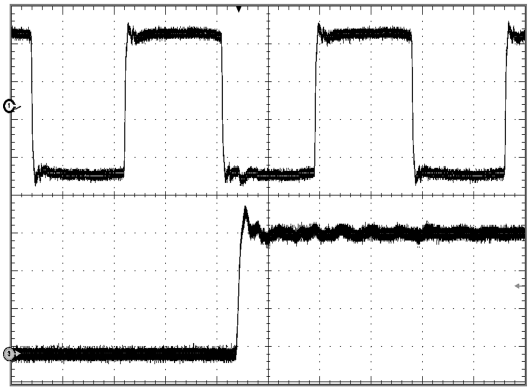
Under some circumstances, it is possible for an LMH1983 to power up in an anomalous state in which the output of PLL3 exhibits a large amount of cycle-to-cycle jitter. A simple register write after power up will prevent the device from remaining in this state. Writing to Register 0x13[5:4] = 10'b to force Always Align Mode ensures that the device will not exhibit poor duty cycle performance on CLKout3.

8.3.12 TOF4 Alignment

CLKout4 of the LMH1983 is most often used to generate an audio clock. The default base audio clock rate is 48 kHz, and this sample clock is synchronous in phase with the video frame only once every 5 frames for 29.97 and 30 Hz frame rate standards, or once every ten frames for 60 Hz and 59.94 Hz systems. The LMH1983 can generate a TOF4 pulse that occurs at this rate, allowing audio frames to be synchronized with the video frames.

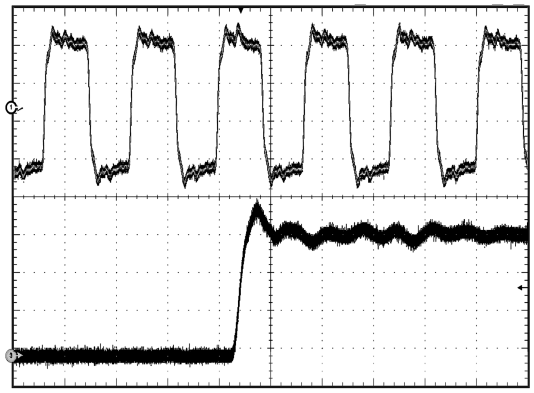
TOF4 may be aligned either to TOF1 or to the F_{IN} input. Additionally, there is an external INIT input that can be used to set TOF4 alignment.

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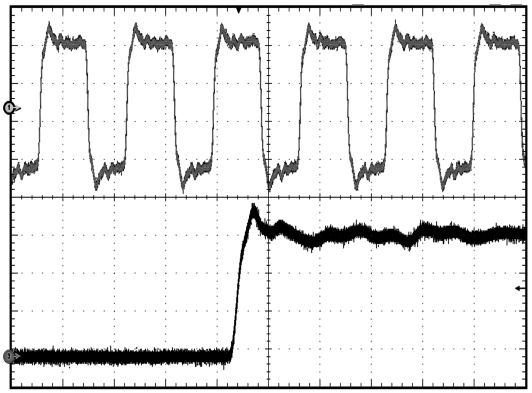
10ns / div
Top 200mV / div
Bottom 1V / div

Figure 15. TOF1 Timing
Top Trace CLKout1, Bottom Trace TOF1



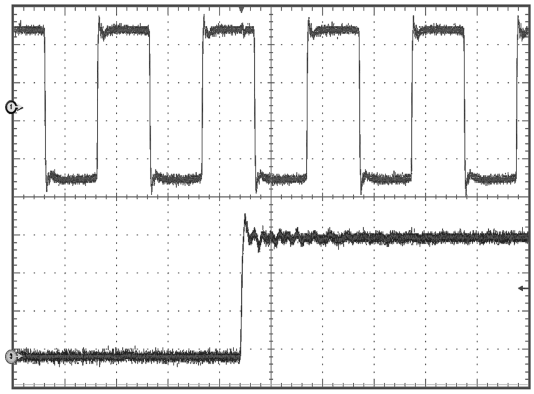
4 ns / div
Top 200 mV / div
Bottom 1V / div

Figure 16. TOF2 Timing
Top Trace CLKout2, Bottom Trace TOF2



4ns / div
Top 200mV / div
Bottom 1V / div

Figure 17. TOF3 Timing
Top Trace CLKout3, Bottom Trace TOF3



10 ns / div
Top 200 mV / div
Bottom 1V / div

Figure 18. TOF4 Timing
Top Trace CLKout4, Bottom Trace TOF4

8.4 Device Functional Modes

8.4.1 Reference Detection

The device uses *Auto Format Detect* as the default mode, as the device determines the reference format among those shown in *Auto Format Detection Codes*, and initiates the internal configurations accordingly. There are 31 pre-defined formats plus one format that the user can define. The device recognizes a format by measuring the H_{IN} input frequency and looking at the V_{IN} and F_{IN} inputs. The device then determines if the reference input format is an interlaced or progressive input. For some formats such as a 10 MHz or 27 MHz Hsync reference, if H_{IN} and V_{IN} create a spurious input, the device will not properly recognize the reference input and will not lock properly to the reference. Because of this, if H_{IN} has one of these 'special' signals on it, V_{IN} and F_{IN} should be muted.

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Device Functional Modes (continued)

8.4.2 User Defined Formats

There are several registers in the LMH1983 that are loaded automatically based on the format of the reference that is detected. The LMH1983 allows the user to define a non-standard format and a corresponding set of values to load into the appropriate registers if that format is detected. In order to identify the format, the LMH1983 measures the frequency of the Hsync input, counts the number of lines per frame in the format, and detects if the particular format is interlaced or progressive. The Hsync frequency is measured by counting the number of 27 MHz clock edges that occur in a period of time equal to 20 horizontal sync times. To implement a user defined format, the following registers are configured:

- The minimum and maximum permissible count must be set, thereby establishing a window of frequency for Hsync. Registers 0x51 and 0x52 define the 16-bit value for the low end of the frequency range, while Registers 0x53 and 0x54 define the high end of the frequency range.
- Registers 0x5A and 0x5B define the number of lines per frame for the format.
- Register 0x5D, Bit 4 indicates whether the user defined format is interlaced or not.
- Register 0x5D, Bit 7 enables the detection of a user-defined format.
- Once the user-defined format is detected, the contents of Registers 0x55 through 0x59 configure PLL1 to lock to 27MHz, which is then used as the reference for PLL2, PLL3, and PLL4.

Table 2 lists the supported standard timing formats. Table 2 includes the relevant parameters used to configure the LMH1983 for the input and output formats. Auto-detection of the input is supported for the formats listed in Table 2. The input format can also be programmed manually by the host via I^2C if it is necessary to override the auto-detection feature.

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Table 2. Supported Formats Lookup Table (LUT)

FORMAT	INPUT TIMING / PLL1 PARAMETERS				OUTPUT TIMING (OUT1–4) PARAMETERS				
	Reference Divider	Feedback Divider	Phase Detector (PD) Freq. (kHz)	PD Periods per Frame Counter	PLL#	PLL Clock Freq. (MHz)	Total Clocks per Line Counter	Total Lines per Frame Counter	Frame Rate (Hz)
NTSC, 525i	1	1716	15.7343	525	1	27.0	1716	525	29.97
					2	148.5	9438		
PAL, 625i	1	1728	15.625	625	1	27.0	1728	625	25
					2	148.5	9504		
525p	1	858	31.4685	525	1	27.0	858	525	59.94
					2	148.5	4719		
625p	1	864	31.25	625	1	27.0	864	625	50
					2	148.5	4752		
720p/60	1	600	45.0	750	2	148.5	3300	750	60
720p/59.94	5	3003	8.99101	150	3	148.35	3300	750	59.94
720p/50	1	720	37.5	750	2	148.5	3960	750	50
720p/30	1	1200	22.5	750	2	148.5	6600	750	30
720p/29.97	5	6006	4.49550	150	3	148.35	6600	750	29.97
720p/25	1	1440	18.75	750	2	148.5	7920	750	25
720p/24	1	1500	18.0	750	2	148.5	8250	750	24
720p/23.98	2	3003	8.99101	375	3	148.35	8250	750	23.98
1080p/60	1	400	67.5	1125	2	148.5	2200	1125	60
1080p/59.94	5	2002	13.48651	225	3	148.35	2200	1125	59.94
1080p/50	1	480	56.25	1125	2	148.5	2640	1125	50
1080p(psF)/30	1	800	33.75	1125	2	148.5	4400	1125	30
1080p(psF)/29.97	5	4004	6.74326	225	3	148.35	4400	1125	29.97
1080p(psF)/25	1	960	28.125	1125	2	148.5	5280	1125	25
1080p(psF)/24	1	1000	27.0	1125	2	148.5	5500	1125	24
1080p(psF)/23.98	1	1001	26.9730	1125	3	148.35	5500	1125	23.98
1080i/60	1	800	33.75	1125	2	148.5	4400	1125	30
1080i/59.94	5	4004	6.74326	225	3	148.35	4400	1125	29.97
1080i/50	1	960	28.125	1125	2	148.5	5280	1125	25
48 kHz word clock	2	1125	24.0	1	4	98.304	2048	1	48000
96 kHz word clock	4	1125	24.0	1	4	98.304	1024	1	96000
27 MHz osc clk	1000	1000	27.000	1	Input only				
10 MHz GPS osc clk	600	1620	16.6666	1	Input only				

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8.4.3 Auto Format Detection Codes

The Auto Format Detection Codes apply to Registers 0x07 (Output Mode – PLL2 Format), 0x08 (Output Mode – PLL3 Format), and 0x20 (Input Format).

FORMAT CODE	DESCRIPTION	Hsync PERIOD (in 27 MHz CLOCKS)	INTERLACED (I) / PROGRESSIVE (P)
0	525I29.97(1)	1716	I
1	625I25(2)	1728	I
2	525P59.94(1)	858	P
3	625P50(2)	864	P
4	720P60	600	P
5	720P59.94	600.6	P
6	720P50	720	P
7	720P30	1200	P
8	720P29.97	1201.2	P
9	720P25	1440	P
10	720P24	1500	P
11	720P23.98	1501.5	P
12	1080P60	400	P
13	1080P59.94	400.4	P
14	1080P50	480	P
15	1080P30	800	P
16	1080P29.97	800.8	P
17	1080P25	960	P
18	1080P24	1000	P
19	1080P23.98	1001	P
20	1080I30	800	I
21	1080I29.97	800.8	I
22	1080I25	960	I
23	1080I24	1000	I
24	1080I23.98	1001	I
25	48 kHz Audio	562.5	—
26	96 kHz Audio	281.25	—
27	44.1 kHz Audio	612.244898	—
28	32 kHz Audio	843.75	—
29	27 MHz Hsync	1	—
30	10 MHz Hsync	2.7	—
31	User Defined	User Defined	User Defined
63	Unknown	All Others	

(1) NTSC, 525i and 525p formats are also commonly known as 480I29.97 and 480P59.94, respectively, since the visible screen resolution consists of 480 pixels.
(2) PAL, 625i and 625p formats are also commonly known as 576I25 and 576P50, respectively, since the visible screen resolution consists of 576 pixels.

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8.4.4 Free-Run, Genlock, and Holdover Modes

The LMH1983 primary PLL can operate in three different modes, selected via Register 0x05. These modes are Free-run, Genlock, and Holdover Mode:

- Free-run mode: H_{IN}, V_{IN}, and F_{IN} are not used, and the VCXO control voltage is set by the contents of Registers 0x18 and 0x19. By writing to these registers, the VCXO voltage can be trimmed up or down. The slave PLLs will remain locked to the primary PLL.
- Genlock mode: The VCXO control voltage is actively controlled to maintain lock between H_{IN} and the VCXO output frequency. In addition, there is a second PLL loop that may take over to assert a lock between TOF1 and F_{IN}. See *TOF1 Alignment* for more details.
- Holdover mode: In the event that the reference is lost, there is an A/D — D/A pair that is able to take over for the PLL control loop and hold the VCXO control voltage constant. For this to work properly, the device must realize that it has lost its reference shortly after the reference is actually lost. Some sync separators, when the analog input is lost, will output random pulses from the H, V, and F outputs. This can confuse the device. Therefore if Holdover mode is to be used in conjunction with an analog sync separator, it is best to gate the H, V, and F signals with a signal that indicates if there is a valid reference input.

8.5 Programming

8.5.1 I²C Interface Protocol

The protocol of the I²C interface begins with the start pulse, followed by a byte which consists of a seven-bit slave device address and a Read/Write bit as an LSB. The default address of the LMH1983 for write sequences is 0xCC (11001100'b) and for read sequences is 0xCD (11001101'b). The base address can be changed with the ADDR pin. When ADDR is left open, the base address is 0x66 (which, when left shifted for a write sequence becomes 0xCC). When ADDR is connected to GND, the base address is 0x65, and when ADDR is connected to V_{DD}, the base address is 0x67.

Please note: The I2C interface of the LMH1983 requires the 27 MHz VCXO clock input to be running in order to read I2C data packets into the 27 MHz clock domain. If the 27 MHz clock is not running, the I2C interface should still respond (ACK), but Write commands may be ignored and Read commands may return invalid data.

8.5.2 Write Sequence

The write sequence begins with a start condition, which consists of the master pulling SDA low while SCL is high. The slave address is sent next. The slave address is a seven-bit address followed by the Read/Write bit (Read = 1'b and Write = 0'b). For the default base address of 0x66 (1100110'b), the 0 is appended to the end, and the net address is 0xCC. Each byte sent after the address is followed by an ACK bit. When SCL is high, the master will release the SDA line, and the slave pulls SDA low to acknowledge. Once the device address has been sent, the next byte sent is the register address. Following the register address and the ACK, the data byte is sent. When more than one data byte is sent, the register address is automatically incremented so that the data is written into the next address location. The Write Sequence Timing Diagram is shown in Figure 19. Note that there is an ACK bit following each data byte.

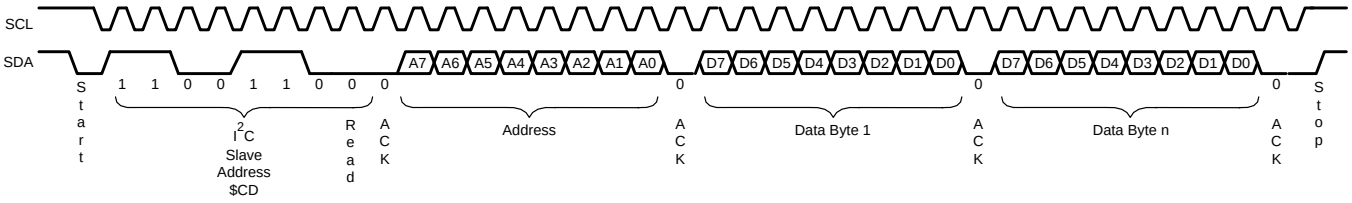


Figure 19. Write Sequence Timing Diagram

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Programming (continued)

8.5.3 Read Sequence

Read sequences consist of two I^2C transfers. The first is the address access transfer, which consists of a write sequence that transfers only the address to be accessed. The second is the data read transfer which starts at the address indicated in the first transfer and increments to the next address, continuing to read addresses until a stop condition is encountered. The timing diagram of the address access transfer is shown in Figure 20. A read sequence begins with a start pulse, the slave device address including the Read/Write bit (Read = 1'b and Write = 0'b), and then its ACK bit. The next byte is the address to be read, followed by the ACK bit and the stop bit to indicate the end of the address access transfer. The subsequent read data transfer shown consists of the start pulse, the slave device address including the Read/Write bit (this time a R/W Bit = 1'b, indicating that the data is to be read) and the ACK bit. The next byte is the data read from the initial access address. After each data byte is read, the address is incremented, thereby allowing the next byte of data to be read from the subsequent address of the device. Each byte is separated from the previous byte by an ACK bit, and the end of the read sequence is indicated with a STOP bit. The timing diagram for a read data transfer is shown in Figure 21 for additional timing details.

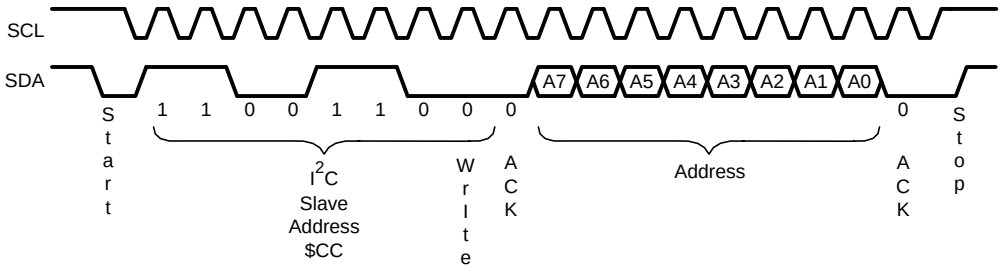


Figure 20. Read Sequence — Address Access Transfer

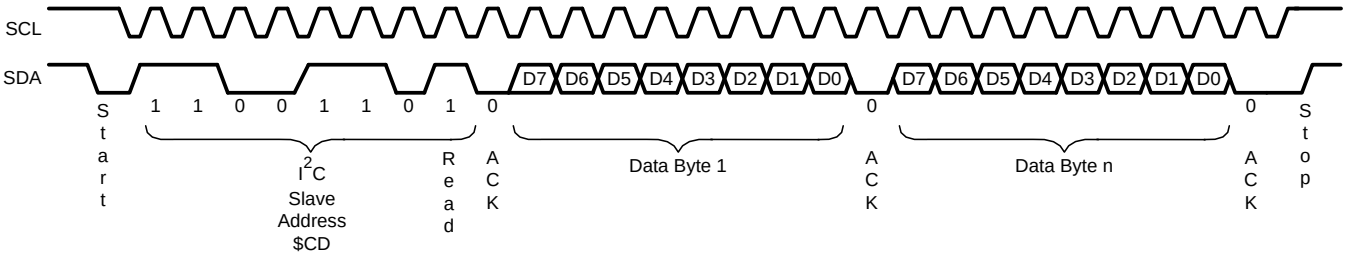


Figure 21. Read Sequence — Data Read Transfer

8.6 Register Map

The following table provides details on the device's configuration registers. Default value for fields that are seven bits or less are expressed in binary, and default values for fields that are 8 bits (Byte) are expressed in hex. Do not write to Reserved (RSVD) fields.

Table 3. LMH1983 Register Map

ADD	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x00	Device Status — Input Reference	7	INTERLACED	R	—	Indicates if the input reference format is an interlaced format
		6	ANALOG_REF	R	—	This bit is set depending on if the sync detection circuit had determined if the reference is an analog or digital derived signal
		5	INPUT_POLARITY	R	—	Returns the value of the input polarity determined by the sync detector for HSYNC — 0 indicates an active low sync
		4	HSYNC_STATUS	R	—	This bit is set if the Hsync During Vsync detector will set NO_H_DURING_V on the next rising edge of VSYNC
		3	H_ONLY	R	—	This is set by the Interlaced detector
		2	LOR_STATUS	R	—	Returns the inverse of the NO_REF output pin state
		1	LOST_HSYNC	R	—	Set if HSYNC_MISSING is high wile no_h_during_v is low. Remains set until read, then self-clears
		0	Reserved	R	0	Reserved — always returns '0'
0x01	Device Status	7	Lock_Status	R	1	Returns lock status for all unmasked and enabled PLLs
		6	Align_Status	R	0	Returns the Align Status for all enabled TOFs
		5	Wrong_Format	R	1	Returns the value of the Wrong_Format bit.
		4	Holdover	R	0	Returns the value of the PLL Holdover Bit
		3:0	RSVD		0000	Reserved
0x02	PLL Lock and Output Alignment Status	7:4	Lock_Detect	R	—	[7] indicates the lock status of PLL4. [6] indicates the lock status of PLL3. [5] indicates the lock status of PLL2. [4] indicates the lock status of PLL1. 0 = PLL Not Locked 1 = PLL Locked
		3:0	Align_Detect	R	—	[3] indicates the lock status of TOF4. [2] indicates the lock status of TOF3. [1] indicates the lock status of TOF2. [0] indicates the lock status of TOF1. 0 = TOF Alignment not detected 1 = TOF alignment detected
0x03	Revision ID	7:0		R	0xC0	Returns device revision code
0x04	Reserved	7:0	RSVD		0x00	Reserved
0x05	Device Control	7	Soft_Reset	R/W	0	Writing a '1' will reset all registers to their default values. This bit is self-clearing and always returns '0' when read.
		6	Powerdown	R/W	0	Controls the power down function.
		5	EN_AFD	R/W	1	Enables Auto Format Detection (AFD). 0 = Auto Format Detect disabled 1 = Auto Format Detect enabled
		4:3	PLL1_Mode	R/W	01	Sets PLL1 operating mode: 00 = Force Free-run 01 = Genlock 10 = Force Holdover 11 = Reserved
		2	LOR Mode	R/W	0	Sets default mode of operation on Loss of Reference (LOR) condition: 0 = Holdover on LOR 1 = Free-run on LOR
		1	Force_148	R/W	1	When this bit is set, it forces the PLL2 and PLL3 clock rates to 148.xx MHz regardless of chosen output format. Otherwise, the native clock rate of the chosen output format will be used. 0 = Uses the native clock rates 1 = Forces PLL2 = 148.5 MHz and PLL3 = 148.35 MHz clock rate
		0	GOE	R/W	1	Global Output Enable 0 = Disables all CLKout and Fout output buffers (Hi-Z) 1 = Enable active outputs

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Register Map (continued)

Table 3. LMH1983 Register Map (continued)

ADD	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x06	Input Polarity	7:4	RSVD		0000	Reserved
		3	EN_AUTOPOL	R/W	1	Enables Auto Polarity Detection and Correction. The proper polarity needs to be set to synchronize the output timing signals to the leading edges of the H and V inputs. 0 = The polarities of HVF inputs are manually set by their respective polarity override registers. 1 = The polarity of the H input is auto-detected. The polarity correction applied to the H input will also be applied to V and F inputs.
		2	HIN_POL_OVR	R/W	0	Used to manually set the H input Polarity. 0 = Active Low (Negative polarity) 1 = Active High (Positive polarity)
		1	VIN_POL_OVR	R/W	0	Used to manually set the V input Polarity. 0 = Active Low (Negative polarity) 1 = Active High (Positive polarity)
		0	FIN_POL_OVR	R/W	0	Used to manually set the F input Polarity. 0 = Active Low (Negative polarity) 1 = Active High (Positive polarity)
0x07	Output Mode – PLL2 Format	7:6	RSVD		00	Reserved
		5:0	PLL2_Format	R/W	001110	Sets the video format output timing for PLL2.
0x08	Output Mode – PLL3 Format	7:6	RSVD		00	Reserved
		5:0	PLL3_Format	R/W	001101	Sets the video format output timing for PLL3.
0x09	Output Mode – Misc	7:5	RSVD		000	Reserved
		4	AFS Mode	R/W	0	Sets the TOF4 output timing mode. 0 = Secondary Audio Clock Output (derived from PLL4 clock) 1 = Audio Frame Sync (derived from TOF1)
		3:0	XPT_Mode	R/W	0000	Sets the PLL crosspoint mode for Out2 and Out3. Refer to Table 4.
0x0A	Output Buffer Control	7:4	CLK_HIZ	R/W	0000	[3] sets CLKout4 output buffer mode. [2] sets CLKout3 output buffer mode. [1] sets CLKout2 output buffer mode. [0] sets CLKout1 output buffer mode. 0 = CLKoutx enabled 1 = CLKoutx Hi-Z
		3:0	FOUT_HIZ	R/W	1111	[3] sets Fout4 output buffer mode. [2] sets Fout3 output buffer mode. [1] sets Fout2 output buffer mode. [0] sets Fout1 output buffer mode. 0 = Foutx enabled 1 = Foutx Hi-Z
0x0B	Output Frame Control – Offset1_MSB	7:5	RSVD		000	Reserved
		4:0	TOF1 Offset MSB	R/W	00000	TOF1_Offset[12:0] sets number of lines to delay TOF1. TOF1_Offset_MSB[4:0] sets TOF1_Offset[12:8] TOF1_Offset_LSB[7:0] sets TOF1_Offset[7:0]
0x0C	Output Frame Control – Offset1_LSB	7:0	TOF1 Offset LSB	R/W	0x00	
0x0D	Output Frame Control – Offset2_MSB	7:5	RSVD		000	Reserved
		4:0	TOF2 Offset MSB	R/W	00000	TOF2_Offset[12:0] sets number of lines to delay TOF2. TOF2_Offset_MSB[4:0] sets TOF2_Offset[12:8] TOF2_Offset_LSB[7:0] sets TOF2_Offset[7:0]
0x0E	Output Frame Control – Offset2_LSB	7:0	TOF2 Offset LSB	R/W	0x00	
0x0F	Output Frame Control – Offset3_MSB	7:5	RSVD		000	Reserved
		4:0	TOF3 Offset MSB	R/W	00000	TOF3_Offset[12:0] sets number of lines to delay TOF3. TOF3_Offset_MSB[4:0] sets TOF3_Offset[12:8] TOF3_Offset_LSB[7:0] sets TOF3_Offset[7:0]
0x10	Output Frame Control – Offset3_LSB	7:0	TOF3 Offset LSB	R/W	0x00	

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Register Map (continued)

Table 3. LMH1983 Register Map (continued)

ADD	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x11	Alignment Control – TOF1	7:6	RSVD		00	Reserved
		5:4	TOF1_Align_Mode	R/W	11	00 = Auto-align when misaligned 01 = Reserved 10 = Always Align 11 = Never Align (1)
		3:2	TOF1_Sync	R/W	01	This bit sets the PLL1/TOF1 output synchronization behavior when the same reference is reapplied following a momentary LOR condition and TOF1 is within 2 lines of the expected location. 00 = Always Drift Lock – ensures the outputs drift smoothly back to frame alignment without excessive output phase disturbances 01 = Drift Lock if output < (2^{LOA_window} x 27 MHz Clock). Crash Lock otherwise. 1X = Always Crash Lock – achieves the fastest frame alignment through PLL/TOF counter resets, which can result in output phase disturbances
		1	TOF1_Sync_Slew	R/W	0	Sets the direction that TOF1 slews to achieve frame alignment when a new reference is applied and TOF1 is outside of 2 lines of the expected location. 0 = TOF1 lags by railing the VCXO input low 1 = TOF1 advances by railing the VCXO input high
		0	RSVD		0	Reserved
0x12	Alignment Control – TOF2	7:6	RSVD		00	Reserved
		5:4	TOF2_Align_Mode	R/W	11	00 = auto align when misaligned 01 = one shot manual align when writing TOF2_INIT=1 10 = always align 11 = never align
		3:1	RSVD		000	Reserved
		0	TOF2_INIT	R/W	0	Writing one to this bit while also writing TOF2_Align_Mode = 3, will cause the TOF2_INIT output to go high for at least one vframe period + one Hsync period and not more than one vframe period + two Hsync periods. The assertion of TOF2_INIT must happen immediately (it cannot wait for Hsync). If TOF2_Align_Mode is being written to 3, this bit will have no effect. This bit is self-clearing and will always read zero.
0x13	Alignment Control – TOF3	7:6	RSVD		00	Reserved
		5:4	TOF3_Align_Mode	R/W	11	00 = auto align when misaligned 01 = one shot manual align when writing TOF3_INIT=1 10 = always align 11= never align
		3:1	RSVD		000	Reserved
		0	TOF3_INIT	R/W	0	Writing one to this bit while also writing TOF3_Align_Mode ≠ 3, will cause the TOF3_INIT output to go high for at least one vframe period + one Hsync period and not more than one vframe period + two Hsync periods. The assertion of TOF3_init must happen immediately (it cannot wait for Hsync). If TOF3_Align_Mode is being written to 3, this bit will have no effect. This bit is self-clearing and will always read zero.

(1) **NOTE:** When H_ONLY is 1, TOF1 align mode is forced to never align.

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Register Map (continued)

Table 3. LMH1983 Register Map (continued)

ADD	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x14	Alignment Control – AFS	7:6	RSVD		00	Reserved
		5:4	AFS_Align_Mode	R/W	11	00 = auto align when misaligned 01 = one shot manual align. AFS_Init_Input reg determines if done by pin (INIT) or register (AFS_INIT = 1) 10 = always align 11= never align
		3	AFS_Init_Input	R/W	0	0 = Rising edges on INIT (pin 6) trigger AFS one shot manual align. 1 = Writing '1' to AFS_Init register triggers AFS one shot manual align.
		2:1	RSVD		00	Reserved
		0	AFS_INIT	R/W	0	Writing one to this bit while also writing AFS_Align_Mode = 3 and AFS_Init_Input=1, or providing a rising edge on the init input when AFS_Align_Mode ≠ 3 and AFS_Init_Input=0, will cause the AFS_INIT output to go high for at least one vframe period + one Hsync period and not more than one vframe period + two Hsync periods. The assertion of AFS_INIT must happen immediately (it cannot wait for Hsync). If AFS_Align_Mode = 3, toggling the init input will have no effect. This bit is self-clearing and will always read zero.
0x15	Loss of Alignment Control	7:3	RSVD		00000	Reserved
		2:0	LOA_Window	R/W	010	Number of 27 MHz clocks between the TOF1 and Vsync before Loss of Alignment is reported. If the code loaded in this register is n, then Loss of Alignment will be reported if the difference between TOF1 and Vsync exceeds 2^n 27 MHz clock cycles
0x16	LOR Control – Holdover Sampled Voltage MSB	7:2	RSVD		000000	Reserved
		1:0	VC_Hold_MSB	R	10	The VC_Hold[9:0] input signal changes rather slowly. For synchronization, it should be sampled on consecutive 27 MHz clocks until two identical values are found. This value will be saved as VC_Hold_sampled[9:0]. Whenever the VC_Hold[9:8] register is read, VC_Hold_sampled[9:8] is returned, and VC_Hold[7:0] will memorize the current value of VC_Hold_sampled[7:0] (to be read at a later time). This scheme allows a coherent 10-bit value to be read. Returns a synchronized snapshot of the VC_Hold[9:8] (MSB).
0x17	LOR Control – Holdover Sampled Voltage LSB	7:0	VC_Hold_LSB	R	—	The VC_Hold[9:0] input signal changes rather slowly. For synchronization, it should be sampled on consecutive 27 MHz clocks until two identical values are found. This value will be saved as VC_Hold_sampled[9:0]. Whenever the VC_Hold[9:8] register is read, VC_Hold_sampled[9:8] is returned, and VC_Hold[7:0] will memorize the current value of VC_Hold_sampled[7:0] (to be read at a later time). This scheme allows a coherent 10-bit value to be read. Returns a synchronized snapshot of the VC_Hold[7:0] (LSB)
0x18	LOR Control Free-run Control Voltage MSB	7:2	RSVD			Reserved
		1:0	VC_Free_MSB	R/W	01	Free-run Control Voltage (VC_Free[9:0]) is the voltage asserted on VC_LPF pin in free-run mode. Writing will change the MSB (VC_Free[9:8])
0x19	LOR Control – Free-run Control Voltage LSB	7:0	VC_Free_LSB	R/W	0xFF	Free-run Control Voltage (VC_Free[9:0]) is the voltage asserted on VC_LPF pin in free-run mode. Writing will change the LSB (VC_Free[7:0])
0x1A	LOR Control – ADC and DAC Disable	7:2	RSVD		000000	Reserved
		1	ADC_Disable	R/W	0	Directly controls the ADC_Disable output port. 0 = enable holdover ADC 1 = disable holdover ADC
		0	DAC_Disable	R/W	0	Directly controls the DAC_Disable output port. 0 = enable Free-run/Holdover DAC 1 = disable Free-run/Holdover DAC

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Register Map (continued)

Table 3. LMH1983 Register Map (continued)

ADD	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x1B	Loss of Reference Threshold	7	RSVD		0	Reserved
		6:4	HSYNC_Missing Threshold	R/W	00	Sets the threshold for number of additional clocks to wait before setting HSYNC_Missing.
		3	RSVD		0	Reserved
		2:0	LOR_Threshold	R/W	001	Sets the number of Hsync periods to wait before setting loss of reference. Since during blanking there can have up to 5 missing Hsync pulses, this value is usually set to 6.
0x1C	Loss of Lock Threshold	7:5	RSVD		000	Reserved
		4:0	LOCK1_Threshold	R/W	10000	Sets the number of Hsync periods to wait before setting loss of lock. Since during blanking there can have up to 5 missing Hsync pulses, this value is usually set > 6.
0x1D	Mask Control – PLL Lock and Output Align	7	MASK_LOCK4	R/W	0	Setting this bit masks the PLL4 lock status in the global LOCK_STATUS bit.
		6	MASK_LOCK3	R/W	0	Setting this bit masks the PLL3 lock status in the global LOCK_STATUS bit.
		5	MASK_LOCK2	R/W	0	Setting this bit masks the PLL2 lock status in the global LOCK_STATUS bit.
		4	MASK_LOCK1	R/W	0	Setting this bit masks the PLL1 lock status in the global LOCK_STATUS bit.
		3	MASK_TOF4_ALIGN	R/W	0	Setting this bit masks the TOF4 align status in the global ALIGN_STATUS bit.
		2	MASK_TOF3_ALIGN	R/W	0	Setting this bit masks the TOF3 align status in the global ALIGN_STATUS bit.
		1	MASK_TOF2_ALIGN	R/W	0	Setting this bit masks the TOF2 align status in the global ALIGN_STATUS bit.
		0	MASK_TOF1_ALIGN	R/W	0	Setting this bit masks the TOF1 align status in the global ALIGN_STATUS bit.
0x1E	Reserved	7:0	RSVD		0x00	Reserved
0x1F	Reserved	7:0	RSVD		0x00	Reserved
0x20	Input Format	7:6	RSVD		00	Reserved
		5:0	Input Format		000000	When Auto Format Detection is enabled (EN_AFD, address 0x05), this register is read-only and controlled automatically. When Auto Format Detection is disabled, this register is writable via I^2C. All writes to this register (whether automatic or manual) will update all the LUT1 (Lookup Table 1), LUT2_2, and LUT2_3 output registers based on the value written here. Writing to any of the LUT1, LUT2_2, or LUT2_3 output registers will set this field to 6'd62 (0x3E) indicating that custom changes have been made.
0x21	Output Frame Lookup – Input Vsync Code	7:4	RSVD		00	Reserved
		3:0	Input Vsync Code	R/W	0011	Writes to this register update the Vsync code which tells the device what the Input frame rate is. There is a table which correlates the Vsync codes to the actual frame rates. When Auto Format Detection is enabled (EN_AFD, address 5), this register is read-only, and is automatically loaded by the device.
0x22	Output Frame Lookup – PLL2 Vsync Code	7:4	RSVD		00	Reserved
		3:0	PLL2 Vsync Code	R/W	0101	Whenever PLL2_FORMAT (address 7) is written, this field is updated with the appropriate Vsync code. If any custom changes are made the device will set this field to 4'd14 (0x0E) to so indicate.
0x23	Output Frame Lookup – PLL3 Vsync Code	7:4	RSVD		0000	Reserved
		3:0	PLL3 Vsync Code	R/W	0110	Whenever PLL3_FORMAT (address 8) is written, this field is updated with the appropriate Vsync code. If any custom changes are made the device will set this field to 4'd14 (Ox0E) to so indicate.
0x24	Reserved	7:0	RSVD		0x00	Reserved

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Register Map (continued)

Table 3. LMH1983 Register Map (continued)

ADD	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x25	PLL1 Advanced Control	7:5	RSVD		000	Reserved
		4	PLL1_DIV	R/W	0	0 = Divide by 1 (Output is 27 MHz) 1 = Divide by 2 (Output is 13.5 MHz)
		3	RSVD		0	Reserved
		2	PLL1 Input Mode	R/W	0	Directly controls the mode of the PLL1 input buffer. 0 = Single Ended 1 = Differential
		1	RSVD		0	Reserved
		0	FastLock		1	This bit enables ICP1_FAST (address 0x27) to be used during locking. 0 = FastLock disabled 1 = FastLock enabled
0x26	PLL1 Advanced Control FastLock Delay	7:4	RSVD		0000	Reserved
		3:0	FastLock Delay	R/W	0000	Sets the amount of time that PLL1_Lock must be asserted before the PLL1 Charge pump current is reduced from the ICP1_Fast value to the ICP1 value. The time delay is specified in units of half seconds. Delay = FastlockDelay*0.5 Seconds. Valid values are from 0 to 10. Values from 11 to 15 are reserved.
0x27	PLL1 Advanced Control Fastlock CP Current	4:0	FastLock Charge Pump Current	R/W	11111	This field specifies the charge pump current to drive when FastLock is active. Charge pump current is equal to 34.375 µA * register value
0x28	PLL1 Advanced Control Charge Pump Current	4:0	PLL1 Charge Pump Current	R/W	01000	This field defines the charge pump current used when FastLock is not active. Charge pump current is equal to 34.375 µA * register value
0x29	PLL1 Advanced Control R Counter MSB	7:2	RSVD		000000	Reserved
		1:0	MSB	R/W	00	The two LSBs of Register 0x29 along with the eight bits of Register 0x2A form a ten bit word which comprises the R divider for PLL1. This register is internally written based on the input format and when AutoFormatDetect is enabled, these registers are read only.
0x2A	PLL1 Advanced Control R Counter LSB	7:0	LSB	R/W	0x01	
0x2B	PLL1 Advanced Control N Counter MSB	7	RSVD		0	Reserved
		6:0	MSB	R/W	0000110	The 7 LSBs of Register 0x2B along with the eight bits of Register 0x2C comprise the fifteen bit word which is used for the N divider of PLL1. These registers are internally controlled based on the input format detected and when AutoFormatDetect is enabled, these registers are read only.
0x2C	PLL1 Advanced Control N Counter LSB	7:0	LSB	R/W	0xB4	
0x2D	PLL1 Advanced Control Lock Step Size	7:5	RSVD		000	Reserved
		4:0	Lock Step Size	R/W	01000	See *Application Information* section discussion on Lock Detect
0x2E	PLL2 Advanced Control Main	7:5	RSVD		000	Reserved
		4	PLL2_DIV	R/W	0	0 = divide by 1 1 = divide by 2
		3	PLL2_DISABLE	R/W	0	0 = PLL2 disable is determined by XPT_MODE (Address 0x09) 1 = PLL2 is disabled
		2:0	RSVD		000	Reserved
0x2F	PLL2 Advanced Control Charge Pump Current	7:4	RSVD		0000	Reserved
		3:0	ICP2	R/W	0010	Controls PLL2 Charge Pump Current
0x30	PLL2 Advanced Control VCO Range	7:0	VCO_RNG2	R/W	0x0C	Controls the VCO range
0x31	PLL3 Advanced Control Main	7:5	RSVD		000	Reserved
		4	PLL3_DIV	R/W	0	0 = divide by 1 1 = divide by 2
		3	ICP3	R/W	0	0 = PLL3 disable is determined by XPT_MODE (Address 0x09) 1 = PLL3 is disabled
		2:0	RSVD		000	Reserved
0x32	PLL3 Advanced Control Charge Pump Current	7:4	RSVD		0000	Reserved
		3:0	ICP3	R/W	0011	Controls PLL3 Charge Pump Current

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Register Map (continued)

Table 3. LMH1983 Register Map (continued)

ADD	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x33	PLL3 Advanced Control VCO Range	7:0	VCO_RNG3	R/W	0x05	Controls the VCO range
0x34	PLL4 Advanced Control Main	7:4	PLL4_DIV	R/W	0010	Controls the PLL4 output divider — PLL4 is divided by 2^{PLL4_DIV}
		3	PLL4_Disable	R/W	0	0 = PLL4 is enabled 1 = PLL4 is disabled
		2	RSVD		0	Reserved
		1	IS125M	R/W	0	0 = 100 MHz clock 1 = 125 MHz clock
		0	PLL4_Mode	R/W	0	0 = using 27 MHz Clock 1 = using external clock
0x35	PLL4 Advanced Control Charge Pump Current	7:4	RSVD		0000	Reserved
		3:0	ICP4	R/W	1000	Controls PLL4 Charge Pump Current
0x36	PLL4 Advanced Control R counter	7	RSVD		0	Reserved
		6:0	DIV_R4	R/W	1001011	Sets the R divider in PLL4
0x37	PLL4 Advanced Control N counter MSB	7:2	RSVD		000000	Reserved
		1:0	DIV_N4_MSB	R/W	10	Two MSBs of the N divider in PLL4
0x38	PLL4 Advanced Control N counter LSB	7:0	DIV_N4_LSB	R/W	0x00	8 LSBs of the N divider in PLL4
0x39	PLL4 Advanced Control VCO Range	7:0	VCO4 Range	R/W	0x16	The value in the VCO4 Range register is used to adjust the center frequency of PLL4.
0x3A	LVDS Control	7	LVDS Boost	R/W	0	Applies pre-emphasis to LVDS output
		6:4	LVDS_DIFF	R/W	100	Adjusts LVDS Differential output swing
		3:0	LVDS_CM	R/W	1001	Adjusts LVDS Common Mode output voltage
0x3B	TOF1 Adv Control LPF MSB	7:5	RSVD		000	Reserved
		4:0	TOF1_LPF_MSB	R	00010	5 MSBs of the TOF1 lines per Frame count. This is read-only and loaded automatically when Auto Format Detection is enabled
0x3C	TOF1 Advanced Control LPF_LSB	7:0	TOF1_LPF_LSB	R	0x0D	8 LSBs of the TOF1 lines per Frame count. This is read-only and loaded automatically when Auto Format Detection is enabled Together with Register 0x3B this is a 13 bit number which number of lines per frame. TOF1 will be at a frequency of Hsync divided by this value.
0x3D	TOF2 Advanced Control CPL MSB	7	RSVD		0	Reserved
		6:0	TOF2_CPL_MSB	R	0001010	This 15 bit register gives the number of clock cycles per line to calculate TOF2. It is loaded automatically based on the format set with Register 0x07.
0x3E	TOF2 Advanced Control CPL LSB	7:0	TOF2_CPL_LSB	R	0x50	
0x3F	TOF2 Advanced Control LPF MSB	7:5	RSVD		000	Reserved
		4:0	TOF2_LPF_MSB	R	00010	This 13 bit register is loaded automatically based on the format selected via Register 0x07. It sets the number of lines per frame for the selected format to set the TOF2 rate correctly.
0x40	TOF2 Advanced Control LPF_LSB	7:0	TOF2_LPF_LSB	R	0x65	
0x41	TOF2 Advanced Control Frame Reset MSB	7:5	RSVD		000	Reserved
		4:0	TOF2_RST_MSB	R	00010	Automatically loaded based on formats selected.
0x42	TOF2 Advanced Control Frame Reset LSB	7:0	TOF2_RST_LSB	R	0x58	
0x43	TOF3 Advanced Control CPL_MSB	7	RSVD		0	Reserved
		6:0	TOF3_CPL_MSB	R	0001000	This 15 bit register gives the number of clock cycles per line to calculate TOF3. It is loaded automatically based on the format set with Register 0x08.
0x44	TOF3 Advanced Control CPL_LSB	7:0	TOF2_CPL_LSB	R	0x98	
0x45	TOF3 Advanced Control LPF_MSB	7:5	RSVD		000	Reserved
		4:0	TOF3_LPF_MSB	R	00100	This 13 bit register is loaded automatically based on the format selected via Register 0x08. It sets the number of lines per frame for the selected format to set the TOF3 rate correctly.
0x46	TOF3 Advanced Control LPF_LSB	7:0	TOF3_LPF_LSB	R	0x65	

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Register Map (continued)

Table 3. LMH1983 Register Map (continued)

ADD	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x47	TOF3 Advanced Control Frame Reset MSB	7:5	RSVD		000	Reserved
		4:0	TOF3_RST_MSB	R	00000	Automatically loaded based on formats selected.
0x48	TOF3 Advanced Control Frame Reset LSB	7:0	TOF3_RST_LSB	R	0x01	
0x49	TOF4 Advanced Control AFS	7:0	TOF4_AFS	R/W	0x05	See *Detailed Description* section for details. See also PLL4 Block Diagram.
0x4A	TOF4 Advanced Control ACLK	7:4	RSVD		0000	Reserved
		3:0	TOF4_ACLK	R/W	1011	See *Detailed Description* section for details. See also PLL4 Block Diagram.
0x4B to 0x50	Reserved	7:0	RSVD		0x00	Reserved
0x51	User Auto Format 27M High Value MSB	7:0	USR_27M_High_MSB	R/W	0x00	User format detect is determined by looking at the frequency of the Hsync input. This frequency is measured by counting the number of 27 MHz clock cycles that occur in 20 Hsync periods. This 16 bit register lists the maximum number of 27 MHz clock cycles in 20 Hsync periods that could be considered to meet the criteria for the User Format
0x52	User Auto Format 27M High Value LSB	7:0	USR_27M_High_LSB	R/W	0x00	
0x53	User Auto Format 27M Low Value MSB	7:0	USR_27M_Low_MSB	R/W	0x00	User format detect is determined by looking at the frequency of the Hysnc input. This frequency is measured by counting the number of 27 MHz clock cycles that occur in 20 Hsync periods. This 16 bit register lists the minimum number of 27 MHz clock cycles in 20 Hsync periods that could be considered to meet the criteria for the User Format
0x54	User Auto Format 27M Low Value LSB	7:0	USR_27M_Low_LSB	R/W	0x00	
0x55	User Auto Format R divider MSB	7:2	RSVD		000000	Reserved
		1:0	USR_DIV_R1_MSB	R/W	00	See *Detailed Description* section for details.
0x56	User Auto Format R Divider LSB	7:0	USR_DIV_R1_LSB	R/W	0x00	See *Detailed Description* section for details.
0x57	User Auto Format N Divider MSB	7	RSVD		0	Reserved
		6:0	USR_DIV_N1_MSB	R/W	0000000	See *Detailed Description* section for details.
0x58	User Auto Format N Divider LSB	7:0	USR_DIV_N1_LSB	R/W	0x00	See *Detailed Description* section for details.
0x59	User Auto Format Charge Pump Current	7:0	USR_ICP	R/W	0x00	See *Detailed Description* section for details.
0x5A	User Auto Format LPF MSB	7:5	RSVD		000	Reserved
		4:0	USR_TOF_LPF_MSB	R/W	00000	See *Detailed Description* section for details.
0x5B	User Auto Format LPF LSB	7:0	USR_TOF_LPF_MSB	R/W	0x00	See *Detailed Description* section for details.
0x5C	User Auto Format AFS	7:0	USR_TOF4	R/W	0x00	See *Detailed Description* section for details.
0x5D	User Auto Format Misc	7	EN_USERMODE	R/W	0	Enables the Auto Format Detection User Mode. 0 = disabled 1 = enabled
		6:5	RSVD		00	Reserved
		4	USR_IINTERLACED	R/W	0	Sets the INTERLACED value to output from LUT1 if the INPUT_FORMAT register is set to the user code. This bit also specifies the value that the Auto Format Detection must see on the interlaced signal to detect the user defined mode.
		3:0	USR_IN_VS_CODE	R/W	0000	Sets the INPUT_VS_CODE value to output from LUT1 if the INPUT_FORMAT registers is set to the user code.

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Table 4. Crosspoint Output Selection Table

REGISTER 0x09 [3:0]	PLL2_DISABLE(1)	PLL3_DISABLE(1)	OUT2 SOURCE	OUT3 SOURCE
0000 (default)	0	0	PLL2	PLL3
0001	1	1	PLL1	PLL1
0010	0	1	PLL2	PLL2
0011	1	0	PLL3	PLL3
0100	0	0	PLL3	PLL2
0101	1	0	PLL1	PLL3
0110	0	1	PLL2	PLL1
0111	0	1	PLL1	PLL2
1000	1	0	PLL3	PLL1
1001	Reserved	Reserved	Reserved	Reserved
1010	Reserved	Reserved	Reserved	Reserved
1011	Reserved	Reserved	Reserved	Reserved
1100	Reserved	Reserved	Reserved	Reserved
1101	Reserved	Reserved	Reserved	Reserved
1110	Reserved	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved	Reserved

(1) PLL2_Disable and PLL3_Disable can be forced via register writes to the PLLx_DISABLE registers independently of the status of the Crosspoint Mode bits.

Table 5. Vsync Codes

Vsync CODE NUMBER (BINARY)(1)	FRAME RATE (Hz)
0 (0000)	23.98 Hz
1 (0001)	24 Hz
2 (0010)	25 Hz
3 (0011)	29.97 Hz
4 (0100)	30 Hz
5 (0101)	50 Hz
6 (0110)	59.94 Hz
7 (0111)	60 Hz

(1) Vsync codes are used by Registers 0x21 (Output Frame Lookup – Input Vsync Code), 0x22 (Output Frame Lookup – PLL2 Vsync Code), and 0x23 (Output Frame Lookup – PLL3 Vsync Code).

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMH1983 is an analog phase locked loop (PLL) clock generator that can output simultaneous clocks at a variety of video and audio rates, synchronized or "genlocked" to Hsync and Vsync input reference timing. The LMH1983 features an output Top of Frame (TOF) pulse generator for each of its four channels, each with programmable timing that can also be synchronized to the reference frame. The clock generator uses a two-stage PLL architecture to attenuate input timing jitter for minimum jitter transfer. The combination of the external VCXO, external loop filter, and programmable PLL parameters provides flexibility to optimize the loop bandwidth and loop response for design applications.

9.2 Typical Applications

9.2.1 Typical Genlock Timing Generation with NTSC 525i/29.97 High Speed Reference

The LMH1983 is commonly used with Hsync, Vsync, and Fsync timing signals as a reference for genlock. Once these signals are provided, the LMH1983 can produce a specific set of clock output signals required by a downstream endpoint. In some video applications, a multi-format video sync separator is used to derive the Hsync, Vsync, and Fsync signals from a standard analog SD/ED/HD video signal. In Figure 22, a LMH1981 multi-format sync separator is used to provide H_{IN}, V_{IN}, and F_{IN} for the LMH1983. In this case, LMH1983 PLLs 1-4 provide a 27 MHz/29.97 Hz, 148.5 MHz/29.97 Hz, 148.35 MHz/59.94 Hz, and 24.576 MHz/5.994 Hz output, respectively, to an A/V Frame Synchronizer. Another example of this application can be seen in Figure 23, where H_{IN}, V_{IN}, and F_{IN} signals are provided directly from an FPGA SDI RX without a sync separator. In the latter example, the NTSC 525i/29.97 H_{IN}, V_{IN}, and F_{IN} parameters are provided individually for the LMH1983, after which the LMH1983 provides 3G, 3G/1.001, and Audio Clock Generation.

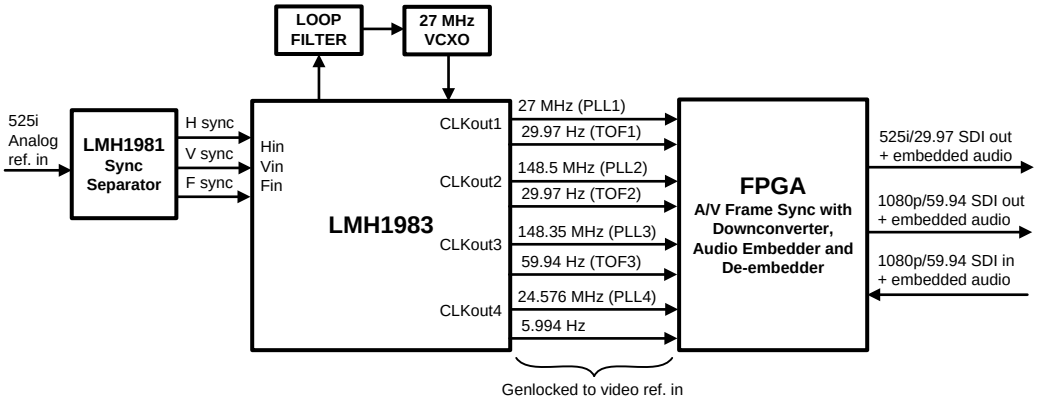


Figure 22. LMH1983 Video Genlock Timing Generation for A/V Frame Synchronizer

Typical Applications (continued)

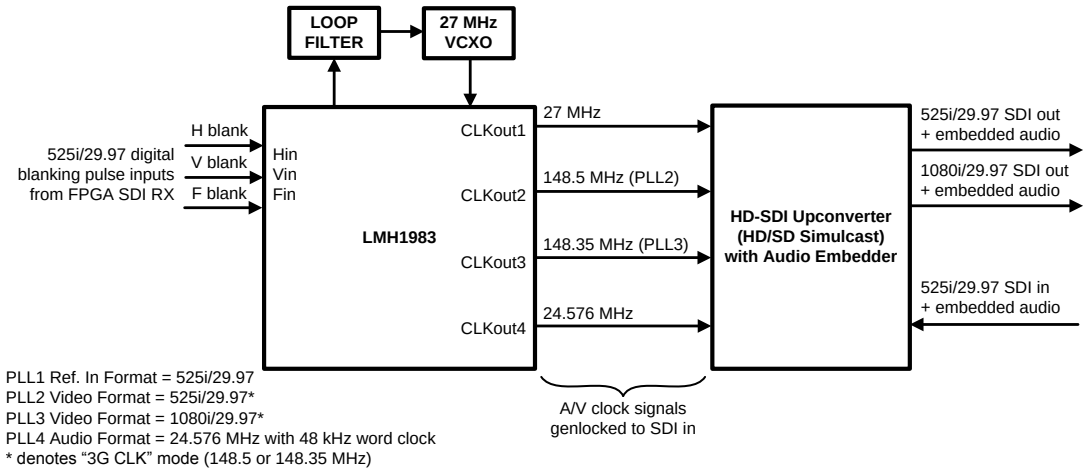


Figure 23. LMH1983 Video Timing Generation for HD-SDI Up-Conversion with Audio Embed/De-embed

9.2.1.1 Design Requirements

When designing for the LMH1983, it is essential to choose the correct VCXO and external loop filter capacitors. The following subsections provide guidance regarding how to select these components to improve timing stability and accuracy.

9.2.1.1.1 VCXO Selection Criteria

The recommended VCXO is CTS part number 357LB3C027M0000, which has an absolute pull range of ±50 ppm and a temperature range of –20°C to +70°C. A VCXO with a smaller APR can provide better frequency stability and slightly lower jitter, but the APR must be larger than the anticipated variation of the input frequency range.

9.2.1.1.2 Loop Filter Capacitors

The most common types of capacitors used in many circuits today are ferroelectric ceramic capacitors such as X7R, Y5V, X5R, Y5U, and so on. These capacitors suffer from piezoelectric effects, which generate an electrical signal in response to mechanical vibration, stress, and shock. This effect can adversely affect the jitter performance when presented to the control input to the VCXO. The easiest way to eliminate this effect is to use tantalum capacitors that do not exhibit the piezoelectric effect.

9.2.1.2 Detailed Design Procedure

Once the appropriate external VCXO and loop filter components are selected, the input timing signaling should be referenced to Table 2 to determine whether NTSC 525i/29.97 sync format is supported. This video format is a supported video format for automatic detection under Auto Format Detection Code 0, so it is not necessary to override the input auto-detection feature.

Once PLL1 has genlocked to the chosen NTSC, 525i input reference signal, PLLs 2-3 can be set according to the desired output signals specified in Figure 23. Refer to Table 6 and Table 7 for a list of possible input and output formats available for auto-format detection in Figure 22 and Figure 23, respectively. The format code can be applied as an expected input format for PLL1 (Register 0x20) or a programmed output format for PLL2 (Register 0x07) and PLL3 (Register 0x08).

Table 6. Relevant Auto-Format Detection Codes for Figure 22

PLLx (INPUT/OUTPUT)	FORMAT CODE	DESCRIPTION	HSync PERIOD (in 27 MHz CLOCKS)
PLL1 (Input)	0	525I29.97	1716
PLL2 (Output)	0	525I29.97	1716
PLL3 (Output)	13	1080P59.94	400.4

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Table 7. Relevant Auto-Format Detection Codes for Figure 23

PLLx (INPUT/OUTPUT)	FORMAT CODE	DESCRIPTION	HSync PERIOD (in 27 MHz CLOCKS)
PLL1 (Input)	0	525I29.97	1716
PLL2 (Output)	0	525I29.97	1716
PLL3 (Output)	21	1080I29.97	800.8

To ensure correct auto-detection and CLKout signaling desired in Figure 22 and Figure 23, the following SMBus register values should be verified or changed from their default values.

Table 8. SMBus Register Settings for Figure 22

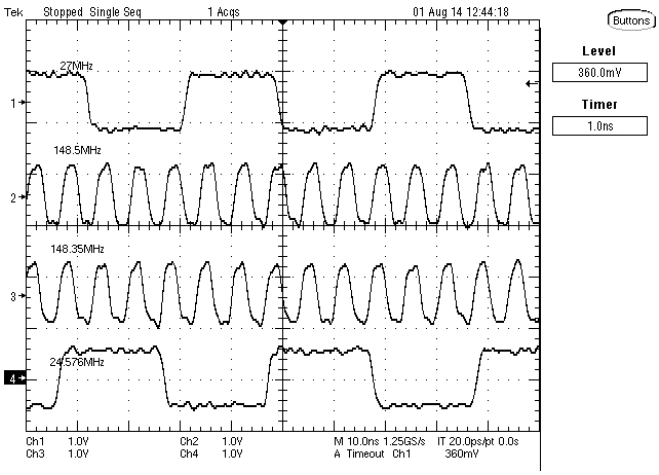
Register[Bit(s)]	WRITE VALUE	COMMENTS
0x05[5]	1'b	Auto Format Detect enabled
0x05[4:3]	01'b	PLL1 operating in Genlock mode
0x05[1]	1'b	Forces PLL2 = 148.5 MHz and PLL3 = 148.35 MHz
0x07[5:0]	000000'b	Set PLL2 Output to Format Detection Code 0 (0x00)
0x08[5:0]	001101'b	Set PLL3 Output to Format Detection Code 13 (0x0D)
0x11[5:4]	10'b	Set to always align when misaligned
0x11[3:2]	01'b	Drift lock (small misalignment), crash lock (large misalignment)
0x12[5:4]	10'b	Set TOF2 to always align when misaligned
0x13[5:4]	10'b	Set TOF3 to always align when misaligned
0x14[5:4]	10'b	Set AFS_Align_Mode to always align when misaligned
0x34[7:4]	0010'b	Set PLL4_DIV to divide-by-4 for 24.576 MHz

Table 9. SMBus Register Settings for Figure 23

Register[Bit(s)]	WRITE VALUE	COMMENTS
0x05[5]	1'b	Auto Format Detect enabled
0x05[4:3]	01'b	PLL1 operating in Genlock mode
0x05[1]	1'b	Forces PLL2 = 148.5 MHz and PLL3 = 148.35 MHz
0x07[5:0]	000000'b	Set PLL2 Output to Format Detection Code 0 (0x00)
0x08[5:0]	010101'b	Set PLL3 Output to Format Detection Code 21 (0x15)
0x11[5:4]	10'b	Set to always align when misaligned
0x11[3:2]	01'b	Drift lock (small misalignment), crash lock (large misalignment)
0x12[5:4]	10'b	Set TOF2 to always align when misaligned
0x13[5:4]	10'b	Set TOF3 to always align when misaligned
0x14[5:4]	10'b	Set AFS_Align_Mode to always align when misaligned
0x34[7:4]	0010'b	Set PLL4_DIV to divide-by-4 for 24.576 MHz

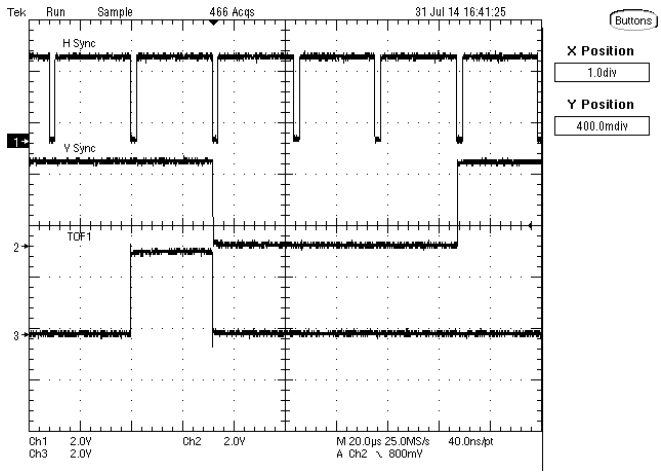
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9.2.1.3 Application Curves



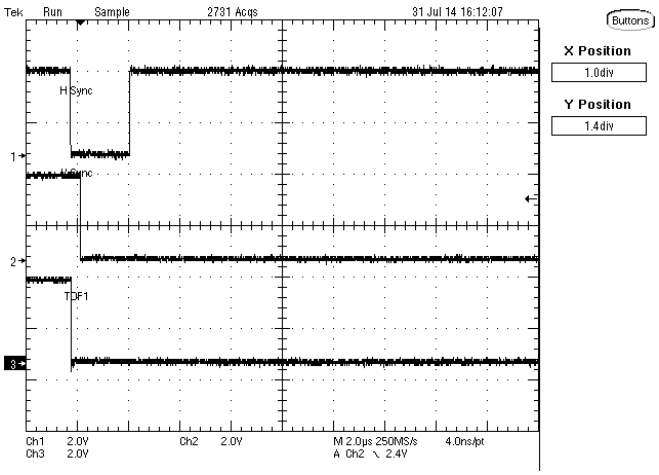
10 ns / div
Traces 1-4: 1V / div

Figure 24. CLKout 1-4 Signals after Genlock to 525i/29.97 Input Reference



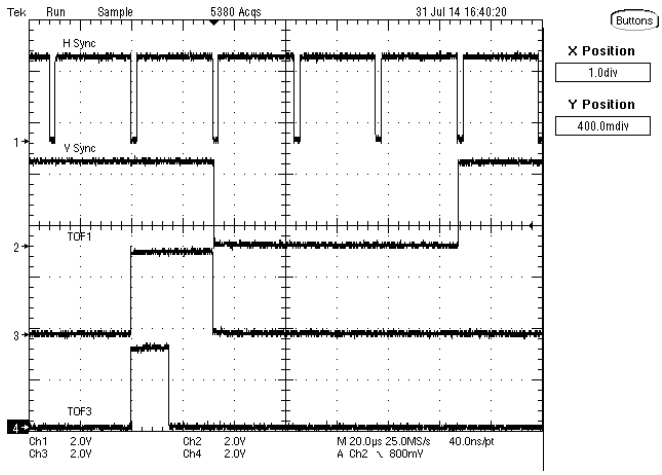
20 µs / div
Traces 1-3: 2V / div

Figure 25. TOF1 Falling Edge Alignment with HSync and VSync Reference Timing



20 µs / div
Traces 1-3: 2 V / div

Figure 26. TOF1 Alignment Comparison to HSync and VSync Reference Timing



20 µs / div
Traces 1-4: 2 V / div

Figure 27. TOF1 and TOF3 Alignment on Rising Edge

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9.2.2 A/V Clock Generation with Recognized Clock-based Input Reference

The LMH1983 is shown in the following application example where the H_{IN} input reference timing signal is clock-based. After achieving genlock, the LMH1983 can produce a specific set of clock output signals required downstream. In this case, LMH1983 PLLs 1-4 provide a 27 MHz, 74.25 MHz, 74.176 MHz, and 98.304 MHz output, respectively.

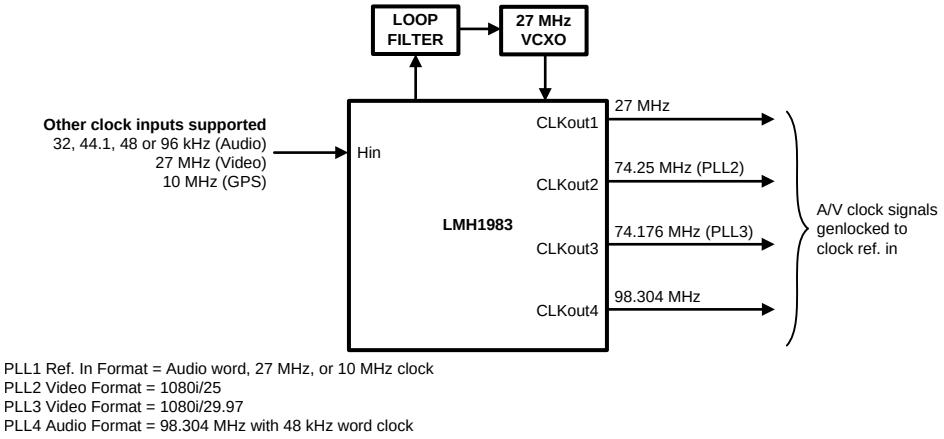


Figure 28. LMH1983 A/V Clock Generation with Non-Format Specific Input Clock Reference

9.2.2.1 Design Requirements

When designing for the LMH1983, it is essential to ensure that the correct VCXO and external loop filter capacitors are chosen. Refer to *VCXO Selection Criteria* and *Loop Filter Capacitors* for guidance regarding how to select these components to improve timing stability and accuracy.

9.2.2.2 Detailed Design Procedure

Once the appropriate external VCXO and loop filter components are selected, the input timing signaling should be referenced to the "Supported Formats Lookup Table (LUT)" (see Table 2) to determine whether the video clock, GPS clock, and audio clock are supported by automatic format detection. From Table 2 and the *Auto Format Detection Codes*, all of the reference clock inputs mentioned in this application are supported under the auto format detection feature. Once PLL1 has genlocked to the chosen H_{IN} signal, PLLs 2-3 can be set according to the desired output signals specified in *Auto Format Detection Codes*. Refer to Table 10 for a list of possible input and output formats available for auto-format detection in this application. The format code can be applied as an expected input format for PLL1 (Register 0x20) or a programmed output format for PLL2 (Register 0x07) and PLL3 (Register 0x08).

Table 10. Relevant Auto-Format Detection Codes for Figure 28

PLLx (INPUT/OUTPUT)	FORMAT CODE	DESCRIPTION	HSync PERIOD (in 27 MHz CLOCKS)
PLL2 (Output)	22	1080I25	960
PLL3 (Output)	21	1080I29.97	800.8
PLL1 (Input)	25	48 kHz Audio	562.5
PLL1 (Input)	26	96 kHz Audio	281.25
PLL1 (Input)	27	44.1 kHz Audio	612.244898
PLL1 (Input)	28	32 kHz Audio	843.75
PLL1 (Input)	29	27 MHz HSync	1
PLL1 (Input)	30	10 MHz HSync	2.7

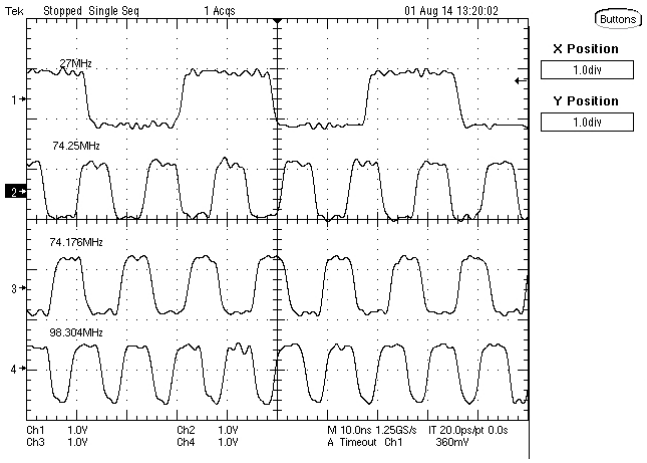
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To ensure correct auto-detection and the correct CLKout signaling desired in Figure 28, the following SMBus register values should be verified or changed from their default values.

Table 11. SMBus Register Settings for Figure 28

REGISTER[Bit(s)]	WRITE VALUE	COMMENTS
0x05[5]	1'b	Auto Format Detect enabled
0x05[4:3]	01'b	PLL1 operating in Genlock mode
0x05[1]	0'b	Allow PLL2 and PLL3 to use the native clock rates
0x07[5:0]	010110'b	Set PLL2 Output to Format Detection Code 22 (0x16)
0x08[5:0]	010101'b	Set PLL3 Output to Format Detection Code 21 (0x15)
0x11[5:4]	10'b	Set to always align when misaligned
0x11[3:2]	01'b	Drift lock (small misalignment), crash lock (large misalignment)
0x12[5:4]	10'b	Set TOF2 to always align when misaligned
0x13[5:4]	10'b	Set TOF3 to always align when misaligned
0x14[5:4]	10'b	Set AFS_Align_Mode to always align when misaligned
0x2E[4]	1'b	Set PLL2_DIV to divide-by-2 for 74.25 MHz
0x31[4]	1'b	Set PLL3_DIV to divide-by-2 for 74.176 MHz
0x34[7:4]	0000'b	Set PLL4_DIV to divide-by-1 for 98.304 MHz

9.2.2.3 Application Curve



10ns / div
Traces 1-4: 1V / div

Figure 29. CLKout 1-4 Signals after Genlock to Clock-Based Reference

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9.2.3 A/V Clock Generation Using Free-Run Mode

The LMH1983 can be used in free-run mode, as shown in the following application example. No H_{IN}, V_{IN}, and F_{IN} input reference timing signals are provided. Instead, the LMH1983 tracks a 27 MHz TCXO reference, which replaces the external VCXO and loop filter mentioned in previous applications. The LMH1983 can still produce a specific set of clock output signals required by a downstream endpoint. In this application, LMH1983 PLLs 1-4 provide a 27 MHz, 148.5 MHz, 148.35 MHz, and 98.304 MHz output, respectively.

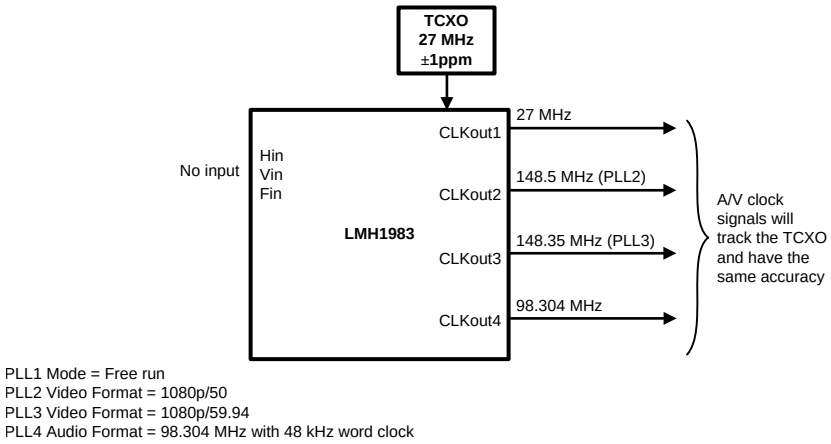


Figure 30. High-Precision, Stable A/V Clock Generation Using a 27 MHz TCXO Reference

9.2.3.1 Design Requirements

This application requires less components than the previous applications mentioned in this section. This is because there is no H_{IN} reference, external VCXO, or loop filter. However, the PLL1 signal is still applied via the 27 MHz TCXO clock signal on the XOin± pins. Using a TCXO for reference allows a stable, standalone clock generation for PLLs 2-4.

9.2.3.2 Detailed Design Procedure

Since no H_{IN} input timing signaling is provided, this application example cannot use the "Supported Formats Lookup Table (LUT)" (see Table 2) for automatic format detection. However, PLLs 2-4 can still be manually programmed to output the correct output format using *Auto Format Detection Codes*. To output the desired video and audio formats from PLLs 2-3, the following output codes should be used:

Table 12. Auto-Format Detection Output Codes for Figure 30

PLLx (INPUT/OUTPUT)	FORMAT CODE	DESCRIPTION	HSync PERIOD (in 27 MHz CLOCKS)
PLL2 (Output)	14	1080P50	480
PLL3 (Output)	13	1080P59.94	400.4

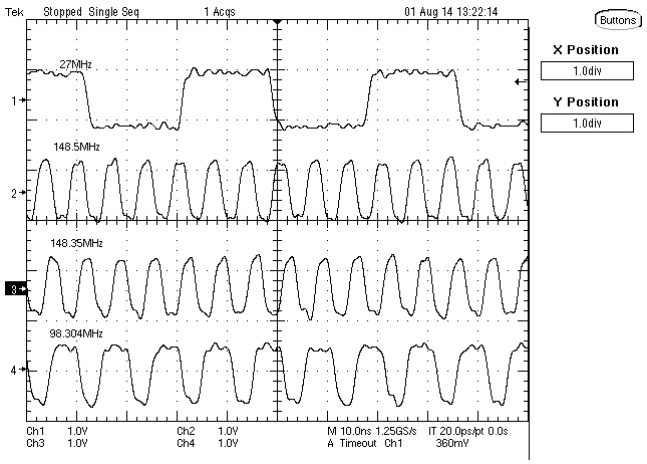
To ensure correct auto-detection and the correct CLKout signaling desired in Figure 30, the following SMBus register values should be verified or changed from their default values.

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Table 13. SMBus Register Settings for Figure 30

REGISTER[Bit(s)]	WRITE VALUE	COMMENTS
0x05[5]	1'b	Auto Format Detect enabled
0x05[4:3]	00'b	PLL1 operating in Free-run mode
0x05[1]	1'b	Forces PLL2 = 148.5 MHz and PLL3 = 148.35 MHz
0x07[5:0]	001110'b	Set PLL2 Output to Format Detection Code 14 (0x0E)
0x08[5:0]	001101'b	Set PLL3 Output to Format Detection Code 13 (0x0D)
0x11[5:4]	10'b	Set to always align when misaligned
0x11[3:2]	01'b	Drift lock (small misalignment), crash lock (large misalignment)
0x12[5:4]	10'b	Set TOF2 to always align when misaligned
0x13[5:4]	10'b	Set TOF3 to always align when misaligned
0x34[7:4]	0000'b	Set PLL4_DIV to divide-by-1 for 98.304 MHz

9.2.3.3 Application Curve



10 ns / div
Traces 1-4: 1 V / div

Figure 31. CLKout 1-4 Signals after Tracking 27 MHz TCXO Reference

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10 Power Supply Recommendations

It is important to ensure that the LMH1983 is provided with an adequate power supply that provides the cleanest voltage to the VDD_IO and VDD supply pins. One potential source of jitter on a multiple clock system such as the LMH1983 is interference among the four PLLs on the chip. To help reduce this effect, each PLL is run from a separate power supply internally on the LMH1983, and each supply has its own internal regulator. These regulators each require their own external bypass as seen in Figure 32 with bypass capacitors.

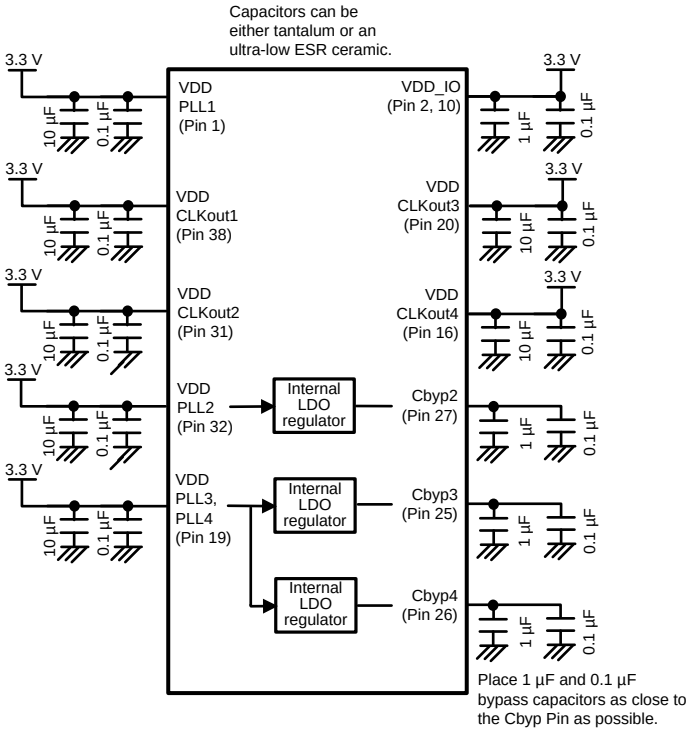


Figure 32. LMH1983 Power Supply Connection Diagram

11 Layout

11.1 Layout Guidelines

When designing the PCB layout for the LMH1983, it is important to follow these the guidelines:

- Whenever possible, dedicate an entire layer to each power supply. This will reduce the inductance in the supply plane.
- Use surface mount components whenever possible.
- Place bypass capacitors and filter components as close as possible to each power pin.
- Place the loop filter components, including the buffer amplifier, and VCXO as close as possible to the LMH1983.
- Do not allow discontinuities in the ground planes – return currents follow the path of least resistance. For high frequency signals this will be the path of least inductance.
- Make sure to match the trace lengths of all differential traces.
- Remember that vias have significant inductance — when using a via to connect to a power supply or ground layer, two in parallel will reduce the inductance over a single via.
- Connect the pad on the bottom of the package to a solid ground connection. This contact is used as a major ground connection as well as providing a thermal conduit which helps to maintain a constant die temperature.
- See Application Note: AN-1187, *Leadless Leadframe Package (LLP)* (SNOA401) for more Information on the LLP (WQFN) style package.

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11.2 Layout Example

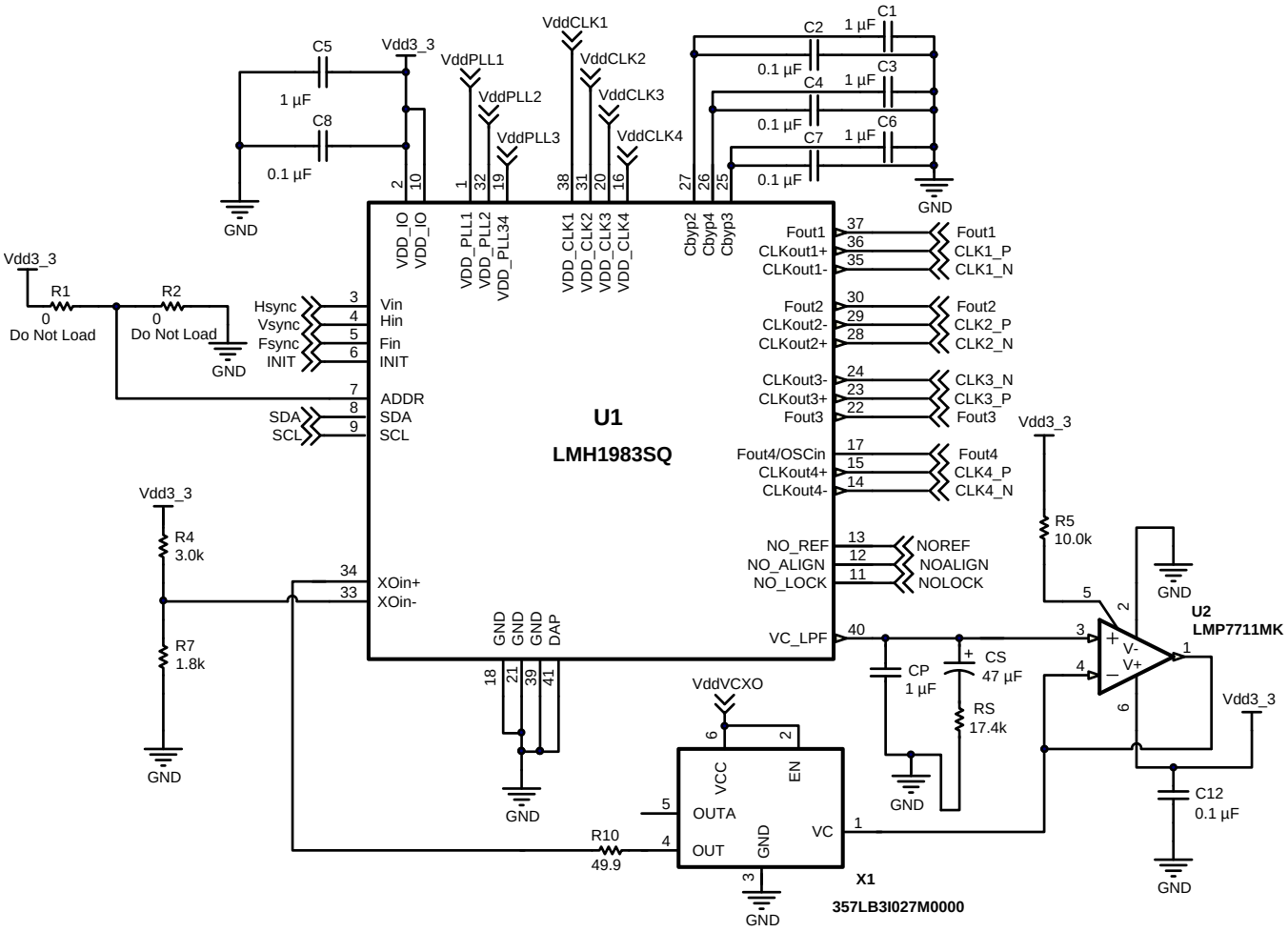


Figure 33. LMH1983 Typical Interface Circuit

An example of a typical application circuit for the LMH1983 is shown in the Figure 33. When performing PCB layout, key areas to consider regarding this circuit are the loop filter – which consists of R_S, C_S, C_P and the LM7711 Operational Amplifier which buffers the loop filter output prior to driving the control voltage input of the VCXO. Care must be taken in the component selection for the loop filter components (see *VCXO Selection Criteria* and *Loop Filter Capacitors*). The CLKout outputs are differential LVDS signals and should be treated as differential signals. These signals may be laid out as fully differential lines, in which the characteristic impedance between the two lines is nominally 100 Ω. Alternately, loosely coupled lines may be used, in which case the characteristic impedance of each line should be 50 Ω referenced to GND. In either case, care should be taken to match the lengths of the traces as closely as possible. Trace length mismatches on a differential line will add to the jitter seen on that line. Jitter is also added to the clock outputs if other signals are allowed to interfere with the signal traces. Therefore, to the greatest extent possible, the clock traces should be isolated from other signals. Long parallel runs should also be avoided. In places where a hostile signal must cross a sensitive clock signal, it should be routed such that it crosses as closely as possible to a 90° crossing.

When performing board layouts with the LMH1983, stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in Figure 34.

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Layout Example (continued)

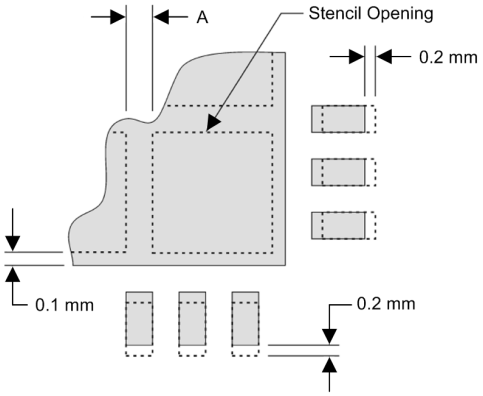


Figure 34. No Pullback LLP, Single Row Reference Diagram

Table 14. No Pullback LLP Stencil Aperture Summary for LMH1983

DEVICE	PIN COUNT	MKT. DWG.	PCB I/O PAD SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE (mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER of DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (DIM A mm)
LMH1983	40	SNA40A	0.25 x 0.6	0.5	4.6 x 4.6	0.25 x 0.7	1.0 x 1.0	16	0.2

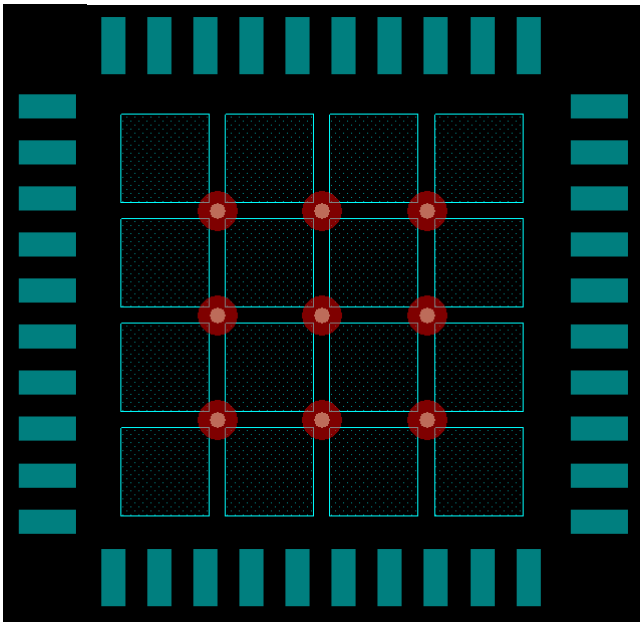


Figure 35. 40-Pin WQFN Stencil Example of Via and Opening Placement

The following PCB layout example is derived from the layout design of the LMH1983 in the *SD1983EVK Evaluation Module User's Guide* (SNLU001). This graphic and additional layout board description demonstrates both proper routing and solder techniques when designing in this clock generator.

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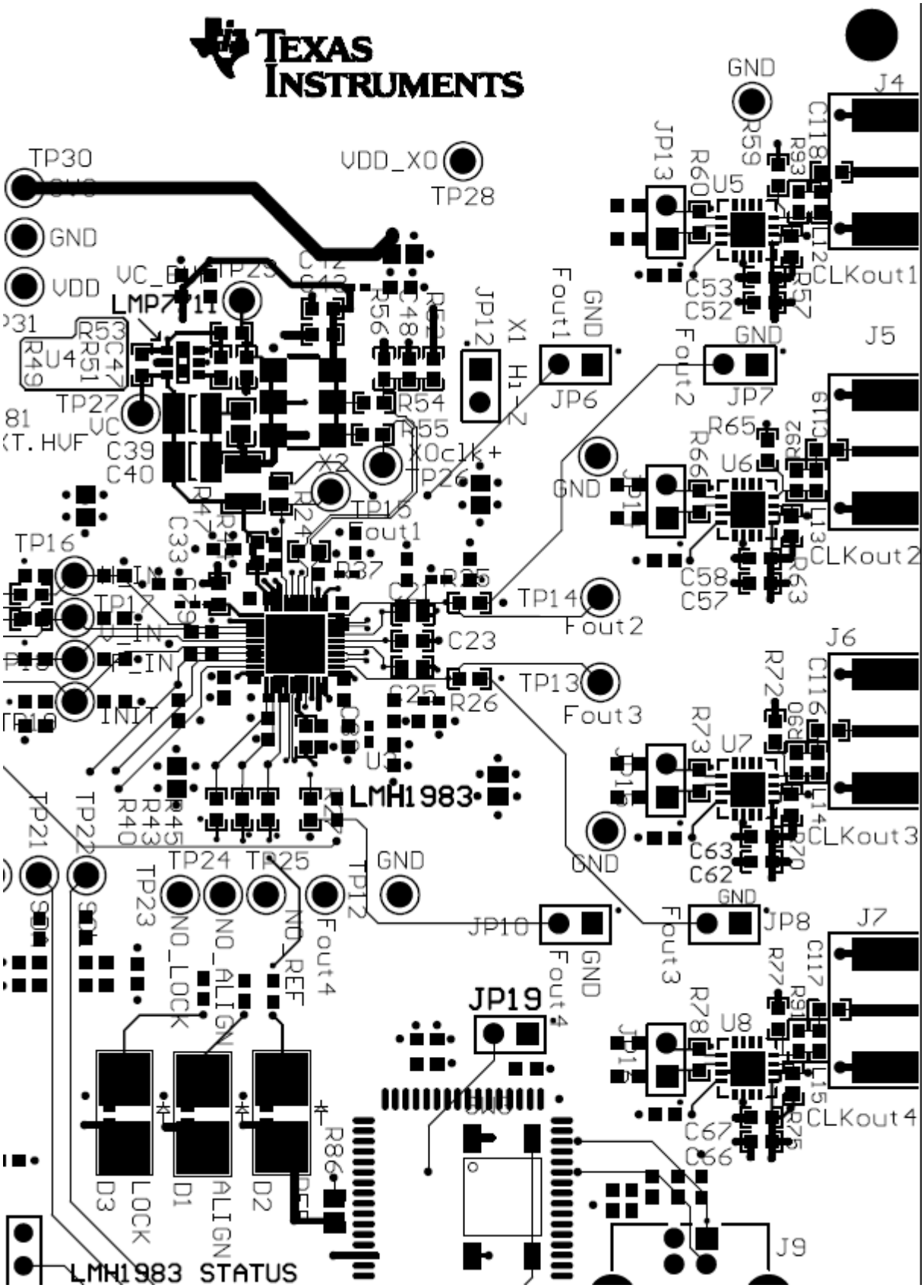


Figure 36. LMH1983 Example Layout

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549).
- *Generating 44.1 kHz Based Clocks with the LMH1983*, Application Note AN–2108 (SNLA129).
- *Leadless Leadframe Package (LLP)*, Application Note AN-1187 (SNOA401).
- *SD1983EVK/LMH1983 Evaluation Kit User Guide* (SNLU001).
- *Semiconductor and IC Package Thermal Metrics* (SPRA953).

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH1983SQ/NOPB	ACTIVE	WQFN	RTA	40	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	LMH1983	Samples
LMH1983SQE/NOPB	ACTIVE	WQFN	RTA	40	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	LMH1983	Samples
LMH1983SQX/NOPB	ACTIVE	WQFN	RTA	40	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	LMH1983	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

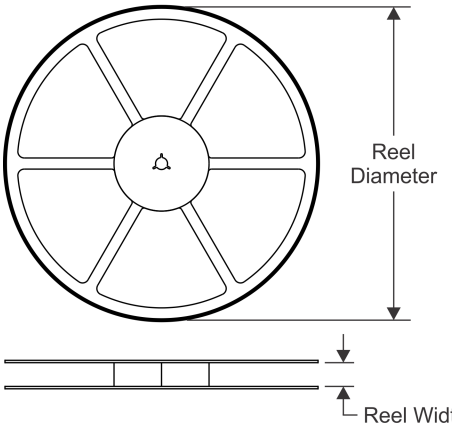
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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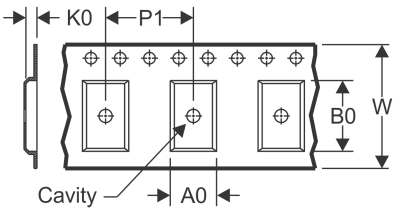
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

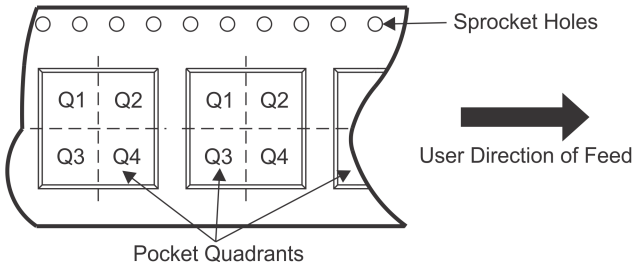


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

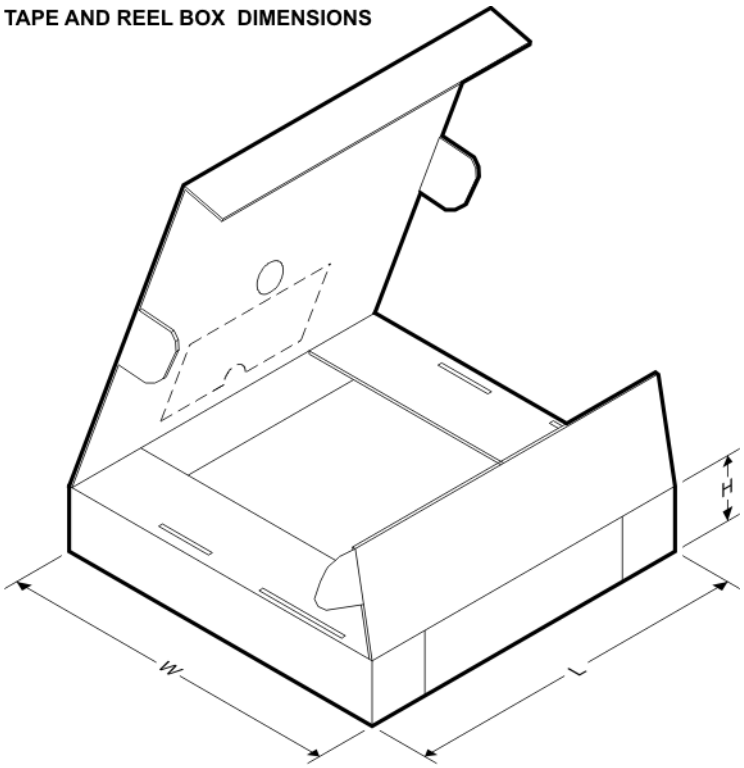
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH1983SQ/NOPB	WQFN	RTA	40	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LMH1983SQE/NOPB	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LMH1983SQX/NOPB	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

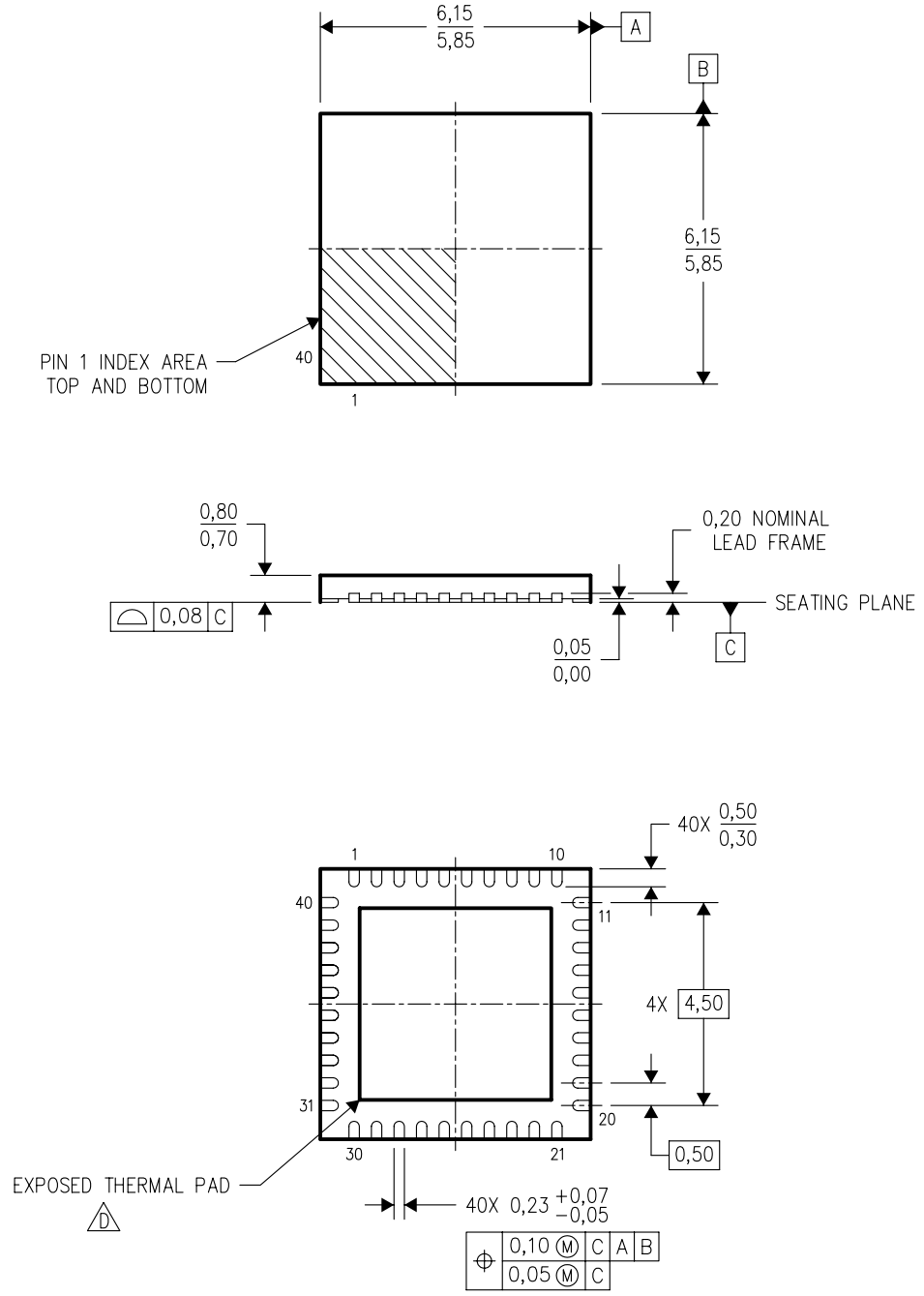
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH1983SQ/NOPB	WQFN	RTA	40	1000	367.0	367.0	38.0
LMH1983SQE/NOPB	WQFN	RTA	40	250	210.0	185.0	35.0
LMH1983SQX/NOPB	WQFN	RTA	40	2500	367.0	367.0	38.0

RTA (S–PQFP–N40) PLASTIC QUAD FLATPACK



4204422/B 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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