# 1.8-V PHASE LOCK LOOP CLOCK DRIVER

## FEATURES

- **1.8-V/1.9-V Phase Lock Loop Clock Driver for Double Data Rate (DDR II) Applications**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency: 125 MHz to 410 MHz**
- **Application Frequency: 160 MHz to 410 MHz**
- **Low Current Consumption: <200 mA Typ**
- **Low Jitter (Cycle-Cycle): ±40 ps**
- **Low Output Skew: 35 ps**
- **Stabilization Time <6 µs**
- **Distributes One Differential Clock Input to Ten Differential Outputs**
- **52-Ball µBGA (MicroStar Junior™ BGA, 0,65-mm pitch)**
- **External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) are Used to Synchronize the Outputs to the Input Clockst**
- **Meets or Exceeds CUA877/CAU878 Specification PLL Standard for PC2-3200/4300/5300/6400o**
- **Fail-Safe Inputs**

## DESCRIPTION

The CDCUA877 is a high-performance, low-jitter, low-skew, zero-delay buffer that distributes a differential clock input pair (CK, $\overline{\text{CK}}$) to ten differential pairs of clock outputs (Yn, $\overline{\text{Yn}}$) and to one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the input clocks (CK, $\overline{\text{CK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the LVCMOS control pins (OE, OS), and the analog power input ($AV_{DD}$). When OE is low, the clock outputs, except FBOUT/$\overline{\text{FBOUT}}$, are disabled while the internal PLL continues to maintain its locked-in frequency. OS (output select) is a program pin that must be tied to GND or $V_{DD}$. When OS is high, OE functions as previously described. When OS and OE are both low, OE has no affect on Y7/$\overline{\text{Y7}}$, they are free running. When $AV_{DD}$ is grounded, the PLL is turned off and bypassed for test purposes.

When both clock inputs (CK, $\overline{\text{CK}}$) are logic low, the device enters in a low power mode. An input logic detection circuit on the differential inputs, independent from input buffers, detects the logic low level and performs in a low power state where all outputs, the feedback, and the PLL are off. When the clock inputs transition from being logic low to being differential signals, the PLL turns back on, the inputs and the outputs are enabled, and the PLL obtains phase lock between the feedback clock pair (FBIN, $\overline{\text{FBIN}}$) and the clock input pair (CK, $\overline{\text{CK}}$) within the specified stabilization time.

The CDCUA877 is able to track spread spectrum clocking (SSC) for reduced EMI. This device operates from –40°C to 85°C).

**AVAILABLE OPTIONS**

| $T_A$ | 52-Ball BGA (1) |
|---|---|
| –40°C to 85°C | CDCUA877ZQL |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

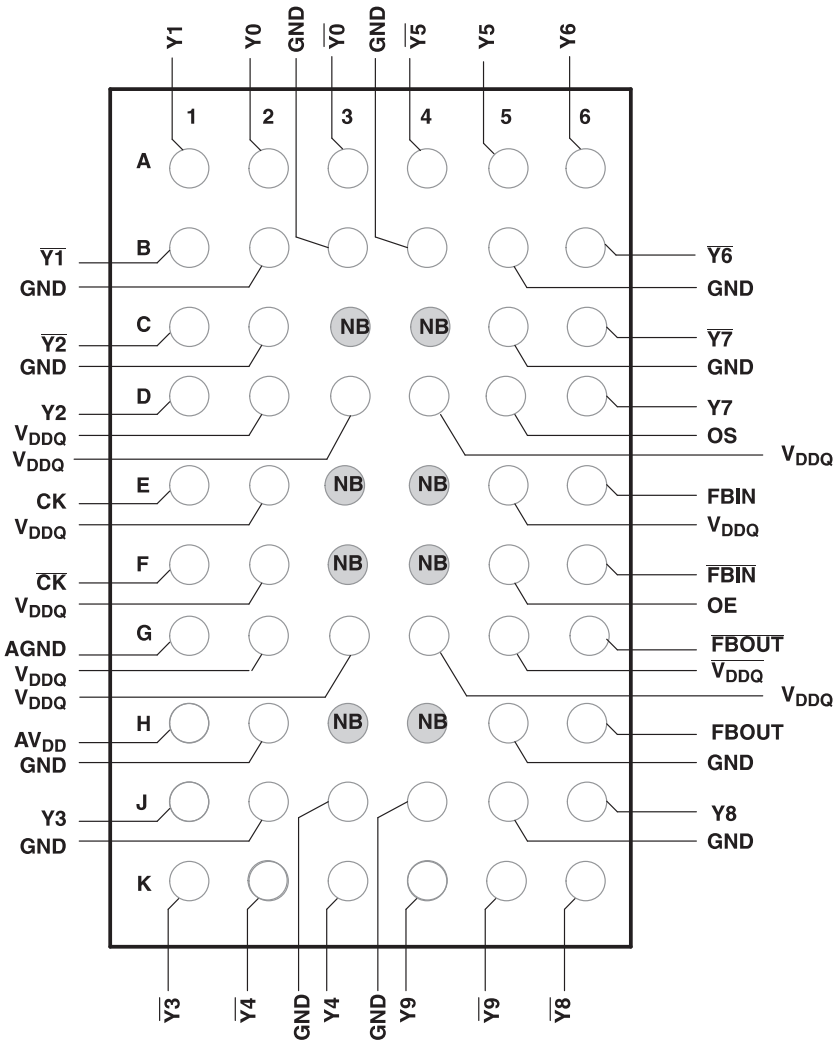
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MicroStar Junior is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2006–2007, Texas Instruments Incorporated

MicroStar™ Junior (GQL) Package
(TOP VIEW)




NC – No Connection
NB – No Ball

## Table 1. Terminal Functions

| NAME | BGA | MLF | I/O | DESCRIPTION |
|---|---|---|---|---|
| AGND | G1 | 7 | | Analog ground |
| $AV_{DD}$ | H1 | 8 | | Analog power |
| CK | E1 | 4 | I | Clock input with a (10 kΩ to 100 kΩ) pulldown resistor |
| $\overline{CK}$ | F1 | 5 | I | Complementary clock input with a (10 kΩ to 100 kΩ) pulldown resistor |
| FBIN | E6 | 27 | I | Feedback clock input |
| $\overline{FBIN}$ | F6 | 26 | I | Complementary feedback clock input |
| FBOUT | H6 | 24 | O | Feedback clock output |
| $\overline{FBOUT}$ | G6 | 25 | O | Complementary feedback clock output |
| OE | F5 | 22 | I | Output enable (asynchronous) |
| OS | D5 | 21 | I | Output select (tied to GND or VDD) |
| GND | B2, B3, B4, B5, C2, C5, H2, H5, J2, J3, J4, J5 | 10 | | Ground |
| $V_{DDQ}$ | D2, D3, D4, E2, E5, F2, G2, G3, G4, G5 | 1, 6, 9, 15, 20, 23, 28, 31, 36 | | Logic and output power |
| Y[0:9] | A2, A1, D1, J1, K3, A5, A6, D6, J6, K4 | 38, 39, 3, 11, 14, 34, 33, 29, 19, 16 | O | Clock outputs |
| $\overline{Y[0:9]}$ | A3, B1, C1, K1, K2, A4, B6, C6, K6, K5 | 37, 40, 2, 12, 13, 35, 32, 30, 18, 17 | O | Complementary clock outputs |

## Table 2. Function Table

| INPUTS | | | | | OUTPUTS | | | | PLL |
|---|---|---|---|---|---|---|---|---|---|
| $AV_{DD}$ | OE | OS | CK | $\overline{CK}$ | Y | $\overline{Y}$ | FBOUT | $\overline{FBOUT}$ | |
| GND | H | X | L | H | L | | L | H | Bypassed/Off |
| GND | H | X | H | L | H | | H | L | Bypassed/Off |
| GND | L | H | L | H | $L_Z$ | $L_Z$ | L | H | Bypassed/Off |
| GND | L | L | H | L | $L_Z$ Y7 Active | $L_Z$ $\overline{Y7}$ Active | H | L | Bypassed/Off |
| 1.8 V Nomnal | L | H | L | H | $L_Z$ | $L_Z$ | L | H | On |
| 1.8 V Nomnal | L | L | H | L | $L_Z$ Y7 Active | $L_Z$ $\overline{Y7}$ Active | H | L | On |
| 1.8 V Nomnal | H | X | L | H | L | H | L | H | On |
| 1.8 V Nomnal | H | X | H | L | H | L | H | L | On |
| 1.8 V Nomnal | X | X | L | L | $L_Z$ | $L_Z$ | $L_Z$ | $L_Z$ | Off |
| X | X | X | H | H | Reserved | | | | |

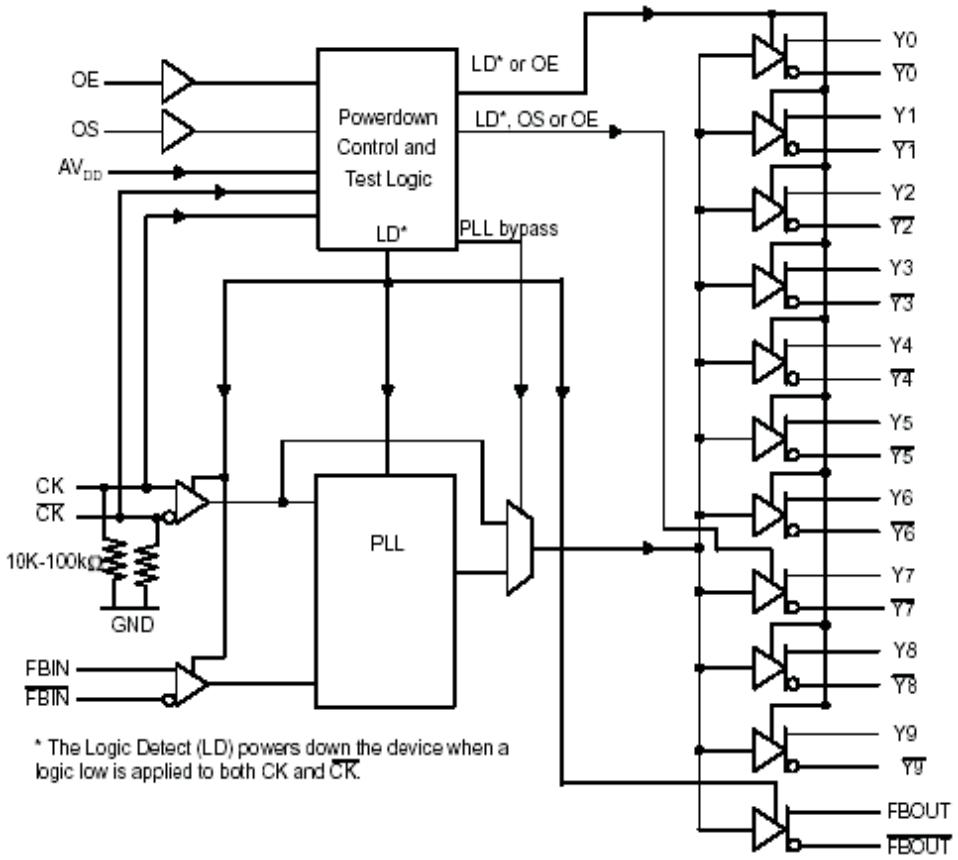



**Figure 1. Logic Diagram (Positive Logic)**

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{DDQ}$ $A_{VDD}$ | Supply voltage range | | –0.5 to 2.5 | V |
| $V_I$ | Input voltage range(2) (3) | | –0.5 to $V_{DDQ}$ + 0.5 | V |
| $V_O$ | Output voltage range(2) (3) | | –0.5 to $V_{DDQ}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current, ($V_I$ < 0 or $V_I$ > $V_{DDQ}$) | | ±50 | mA |
| $I_{OK}$ | Output clamp voltage, ($V_O$ < 0 or $V_O$ > $V_{DDQ}$) | | ±50 | mA |
| $I_O$ | Continuous output current, ($V_O$ = 0 to $V_{DDQ}$) | | ±50 | mA |
| $I_{DDC}$ | Continuous current through each $V_{DDQ}$ or GND | | ±100 | mA |
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient(4) | No airflow | 151.9 | K/W |
| | | Airllflow 150 ft/min | 146.1 | |
| $R_{\theta JC}$ | Thermal resistance, junction-to-case(4) | No airflow | 102.4 | |
| $T_{STG}$ | Storage temperature range | | –65 to 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 2.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD51 and JEDEC2S1P (high-k board).

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DDQ}$ | Output supply voltage | | 1.7 | 1.8 | 1.9 | V |
| $AV_{DD}$ | Supply voltage(1) | | | $V_{DDQ}$ | | |
| $V_{IL}$ | Low-level input voltage(2) | CK, $\overline{CK}$, OE, OS | | | $0.35 \times V_{DDQ}$ | V |
| $V_{IH}$ | High-level input voltage(2) | CK, $\overline{CK}$, OE, OS | $0.65 \times V_{DDQ}$ | | | V |
| $I_{OH}$ | High-level output current (see Figure 2) | | | | –9 | mA |
| $I_{OL}$ | Low-level output current (see Figure 2) | | | | 9 | mA |
| $V_{IX}$ | Input differential-pair cross voltage | | $(V_{DDQ}/2)-0.15$ | | $(V_{DDQ}/2)+0.15$ | V |
| $V_I$ | Input voltage level | | –0.3 | | $V_{DDQ}+0.3$ | V |
| $V_{ID}$ | Input differential voltage(2) (see Figure 10) | DC | 0.3 | | $V_{DDQ}+0.4$ | V |
| | | AC | 0.6 | | $V_{DDQ}+0.4$ | V |
| $T_A$ | Operating free-air temperature | | –40 | | 85 | °C |

(1) The PLL is turned off and bypassed for test purposes when $AV_{DD}$ is grounded. During this test mode, $V_{DDQ}$ remains within the recommended operating conditions and no timing parameters are ensured.

(2) $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$, see Figure 10 for definition. The CK and $\overline{CK}$ $V_{IH}$ and $V_{IL}$ limits define the dc low and high levels for the logic detect state.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range

| PARAMETER | | | TEST CONDITIONS | $AV_{DD}$, $V_{DDG}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input (cl inputs) | | $I_I$ = –18 mA | 1.7 V | | | –1.2 | V |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = -100 = A | 1.7 V to 1.9 V | VDDQ – 0.2 | | | V |
| | | | $I_{OH}$ = –9 mA | 1.7 V | 1.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 100 µA | | | | 0.1 | V |
| | | | $I_{OL}$ = 9 mA | 1.7 V | | | 0.6 | |
| $I_{O(DL)}$ | Low-level output current, disabled | | $V_{O(DL)}$ = 100 mV, OE = L | 1.7 V | 100 | | | µA |
| $V_{OD}$ | Differential output voltage(1) | | | 1.7 V | 0.5 | | | V |
| $I_I$ | Input current | CK, $\overline{CK}$ | | 1.9 V | | | ±250 | µA |
| | | OE, OS, FBIN, $\overline{FBIN}$ | | 1.9 V | | | ±10 | |
| $I_{DD(LD)}$ | Supply current, static ($I_{DDQ}$ + $I_{ADD}$) | | CK and $\overline{CK}$ = L | 1.9 V | | | 500 | µA |
| $I_{DD}$ | Supply current, dynamic ( $I_{DDQ}$ + $I_{ADD}$) (see (2) for $C_{PD}$ calculation) | | CK and $\overline{CK}$ = 410 MHz, All outputs are open (not connected to a PCB) | 1.9 V | | | 225 | mA |
| | | | All outputs are loaded with 2 pF and 120-Ω termination resistor, CK and $\overline{CK}$ = 410 MHz | 1.9 V | | | 225 | mA |
| $C_I$ | Input capacitance | CK, $\overline{CK}$ | $V_I$ = $V_{DD}$ or GND | 1.8 V | 2 | | 3 | pF |
| | | FBIN, $\overline{FBIN}$ | $V_I$ = $V_{DD}$ or GND | 1.8 V | 2 | | 3 | |
| $C_{I(\Delta)}$ | Change in input current | CK, $\overline{CK}$ | $V_I$ = $V_{DD}$ or GND | 1.8 V | | | 0.25 | pF |
| | | FBIN, $\overline{FBIN}$ | $V_I$ = $V_{DD}$ or GND | 1.8 V | | | 0.25 | |

(1) $V_{OD}$ is the magnitude of the difference between the true and complimentary outputs. See Figure 10 for a definition.
(2) Total $I_{DD}$ = $I_{DDQ}$ + $I_{ADD}$ = $f_{CK} \times C_{PD} \times V_{DDQ}$, solving for $C_{PD}$ = ($I_{DDQ}$ + $I_{ADD}$)/($f_{CK} \times V_{DDQ}$) where $f_{CK}$ is the input frequency, $V_{DDQ}$ is the power supply, and $C_{PD}$ is the power dissipation capacitance.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{CK}$ | Clock frequency (operating)(1) (2) | $AV_{DD}$, $V_{DD}$ = 1.8 V ±0.1 V | 125 | | 410 | MHz |
| | Clock frequency (application)(1) (3) | $AV_{DD}$, $V_{DD}$ = 1.8 V ±0.1 V | 160 | | 410 | MHz |
| $t_{DC}$ | Duty cycle, input clock | $AV_{DD}$, $V_{DD}$ = 1.8 V ±0.1 V | 40% | | 60% | |
| $t_L$ | Stabilization time(4) | $AV_{DD}$, $V_{DD}$ = 1.8 V ±0.1 V | | | 6 | µs |

(1) The PLL must be able to handle spread spectrum induced skew.
(2) Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters (used for low speed system debug).
(3) Application clock frequency indicates a range over which the PLL must meet all timing parameters.
(4) Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal, within the value specified by the static phase offset $t_{(\varphi)}$, after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and $\overline{CK}$ go to a logic low state, enter the power-down mode, and later return to active operation. CK and $\overline{CK}$ may be left floating after they have been driven low for one complete clock cycle.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{en}$ | Enable time, OE to any Y/$\overline{Y}$ | See Figure 12 | | | 8 | ns |
| $t_{dis}$ | Disable time, OE to any Y/$\overline{Y}$ | See Figure 12 | | | 8 | ns |
| $t_{jit(cc+)}$ | Cycle-to-cycle period jitter(2) | 160 MHz to 410 MHz, See Figure 5 | 0 | | 40 | ps |
| $t_{jit(cc-)}$ | | | 0 | | –40 | |
| $t_{(\varphi)}$ | Static phase offset time(3) | See Figure 6 | –50 | | 50 | ps |
| $t_{(\varphi)dyn}$ | Dynamic phase offset time,(4) | See Figure 11 | –20 | | 20 | ps |
| $t_{sk(o)}$ | Output clock skew(4) | See Figure 7 | | | 35 | ps |
| $t_{jit(per)}$ | Period jitter (2)(5) | 160 MHz to 270 MHz, see Figure 8 | –30 | | 30 | ps |
| | | 271 MHz to 410 MHz, see Figure 8 | –20 | | 20 | |
| $t_{jit(hper)}$ | Half-period jitter (2) (5) | 160 MHz to 270 MHz, see Figure 9 | –75 | | 75 | ps |
| | | 271 MHz to 410 MHz, see Figure 9 | –50 | | 50 | |
| $\Sigma t_{(su)}$ | $\lvert t_{jit(per)}\rvert + \lvert t_{(\varphi)dyn}\rvert + t_{sk(o)}$ (6) | 271 MHz to 410 MHz | | | 80 | ps |
| $\Sigma t_{(h)}$ | $\lvert t_{(\varphi)dyn}\rvert + + t_{sk(o)}$ (6) | 271 MHz to 410 MHz | | | 60 | ps |
| SR | Slew rate, OE | See Figure 3 and Figure 8 | 0.5 | | | V/ns |
| | Input clock skew rate | See Figure 3 and Figure 8 | 1 | 2.5 | 4 | |
| | Output clock slew rate(7)(8) | See Figure 3 and Figure 8 | 1.5 | 2.5 | 3 | |
| $V_{OX}$ | Output differential-pair cross voltage(9) | See Figure 2 | $(V_{DDQ}/2) – 0.1$ | | $(V_{DDQ}/2) + 0.1$ | V |
| | SSC modulation frequency | | 30 | | 33 | kHz |
| | SSC clock input frequency deviation | | 0% | | –0.5% | |
| | PLL loop bandwidth | | 2 | | | MHz |

(1) There are two different terminations that are used with the following tests. The load/board in Figure 2 is used to measure the input and output differential-pair cross voltage only. The load/board in Figure 3 is used to measure all other tests. For consistency, equal length cables must be used.
(2) This parameter is assured by design and characterization.
(3) Phase static offset time does not include jitter.
(4) For full frequency range of 160MHz to 410MHz.
(5) Period jitter, half-period jitter specifications are separate specifications that must be met independently of each other.
(6) In the frequency range of 271 MHz to 410 MHz, the minimum and maximum values of $t_{jit(per)}$ and $t_{(\varphi)dyn}$ and the maximum value for $t_{sk(o)}$ must not exceed the corresponding minimum and maximum values of the 160 MHz to 270 MHz range. In addition, the sum of the specified values for $\lvert t_{jit(per)}\rvert$, $\lvert t_{(\varphi)dyn}\rvert$, and $t_{sk(o)}$ must meet the requirements for the $\Sigma t_{(su)}$ and the sum of the specified values for $\lvert t_{(\varphi)dyn}\rvert$ and $t_{sk(o)}$ must meet the requirements for the $\Sigma t_{(h)}$.
(7) The output slew rate is determined from the IBIS model into the load shown in Figure 4.
(8) To eliminate the impact of input slew rates on static phase offset, the input skew rates of reference clock input CK and $\overline{CK}$ and feedback clock inputs FBIN and $\overline{FBIN}$ are recommended to be nearly equal. The 2.5-V/ns skew rates are shown as a recommended target. Compliance with these typical values is not mandatory if it can adequately shown that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
(9) Output differential-pair cross voltage specified at the DRAM clock input or the test load.

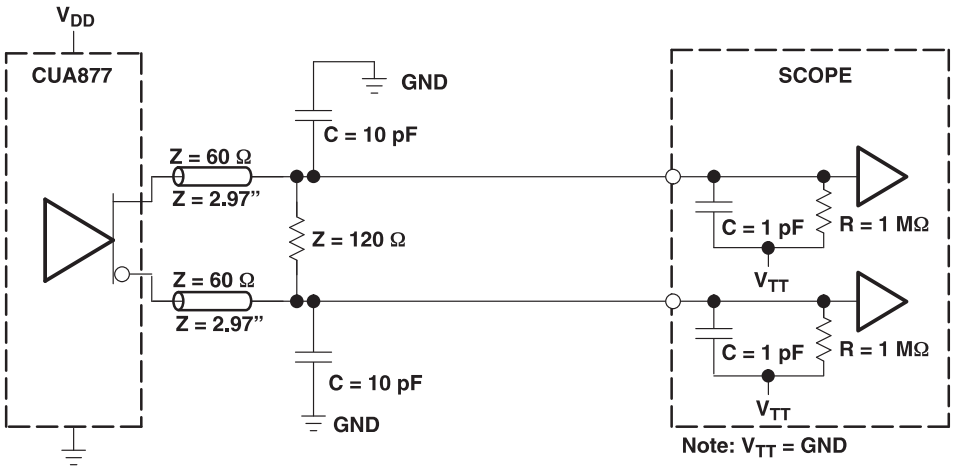



**Figure 2. Output Load Test Circuit 1 (Using High-Impedance Probe)**

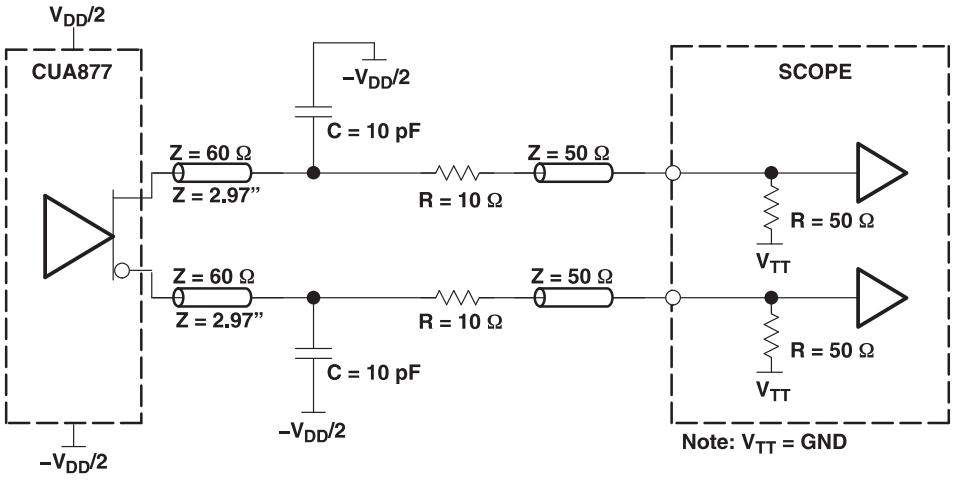



**Figure 3. Output Load Test Circuit 2 (Using SMA Coaxial Cable)**

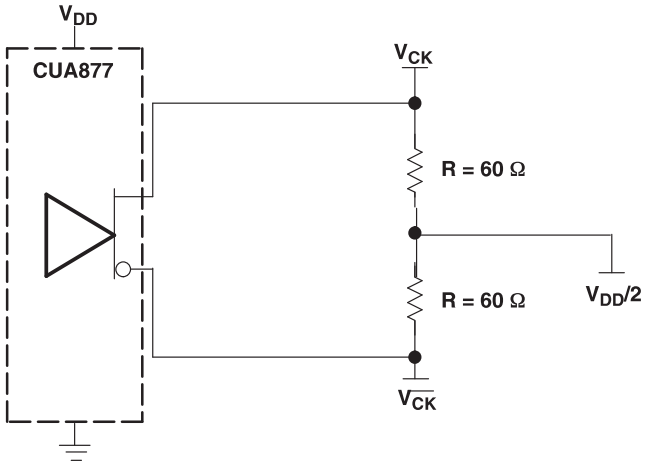



**Figure 4. IBIS Model Output Load**

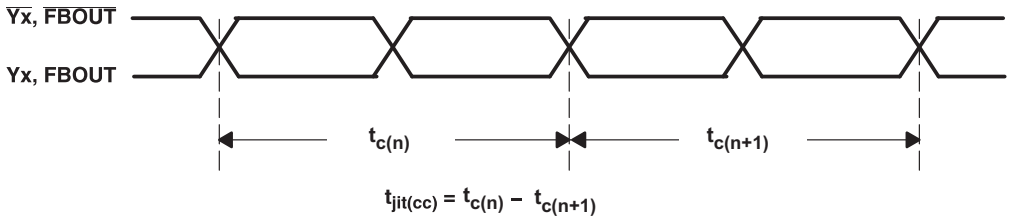



**Figure 5. Cycle-To-Cycle Period Jitter**

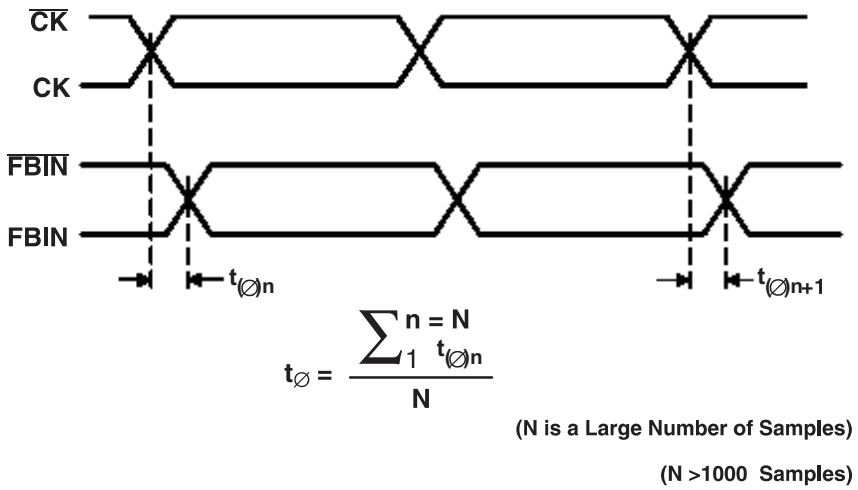



**Figure 6. Static Phase Offset**

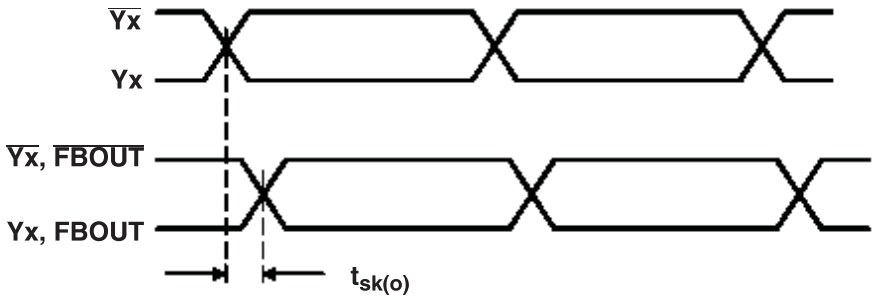
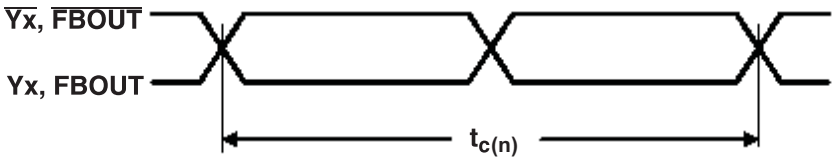
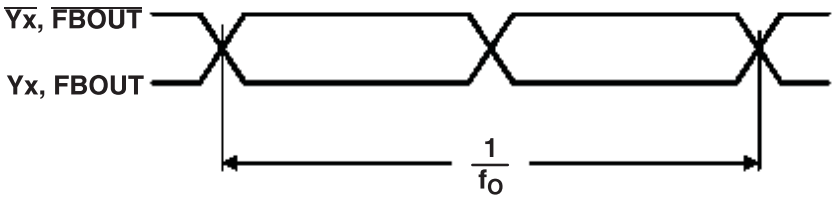



**Figure 7. Output Skew**

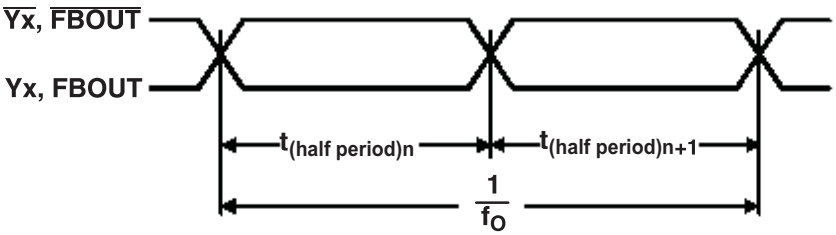



$$t_{jit(per)} = t_{c(n)} - \frac{1}{f_O}$$

$f_O$ = Average Input Frequency Measured at CK/$\overline{CK}$

**Figure 8. Period Jitter**

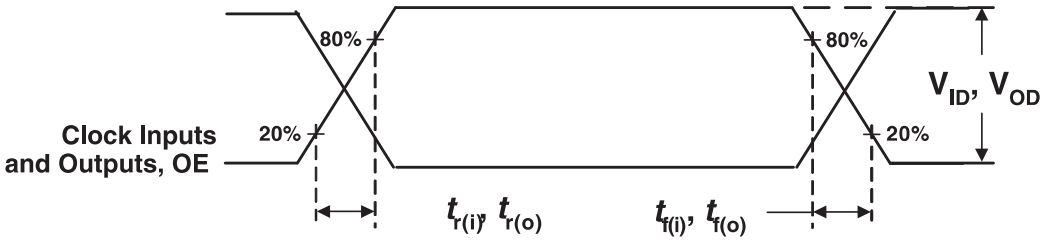



$$t_{jit(hper)} = t_{(half\ period)n} - \frac{1}{2 * f_O}$$

n = any half cycle

($f_O$ = Average Input Frequency Measured at CK/$\overline{CK}$)

**Figure 9. Half-Period Jitter**




$$slrr_{(i/o)} = \frac{V_{80\%} - V_{20\%}}{t_{r(i/o)}} \qquad slrf_{(i/o)} = \frac{V_{80\%} - V_{20\%}}{t_{f(i/o)}}$$

**Figure 10. Input and Output Slew Rates**

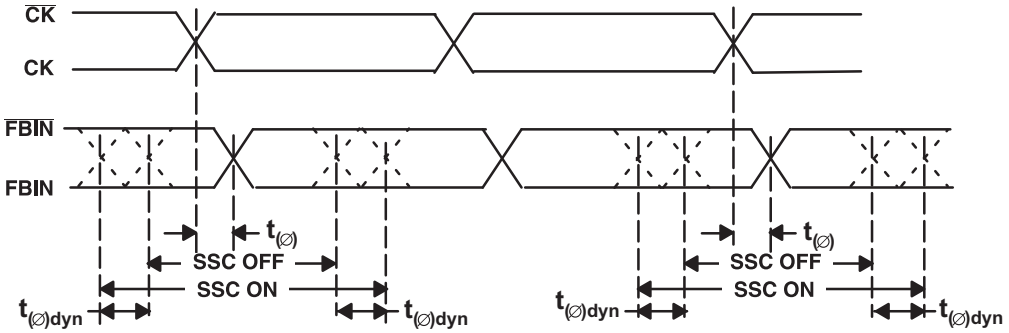



**Figure 11. Dynamic Phase Offset**

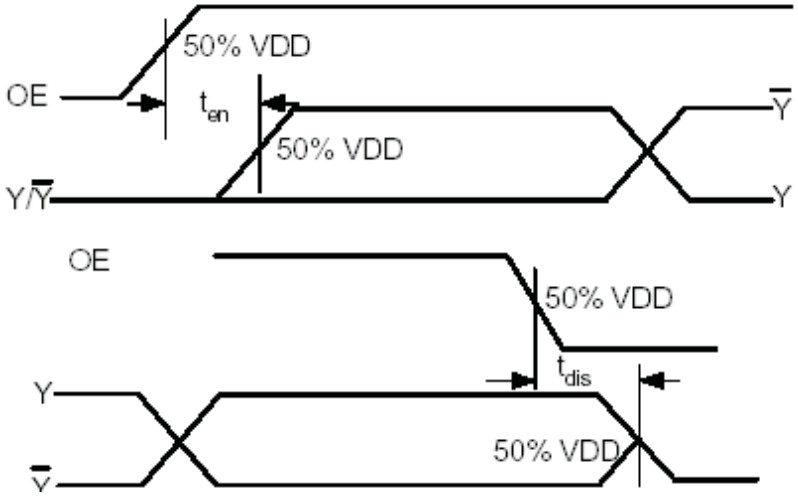
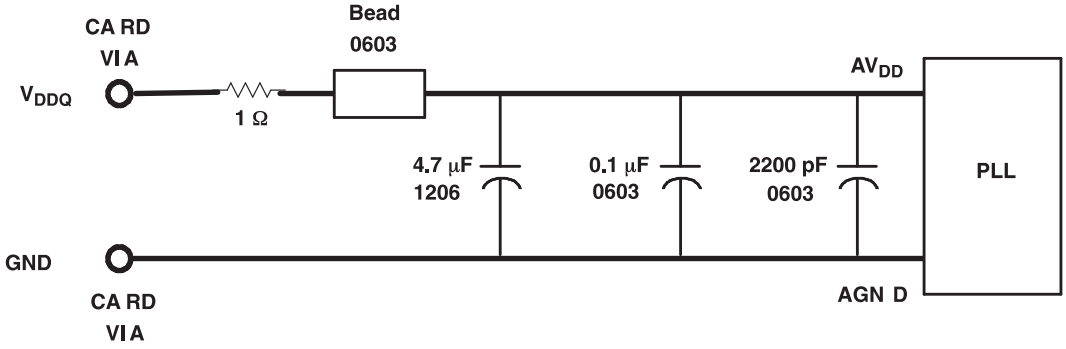



**Figure 12. Time Delay Between OE and Clock Output (Y, $\overline{Y}$)**




A. Place the 2200-pF capacitor close to the PLL.

B. Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).

C. Recommended bead: Fair-Rite PN 2506036017Y0 or equilvalent (0.8Ω dc maximum, 600Ω at 100 MHz).

**Figure 13. Recommended $AV_{DD}$ Filtering**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| CDCUA877ZQLR | ACTIVE | BGA MICROSTAR JUNIOR | ZQL | 52 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-2-260C-1 YEAR |
| CDCUA877ZQLT | ACTIVE | BGA MICROSTAR JUNIOR | ZQL | 52 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-2-260C-1 YEAR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

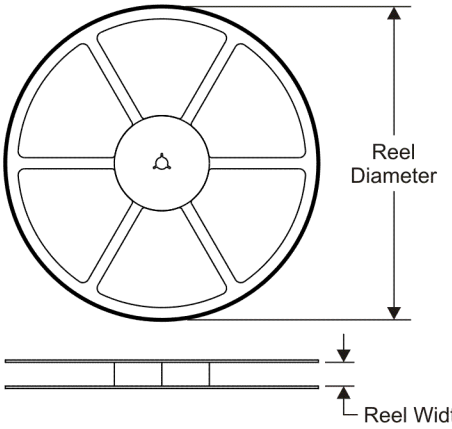
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

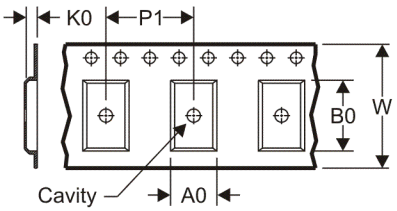
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

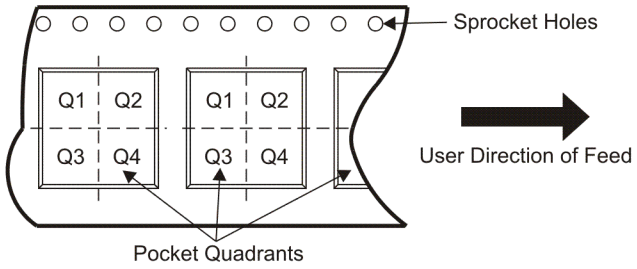



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

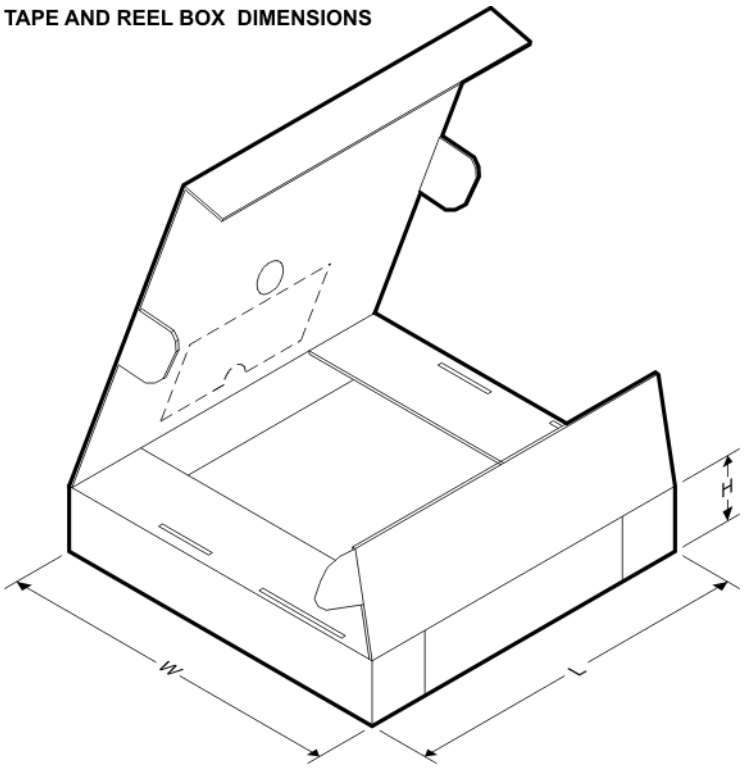
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CDCUA877ZQLR | BGA MICROSTAR JUNIOR | ZQL | 52 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.5 | 8.0 | 16.0 | Q1 |
| CDCUA877ZQLT | BGA MICROSTAR JUNIOR | ZQL | 52 | 250 | 330.0 | 16.4 | 4.8 | 7.3 | 1.5 | 8.0 | 16.0 | Q1 |

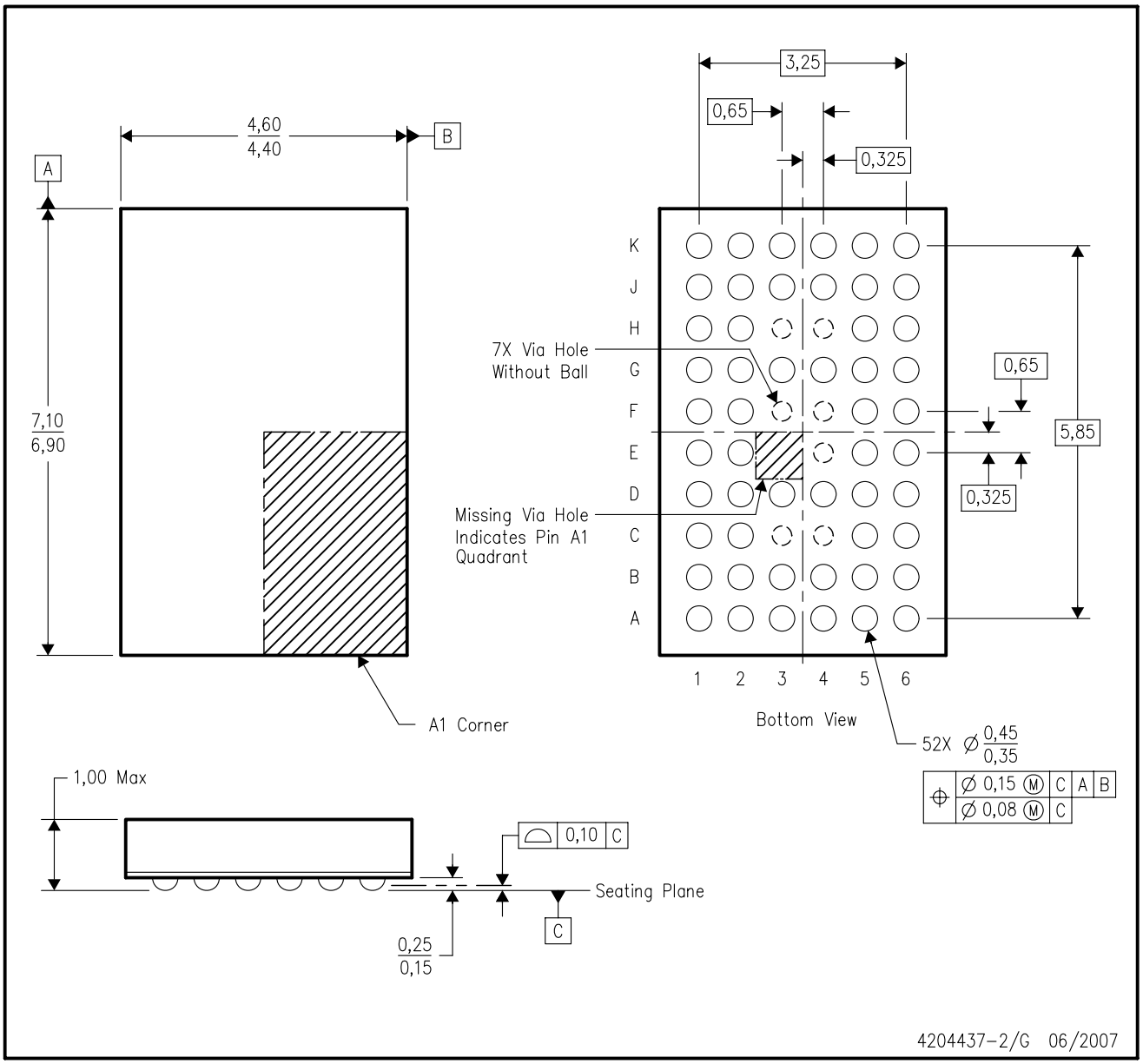
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CDCUA877ZQLR | BGA MICROSTAR JUNIOR | ZQL | 52 | 1000 | 333.2 | 345.9 | 28.6 |
| CDCUA877ZQLT | BGA MICROSTAR JUNIOR | ZQL | 52 | 250 | 333.2 | 345.9 | 28.6 |

## ZQL (R–PBGA–N52) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–285 variation BA–2.
D. This package is lead–free. Refer to the 52 GQL package (drawing 4200583) for tin–lead (SnPb).

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DLP® Products | www.dlp.com | Broadband | www.ti.com/broadband |
| DSP | dsp.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Clocks and Timers | www.ti.com/clocks | Medical | www.ti.com/medical |
| Interface | interface.ti.com | Military | www.ti.com/military |
| Logic | logic.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Power Mgmt | power.ti.com | Security | www.ti.com/security |
| Microcontrollers | microcontroller.ti.com | Telephony | www.ti.com/telephony |
| RFID | www.ti-rfid.com | Video & Imaging | www.ti.com/video |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated