dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family devices that you have received conform functionally to the current Device Data Sheet (DS70000318**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 21, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
    a) For MPLAB IDE 8, select *Programmer > Reconnect*.
    b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number and Device ID and Revision ID values appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID[1]	Revision ID for Silicon Revision[2]		
		A2	A3	A4
dsPIC33FJ06GS101	0x0C00	0x3002	0x3003	0x3004
dsPIC33FJ06GS102	0x0C01			
dsPIC33FJ06GS202	0x0C02			
dsPIC33FJ16GS402	0x0C04			
dsPIC33FJ16GS404	0x0C06			
dsPIC33FJ16GS502	0x0C03			
dsPIC33FJ16GS504	0x0C05			

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				A2	A3	A4
PWM	Leading-Edge Blanking	1.	Reading LEBCONx registers, as well as writing individual bits and bytes within these registers, does not work.	X	X	X
PWM	Immediate Updates	2.	PWM Immediate Update mode (IEU = 1) for the Master Duty Cycle register (MDC) is not functional.	X	X	X
PWM	Status Bits	3.	PWM Fault status bits do not function if the associated PWM Fault interrupts are disabled.	X	X	X
PWM	Clock	4.	PWM output will exhibit jitter with some PWM clock divider settings.	X	X	X
PWM	Faults	5.	If the PWM is in Complementary, Redundant and Push-Pull mode, and the Independent Time Base (ITB) bit is set, the Independent Fault mode may not work as expected for the PWMxL pin.	X	X	X
PWM	Independent Time Base	6.	The Independent Time Base PWM outputs may not be synchronized with the master time base PWM outputs when both modes are used simultaneously.	X	X	X
PWM	Latched Faults	7.	In PWM Latched Fault mode, the PWM outputs may be latched on both the rising as well as the falling edge of the Fault signal, regardless of the Fault input polarity selection (set with the FLTPOL (FCLCONx[2]) bit setting).	X	X	X
PWM	Faults	8.	A bit write to the CLMOD bit (FCLCONx[8]), or consecutive writes to the lower byte and higher byte of the FCLCONx register, causes all other bits of the high byte to be loaded with zeros.	X	X	X
PWM	Sleep Mode	9.	The PWM module fails to wake the CPU from Sleep mode on a PWM Fault event.	X	X	X
Comparator	—	10.	For slow input signals, the comparator module may generate erroneous triggers/interrupts.	X	X	X
ADC	Clock	11.	Selecting the primary FRC (F_{VCO}) as a clock source for the ADC module by setting the SLOWCLK bit (ADCON[12]) to the default setting of '0' does not work.	X	X	X
Auxiliary Clock	Module Disable	12.	When the PWMMD bit in the PMD1 register is set, the Auxiliary Clock (ACLK) to both the ADC and PWM modules is disabled.	X	X	X
Comparator	Interrupts	13.	Comparator interrupts are incorrectly generated when the high-speed analog comparator is configured for an inverted polarity setting (CMPPOL (CMPCONx[1]) = 1).	X	X	X
UART	4x Mode	14.	When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.	X	X	X
UART	IR Interface Operations	15.	The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.	X	X	X
I^{2}C	10-Bit Addressing Mode	16.	When the I^{2}C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^{2}C devices, the A10 and A9 bits may not work as expected.	X	X	X
PWM	ADC Conversion	17.	The PWM module may fail to trigger a conversion on certain ADC pairs when the primary or secondary PWMx generator is selected as a trigger source.	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: **SILICON ISSUE SUMMARY (CONTINUED)**

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				A2	A3	A4
Core	PGEC3/PGED3 Programming Pins	18.	When using the PGEC3/PGED3 pins for device programming, the programming time may be slower as compared to other available PGECx/PGEDx pin pairs.	X	X	X
UART	Break Character Generation	19.	The UART module will not generate back-to-back Break characters.	X	X	X
PWM	Current Limit	20.	Cycle-by-cycle current-limit operation does not work when the PWM module is configured for Center-Aligned mode.	X	X	X
PWM	Current Reset Mode	21.	Current Reset mode does not work when the Current-Limit Source (CLSRC) occurs during, and persists past, the assertive time interval of the PWM, and Leading-Edge Blanking (LEB) time is less than the PWM assertive time interval.	X	X	X
UART	IrDA® Encoder/ Decoder (8-Bit Mode)	22.	When the UART module is operating in 8-bit mode (PDSEL[1:0] = 0x) and using the IrDA encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.	X	X	X
UART	U1E Interrupt	23.	The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.	X	X	X
I²C	10-Bit Addressing Mode	24.	When the I²C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.	X	X	X
I²C	10-Bit Addressing Mode	25.	The 10-bit slave does not set the RBF flag or load the I2CxRCV register on address match if the Least Significant bits (LSbs) of the address are the same as the 7-bit reserved addresses.	X	X	X
PSV Operations	Addressing Modes	26.	An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.	X	X	X
Comparator	Sleep Mode	27.	The comparator fails to wake the CPU from Sleep mode when the internal voltage reference is used.	X	X	X
PWM	Independent Time Base	28.	When updating the frequency on the fly, push-pull PWM outputs may not be synchronized with other PWM output modes.	X	X	X
Analog Comparator	Internal Band Gap Reference Voltage	29.	The Internal Band Gap Reference Voltage (INTREF) for the analog comparator does not meet the stated accuracy specifications.	X	X	X
Auxiliary PLL	Input Frequency	30.	For extended temperature devices, the auxiliary PLL input frequency does not meet the published specification range.	X	X	X
ADC	Current Consumption in Sleep Mode	31.	If the ADC module is in an enabled state when the device enters Sleep mode, the Power-Down Current (IPD) of the device may exceed the device data sheet specifications.	X	X	X
High-Speed PWM	PWM Module Enable	32.	A glitch may be observed on the PWM pins when the PWM module is enabled after assignment of pin ownership to the PWM module.	X	X	X
Reserved	—	33.	—	—		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 2: **SILICON ISSUE SUMMARY (CONTINUED)**

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				A2	A3	A4
PWM	Duty Cycle or Dead-Time Updates	34.	When the PWM duty cycle or dead-time update coincides with the PWM period rollover, the PWM output may be corrupted for one PWM period.	X	X	X
JTAG	Active Pull-up	35.	In JTAG mode, the TMS pin will not have an active pull-up as required by the JTAG specification.	X	X	X
SPI	Framed Master Mode	36.	When the SPI module is configured in Framed Master mode and the Frame Sync Pulse Edge Select bit (FRMDLY) is set to '1', transmitting a word and then buffering another word in the SPIxBUF register before the transmission has completed, results in an incomplete transmission of the first data word.	X	X	X
Comparator	Trigger Voltage Level	37.	Output signal transitions occurring on the DACOUT pin (with DAC output disabled) can cause the comparator trigger voltage level to change.	X	X	X
CPU	Interrupt Disable	38.	When a previous DISI instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.	X	X	X
CPU	div.sd	39.	When using the div.sd instruction, the Overflow bit is not getting set when an overflow occurs.	X	X	X
UART	TX Interrupt	40.	A Transmit (TX) interrupt may occur before the data transmission is complete.	X	X	X
JTAG	Flash Programming	41.	JTAG Flash programming is not supported.	X	X	X
PWM	PWM Module Enable	42.	If the PWM Clock Divider Select register, PTCON2, is not equal to zero, the PWM module may or may not initialize from an override state.	X	X	X
PWM	PWM SWAP	43.	If the PWM is configured for Complementary mode and the SWAP bit is enabled, the PWM outputs might operate as in Redundant mode when the PHASEx value is greater than the programmed PWMx Dead-Time (DTRx) value.	X	X	X
PWM	Current-Limit Mode	44.	A <8 ns glitch may be observed on the PWM output pins when the current-limit event occurs.	X	X	X
PWM	Immediate Update	45.	Dead time is not asserted when PDCx is updated to cause an immediate transition on the PWMxH and PWMxL outputs.	X	X	X
ADC	—	46.	ADC measurement of INTREF may be zero under certain start-up conditions.	X	X	X
PWM	Redundant/ Push-Pull Output Mode	47.	When the Immediate Update is disabled, changing the duty cycle value from a non-zero value to zero will produce a glitch pulse equal to 1 PWM clock.	X	X	X
PWM	Master Time Base Mode	48.	When the Immediate Update is disabled, certain changes to the PHASEx register may result in missing dead time.	X	X	X
PWM	Trigger Compare Match	49.	The first PWM/ADC trigger event on a TRIGx/STRIGx match may not occur under certain conditions.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				A2	A3	A4
I^{2}C	Slave Mode	50.	Clock stretching may not occur when enabled.	X	X	X
UART	Transmit Mode	51.	TRMT bit is set before the Shift register is empty.	X	X	X
PWM	Fault	52.	When the PWM module is operated in Complementary, Redundant, Push-Pull or True Independent Output modes, the PWM Fault/Current-Limit Fault signal fails to recognize the Fault event, where the Fault event active edge matches the PWM End-of-Cycle (EOC).	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: PWM

Reading LEBCONx registers, as well as writing individual bits and bytes within these registers, does not work.

Work around

Use a word write operation to modify the LEBCONx registers. For example, to set the PHR bit within the LEBCON1 register, use the following C code:

```
LEBCON1 = 0x8000
```

There is no work around for reading LEBCONx registers.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

2. Module: PWM

If PWM Immediate Update mode is selected (IUE = 1), and the PWM duty cycle is provided via the Master Duty Cycle (MDC) register (MDCS = 1 mode), the updates to the MDC register are synchronized to the PWM time base instead of an immediate update (duty cycle will be updated on the next PWM period).

Work arounds

Work around 1:

Use the Enable Immediate Period Update mode (EIPU = 1) in conjunction with PWM Immediate Update mode (IUE = 1). This will update the period and duty cycle on an immediate basis.

Work around 2:

Use individual duty cycle registers (PDCx) and PWM Immediate Update mode (IUE = 1) to update individual duty cycle registers on an immediate basis.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

3. Module: PWM

If PWM Fault interrupts are disabled (FLTIEN = 0 or CLIEN = 0), then associated status bits (FLTSTAT and CLSTAT) will not function.

Work around

Enable PWM Fault interrupts (FLTIEN = 1, CLIEN = 1).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

4. Module: PWM

The PWM output will exhibit jitter under the following conditions:

When the PWM clock divider has the value of 1, 5 or 6 (PCLKDIV[2:0] (PTCON2[2:0]) = 0b001, 0b101 or 0b110), and the three Least Significant bits of the PWM Period register (PTPER or PHASEx), the Duty Cycle register (MDC or PDCx) or Phase-Shift register (PHASEx) are non-zero.

Work around

Use PWM clock dividers other than 1, 5 or 6.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

5. Module: PWM

When the PWM module is operated in Complementary, Redundant and Push-Pull Output modes, with Independent Time Base (ITB = 1) and Independent Fault mode (IFLTMOD = 1) enabled, the PWMxH and PWMxL outputs should be affected by the Fault and current-limit events as follows:

- PWMxH is affected by the current-limit source, CLSRC[4:0] (FCLCONx[14:10]), and the current-limit should be reset at the end of the primary local time base.
- PWMxL is affected by the Fault source, FLTSRC[4:0] (FCLCONx[7:3]), and the Fault should be reset at the end of the primary local time base.

On silicon revisions affected by this erratum, the current-limit event works correctly for the PWMxH pin. However, the Fault event is reset by the secondary local time base, although it is not used to generate the time base value. As a result, the Fault event on the PWMxL pin may not work as expected. This erratum only applies to the cycle-by-cycle Fault mode (FLTMOD[1:0] = 0b01).

Work around

If PWM is in Complementary, Redundant or Push-Pull mode and ITB = 1, set SPHASEx to have the same value as PHASEx. This will ensure that the Fault event on the PWMxL pin is reset at the start of the new PWM period for cycle-by-cycle independent Fault operation.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

6. Module: PWM

The Independent Time Base PWM outputs may not be synchronized with the master time base PWM outputs when both modes are used simultaneously.

Work around

To synchronize the independent PWM outputs with the master time base PWM outputs, disable the Immediate Update Enable bit (IUE = 0), ensure that the three Least Significant bits of the period are zero, and that the duty cycle is between 8 ns and the period minus 0x8.

This work around will not work if the frequency of the PWM module is being updated on-the-fly.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

7. Module: PWM

In PWM Latched Fault mode, the PWM outputs may be latched on both the rising, as well as the falling, edge of the Fault signal, regardless of the Fault input polarity selection (set with the FLTPOL (FCLCONx[2]) bit setting).

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

8. Module: PWM

A bit write to the CLMOD bit (FCLCONx[8]), or consecutive writes to the lower byte and higher byte of the FCLCONx register, causes all other bits of the high byte to be loaded with zeros.

Work around

Use word writes for the FCLCONx register instead of bit or byte writes.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

9. Module: PWM

The PWM module fails to wake the CPU from Sleep mode on a PWM Fault event.

Work around

Use the external interrupt pins to wake the CPU from Sleep mode.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

10. Module: Comparator

If the slew rate of the comparator input signal is lower than 198 mV/µs, the comparator module generates erroneous triggers/interrupts.

Work around

The slew rate of the comparator input signal must be higher than 198 mV/µs to avoid multiple triggers/interrupts.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

11. Module: ADC

Selecting the primary FRC (F$_{VCO}$) as a clock source for the ADC module by setting the SLOWCLK bit (ADCON[12]) to the default setting of '0' does not work.

Work around

Always set the SLOWCLK bit (ADCON[12]) to '1', which selects the Auxiliary Clock (ACLK) as a clock source for the ADC. Use the Auxiliary Clock Configuration registers to select the primary FRC (F$_{VCO}$) as a source (if desired) or other clock sources as inputs. See **Section 8.0 "Oscillator Configuration"** of the device data sheet (DS70000318**G**) for more information.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

12. Module: Auxiliary Clock

When the PWMMD bit in the PMD1 register is set, the Auxiliary Clock to both the ADC and PWM modules is disabled.

Work around

To disable the Auxiliary Clock for the PWM module, but not for the ADC module, set the individual PWM generator PMD bits in the PMD6 register.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

13. Module: Comparator

The comparator interrupt should be generated on a rising edge of the comparator output. When using the inverted polarity setting for the analog comparator (CMPPOL (CMPCON[1]) = 1), the interrupt should be generated when the analog voltage at the comparator input falls below the programmable threshold determined by the CMPDACx register setting. However, with this setting, the interrupts may be generated regardless of the state of the comparator.

Work around

When using comparator interrupts, configure the external circuit to use the non-inverted polarity comparator setting (CMPPOL (CMPCON[1]) = 0).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

14. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

15. Module: UART

When the UART is configured for IR interface operations (UxMODE[9:8] = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is Idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

16. Module: I²C

If there are two I²C devices on the bus, one of them is acting as the master receiver and the other as the slave transmitter. If both devices are configured for 10-Bit Addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the slave select address is sent from the master, both the master and slave Acknowledge it. When the master sends out the read operation, both the master and the slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I²C devices, the addresses, as well as bits A10 and A9, should be different.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

17. Module: PWM

When the primary or secondary PWMx generator is selected as a trigger source for ADC Convert Pairs 3, 4, 5 or 6 and the PWM module is running at the maximum speed, the PWM module may fail to trigger a conversion on these ADC pairs.

Work arounds

Work around 1:

Configure the PWM module to trigger the ADC module per the following steps (see Example 1 for the code used in this work around):

1. Enable the Dual Trigger Mode bit (DTM) in the TRGCONx register.
2. Configure the TRIGx register to the desired trigger point.
3. Configure the STRIGx register to TRIGx + 0x8.
4. Select the PWMx primary trigger as the ADC trigger source for conversion.

If the PWM channel is configured for Independent Output mode and both channels are operating on the same time base, the phase difference between the two channels must be considered when setting the STRIGx register. This work around will not work for True Independent Time Base mode.

With this work around, the PWMx secondary trigger should not be selected as the trigger source for the ADC convert pair.

Work around 2:

Configure the PWM Input Clock Prescaler bits (PCLKDIV[2:0]) for divide-by-2 or higher.

Work around 3:

Utilize other available trigger sources, such as software or timer triggers, to initiate conversion on the affected ADC convert pairs.

Affected Silicon Revisions

A2	A3	A4					
X							

EXAMPLE 1:   USING DUAL TRIGGER MODE

```
TRGCON1bits.DTM = 1;        /* Dual trigger mode (DTM) and STRIG used in combination to generate */
                           /* ADCPx triggers */
TRIG1 = 1224;              /* Configure desired trigger */
STRIG1 = 1232;             /* STRIG1 should be configured for TRIG1 + 8 */
ADCPC2bits.TRGSRC5 = 0x4;  /* PWM1 primary trigger selected as ADC trigger source for ADCP5*/
```

18. Module: Core

When using the PGEC3/PGED3 pins for device programming, the programming time may be slower as compared to other available PGECx/PGEDx pin pairs, because the Enhanced ICSP™ programming algorithm cannot be executed on this pin pair.

Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for additional information on this limitation.

Work around

Use alternate PGECx/PGEDx programming pin pairs.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

19. Module: UART

The UART module will not generate consecutive Break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

20. Module: PWM

Cycle-by-cycle current-limit operation does not work when the PWM module is configured for Center-Aligned mode.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

21. Module: PWM

During normal operation, if Leading-Edge Blanking (LEB) is triggered to start counting at a rising edge of PWM and the PWM module has a blanking time period less than the PWM assertive time (T_{ON} time), and the current-limit event occurs during the T_{ON} period and is still pending after the T_{ON} period is over, the current-limit event should be ignored during T_{ON} time, but should be recognized after the T_{ON} time is over.

However, the device fails to recognize the current-limit event after T_{ON} time is over when the previously described conditions exist.

Work around

Initialize the LEBCONx register, as shown below, which specifies the LEB function for the (CLSRC[4:0]) input to be triggered on the falling (trailing) edge of PWM and set the LEB delay to a minimum value of 8 ns:

- PHF bit is set
- CLLEBEN bit is set
- LEB[6:3] bits are set to a minimum value of '1'

If the user application needs LEB to be triggered at a falling edge, make sure that the LEB delay is set for more than the T_{ON} time.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

22. Module: UART

When the UART is operating in 8-bit mode (PDSEL[1:0] = `0x`) and using the IrDA® encoder/decoder (IREN = `1`), the module incorrectly transmits a data payload of 80h as 00h.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

23. Module: UART

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

24. Module: I²C

When the I²C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01, rather than 0x02; however, the module Acknowledges both address bytes.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

25. Module: I²C

In 10-Bit Addressing mode, some address matches do not set the RBF flag or load the I2Cx Receive register, I2CxRCV, if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form, 'xx0000xx' and 'xx1111xxxx', with the following exceptions:

- '001111000x'
- '011111001x'
- '101111010x'
- '111111011x'

Work around

Ensure that the lower address byte in 10-Bit Addressing mode does not match any 7-bit reserved addresses.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

26. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of a PSV page. This occurs only when using the following addressing modes:

- MOV.D
- Register Indirect Addressing (Word or Byte mode) with Pre/Post-Decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB® C30 Version 3.11 or higher, the version provides the following command-line switch that implements a work around for the erratum:

```
-merrata=psv_trap
```

Refer to the readme.txt file in the MPLAB C30 v3.11 toolsuite for further details.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

27. Module: Comparator

The comparator fails to wake the CPU from Sleep mode when the internal voltage reference is used (i.e., the EXTREF bit is set to '0').

Work around

Use the external reference source by setting the EXTREF bit to '1'.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

28. Module: PWM

When multiple PWM channels are operating in Independent Time Base mode (ITB = 1) and the frequency is being updated on-the-fly, PWM channels configured for Push-Pull mode may not remain synchronized with other PWM output modes.

Work around

When multiple PWM channels are operating in Independent Time Base mode, immediate updates to the PWM module (IUE = 1) must be enabled for PWM channels to remain synchronized.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

29. Module: Analog Comparator

The Internal Band Gap Reference Voltage (INTREF) for the analog comparator provides the reference to the analog comparator if the EXTREF bit (CMPCONx[5]) = 0 and the RANGE bit (CMPCONx[0]) = 0. The data sheet states that the INTREF voltage should be 1.2V nominal and within ±1%.

However, the Internal Band Gap Reference Voltage does not meet the specification stated above. For the actual range of the INTREF voltage, refer to the IV$_{REF}$ specification in the **"Electrical Characteristics"** chapter of the device data sheet.

Work arounds

To avoid this issue, implement one of the following two work arounds, depending on the application requirements.

Work around 1:

Use an external voltage reference for the analog comparator by setting the EXTREF bit (CMPCONx[5]) = 1 and providing an external reference to the EXTREF pin.

Work around 2:

Use the high-range setting for the internal reference by setting the EXTREF bit (CMPCONx[5]) = 0 and the RANGE bit (CMPCONx[0]) = 1. This setting uses AV$_{DD}$/2 as the comparator reference voltage.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

30. Module: Auxiliary PLL

For extended temperature devices (designated with the -E suffix in the device part number) with the date code of 09XX, the auxiliary PLL input frequency does not meet the published specification range at operating temperatures above +85ºC.

Work around

Use the internal FRC oscillator as the input to the auxiliary PLL or use the external oscillator with a frequency of 7.37 MHz.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

31. Module: ADC

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a `PWRSAV #0` instruction, the device Power-Down Current (I$_{PD}$) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

Work arounds

Work around 1:

In order to remain within the I$_{PD}$ specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC Module Disable bit in the corresponding Peripheral Module Disable x register (PMDx), prior to executing a `PWRSAV #0` instruction.

Note:	The ADC module must be reinitialized by the user application before resuming ADC operation.

Work around 2:

If the ADC module was previously initialized and enabled before entering Sleep, execute the lines of code provided in Example 2.

Note:	Unlike **Work around 1**, the user application does not need to reinitialize the ADC module; however, it is necessary to re-enable the ADC module by setting the ADON bit after waking from Sleep.

EXAMPLE 2:

```
AD1CON1bits.ADON = 0;            //Disable the ADC module
__asm__ volatile ("REPEAT #50"); //Wait 50 Tcy
__asm__ volatile ("NOP");        //Repeat NOP 51 times
Sleep();                         // Execute PWRSAV #0 and go to Sleep
```

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

32. Module: High-Speed PWM

The PENH and PENL bits in the IOCONx register are used to assign ownership of the pins to either the PWM module or the GPIO module. The correct procedure to configure the PWM module is to assign pin ownership to the PWM module and then enable it using the PTEN bit in the PTCON register.

If the PWM module is enabled using the above sequence, then a glitch may be observed on the PWM pins before the actual switching of the PWM outputs begins. This glitch may cause momentary turn-on of power MOSFETs that are driven by the PWM pins and may cause damage to the application hardware.

Work around

Follow the given sequence to avoid any glitches from appearing on the PWM outputs at the time of enabling.

1. Configure the respective PWM pins to digital inputs using the TRISx registers. This step will put the PWM pins in a high-impedance state. The PWM outputs must be maintained in a safe state by using pull-up or pull-down resistors.

2. Assign pin ownership to the GPIO module by configuring PENH (IOCONx[15]) = `0` and PENL (IOCONx[14]) = `0`.

3. Specify the PWM override state to the desired safe state for the PWM pins using the OVRDAT[1:0] bit field in the IOCONx register.

4. Override the PWM outputs by setting OVRENH (IOCONx[9]) = `1` and OVRENL (IOCONx[8]) = `1`.

5. Enable the PWM module by setting PTEN (PCON[15]) = `1`.

6. Remove the PWM overrides by making OVRENH = `0` and OVRENL = `0`.

7. Ensure a delay of at least one full PWM cycle.

8. Assign pin ownership to the PWM module by setting PENH (IOCONx[15]) = `1` and PENL (IOCONx[14]) = `1`.

The code in Example 3 illustrates the use of this work around.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

EXAMPLE 3: CONFIGURE PWM MODULE TO PREVENT GLITCHES ON PWM1H AND PWM1L PINS AT THE TIME OF ENABLING

```
TRISAbits.TRISA4 = 1;      // Configure PWM1H/RA4 as digital input
                           // Ensure output is in safe state using pull-up or
                           // pull-down resistors
TRISAbits.TRISA3 = 1;      // Configure PWM1L/RA3 as digital input
                           // Ensure output is in safe state using pull-up or
                           // pull-down resistors

IOCON1bits.PENH = 0;       // Assign pin ownership of PWM1H/RA4 to GPIO module
IOCON1bits.PENL = 0;       // Assign pin ownership of PWM1L/RA3 to GPIO module

IOCON1bits.OVRDAT = 0;     // Configure override state of the PWM outputs to
                           // desired safe state.

IOCON1bits.OVRENH = 1;     // Override PWM1H output
IOCON1bits.OVRENL = 1;     // Override PWM1L output

PTCONbits.PTEN = 1;        // Enable PWM module

IOCON1bits.OVRENH = 0;     // Remove override for PWM1H output
IOCON1bits.OVRENL = 0;     // Remove override for PWM1L output

Delay(x);                  // Introduce a delay greater than one full PWM cycle

IOCON1bits.PENH = 1;       // Assign pin ownership of PWM1H/RA4 to PWM module
IOCON1bits.PENL = 1;       // Assign pin ownership of PWM1L/RA3 to PWM module
```

33. Module: Reserved

The issue in a previous version of the document was removed.

34. Module: PWM

The high-speed PWM provides a feature to update the PWM duty cycle and dead time at any time during the PWM period. The new duty cycle and new dead time should take effect:

- On the next PWM period when immediate duty cycle and dead-time updates are disabled (IUE (PWMCONx[0]) = 0).
- On the same PWM period when immediate duty cycle and dead-time updates are enabled (IUE (PWMCONx[0]) = 1).

However, when the immediate duty cycle and dead-time updates are disabled (IUE (PWMCONx[0]) = 0), the following consequences may occur.

1. If the duty cycle update coincides with a PWM period rollover, the PWM output may be corrupted and exhibit a 100% duty cycle for one PWM period. The new duty cycle value will take effect on the next PWM period.
2. If the dead-time update coincides with a PWM period rollover, the PWM output may be corrupted and exhibit a truncation in duty cycle for one PWM period. The new dead-time value will take effect on the next PWM period.

Work around

1. Enable immediate duty cycle updates by configuring (IUE (PWMCONx[0]) = 1).
2. Ensure that duty cycle and dead-time updates occur away from the PWM rollover event.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

35. Module: JTAG

In JTAG mode, the TMS pin will not have an active pull-up as required by the JTAG specification. Instead, the pull-up function will be enabled on the TCK pin.

> **Note:** This issue is only present in the dsPIC33FJ06GS101 device.

Work around

An external pull-up resistor can be connected to the TMS pin to ensure that the signal does not enter a tri-state condition when in JTAG mode.

There is no work around for the wrongly enabled pull-up function on the TCK pin.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

36. Module: SPI

When the SPI module is configured in Framed Master mode and the Frame Sync Pulse Edge Select bit (FRMDLY) is set to '1', transmitting a word and then buffering another word in the SPIxBUF register before the transmission has completed results in an incomplete transmission of the first data word. Only the first 15 bits from the first data word are transmitted, followed by the sync pulse and the complete second word.

Work around

Between the two back-to-back SPI operations, add a delay to ensure that the first word is fully transmitted before the second word is written to the SPIxBUF register, as shown in Example 4.

EXAMPLE 4:

```
SPI1BUF = 0x0001;

while  (SPI1STATbits.SPITBF);

      asm ("REPEAT #50");.
      asm ("NOP");

// The number of NOPs depends on the SPI
// clock prescalers

SPI1BUF = 0x0002;
```

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

37. Module: Comparator

With the DAC output is disabled by clearing the DACOEN bit (CMPCONx[8]), output signal transitions occurring on the DACOUT pin can cause the comparator trigger voltage level to change. For example, if the UART1 Transmit (U1TX) signal is mapped to the same pin as DACOUT, UART data transmissions can cause the comparator to get triggered at different trigger levels than what is programmed through the CMPDACx register.

Work around

When the comparator is enabled, do not use the DACOUT pin, either as a general purpose I/O pin or a peripheral output signal.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

38. Module: CPU

When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.

Work around

Avoid updating the DISICNT register manually. Instead, use the `DISI #n` instruction with the required value for 'n'.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

39. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the Overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

40. Module: UART

When using UTXISEL[1:0] = `01` (interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register, the Transmit (TX) interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occurs only when all transmit operations are complete, hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

41. Module: JTAG

JTAG Flash programming is not supported.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

42. Module: PWM

If the PWM Clock Divider Select register, PTCON2, is not equal to zero, the PWM module may or may not initialize from an override state (OVRENH (IOCONx[9]) = `1` or OVRENL (IOCONx[8]) = `1`).

Work around

When configuring the Override Enable bits (OVRENL/OVRENH) in the PWMx I/O Control register, IOCONx, set these bits implicitly via word format and not explicitly via bit format.

For example:

```
IOCONx = IOCONx & 0xFCFF;
```

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

43. Module: PWM

If the PWM is configured for Complementary mode and the SWAP bit is enabled, the PWM outputs might operate as if in Redundant mode when the PHASEx value is greater than the programmed PWMx Dead-Time (DTRx) value.

Work around

Using True Independent Output mode with the Independent Time Base mode bit (ITB) set to '0', the PWMx module can be configured to replicate the original complementary signal by properly setting up the phase (PHASEx, SPASEx) and the independent duty cycle (PDCx, SDCx).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

44. Module: PWM

The PWMx current-limit operation allows the PWMx module to set/reset the output signals when a specific current limit is detected with a minimum latency delay. When operating the PWMx module in Complementary mode (PMOD = 0), positive dead time, and with Current-Limit Interrupt Enable (CLIEN = 1), a less than 8 ns pulse glitch on the complementary output may be present right after the current limit is detected. This glitch, if present, will occur prior to the implementation of the dead time.

Work around

In order to avoid the <8 ns glitch to be propagated into the MOSFET gate driver, a low-pass filter (e.g., resistor-capacitor network) should be implemented between the dsPIC$^®$ DSC PWMx output pin and the gate driver IC input pin.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

45. Module: PWM

The PWMx generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

- The PWMx generator is configured to operate in Complementary mode with the Independent Time Base or master time base;
- Immediate update is enabled; and
- The value in the PDCx register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

The current duty cycle, PDC$_{OLD}$, newly calculated duty cycle, PDC$_{NEW}$, and the point at which the write to the Duty Cycle register occurs within the PWMx time base, will determine if the PWMxH and PWMxL outputs make an immediate transition. PWMxH and PWMxL outputs make an immediate transition if the Duty Cycle register is written with a new value, PDC$_{NEW}$, at a point of time when the PWMx time base is counting a value that is in between PDC$_{NEW}$ and PDC$_{OLD}$. Additionally, writing to the Duty Cycle register close to the instant of time where dead time is being applied may result in reduced dead time, effective on the PWMxH and PWMxL transition edges.

In Figure 1 (following page), if the duty cycle write occurred in the shaded box, then PWMxH and PWMxL will make an immediate transition without dead time.

Work around

None. However, in most applications, the duty cycle update timing can be controlled using the TRIGx trigger or Special Event Trigger, such that the above mentioned conditions are avoided altogether.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

FIGURE 1: **TIMING DIAGRAMS FOR CENTER-ALIGNED AND EDGE-ALIGNED MODES**
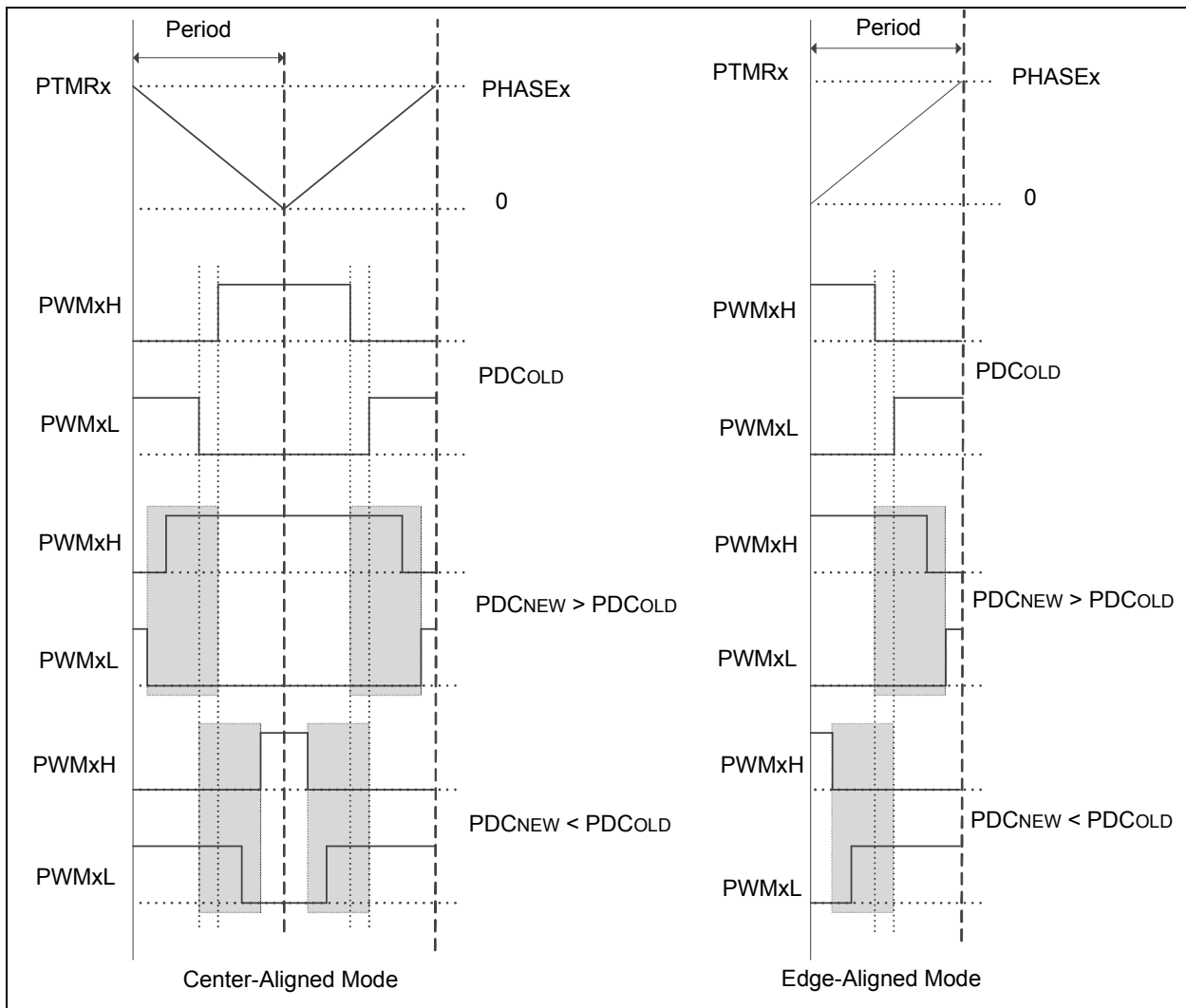
46. Module: ADC

Depending on device start-up conditions, measuring the Internal Voltage Reference (INTREF) with the ADC may return a value of 0V in the result buffer.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

47. Module: PWM

In Redundant Output mode (IOCONx[11:10] = 01) and Push-Pull Output mode (IOCONx[11:10] = 10), with the Immediate Update disabled (PWMCONx[0] = 0), when the Duty Cycle register is updated from a non-zero value to zero, a glitch pulse of a width equal to 1 PWM clock will appear at the next PWM period boundary, as shown in Figure 2 (for the Redundant Output mode). The Duty Cycle register refers to the PDCx register if PWMCONx[8] = 0 or the MDC register if PWMCONx[8] = 1.

FIGURE 2:   ISSUE EXAMPLE FOR REDUNDANT OUTPUT MODE
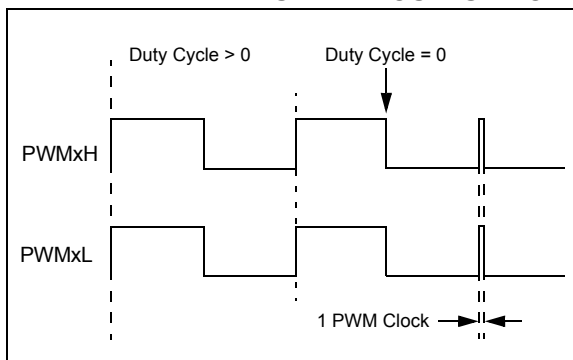
Work around

If the application requires a zero duty cycle output, there are two possible work around methods:

1. Use the PWM override feature to override the PWM output to a low state instead of writing to the Duty Cycle register. In order to switch back to a non-zero duty cycle output, turn off the PWM override. The override-on and override-off events must be timed close to the PWM period boundary if the IOCONx register has been configured with IOCON[0] = 0 (i.e., output overrides through the OVRDAT[1:0] bits occur on the next CPU clock boundary).

2. Enable the Immediate Update bit (PWMCONx[0] = 1) while configuring the PWMx module (i.e., before enabling the PWMx module (PTCON[15] = 1)). With Immediate Update enabled, writes to the Duty Cycle register can have an immediate effect on the PWM output. Therefore, the duty cycle write operations must be timed close to the PWM period boundary in order to avoid distortions in the PWM output.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

48. Module: PWM

In Edge-Aligned PWM mode with Master Time Base (PWMCONx[9] = 0) and Immediate Update disabled (PWMCONx[0] = 0), after enabling the PWMx module (PTCON[15] = 1), changes to the PHASEx register, such that PHASEx < DTRx or PHASEx > PDCx, will result in missing dead time at the PWMxH-PWMxL transition that will occur at the next master period boundary.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

49. Module: PWM

The triggers generated by the PWMx Primary Trigger Compare Value register (TRIGx) and PWMx Secondary Trigger Compare Value register (STRIGx) will not trigger at the point defined by the TRIGx/STRIGx register values on the first instance of the configurations listed below. Subsequent trigger instances are not affected.

- Trigger compare values for TRIGx and STRIGx are less than 8 counts
- Trigger Output Divider bits, TRGDIV[3:0] (TRGCONx[15:12]), are greater than '0'
- Trigger Postscaler Start Enable Select bits, TRGSTRT[5:0] (TRGCONx[5:0]), are greater than '0'

Work around

Configure the PWMx Primary Trigger Compare Value register (TRIGx) and PWMx Secondary Trigger Compare Value register (STRIGx) values to be equal to or greater than 8.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

50. Module: I²C

In Slave mode, clock stretching may not occur during address detect, even when it has been enabled (STREN = 1). As a result, the SCLREL bit may not be cleared upon address reception when the R/W̄ bit is '0'. This is seen in both 7-Bit and 10-Bit Addressing modes.

Work around

User software should read Acknowledged address from the receive buffer before the data byte is received. User software also needs to configure the slave interrupt priority, such that the interrupt latency time should be less (before the reception of the data byte).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

51. Module: UART

In Transmit mode, the TRMT bit may be set before the Shift register is empty. In back-to-back transmission, if the data is loaded into the TXREG when the TRMT bit is set, the new byte transmission starts immediately and the Stop bit may be abbreviated as in the below condition:

- When BRGH (UxMODE[3]) = 1, the Stop bit may be shortened by 1/4 of a bit clock
- When BRGH (UxMODE[3]) = 0, the Stop bit may be shortened by 1/16th of a bit clock

Work around

- Use the TXBF flag instead of the TRMT bit for loading new data into the TXREG
- Use FIFO mode instead of Buffer mode

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

52. Module: PWM

When the PWM module is operated in Complementary, Redundant, Push-Pull or True Independent Output modes and the PWM Fault/Current-Limit Fault are configured to provide a Fault event to the PWM, under certain conditions where the Fault event active edge happens to coincide with the PWM End-of-Cycle (EOC) event, the PWM fails to recognize the Fault event.

Fault Signal Coincides with PWM End-of-Cycle
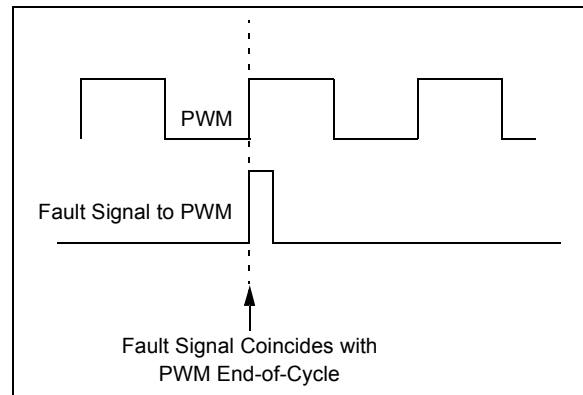
Work around

Configure the PWM module to include Leading-Edge Blanking bits, LEB[6:0] (LEBCONx [9:3]), with a count always greater than eight, with the appropriate PWMxH/PWMxL Leading-Edge Blanking triggers.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70000318**G**):

> **Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Table 24-9: DC Characteristics: I/O Pin Input Specifications

Notes 6 and 7 for Table 24-9: DC Characteristics: I/O Pin Input Specifications are incorrect.

They should be changed to:

6: V_{IH} source > (V_{DD} + 0.3) for non-5V tolerant pins only. Characterized but not tested.

7: Digital 5V tolerant pins do not have an internal high-side diode to V_{DD}, and therefore, cannot tolerate any "positive" input injection current.

2. Module: Appendix A: Revision History

In the Revision History, there is the following text:

Revision G (May 2014)

The values for the TUN[5:0] bits in Register 8-4 (OSCTUN) have changed.

This is not correct. The TUN[5:0] values have 'not' changed for any silicon revision.

APPENDIX A: REVISION HISTORY

Rev A Document (3/2009)

Initial release of this document; issued for revision A2 silicon.

Includes silicon issues 1-9 (PWM), 10 (Comparator), 11 (ADC), 12 (Auxiliary Clock), 13 (Comparator), 14-15 (UART) and 16 (I^2C).

Rev B Document (4/2009)

Added silicon issue 17 (PWM).

Rev C Document (5/2009)

Updated silicon issue 17 (PWM) to clarify which ADC pairs are involved.

Rev D Document (5/2009)

Revised to include revision A3 silicon information. Added silicon issues 18 (Core), 19 (UART) and 20-21 (PWM).

Added data sheet clarification 1 (The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70000318G):).

Rev E Document (8/2009)

Added silicon issues 22-23 (UART), 24-25 (I^2C), 26 (PSV Operations), 27 (Comparator) and 28 (PWM).

Rev F Document (1/2010)

Added silicon issues 29 (Analog Comparator) and 30 (Auxiliary PLL).

Added data sheet clarification 2 (Auxiliary PLL).

Rev G Document (6/2010)

Added silicon issues 31 (ADC) and 32 (High-Speed PWM) and data sheet clarification 3 (DC Characteristics: I/O Pin Input Specifications).

Rev H Document (10/2010)

Added revision A4 silicon information to all tables.

Updated the work arounds for silicon issue 31 (ADC).

Removed silicon issue 33 (PWM) and marked its location as reserved.

Added silicon issues 34 (PWM) and 35 (JTAG).

Rev J Document (3/2011)

Updated silicon issue 29 (Analog Comparator).

Added silicon issues 36 (SPI) and 37 (Comparator).

Added data sheet clarification 4.

Rev K Document (11/2011)

Added silicon issues 38 (CPU), 39 (CPU), 40 (UART), 41 (JTAG), and 42 (PWM).

Rev L Document (5/2012)

Removed data sheet clarifications 2, 3 and 4.

Updated silicon issues 29 (Analog Comparator) and 32 (High-Speed PWM).

Added silicon issues 43 (PWM) and 44 (PWM).

Rev M Document (1/2013)

Amended silicon issue 43 with correct PWM Clock Divider Select register bit name (changed from PTCON to PTCON2).

Included silicon issue 45 (PWM).

Rev N Document (9/2013)

Removed existing silicon issue 42 (PWM); subsequent issues are renumbered accordingly.

Added new silicon issues 45 (PWM) and 46 (ADC).

Added new data sheet clarification 2 (Packaging).

Corrected the module for issue 18 from "PGEC3/PGED3 Programming Pins" to "Core", to conform with standard nomenclature practice (the issue itself is unchanged).

Rev P Document (10/2014)

Added new silicon issues 47, 48 and 49 (PWM).

Removed data sheet clarifications 1 and 2.

Rev Q Document (1/2015)

Added new silicon issue 50 (I^2C).

Rev R Document (1/2016)

Updated silicon issues 34 (PWM) and 50 (I^2C).

Rev S Document (4/2016)

Added new silicon issue 51 (UART).

Added new data sheet clarifications 1 (Table 24-9: DC Characteristics: I/O Pin Input Specifications) and 2 (Appendix A: Revision History).

Rev T Document (3/2019)

Added new silicon issue 52 (PWM).

This revision shows modified bit representation (e.g., bits<3:0> have been changed to bits[3:0]). This is done to be consistent with documents that were created in the SDL software.

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