NUS6160MN

Low Profile Overvoltage Protection IC with Integrated MOSFET

This device represents a new level of safety and integration by combining an overvoltage protection circuit (OVP) with a dual 20 V P−channel power MOSFET. The OVP is specifically designed to protect sensitive electronic circuitry from overvoltage transients and power supply faults. During such events, the IC quickly disconnects the input supply from the load, thus protecting it. The integration of the additional transistor and power MOSFET reduces layout space and promotes better charging performance.

The IC is optimized for applications that use an external AC−DC adapter or a car accessory charger to power a portable product or recharge its internal batteries.

Features

- Overvoltage Turn−Off Time of Less Than 1.5 μs
- Undervoltage Lockout Protection; 3.0 V, Nominal
- High Accuracy Undervoltage Threshold of 5.0%
- −20 V Integrated P−Channel Power MOSFET
- Low $R_{DS(on)}$ = 64 mΩ @ −4.5 V
- Compact 3.0 x 4.0 mm QFN Package
- Maximum Solder Reflow Temperature @ 260°C
- This is a Pb−Free Device

Benefits

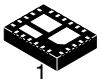
- Provide Battery Protection
- Integrated Solution Offers Cost and Space Savings
- Integrated Solution Improves System Reliability
- Optimized for Commercial PMUs from Top Suppliers

Applications

- Portable Computers and PDAs
- Cell Phones and Handheld Products
- Digital Cameras

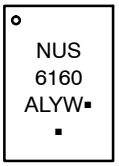
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QFN22
CASE 485AT

MARKING DIAGRAM



NUS6160 = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUS6160MNTWG	QFN22 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Publication Order Number:
NUS6160MN/D

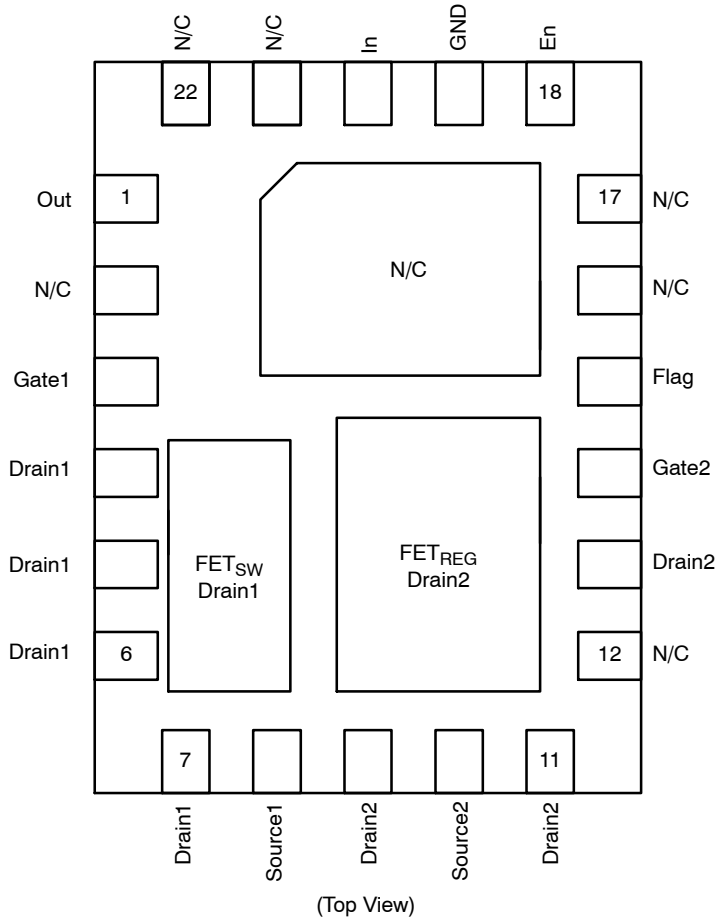


Figure 1. Pinout

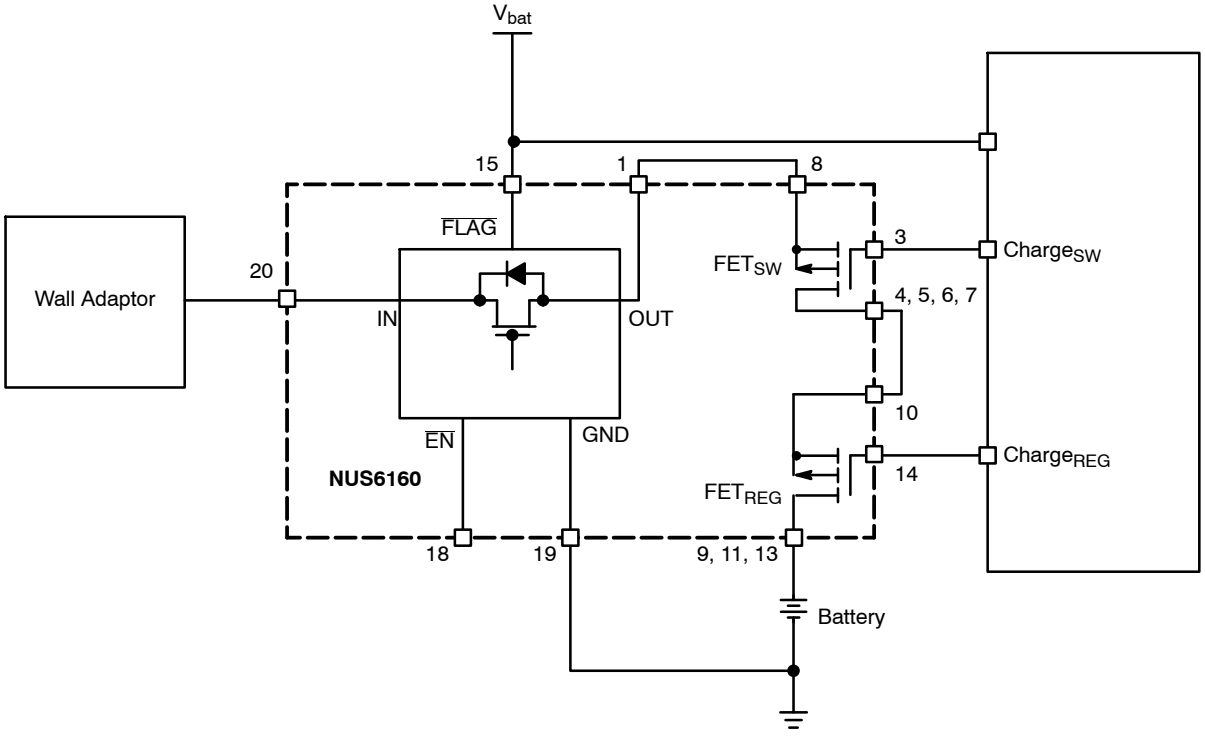


Figure 2. Typical Charging Solution

MAXIMUM RATINGS (T_J = 25°C, unless otherwise stated)

Rating	Symbol	Min	Max	Unit
V_{IN} to Ground	V_{IN}	−0.3	21	V
OUT, $\overline{EN}$, $\overline{FLAG}$ Pins Voltage to Ground	V_{OUT}, $\overline{V_{EN}}$, $\overline{V_{FLAG}}$	−0.3	7.0	V
Maximum Current from V_{IN} to V_{OUT} (PMOS)	I_{max}		600	mA
Drain−to−Source Voltage	V_{DSS}		−20	V
Gate−to−Source Voltage	V_{GS}	−8.0	8.0	V
Continuous Drain Current, Steady State	I_D		−2.0	A
Pulsed Drain Current, t_p = 10 ms	I_{DM}		−4.0	A
Source Current	I_S		−1.1	A
Operating Ambient Temperature	T_A	−40	85	°C
Storage Temperature	T_{STG}	−55	150	°C
Operating Junction Temperature	T_J		150	°C
Thermal Resistance (Note 1) 1 in^2 (645 mm^2) (All devices fully enhanced) OVP FET FET_{SW} FET_{REG} 1 in^2 (645 mm^2) (OVP and FET_{SW} fully enhanced, 1 V drop across FET_{REG}) OVP FET FET_{SW} FET_{REG} 0.25 in^2 (161 mm^2) (All devices fully enhanced) OVP FET FET_{SW} FET_{REG} 0.25 in^2 (161 mm^2) (OVP and FET_{SW} fully enhanced, 1 V drop across FET_{REG}) OVP FET FET_{SW} FET_{REG}	θ_{JA}	 68 42 46 43 39 80 79 53 56 53 49 92		°C/W
ESD Performance (Human Body Model) Pins 1, 15, 18, 19, 20	−		2.5	kV
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)	T_L		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 1 oz. copper, double sided board. Thermal impedance requires total for ΔT calculations. See example in thermal description.

PIN DESCRIPTION

Pin	Name	Description
1	Out	This pin is the output of the internal OVP chip. It must be connected to the source of the upper FET (Pin 8).
3	Gate FET_{SW}	This pin is the gate of the upper FET which is normally used for a switch in series with the battery. It is controlled by the PMU.
4, 5, 6, 7	Drain FET_{SW}	These pins are the drain of the upper FET. For the lowest on resistance connect all pins together. This set of pins must be connected to the source of the lower (regulator) FET, Pin 10.
8	Source FET_{SW}	This pin is the source of the upper FET and must be connected to the output pin of the internal OVP chip (Pin 1).
9, 11, 13	Drain FET_{REG}	These pins are the drain of the lower FET which is normally used for the regulation function. It connects to the positive terminal of the battery.
10	Source FET_{REG}	This pin is the source of the lower FET and must be connected to the drain pins of the upper FET.
12	N/C	This pin has no internal connections and is isolated from all internal circuitry within the chip.
14	Gate FET_{REG}	This pin is the gate of the lower FET which is normally used for the regulation function in series with the battery. It is controlled by the PMU.
15	$\overline{\text{FLAG}}$	The fault flag is an open drain output and therefore requires a pullup resistor. The $\overline{\text{FLAG}}$ pin will be driven low when the input voltage exceeds the OVLO trip level.
2, 16, 17, 21, 22	N/C	These pins are connected to the ground of the analog chip. This is a medium impedance connection and should not be used for the ground signal. These pins should either be left floating or connected to ground, but not any other potential. If these pins are connected to ground, the ground pin (19) must still be used.
18	$\overline{\text{EN}}$	The $\overline{\text{ENABLE}}$ pin must be held low for normal operation. When this pin is tied high the unit will be shut down. The state of the enable pin has no impact on the $\overline{\text{FAULT}}$ pin.
19	Gnd	This is the ground reference pin for the internal OVP chip.
20	In	This pin is the input to the internal OVP chip and connects to the wall, or car adaptor.

OVP ELECTRICAL CHARACTERISTICS

(Min/Max limits values (−40°C < T_A < +85°C) and V_{in} = +5.0 V. Typical values are T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}		1.2		20	V
Undervoltage Lockout Threshold	UVLO	V_{in} falls down UVLO threshold	2.85	3.0	3.15	V
Undervoltage Lockout Hysteresis	$UVLO_{hyst}$		30	50	70	mV
Overvoltage Lockout Threshold	OVLO	V_{in} rises up OVLO threshold	6.9	7.07	7.4	V
Overvoltage Lockout Hysteresis	$OVLO_{hyst}$		50	100	125	mV
V_{in} versus V_{out} Dropout	V_{drop}	V_{in} = 5 V, I charge = 500 mA		105	200	mV
Supply Quiescent Current	Idd	No Load, V_{in} = 5.25 V		24	35	μA
OVLO Supply Current	Idd_{ovlo}	V_{in} = 8 V		50	85	μA
Output Off State Current	I_{std}	V_{in} = 5.25 V, EN = 1.2 V		26	37	μA
$\overline{FLAG}$ Output Low Voltage	Vol_{flag}	V_{in} > OVLO, Sink 1 mA on $\overline{FLAG}$ pin			400	mV
$\overline{FLAG}$ Leakage Current	$FLAG_{leak}$	$\overline{FLAG}$ level = 5 V		5.0		nA
$\overline{EN}$ Voltage High	V_{ih}	V_{in} from 3.3 V to 5.25 V	1.2			V
$\overline{EN}$ Voltage Low	V_{ol}	V_{in} from 3.3 V to 5.25 V			0.4	V
$\overline{EN}$ Leakage Current	EN_{leak}	EN = 5.5 V or GND		170		nA
TIMINGS						
Start Up Delay	t_{on}	From V_{in} > UVLO to V_{out} = 0.8xV_{in}, See Fig 3 & 9		4.0	15	ms
$\overline{FLAG}$ going up Delay	t_{start}	From V_{in} > UVLO to $\overline{FLAG}$ = 1.2 V, See Fig 3 & 10		3.0		μs
Output Turn Off Time	t_{off}	From V_{in} > OVLO to V_{out} ≤ 0.3 V, See Fig 4 & 11 V_{in} increasing from normal operation to >OVLO at 1V/μs. No output capacitor.		0.8	1.5	μs
Alert Delay	t_{stop}	From V_{in} > OVLO to $\overline{FLAG}$ ≤ 0.4 V, See Fig 4 & 12 V_{in} increasing from normal operation to >OVLO at 1V/μs		1.0	2.0	μs
Disable Time	t_{dis}	From $\overline{EN}$ 0.4 to 1.2V to V_{out} ≤ 0.3V, See Fig 5 & 13 V_{in} = 4.75 V. No output capacitor.		2.0		μs
Thermal Shutdown Temperature	T_{sd}			150		°C
Thermal Shutdown Hysteresis	T_{sdhyst}			30		°C

NOTE: Thermal Shutdown parameter has been fully characterized and guaranteed by design.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted, all parameters apply to both FET_{SW} and FET_{REG})

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(Br)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(Br)DSS}/T_J$				−15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −16 V	T_J = 25°C			−1.0	μA
			T_J = 85°C			−5.0	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.45		−1.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				2.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(ON)}$	V_{GS} = −4.5 V, I_D = −1.0 A			64	80	mΩ
		V_{GS} = −4.5 V, I_D = −0.6 A			62	80	
Forward Transconductance	g_{FS}	V_{DS} = −10 V, I_D = −2.9 A			7.0		S
CHARGES, CAPACITANCES, AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −16 V			750		pF
Output Capacitance	C_{OSS}				100		
Reverse Transfer Capacitance	C_{RSS}				45		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −16 V, I_D = −2.6 A			7.6	8.6	nC
Gate−to−Source Charge	Q_{GS}				1.3		
Gate−to−Drain Charge	Q_{GD}				2.6		
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −16 V, I_D = −2.6 A, R_G = 2.0 Ω			5.5		ns
Rise Time	t_r				12		
Turn−Off Delay Time	$t_{d(OFF)}$				32		
Fall Time	t_f				23		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −1.1 A			−0.8	−1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 1.0 A			20		ns
Charge Time	ta				15		
Discharge Time	tb				5		
Reverse Recovery Charge	Q_{RR}				0.01		μC

2. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2%
3. Switching characteristics are independent of operating junction temperatures

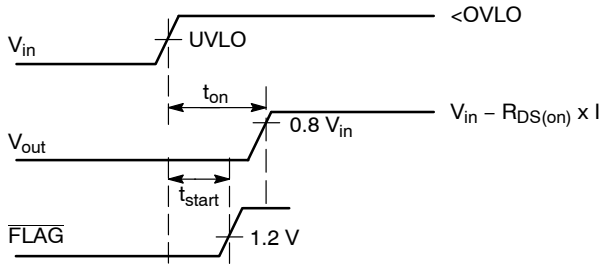


Figure 3. Start Up Sequence

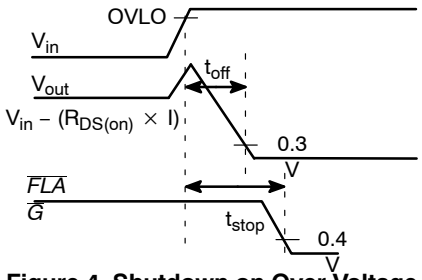


Figure 4. Shutdown on Over Voltage Detection

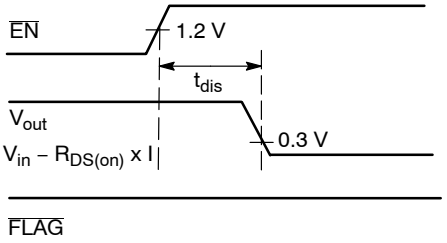


Figure 5. Disable on $\overline{EN}$ = 1

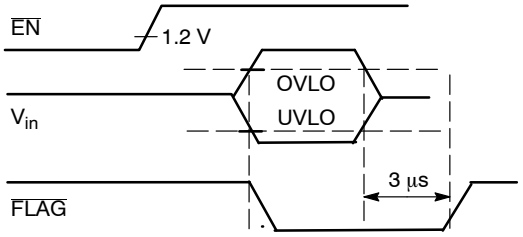


Figure 6. $\overline{FLAG}$ Response with $\overline{EN}$ = 1

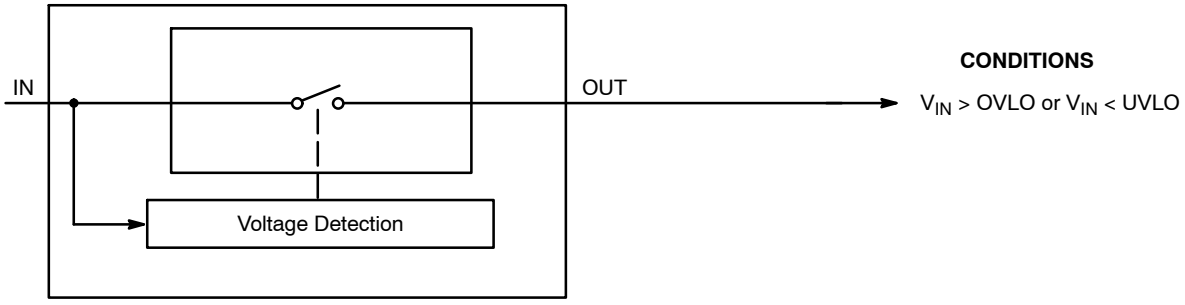


Figure 7.

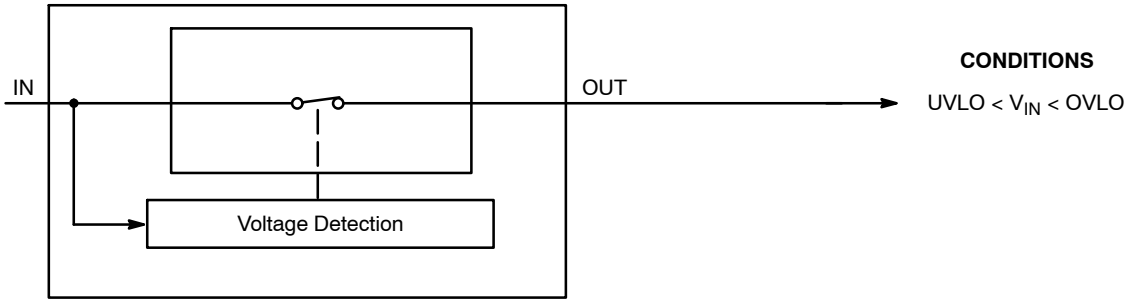


Figure 8.

TYPICAL OPERATING CHARACTERISTICS

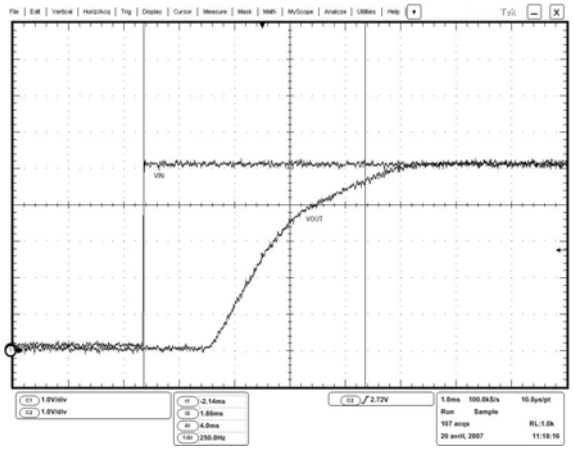


Figure 9. Startup
V_{in} = Ch1, V_{out} = Ch3

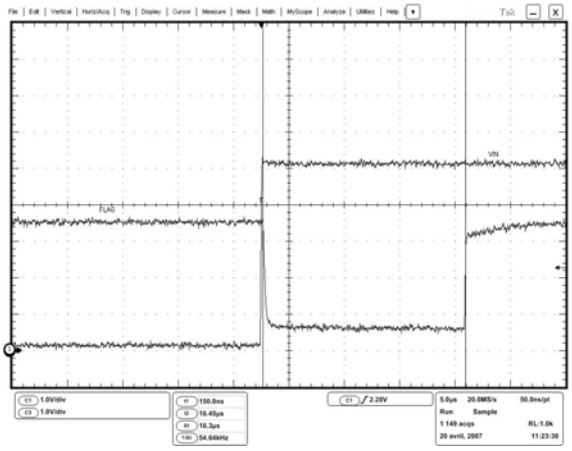


Figure 10. FLAG Going Up Delay
V_{out} = Ch3, FLAG = Ch2

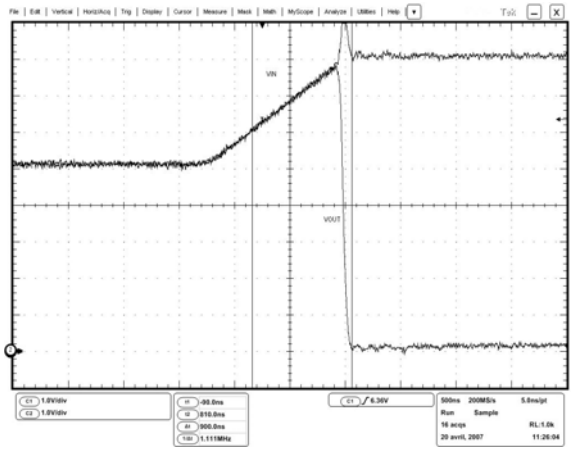


Figure 11. Output Turn Off Time
V_{in} = Ch1, V_{out} = Ch2

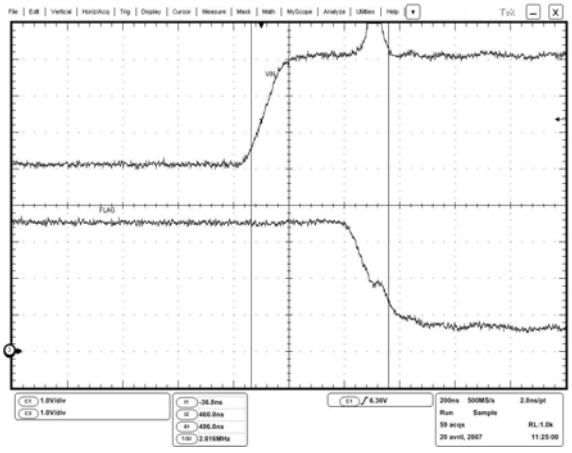


Figure 12. Alert Delay
V_{out} = Ch1, FLAG = Ch3

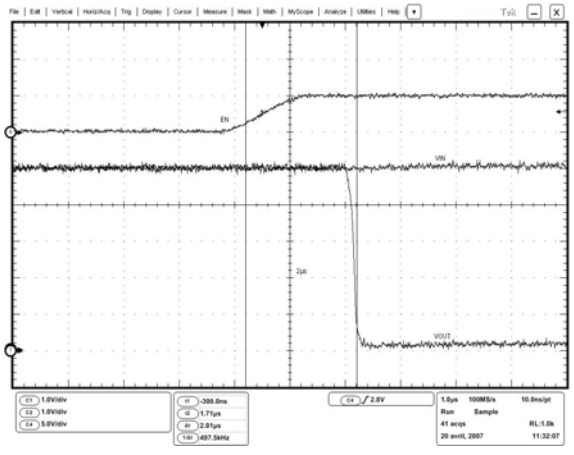


Figure 13. Disable Time
EN = Ch1, V_{out} = Ch2, FLAG = Ch3

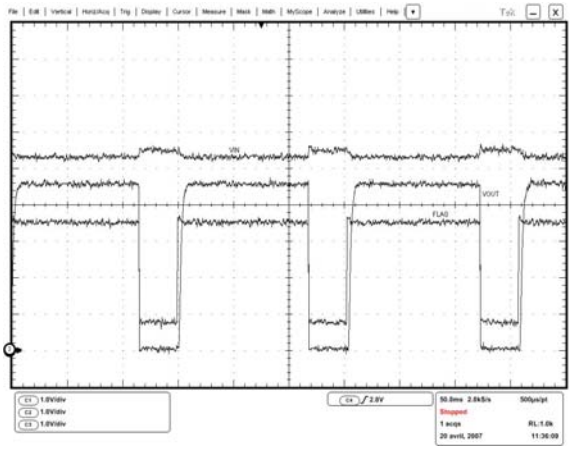


Figure 14. Thermal Shutdown
V_{in} = Ch1, V_{out} = Ch2, FLAG = Ch3

TYPICAL OPERATING CHARACTERISTICS

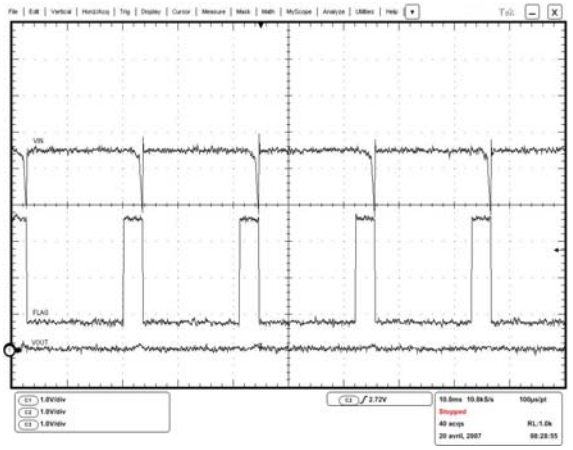


Figure 15. Direct Output Short Circuit

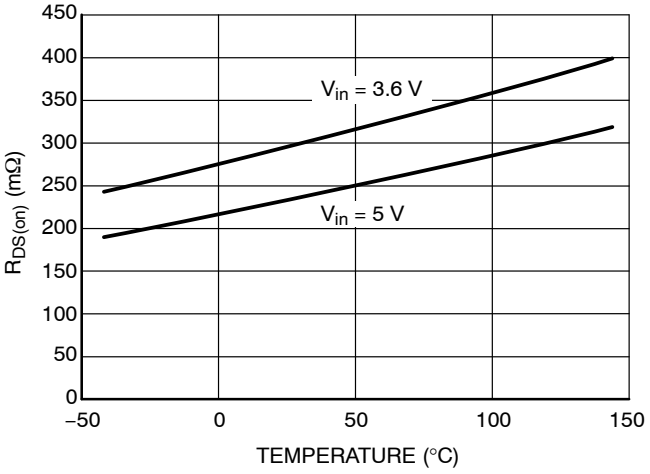


Figure 16. $R_{DS(on)}$ vs. Temperature (Load = 500 mA)

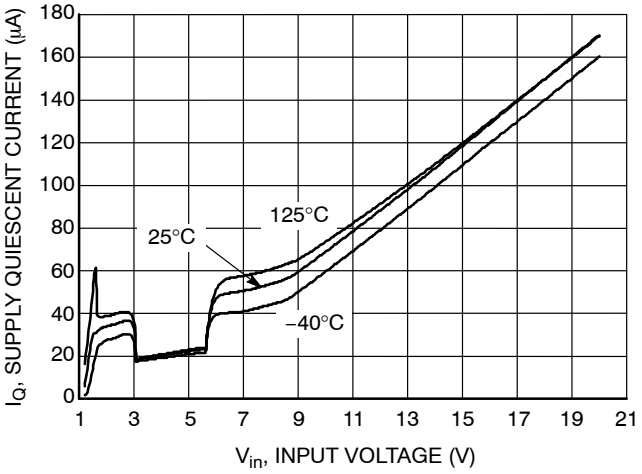


Figure 17. Supply Quiescent Current vs. V_{in}

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

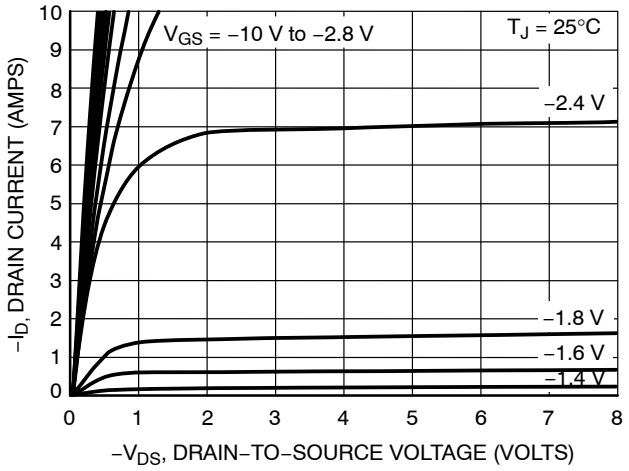


Figure 18. On−Region Characteristics

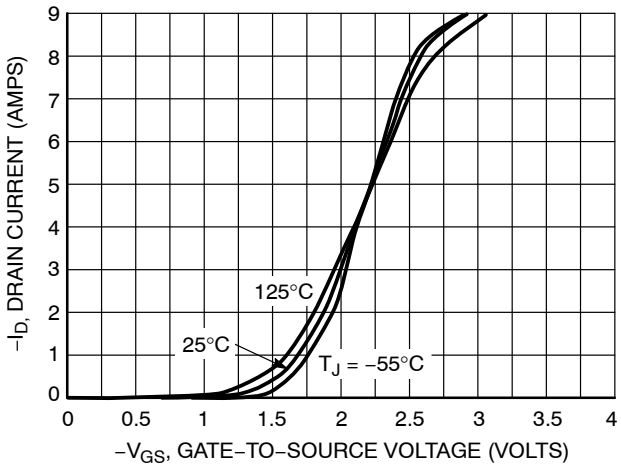


Figure 19. Transfer Characteristics

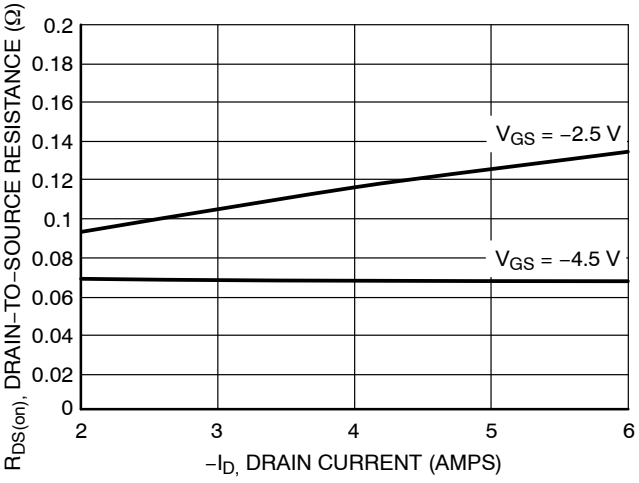


Figure 20. On−Resistance vs. Drain Current and Gate Voltage

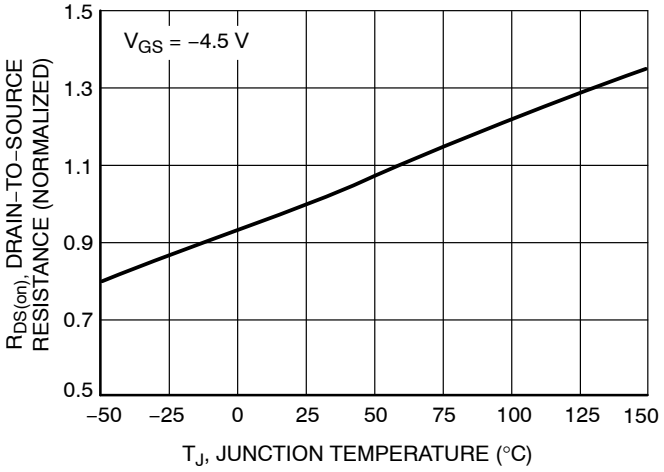


Figure 21. On−Resistance Variation with Temperature

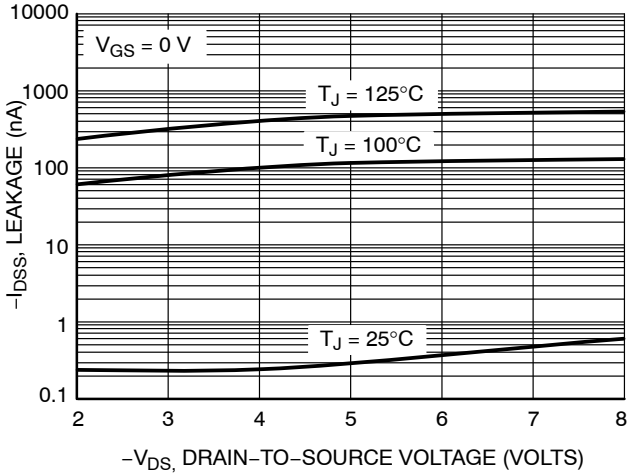


Figure 22. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

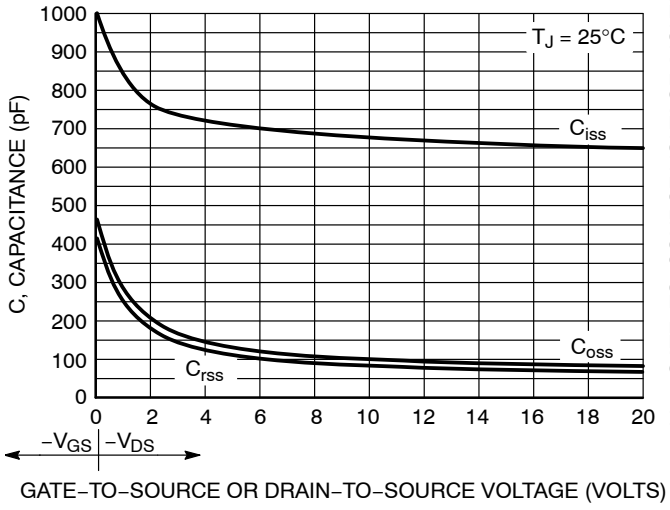


Figure 23. Capacitance Variation

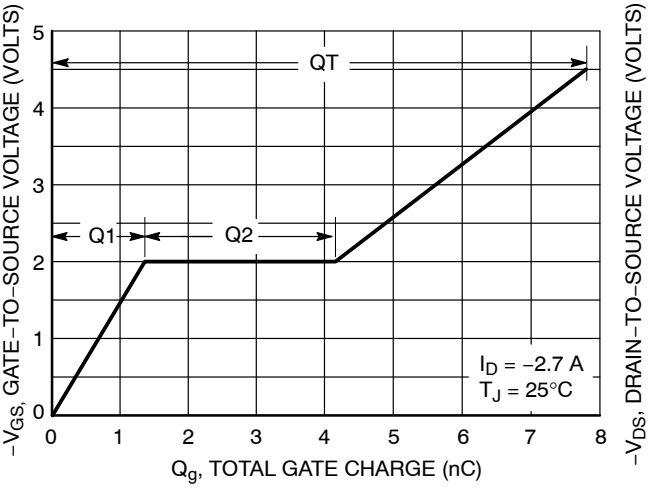


Figure 24. Gate−to−Source and Drain−to−Source Voltage vs. Total Gate Charge

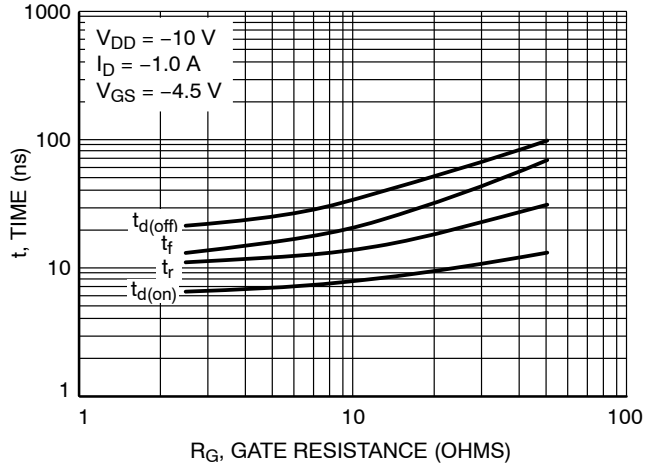


Figure 25. Resistive Switching Time Variation vs. Gate Resistance

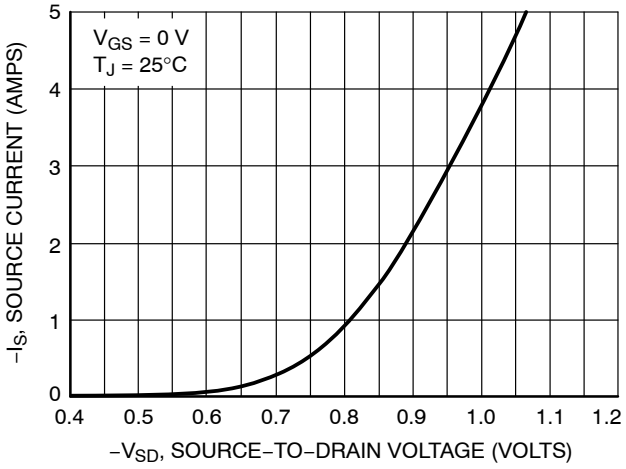


Figure 26. Diode Forward Voltage vs. Current

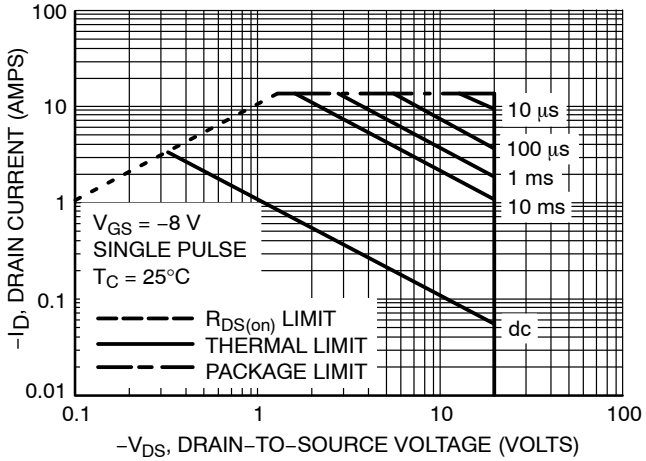


Figure 27. Maximum Rated Forward Biased Safe Operating Area

Operational Description

The NUS6160 provides overvoltage protection for positive voltages up to 20 V. A P−Channel FET protects the load connected on the V_{out} pin, against positive overvoltage conditions. The Output follows the V_{BUS} level until OVLO threshold is reached.

Undervoltage Lockout (UVLO)

To ensure proper operation under all conditions, the device has a built−in undervoltage lock out (UVLO) circuit. As the input ramps from 0 V, the output remains disconnected from input until the V_{in} voltage is above 3.2 V nominal. The FLAG output is pulled to low as long as V_{in} does not reach the UVLO threshold. This circuit incorporates hysteresis on the UVLO pin to provide noise immunity to transient condition.

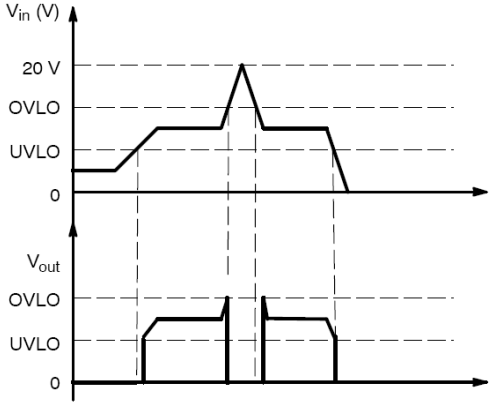


Figure 28. Output Characteristic vs. V_{in}

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} Pin from overvoltage, the device has a built−in overvoltage lock out (OVLO) circuit. During an overvoltage condition, the output remains disabled until the input voltage is reduced to below the OVLO hysteresis level. The FLAG output is tied to low until V_{in} is higher than OVLO. This circuit incorporates hysteresis on the OVLO pin to provide noise immunity from transient conditions.

FLAG Output

The NUS6160 provides a FLAG output, which alerts external systems that a fault has occurred. This pin goes low as soon as the OVLO threshold is exceeded. When V_{in} level recovers to its normal range the FLAG is set high.

The FLAG Pin is an open drain output, thus a pullup resistor (typically 1 MΩ − Minimum 10 kΩ) must be provided to $V_{battery}$.

EN Input

To enable normal operation, the EN pin shall be forced low or connected to ground. A high level on the pin disconnects the OUT Pin from IN Pin. EN does not override an OVLO or UVLO fault.

Internal PMOS FET

The NUS6160 includes an internal PMOS FET which connects the input to the output pin. This FET is turned off in the event of an overvoltage condition to protect the output from a positive overvoltage condition. The low $R_{ds(on)}$, during normal operation will minimize the voltage drop across the device. (See Figure 16).

ESD Tests

The NUS6160 meets the requirements of the IEC61000−4−2, level 4 (Input pin, 1 μF mounted on board). For the air discharge condition, V_{in} is protected up to ±15 kV. In the contact condition, V_{in} is protected up to ±8 kV ESD. Please refer to Figure 29 to see the IEC 61000−4−2 electrostatic discharge waveform.

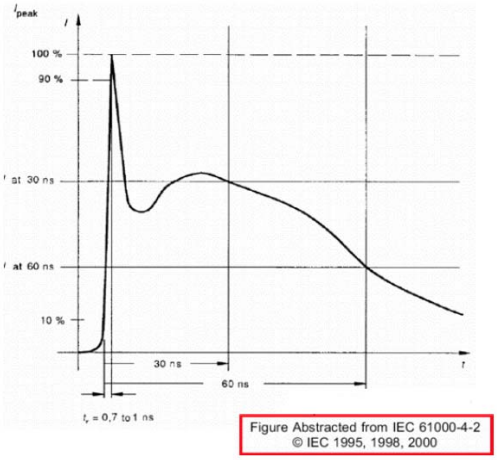


Figure 29. IEC 61000−4−2 Curve

Thermal Impedance

Due to cross heating of the three dice in the package, the equivalent thetas are given for this device rather than the individual thetas. To calculate the junction temperatures of a single die, the total power must be used. For example, given the following parameters, the die temperatures will be as shown:

I_{dc} = 500 mA
$R_{DS(on)}$ OVP = 305 mΩ
$R_{DS(on)}$ FETsw = 72 mΩ
FET_{reg} has a 1.0 V Drop
Board copper area = 161 mm^2

Calculate the individual power dissipations:
$P_{OVP} = (0.50\ A)^2 \times .305\ \Omega = 0.076$ W
$P_{SW} = (0.50\ A)^2 \times .072\ \Omega = 0.018$ W
$P_{REG} = 0.50\ A \times 1.0\ V = 0.50$ W
$P_{TOT} = 0.076 + 0.018 + 0.50 = 0.594$ W

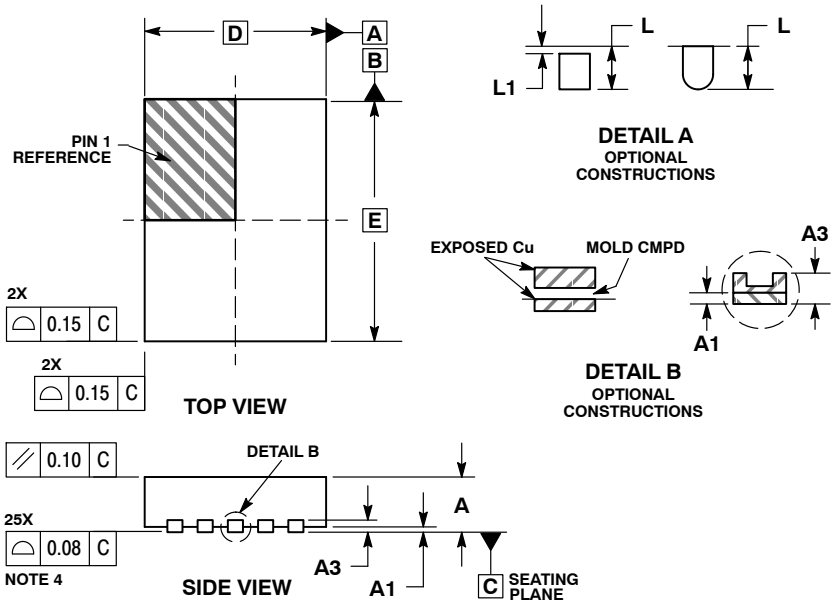
From the Maximum ratings table for thetas, 161 mm^2 and 1 V drop across FET_{REG}:

OVP FET	53°C/W
FET_{SW}	49°C/W
FET_{REG}	92°C/W

The die temperature rises above ambient are:
$T_{OVP} = 53°C/W \times 0.594\ W = 32°C$
$T_{SW} = 49°C/W \times 0.594\ W = 29°C$
$T_{REG} = 92°C/W \times 0.594\ W = 55°C$

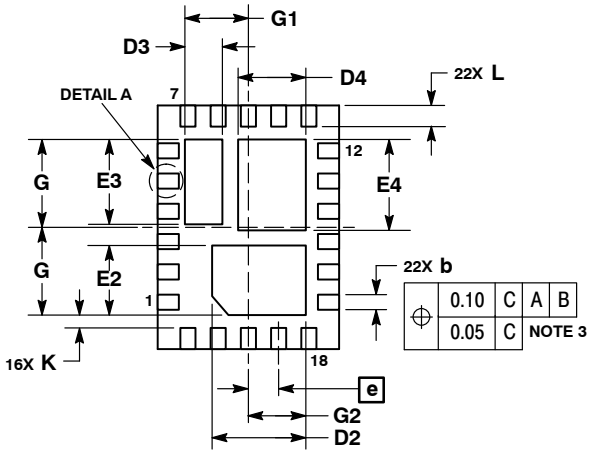
PACKAGE DIMENSIONS

QFN22, 3x4, 0.5P
CASE 485AT−01
ISSUE B

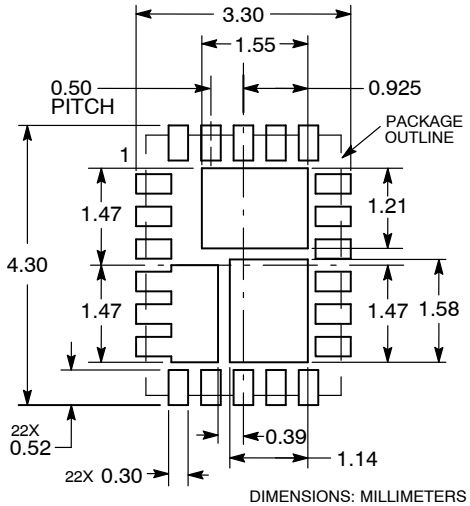


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.025	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		3.00 BSC	
D2	1.45	1.50	1.55
D3	0.52	0.57	0.62
D4	1.02	1.07	1.12
E		4.00 BSC	
E2	1.05	1.10	1.15
E3	1.30	1.35	1.40
E4	1.40	1.45	1.50
e		0.50 BSC	
K	0.25	---	---
L	0.30	0.325	0.35
L1	---	---	0.15
G	1.35	1.40	1.50
G1	0.95	1.05	1.15
G2	0.855	0.885	0.915



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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