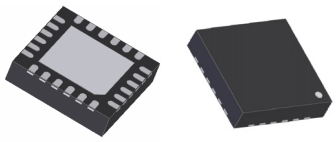
Document Number: MC34712
Rev. 8.0, 8/2016

3.0 A 1.0 MHz fully integrated DDR switch-mode power supply

34712

SWITCH-MODE POWER SUPPLY



EP SUFFIX
98ARL10577D
24-PIN QFN

The SMARTMOS 34712 is a highly integrated, space efficient, low cost, single synchronous buck switching regulator with integrated N-channel power MOSFETs. It is a high performance point-of-load (PoL) power supply with the ability to track an external reference voltage.

Its high efficient 3.0 A sink and source capability combined with its voltage tracking/sequencing ability and tight output regulation, makes it ideal to provide the termination voltage (V_{TT}) for modern data buses such as Double-Data-Rate (DDR) memory buses, including but not limited to DDR, DDR2, DDR3, and DDR4 memories. It also provides a buffered output reference voltage (V_{REF}) to the memory chipset

The 34712 offers the designer the flexibility of many control, supervisory, and protection functions to allow for easy implementation of complex designs. It is housed in a Pb-free, thermally enhanced, and space efficient 24 pin exposed pad QFN.

Features

- 50 mΩ integrated N-channel power MOSFETs
- Input voltage operating range from 3.0 V to 6.0 V
- ±1% Accurate output voltage, ranging from 0.6 V to 1.35 V
- ±1% Accurate buffered reference output voltage
- Programmable switching frequency range from 200 kHz to 1.0 MHz with a default of 1.0 MHz
- Overcurrent limit and short-circuit protection
- Thermal shutdown
- Output overvoltage and undervoltage detection
- Active low power-good output signal
- Active low standby and shutdown inputs

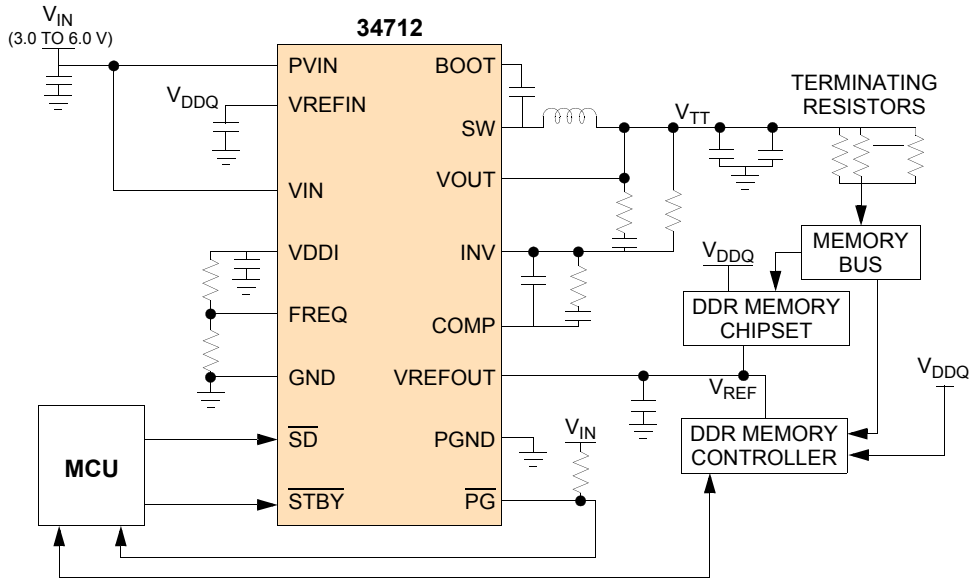


Figure 1. 34712 simplified application diagram

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1 Orderable parts

Table 1. Orderable part variations

Part Number	Temperature (T_A)	Package
MC34712EP [(1)]	-40 °C to 85 °C	24 QFN

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

2 Internal block diagram

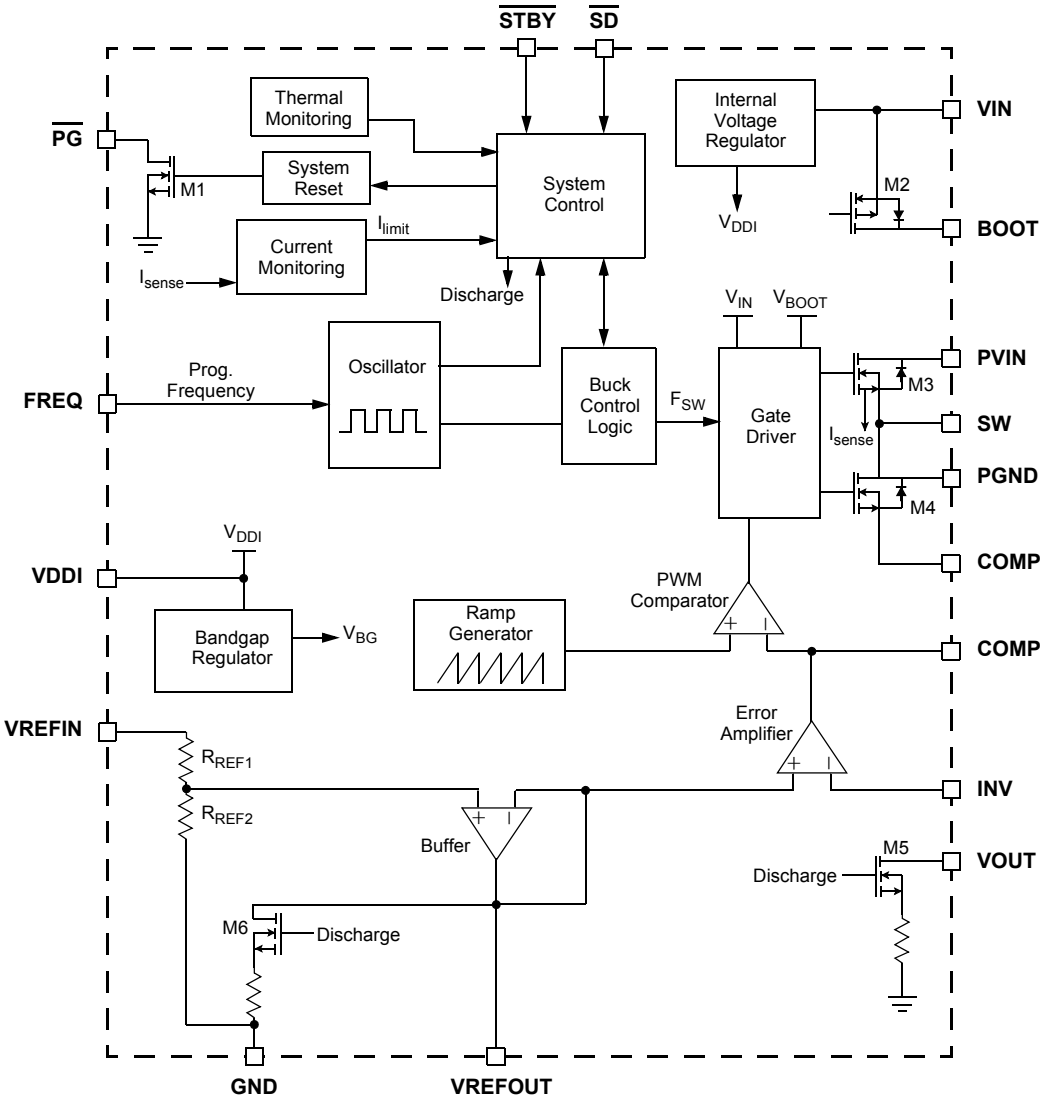


Figure 2. 34712 Simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

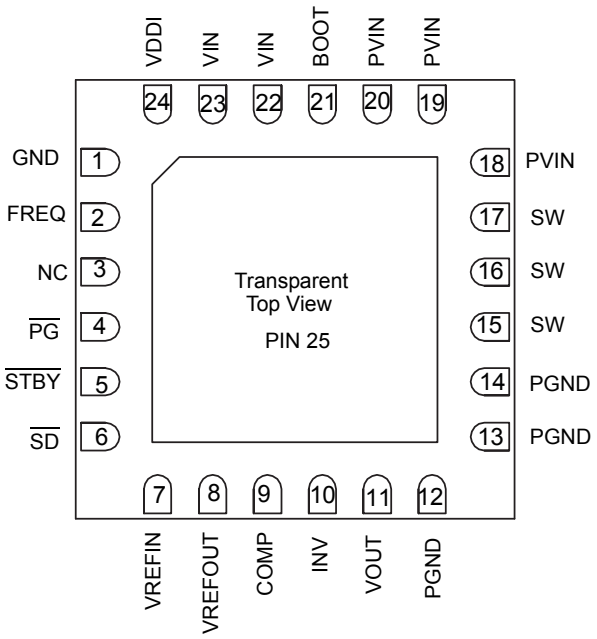


Figure 3. 34712 pin connections

3.2 Pin definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 12.

Table 2. 34712 Pin definitions

Pin number	Pin name	Pin function	Formal name	Definition
1	GND	Ground	Signal Ground	Analog signal ground of IC
2	FREQ	Passive	Frequency Adjustment	Buck converter switching frequency adjustment pin
3	NC	None	No Connect	No internal connections to this pin
4	PG	Output	Power Good	Active-low (open drain) power-good status reporting pin
5	STBY	Input	Standby	Standby mode input control pin
6	SD	Input	Shutdown	Shutdown mode input control pin
7	VREFIN	Input	Voltage Tracking Reference Input	Voltage tracking reference voltage input
8	VREFOUT	Output	Reference Voltage Output	Buffered output equal to 1/2 of voltage-tracking reference
9	COMP	Passive	Compensation	Buck converter external compensation network pin
10	INV	Input	Error Amplifier Inverting Input	Buck converter error amplifier inverting input pin
11	VOUT	Output	Output Voltage Discharge FET	Discharge FET drain connection (connect to buck converter output capacitors)
12,13,14	PGND	Ground	Power Ground	Ground return for buck converter and discharge FET

Table 2. 34712 Pin definitions (continued)

Pin number	Pin name	Pin function	Formal name	Definition
15,16,17	SW	Output	Switching Node	Buck converter power switching node
18,19,20	PVIN	Supply	Power-circuit Supply Input	Buck converter main supply voltage input
21	BOOT	Passive	Bootstrap	Bootstrap switching node (connect to bootstrap capacitor)
22,23	VIN	Supply	Logic-circuit Supply Input	Logic circuits supply voltage input
24	VDDI	Passive	Internal Voltage Regulator	Internal V_{DD} regulator (connect filter capacitor to this pin)
25	GND	Ground	Thermal Pad	Thermal pad for heat transfer. Connect the thermal pad to the analog ground and the ground plane for heat sinking.

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
V_{IN}	Input Supply Voltage (VIN) Pin	-0.3 to 7.0	V	
PV_{IN}	High-side MOSFET Drain Voltage (PVIN) Pin	-0.3 to 7.0	V	
V_{SW}	Switching Node (SW) Pin	-0.3 to 7.0	V	
V_{BOOT} - V_{SW}	BOOT Pin (Referenced to SW Pin)	-0.3 to 7.0	V	
-	PG, VOUT, SD, and STBY Pins	-0.3 to 7.0	V	
-	VDDI, FREQ, INV, COMP, VREFIN, and VREFOUT Pins	-0.3 to 3.0	V	
I_{OUT}	Continuous Output Current	±3.0	A	(2)
V_{ESD1} V_{ESD2} V_{ESD3}	ESD Voltage • Human Body Model • Machine Model (MM) • Device Charge Model (CDM)	 ±2000 ±200 ±750	V	(3)
Thermal ratings				
T_A	Operating Ambient Temperature	-40 to 85	°C	(4)
T_{STG}	Storage Temperature	-65 to +150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	Note 6	°C	(5),(6)
$T_{J(MAX)}$	Maximum Junction Temperature	+150	°C	
P_D	Power Dissipation (T_A = 85 °C)	2.9	W	(7)

Notes

2. Continuous output current capability so long as T_J is $\leq T_{J(MAX)}$.
3. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
4. The limiting factor is junction temperature, taking into account power dissipation, thermal resistance, and heatsinking.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
7. Maximum power dissipation at indicated ambient temperature.

Table 3. Maximum ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal resistance [8]				
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Single-layer Board (1s)	139	°C/W	(9)
$R_{\theta JMA}$	Thermal Resistance, Junction to Ambient, Four-layer Board (2s2p)	43	°C/W	(10)
$R_{\theta JB}$	Thermal Resistance, Junction to Board	22	°C/W	(11)

Notes

8. The PVIN, SW, and GND pins comprise the main heat conduction paths.
9. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
10. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal. There are no thermal vias connecting the package to the two planes in the board.
11. Thermal resistance between the device and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40 °C ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
IC input supply voltage (VIN)						
V_{IN}	Input Supply Voltage Operating Range	3.0	-	6.0	V	
I_{IN}	Input DC Supply Current • Normal Mode: $\overline{SD}$ = 1 & $\overline{STBY}$ = 1, Unloaded Outputs	-	-	25	mA	(12)
I_{INQ}	Input DC Supply Current • Standby Mode, $\overline{SD}$ = 1 & $\overline{STBY}$ = 0	-	-	15	mA	(12)
I_{INOFF}	Input DC Supply Current • Shutdown Mode, $\overline{SD}$ = 0 & $\overline{STBY}$ = X	-	-	100	µA	(12)
Internal supply voltage output (VDDI)						
V_{DDI}	Internal Supply Voltage Range	2.35	2.5	2.65	V	
Buck converter (PVIN, SW, GND, BOOT, INV, COMP)						
P_{VIN}	High-side MOSFET Drain Voltage Range	2.5	-	6.0	V	
V_{OUT}	Output Voltage Adjustment Range	0.6	-	1.35	V	(13), (17)
-	Output Voltage Accuracy	-1.0	-	1.0	%	(13), (14), (15)
REG_{LN}	Line Regulation • Normal Operation, V_{IN} = 3.0 to 6.0 V, I_{OUT} = ±3.0 A	-1.0	-	1.0	%	(13)
REG_{LD}	Load Regulation • Normal Operation, I_{OUT} = -3.0 to 3.0 A	-1.0	-	1.0	%	(13)
V_{REF}	Error Amplifier Common Mode Voltage Range	0.0	-	1.35	V	(13), (16)
V_{UVR}	Output Undervoltage Threshold	-8.0	-	-1.5	%	
V_{OVR}	Output Overvoltage Threshold	1.5	-	8.0	%	
I_{OUT}	Continuous Output Current	-3.0	-	3.0	A	
I_{LIM}	Overcurrent Limit, Sinking and Sourcing	-	4.0	-	A	
I_{SHORT}	Short-circuit Current Limit • (Sourcing and Sinking)	-	6.5	-	A	
$R_{DS(on)HS}$	High-side N-CH Power MOSFET (M3) $R_{DS(ON)}$ • I_{OUT} = 1.0 A, V_{BOOT} - V_{SW} = 3.3 V	10	-	50	mΩ	(13)
$R_{DS(on)LS}$	Low-side N-CH Power MOSFET (M4) $R_{DS(ON)}$ • I_{OUT} = 1.0 A, V_{IN} = 3.3 V	10	-	50	mΩ	(13)

Notes

12. See section Modes of operation, page 16 has a detailed description of the different operating modes of the 34712
13. Design information only, this parameter is not production tested.
14. ±1% is assured at room temperature.
15. Overall output accuracy is directly affected by the accuracy of the external feedback network, 1% feedback resistors are recommended.
16. The 1% output voltage regulation is only guaranteed for a common mode voltage range greater than or equal to 0.6 V at room temperature.
17. If a V_{OUT} =0.6 V is desired, make sure PV_{IN} is kept below 3.6 V and the Switching Frequency FSW is lower than 500 kHz to allow enough room for output regulation

Table 4. Static electrical characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40 °C ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$R_{DS(on)M2}$	M2 $R_{DS(on)}$ • (V_{IN} = 3.3 V, M2 is on)	1.5	-	4.0	Ω	
I_{SW}	SW Leakage Current (Standby and Shutdown modes)	-10	-	10	μA	
I_{PVIN}	PVIN Pin Leakage Current • (Standby and Shutdown Modes)	-10	-	10	μA	
I_{INV}	INV Pin Leakage Current	-1.0	-	1.0	μA	
A_{EA}	Error Amplifier DC Gain	-	150	-	dB	(18)
$UGBW_{EA}$	Error Amplifier Unit Gain Bandwidth	-	3.0	-	MHz	(18)
SR_{EA}	Error Amplifier Slew Rate	-	7.0	-	V/μs	(18)
$OFFSET_{EA}$	Error Amplifier Input Offset	-3.0	0.0	3.0	mV	(18)
T_{SDFET}	Thermal Shutdown Threshold	-	170	-	°C	(18)
$T_{SDHYFET}$	Thermal Shutdown Hysteresis	-	25	-	°C	(18)
Oscillator (FREQ)						
V_{FREQ}	Oscillator Frequency Adjusting Reference Voltage Range	0.0	-	V_{DDI}	V	
Tracking (VREFIN, VREFOUT, VOUT)						
V_{REFIN}	VREFIN External Reference Voltage Range	0.0	-	2.7	V	(18)
V_{REFOUT}	VREFOUT Buffered Reference Voltage Range	0.0	-	1.35	V	
-	VREFOUT Buffered Reference Voltage Accuracy	-1.0	-	1.0	%	(19)
I_{REFOUT}	VREFOUT Buffered Reference Voltage Current Capability	0.0	-	8.0	mA	
$I_{REFOUTLIM}$	VREFOUT Buffered Reference Voltage Overcurrent Limit	-	11	-	mA	
$R_{TDR(M6)}$	VREFOUT Total Discharge Resistance	-	50	-	Ω	(18)
$R_{TDR(M5)}$	VOUT Total Discharge Resistance	-	50	-	Ω	(18)
$I_{VOUTLKG}$	VOUT Pin Leakage Current • (Standby Mode, V_{OUT} = 3.6 V)	-1.0	-	1.0	μA	
Control and supervisory ($\overline{STBY}$, $\overline{SD}$, $\overline{PG}$)						
V_{STBYHI}	$\overline{STBY}$ High Level Input Voltage	2.0	-	-	V	
V_{STBYLO}	$\overline{STBY}$ Low Level Input Voltage	-	-	0.4	V	
R_{STBYUP}	$\overline{STBY}$ Pin Internal Pull-up Resistor	1.0	-	2.0	MΩ	
V_{SDHI}	$\overline{SD}$ High Level Input Voltage	2.0	-	-	V	
V_{SDLO}	$\overline{SD}$ Low Level Input Voltage	-	-	0.4	V	
R_{SDUP}	$\overline{SD}$ Pin Internal Pull-up Resistor	1.0	-	2.0	MΩ	
V_{PGLO}	$\overline{PG}$ Low Level Output Voltage • (I_{PG} = 3.0 mA)	-	-	0.4	V	
I_{PGLKG}	$\overline{PG}$ Pin Leakage Current • (M1 is off, Pulled up to VIN)	-1.0	-	1.0	μA	

Notes

18. Design information only, this parameter is not production tested.
19. The 1 % accuracy is only guaranteed for V_{REFOUT} greater than or equal to 0.6 V at room temperature.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40 °C ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Buck converter (PVIN, SW, GND, BOOT)						
t_{RISE}	Switching Node (SW) Rise Time • (P_{VIN} = 3.3 V, I_{OUT} = ±3.0 A)	-	14	-	ns	(21)
t_{FALL}	Switching Node (SW) Fall Time • (P_{VIN} = 3.3 V, I_{OUT} = ±3.0 A)	-	20	-	ns	(21)
t_{OFFMIN}	Minimum OFF Time	-	150	-	ns	
t_{ONMIN}	Minimum ON Time	-	180	-	ns	
t_{SS}	Soft Start Duration • (Normal Mode)	1.3	-	2.6	ms	
t_{LIM}	Overcurrent Limit Timer	-	10	-	ms	
$t_{TIMEOUT}$	Overcurrent Limit Retry Timeout Period	80	-	120	ms	
t_{FILTER}	Output Undervoltage/Overvoltage Filter Delay Timer	5.0	-	25	µs	
Oscillator (FREQ)						
F_{SW}	Oscillator Default Switching Frequency • (FREQ = GND)	-	1.0	-	MHz	(20)
F_{SW}	Oscillator Switching Frequency Range	200	-	1000	kHz	
Control and supervisory ($\overline{\text{STBY}}$, $\overline{\text{SD}}$, $\overline{\text{PG}}$)						
$t_{PGRESET}$	$\overline{\text{PG}}$ Reset Delay	8.0	-	12	ms	
$t_{TIMEOUT}$	Thermal Shutdown Retry Timeout Period	80	-	120	ms	(21)

Notes

20. Oscillator Frequency tolerance is ±10%.
21. Design information only, this parameter is not production tested.

5 Functional description

5.1 Introduction

In modern microprocessor/memory applications, address commands and control lines require system level termination to a voltage (V_{TT}) equal to 1/2 the memory supply voltage (V_{DDQ}). Having the termination voltage at midpoint, the power supply insures symmetry for switching times. Also, a reference voltage (V_{REF}) that is free of any noise or voltage variations is needed for the DDR SDRAM input receiver, V_{REF} is also equal to 1/2 V_{DDQ}. Varying the V_{REF} voltage effects the setup and hold time of the memory. To comply with DDR requirements and to obtain best performance, V_{TT} and V_{REF} need to be tightly regulated to track 1/2 V_{DDQ} across voltage, temperature, and noise margins. V_{TT} should track any variations in the DC V_{REF} value (V_{TT} = V_{REF} +/- 40mV), (See Figure 4) for a DDR system level diagram.

The 34712 supplies the V_{TT} and a buffered V_{REF} output. To ensure compliance with DDR specifications, the V_{DDQ} line is applied to the VREFIN pin and divided by 2 internally through a precision resistor divider. This internal voltage is then used as the reference voltage for the V_{TT} output. The same internal voltage is also buffered to give the V_{REF} voltage at the VREFOUT pin for the application to use without the need for an external resistor divider. The 34712 provides the tight voltage regulation and power sequencing/tracking required along with handling the DDR peak transient current requirements. Buffering the V_{REF} output helps its immunity against noise and load changes.

The 34712 utilizes a voltage mode synchronous buck switching converter topology with integrated low $R_{DS(ON)}$ (50 mΩ) N-channel power MOSFETs to provide a V_{TT} voltage with an accuracy of less than ±2.0%. It has a programmable switching frequency that allows for flexibility and optimization over the operating conditions and can operate at up to 1.0 MHz to significantly reduce the external components size and cost. The 34712 can sink and source up to 3.0 A of continuous current. It provides protection against output overcurrent, overvoltage, undervoltage, and overtemperature conditions. It also protects the system from short -circuit events. It incorporates a power-good output signal to alert the host when a fault occurs.

For boards that support the Suspend-To-RAM (S3) and the Suspend-To-Disk (S5) states, the 34712 offers the $\overline{\text{STBY}}$ and the $\overline{\text{SD}}$ pins respectively. Pulling any of these pins low, puts the IC in the corresponding state.

By integrating the control/supervisory circuitry along with the Power MOSFET switches for the buck converter into a space-efficient package, the 34712 offers a complete, small-size, cost-effective, and simple solution to satisfy the needs of DDR memory applications.

Besides DDR memory termination, the 34712 can be used to supply termination for other active buses and graphics card memory. It can be used in Netcom/Telecom applications like servers. It can also be used in desktop motherboards, game consoles, set top boxes, and high end high definition TVs.

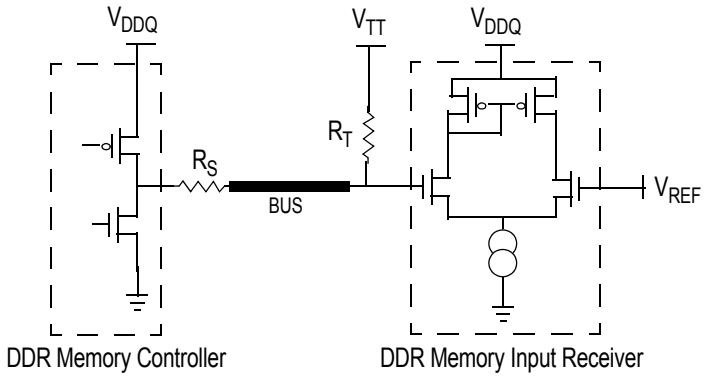


Figure 4. DDR system level diagram

5.2 Functional pin description

5.2.1 Reference voltage input (VREFIN)

The 34712 tracks 1/2 the voltage applied at this pin.

5.2.2 Reference voltage output (VREFOUT)

This is a buffered reference voltage output that is equal to 1/2 V_{REFIN}. It has a 10 mA current drive capability. This output is used as the V_{REF} voltage rail and should be filtered against any noise. Connect a 0.1 µF, 6.0 V low ESR ceramic filter capacitor between this pin and the GND pin and between this pin and V_{DDQ} rail. V_{REFOUT} is also used as the reference voltage for the buck converter error amplifier.

5.2.3 Frequency adjustment input (FREQ)

The buck converter switching frequency can be adjusted by connecting this pin to an external resistor divider between VDDI and GND pins. The default switching frequency (FREQ pin connected to ground, GND) is set at 1.0 MHz. Select the switching frequency based on the PV_{IN} to V_{TT} ratio. Refer to the Switching frequency selection section.

5.2.4 Signal ground (GND)

Analog ground of the IC. Internal analog signals are referenced to this pin voltage.

5.2.5 Internal supply voltage output (VDDI)

This is the output of the internal bias voltage regulator. Connect a 1.0 µF, 6.0 V low ESR ceramic filter capacitor between this pin and the GND pin. Filtering any spikes on this output is essential to the internal circuitry stable operation.

5.2.6 Output voltage discharge path (VOUT)

Output voltage of the Buck Converter is connected to this pin. it only serves as the output discharge path once the $\overline{SD}$ signal is asserted.

5.2.7 Error amplifier inverting input (inv)

Buck converter error amplifier inverting input. Connect the V_{TT} voltage directly to this pin.

5.2.8 Compensation input (COMP)

Buck converter external compensation network connects to this pin. Use a type III compensation network.

5.2.9 Input supply voltage (VIN)

IC power supply input voltage. Input filtering is required for the device to operate properly.

5.2.10 Power ground (PGND)

Buck converter and discharge MOSFETs power ground. It is the source of the buck converter low-side power MOSFET.

5.2.11 Switching node (SW)

Buck converter switching node. This pin is connected to the output inductor.

5.2.12 Power input voltage (PVIN)

Buck converter power input voltage. This is the drain of the buck converter high-side power MOSFET.

5.2.13 Bootstrap input (BOOT)

Bootstrap capacitor input pin. Connect a capacitor (as discussed on page 24) between this pin and the SW pin to enhance the gate of the high-side Power MOSFET during switching.

5.2.14 Shutdown input ($\overline{SD}$)

If this pin is tied to the GND pin, the device is in Shutdown mode. If left unconnected or tied to the VIN pin, the device is in Normal mode. The pin has an internal pull-up of 1.5 MΩ. This input accepts the S5 (Suspend-To-Disk) control signal.

5.2.15 Standby input ($\overline{STBY}$)

If this pin is tied to the GND pin, the device is in Standby mode. If left unconnected or tied to the VIN pin, the device is in Normal mode. The pin has an internal pull-up of 1.5 MΩ. This input accepts the S3 (Suspend-To-RAM) control signal.

5.2.16 Power good output signal ($\overline{PG}$)

This is an active low open drain output that is used to report the status of the device to a host. This output activates after a successful power up sequence and stays active as long as the device is in normal operation and is not experiencing any faults. This output activates after a 10 ms delay and must be pulled up by an external resistor to a supply voltage (e.g.,V_{IN}.).

5.3 Functional internal block description

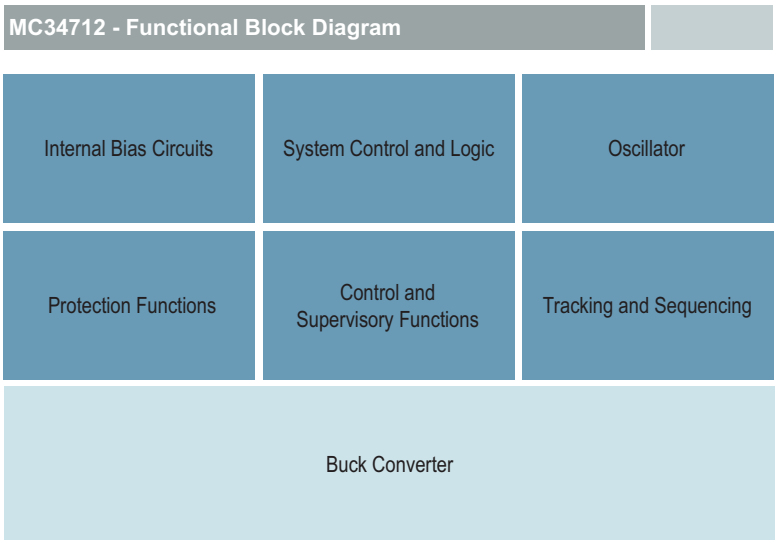


Figure 5. 34712 internal block diagram

5.3.1 Internal bias circuits

This block contains all circuits that provide the necessary supply voltages and bias currents for the internal circuitry. It consists of:

- Internal voltage supply regulator: This regulator supplies the V_{DDI} voltage that is used to drive the digital/analog internal circuits. It is equipped with a Power-On-Reset (POR) circuit that watches for the right regulation levels. External filtering is needed on the VDDI pin. This block turns off during the shutdown mode.
- Internal bandgap reference voltage: This supplies the reference voltage to some of the internal circuitry.
- Bias circuit: This block generates the bias currents necessary to run all of the blocks in the IC.

5.3.2 System control and logic

This block is the brain of the IC where the device processes data and reacts to it. Based on the status of the $\overline{\text{STBY}}$ and $\overline{\text{SD}}$ pins, the system control reacts accordingly and orders the device into the right status. It also takes inputs from all of the monitoring/protection circuits and initiates power up or power down commands. It communicates with the buck converter to manage the switching operation and protects it against any faults.

5.3.3 Oscillator

This block generates the clock cycles necessary to run the IC digital blocks. It also generates the buck converter switching frequency. The switching frequency has a default value of 1.0 MHz and can be programmed by connecting a resistor divider to the FREQ pin, between VDDI and GND pins (See Figure 1).

5.3.4 Protection functions

This block contains the following circuits:

- Overcurrent limit and short-circuit detection: This block monitors the output of the buck converter for overcurrent conditions and short-circuit events and alerts the system control for further command.
- Thermal limit detection: This block monitors the temperature of the device for overheating events. If the temperature rises above the thermal shutdown threshold, this block alerts the system control for further commands.
- Output overvoltage and undervoltage monitoring: This block monitors the buck converter output voltage to ensure it is within regulation boundaries. If not, this block alerts the system control for further commands.

5.3.5 Control and supervisory functions

This block is used to interface with an outside host. It contains the following circuits:

- Standby control input: An outside host can put the 34712 device into standby mode (S3 or Suspend-To-RAM mode) by sending a logic “0” to the $\overline{\text{STBY}}$ pin.
- Shutdown control input: An outside host can put the 34712 device into shutdown mode (S5 or Suspend-To-Disk mode) by sending a logic “0” to the $\overline{\text{SD}}$ pin.
- Power good output signal $\overline{\text{PG}}$: The 34712 can communicate to an external host that a fault has occurred by releasing the drive on the $\overline{\text{PG}}$ pin high, allowing the signal/pin to be pulled high by the external pull-up resistor.

5.3.6 Tracking and sequencing

This block allows the output of the 34712 to track 1/2 the voltage applied at the VREFIN pin. This allows the V_{REF} and V_{TT} voltages to track 1/2 V_{DDQ} and assures that none of them is higher than V_{DDQ} at any point during normal operating conditions. For power down during a shutdown (S5) mode, the 34712 uses internal discharge MOSFETs (M5 and M6 on Figure 2) to discharge V_{TT} and V_{REF} respectively. These discharge MOSFETs are only active during shutdown mode. Using this block along with controlling the $\overline{\text{SD}}$ and $\overline{\text{STBY}}$ pins can offer the user power sequencing capabilities by controlling when to turn the 34712 outputs on or off.

5.3.7 Buck converter

This block provides the main function of the 34712: DC to DC conversion from an un-regulated input voltage to a regulated output voltage used by the loads for reliable operation. The buck converter is a high-performance, fixed frequency (externally adjustable), synchronous buck PWM voltage-mode control. It drives integrated 50 mΩ N-channel power MOSFETs saving board space and enhancing efficiency. The switching regulator output voltage is adjustable with an accuracy of less than ±2.0% to meet DDR requirements. Its output has the ability to track 1/2 the voltage applied at the VREFIN pin. The regulator's voltage control loop is compensated using a type III compensation network, with external components to allow for optimizing the loop compensation, for a wide range of operating conditions. A typical Bootstrap circuit with an internal PMOS switch is used to provide the voltage necessary to properly enhance the high-side MOSFET gate.

The 34712 is designed to address DDR memory power supplies. The integrated converter has the ability to both sink and source up to 3.0 A of continuous current, making it suitable for bus termination power supplies.

6 Functional device operation

6.1 Operational modes

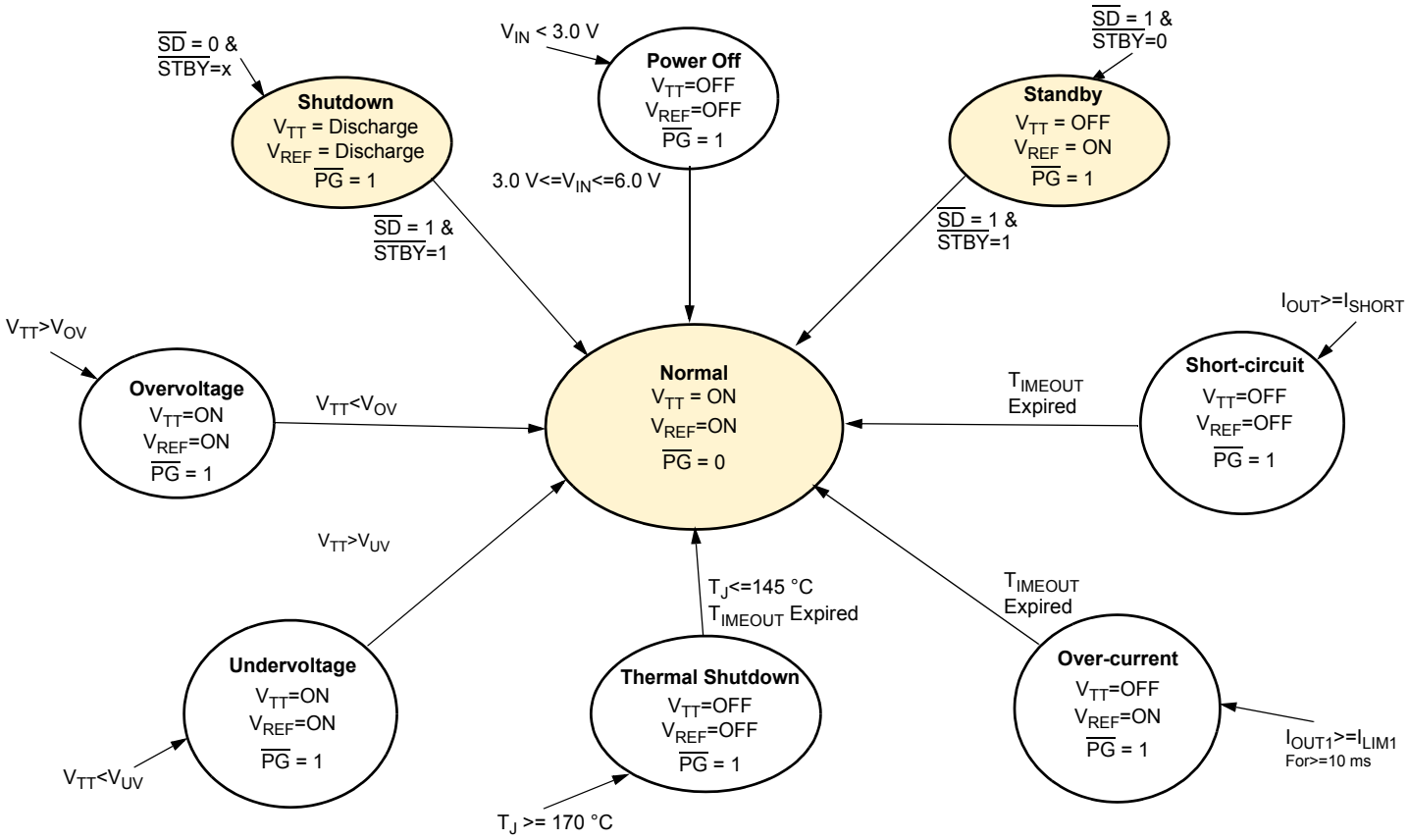


Figure 6. Operation modes diagram

6.1.1 Modes of operation

The 34712 has three primary modes of operation:

6.1.1.1 Normal mode

In normal mode, all functions and outputs are fully operational. To be in this mode, the V_{IN} needs to be within its operating range, both Shutdown and Standby inputs are high, and no faults are present. This mode consumes the most amount of power.

6.1.1.2 Standby mode

This mode is predominantly used in Desktop memory solutions where the DDR supply is desired to be ACPI compliant (Advanced Configuration and Power Interface). When this mode is activated by pulling the $\overline{STBY}$ pin low, V_{TT} is put in High Z state, I_{OUT} = 0 A, and V_{REF} stays active. This is the S3 state Suspend-To-Ram or Self Refresh mode and it is the lowest DRAM power state. In this mode, the DRAM preserves the data. While in this mode, the 34712 consumes less power than in the normal mode, because the buck converter and most of the internal blocks are disabled.

6.1.1.3 Shutdown mode

In this mode, activated by pulling the $\overline{SD}$ pin low, the chip is in a shutdown state and the outputs are all disabled and discharged. This is the S4/S5 power state or Suspend-To-Disk state, where the DRAM loses all of its data content (no power supplied to the DRAM). The reason to discharge the V_{TT} and V_{REF} lines is to ensure upon exiting, the Shutdown mode that V_{TT} and V_{REF} are lower than V_{DDQ}, otherwise V_{TT} can remain floating high, and be higher than V_{DDQ} upon powering up. In this mode, the 34712 consumes the least amount of power since almost all of the internal blocks are disabled.

6.1.2 Start-up sequence

When power is first applied, the 34712 checks the status of the $\overline{SD}$ and $\overline{STBY}$ pins. If the device is in a shutdown mode, no block powers up and the output does not attempt to ramp. If the device is in a standby mode, only the V_{DDI} internal supply voltage and the bias currents are established and no further activities occur. Once the $\overline{SD}$ and $\overline{STBY}$ pins are released to enable the device, the internal V_{DDI} POR signal is also released. The rest of the internal blocks is enabled and the buck converter switching frequency value is determined by reading the FREQ pin. A soft start cycle is then initiated to ramp up the output of the buck converter (V_{TT}). The buck converter error amplifier uses the voltage on the VREFOUT pin (V_{REF}) as its reference voltage. V_{REF} is equal to 1/2 V_{DDQ}, where V_{DDQ} is applied to the VREFIN pin. This way, the 34712 assures that V_{REF} and V_{TT} voltages track 1/2 V_{DDQ} to meet DDR requirements.

Soft start is used to prevent the output voltage from overshooting during startup. At initial startup, the output capacitor is at zero volts; V_{OUT} = 0 V. Therefore, the voltage across the inductor is PV_{IN} during the capacitor charge phase which creates a very sharp di/dt ramp. Allowing the inductor current to rise too high can result in a large difference between the charging current and the actual load current that can result in an undesired voltage spike once the capacitor is fully charged. The soft start is active each time the IC goes out of standby or shutdown mode, power is recycled, or after a fault retry.

To fully take advantage of soft starting, it is recommended not to enable the 34712 output before introducing VDDQ on the VREFIN pin. If this happens after a soft start cycle expires and the VREFIN voltage has a high dv/dt, the output naturally tracks it immediately and ramp up with a fast dv/dt itself and this defeats the purpose of soft starting. For reliable operation, it is best to have the VDDQ voltage available before enabling the output of the 34712.

After a successful start-up cycle where the device is enabled, no faults have occurred, and the output voltage has reached its regulation point, the 34712 pulls the power good output signal low after a 10 ms reset delay, to indicate to the host the device is in normal operation.

6.2 Protection and diagnostic features

The 34712 monitors the application for several fault conditions to protect the load from overstress. The reaction of the IC to these faults ranges from turning off the outputs to just alerting the host that something is wrong. In the following paragraphs, each fault condition is explained:

6.2.1 Output overvoltage

An overvoltage condition occurs once the output voltage goes higher than the rising overvoltage threshold (V_{OVR}). In this case, the power good output signal is pulled high, alerting the host that a fault is present, but the V_{TT} and V_{REF} outputs stays active. To avoid erroneous overvoltage conditions, a 20 µs filter is implemented. The buck converter uses its feedback loop to attempt to correct the fault. Once the output voltage falls below the falling overvoltage threshold (V_{OVF}), the fault is cleared and the power good output signal is pulled low, the device is back in normal operation.

6.2.2 Output undervoltage

An undervoltage condition occurs once the output voltage falls below the falling undervoltage threshold (V_{UVF}). In this case, the power good output signal is pulled high, alerting the host that a fault is present, but the V_{TT} and V_{REF} outputs stays active. To avoid erroneous undervoltage conditions, a 20 µs filter is implemented. The buck converter uses its feedback loop to attempt to correct the fault. Once the output voltage rises above the rising undervoltage threshold (V_{UVR}), the fault is cleared and the power good output signal is pulled low, the device is back in normal operation.

6.2.3 Output overcurrent

This block detects overcurrent in the Power MOSFETs of the buck converter. It is comprised of a sense MOSFET and a comparator. The sense MOSFET acts as a current detecting device by sampling a ratio of the load current. That sample is compared via the comparator with an internal reference to determine if the output is in over-current or not. If the peak current in the output inductor reaches the over current limit (I_{LIM}), the converter starts a cycle-by-cycle operation to limit the current, and a 10 ms over-current limit timer (t_{LIM}) starts. The converter stays in this mode of operation until one of the following occurs:

- The current is reduced back to the normal level before t_{LIM} expires, and in this case normal operation is regained.
- t_{LIM} expires without regaining normal operation, at which point the device turns off the output and the power good output signal is pulled high. At the end of a timeout period of 100 ms ($t_{TIMEOUT}$), the device attempts another soft start cycle.
- The device reaches the thermal shutdown limit (T_{SDFET}) and turns off the output. The power good output signal is pulled high.

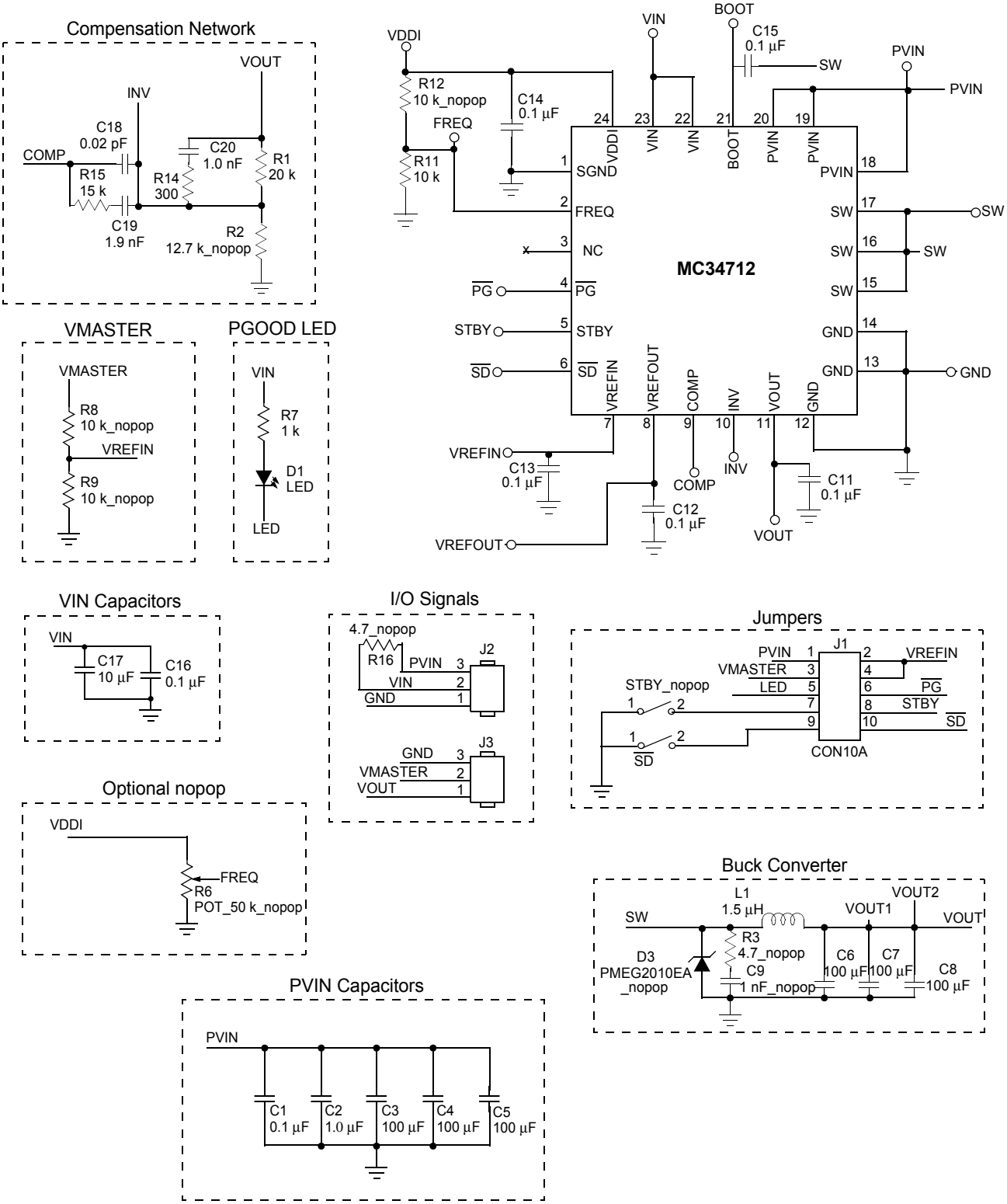
6.2.4 Short-circuit current limit

This block uses the same current detection mechanism as the overcurrent limit detection block. If the load current reaches the I_{SHORT} value, the device reacts by shutting down the output immediately. This is necessary to prevent damage in case of a permanent short circuit. Then, at the end of a timeout period of 100 ms ($t_{TIMEOUT}$), the device attempts another soft start cycle.

6.2.5 Thermal shutdown

Thermal limit detection block monitors the temperature of the device and protects against excessive heating. If the temperature reaches the thermal shutdown threshold (T_{SDFET}), the converter output switches off and the power good output signal indicates a fault by pulling high. The device stays in this state until the temperature has decreased by the hysteresis value and then after a timeout period ($T_{TIMEOUT}$) of 100 ms, the device retries automatically and the output goes through a soft start cycle. If successful normal operation is regained, the power good output signal is asserted low.

7 Typical applications



34712

7.1 Component selection

7.1.1 Switching frequency selection

The switching frequency defaults to a value of 1.0 MHz when the FREQ pin is grounded, and 200 kHz when the FREQ pin is connected to VDDI. Intermediate switching frequencies can be obtained by connecting an external resistor divider to the FREQ pin. Table 6 shows the resulting switching frequency versus FREQ pin voltage. To ensure the V_{TT} (V_{OUT}) regulation, frequency should be selected such that the buck regulator switch ON time is higher than 300 ns. For example, for a 3.3 V_{IN} bus and 0.6 V V_{TT}, choose f_{SW} of 466 kHz.

Table 6. Switching frequency adjustment

Frequency	Voltage applied to pin FREQ
200	2.341 – 2.500
253	2.185 - 2.340
307	2.029 - 2.184
360	1.873 - 2.028
413	1.717 – 1.872
466	1.561 – 1.716
520	1.405 - 1.560
573	1.249 - 1.404
627	1.093 - 1.248
680	0.936 - 1.092
733	0.781 - 0.936
787	0.625 - 0.780
840	0.469 - 0.624
893	0.313 - 0.468
947	0.157 - 0.312
1000	0.000 - 0.156

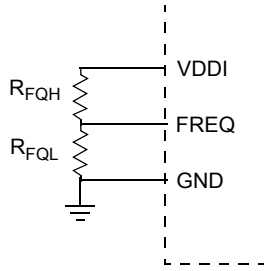


Figure 7. Resistor divider for frequency adjustment

7.2 Selection of the inductor

Inductor calculation is straight forward, being

$$L = D'_{MAX} * T * \frac{(Vo + I_0 * (R_{DS(ON)HS} + R_{INDUCTOR}))}{\Delta I_o}$$

where,

$$D'_{MAX} = 1 - \frac{Vo}{Vin_\max}$$

Maximum OFF time percentage

$$T$$

Switching period.

$$R_{DS(ON)HS}$$

Drain – to – source resistance of FET

$$R_{INDUCTOR}$$

Winding resistance of Inductor

$$\Delta Io = 0.4 * Io$$

Output current ripple.

7.3 Output filter capacitor

For the output capacitor, the following considerations are more important than the actual capacitance value, the physical size, the ESR and the voltage rating:

Transient Response percentage, TR_%

(Use a recommended value of 2 to 4% to assure a good transient response.)

Maximum Transient Voltage, TR_v_dip = Vo*TR_%

Maximum current step,

$$\Delta Io_step = \frac{(Vin_\min - Vo) * D_\max}{F_{SW} * L}$$

Inductor Current rise time,

$$dt_I_rise = \frac{T * Io}{\Delta Io_step}$$

where,

D_max = Maximum ON time percentage.

I_O = Rated output current.

Vin_min = Minimum input voltage at PV_{IN}

As a result, it is possible to calculate

$$Co = \frac{Io * dt_I_rise}{TR_V_dip}$$

In order to find the maximum allowed ESR,

$$ESR_{max} = \frac{\Delta Vo * F_{sw} * L}{Vo(1 - D\min)}$$

The effects of the ESR is often neglected by the designers and may present a hidden danger to the ultimate supply stability. Poor quality capacitors have widely disparate ESR value, which can make the closed loop response inconsistent.

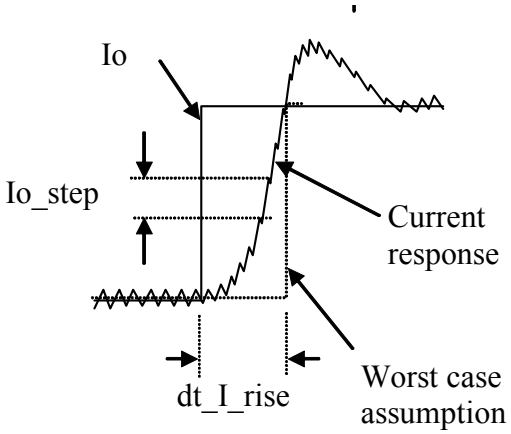


Figure 8. Transient Parameters

7.3.1 Type III compensation network

Power supplies are desired to offer accurate and tight regulation output voltages. To accomplish this requires a high DC gain, but with high gain comes the possibility of instability. The purpose of adding compensation to the internal error amplifier is to counteract some of the gains and phases contained in the control-to-output transfer function that could jeopardized the stability of the power supply. The Type III compensation network used for 34712 comprises two poles (one integrator and one high frequency pole to cancel the zero generated from the ESR of the output capacitor) and two zeros to cancel the two poles generated from the LC filter as shown in Figure 9.

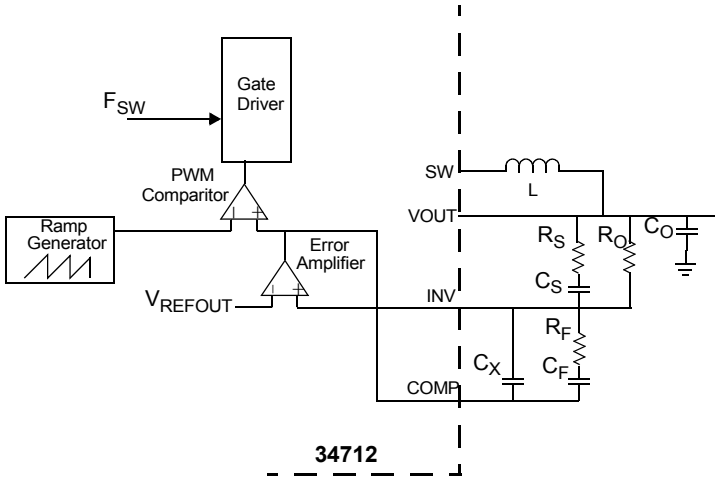


Figure 9. Type III compensation network

Consider the crossover frequency, F_{CROSS}, of the open loop gain at one-tenth of the switching frequency, F_{SW}.
Then,

$$F_{CROSS} = \frac{10}{2\pi \bullet R_O C_F} \Rightarrow$$

$$C_F = \frac{10}{2\pi \bullet R_O F_{CROSS}}$$

where R_O is a user selected resistor. Knowing the LC frequency, it can be obtained the values of R_F and C_S:

$$F_{LC} = \frac{1}{2\pi\sqrt{LC_O}} = F_{Z1} = F_{Z2}$$

$$F_{Z1} = \frac{1}{2\pi * R_F C_F}$$

$$F_{Z2} = \frac{1}{2\pi * R_O C_S}$$

This gives as a result,

$$R_F = \frac{1}{2\pi * C_F F_{Z1}} \quad \&$$

$$C_S = \frac{1}{2\pi * R_O F_{Z2}}$$

Calculate Rs by placing the Pole 1 at the ESR zero frequency:

$$F_{ESR} = \frac{1}{2\pi * C_O * ESR} = F_{P1}$$

$$F_{P1} = \frac{1}{2\pi * R_S C_S}$$

$$\Rightarrow R_S = \frac{1}{2\pi * F_{P1} C_S}$$

Equating the Pole 2 to 5 times the Crossover Frequency to achieve a faster response and a proper phase margin,

$$5 \bullet F_{CROSS} = F_{P2} = \frac{1}{2\pi \bullet R_F \frac{C_F C_X}{C_F + C_X}}$$

$$\Rightarrow \quad C_X = \frac{C_F}{2\pi * R_F C_F F_{P2} - 1}$$

7.3.2 Bootstrap capacitor

The bootstrap capacitor is needed to supply the gate voltage for the high-side MOSFET. This N-Channel MOSFET needs a voltage difference between its gate and source to be able to turn on. The high-side MOSFET source is the SW node, so it is not ground and it is floating and moving in voltage, so it cannot just apply a voltage directly to the gate of the high-side that is referenced to ground, a voltage referenced to the SW node is needed. That is why the bootstrap capacitor is needed for. This capacitor charges during the high-side off time, since the low-side is on during that time, so the SW node and the bottom of the bootstrap capacitor is connected to ground and the top of the capacitor is connected to a voltage source, so the capacitor charges up to that voltage source (say 5.0 V). Now when the low-side MOSFET switches off and the high-side MOSFET switches on, the SW nodes rises up to Vin, and the voltage on the boot pin is V_{CAP} + V_{IN}. So the gate of the high-side has V_{CAP} across it and it is able to stay enhanced. A 0.1 µF capacitor is a good value for this bootstrap element.

7.3.3 Layout guidelines

The layout of any switching regulator requires careful consideration. First, there are high di/dt signals present, and the traces carrying these signals need to be kept as short and as wide as possible to minimize the trace inductance, and therefore reduce the voltage spikes they can create. To do this, an understanding of the major current carrying loops is important. See Figure 10. These loops, and their associated components, should be placed in such a way as to minimize the loop size to prevent coupling to other parts of the circuit. Also, the current carrying power traces and their associated return traces should run adjacent to one another, to minimize the amount of noise coupling. If sensitive traces must cross the current carrying traces, they should be made perpendicular to one another to reduce field interaction.

Second, small signal components which connect to sensitive nodes need consideration. The critical small signal components are the ones associated with the feedback circuit. The high impedance input of the error amp is especially sensitive to noise, and the feedback and compensation components should be placed as far from the switch node, and as close to the input of the error amplifier as possible. Other critical small signal components include the bypass capacitors for VIN, VREFIN, and VDDI. Locate the bypass capacitors as close to the pin as possible.

The use of a multi-layer printed circuit board is recommended. Dedicate one layer, usually the layer under the top layer, as a ground plane. Make all critical component ground connections with vias to this layer. Make sure that the power ground, PGND, is connected directly to the ground plane and not routed through the thermal pad or analog ground. Dedicate another layer as a power plane and split this plane into local areas for common voltage nets.

The IC input supply (VIN) should be connected with a dedicated trace to the input supply. This helps prevent noise from the Buck Regulator's power input (PVIN) from injecting switching noise into the IC’s analog circuitry.

In order to effectively transfer heat from the top layer to the ground plane and other layers of the printed circuit board, thermal vias need to be used in the thermal pad design. It is recommended that 5 to 9 vias be spaced evenly and have a finished diameter of 0.3 mm.

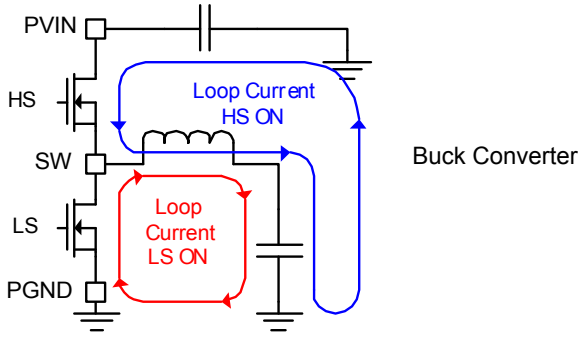


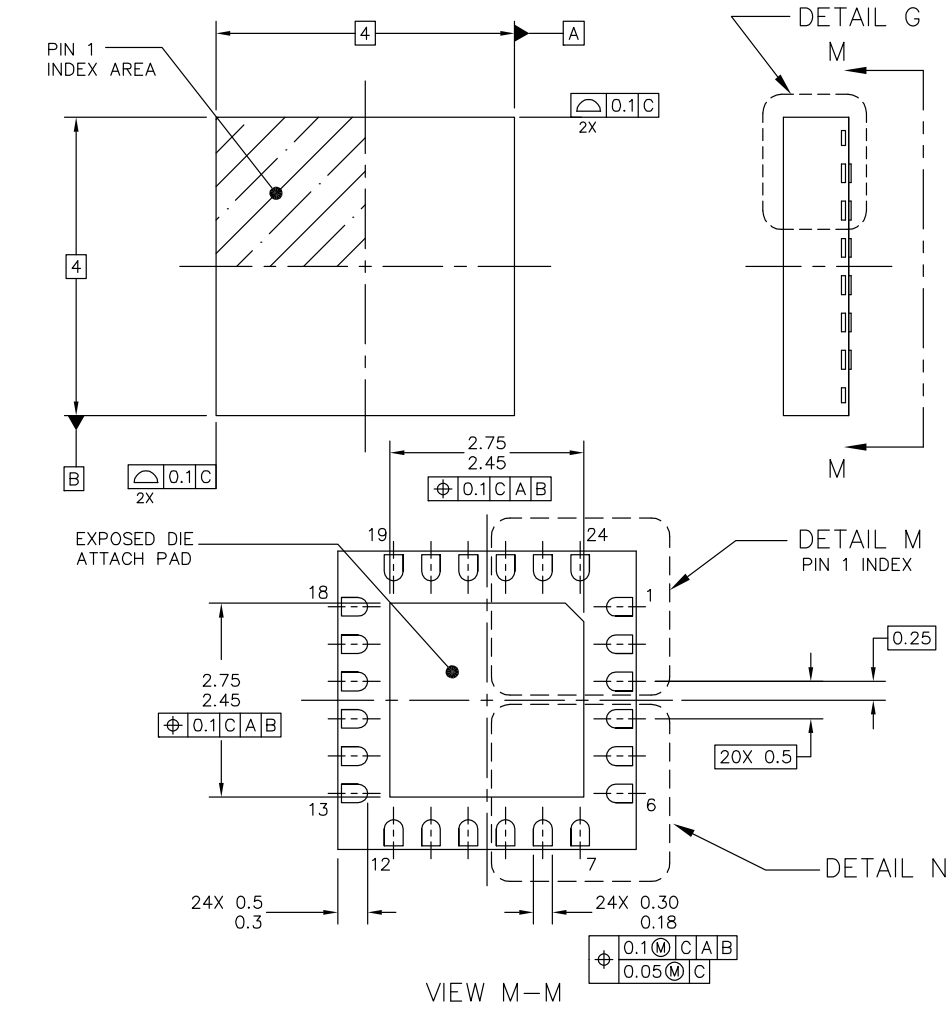
Figure 10. Current loops

8 Packaging

8.1 Packaging dimensions

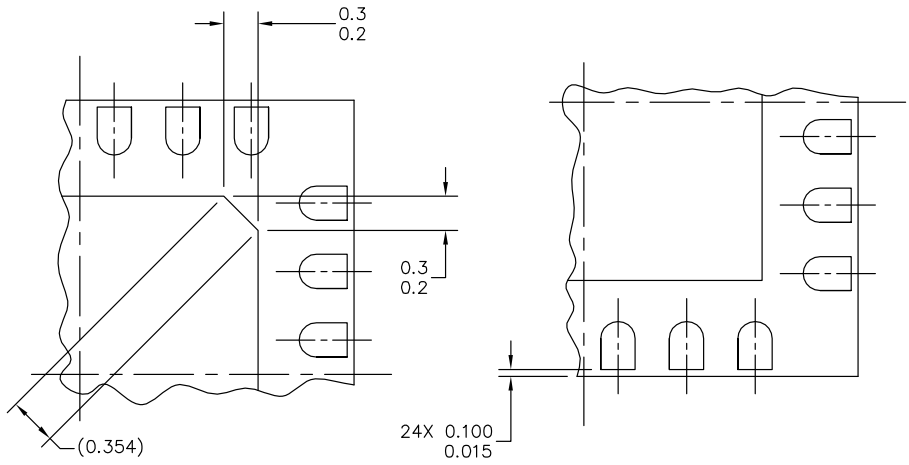
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Package	Suffix	Package outline drawing number
24-Pin QFN	EP	98ARL10577D



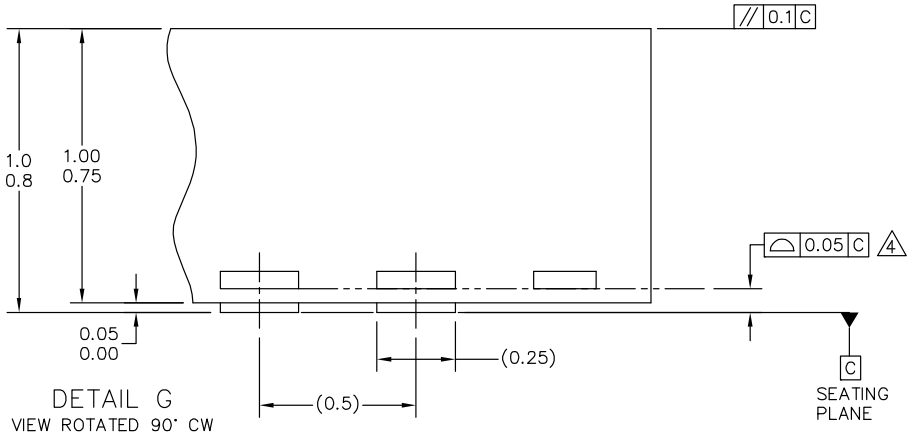
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	CASE NUMBER: 1508–02	28 DEC 2005
	STANDARD: NON–JEDEC	

34712



DETAIL M
PIN 1 BACKSIDE IDENTIFIER

DETAIL N
CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

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34712

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP SHOULD BE 0.2MM.

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9 Revision history

Revision	Date	Description of Changes
1.0	2/2006	• Pre-release version • Implemented Revision History page
2.0	11/2006	• Initial release • Converted format from Market Assessment to Product Preview • Major updates to the data, form, and style
3.0	2/2007	• Replaced all electrolytic capacitors with ceramic ones in Figure 1 • Deleted Deadtime in Dynamic electrical characteristics • Moved Figures 8 ahead of Type III compensation network
4.0	5/2007	• Changed Features from 2% to 1% • Changed 34712 simplified application diagram • Removed Machine Model in Maximum ratings • Added minimum limits to Input DC Supply Current Normal mode, Input DC Supply Current Standby mode, and Input DC Supply Current Shutdown mode • Added High-side MOSFET Drain Voltage Range • Changed Output Voltage Accuracy • Changed Short-circuit Current Limit • Changed High-side N-CH Power MOSFET (M3) RDS(ON) and Low-side N-CH Power MOSFET (M4) RDS(ON) • Changed M2 RDS(on) • Changed PVIN Pin Leakage Current • Changed VREFOUT Buffered Reference Voltage Accuracy, VREFOUT Buffered Reference Voltage Current Capability, and VREFOUT Buffered Reference Voltage Overcurrent Limit • Changed STBY Pin Internal Pull-up Resistor and SD Pin Internal Pull-up Resistor • Changed Soft Start Duration, Overcurrent Limit Retry Timeout Period, and Output Undervoltage/Overvoltage Filter Delay Timer • Changed Oscillator Default Switching Frequency • Changed PG Reset Delay and Thermal Shutdown Retry Timeout Period • Changed drawings in Typical applications • Changed drawing in Type III compensation network • Removed PC34712EP/R2 from the ordering information and added MC34712EP/R2 • Changed the data sheet status to Advance Information
5.0	12/2008	• Made changes to Switching Node (SW) Pin, BOOT Pin (Referenced to SW Pin), Output Undervoltage Threshold, Output Overvoltage Threshold, High-side N-CH Power MOSFET (M3) RDS(ON), Low-side N-CH Power MOSFET (M4) RDS(ON), Device Charge Model (CDM) • Added Machine Model (MM), SW Leakage Current (Standby and Shutdown modes), Error Amplifier DC Gain, Error Amplifier Unit Gain Bandwidth, Error Amplifier Slew Rate, Error Amplifier Input Offset • Added pin 25 to Figure 3 and the 34712 Pin definitions • Added the section Layout guidelines
6.0	4/2012	• Changed typical for Minimum ON Time on page 10
7.0	3/2015	• Added note (17) to Static electrical characteristics
8.0	5/2015	• Minimum output voltage extended to 0.6 V
	8/2016	• Updated to NXP document form and style

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