MIC2310

Single-FET, Constant Power-Limit Hot Swap Controller

General Description

The MIC2310 is a single-channel, positive voltage, constant power-limit hot swap controller designed to provide for the safe insertion and removal of pc boards into fixed, rack, and pedestal mid- or back-planes using few external components. In addition, the MIC2310 employs a patent-pending, output load power-limiting technique where the current limit is inversely proportional to the output load voltage, such that the power product will not exceed the programmed power limit any longer than the externally programmed primary overcurrent period. The MIC2310 is ideally suited to address the power-limiting and timing requirements per the UL60950 specification for 240-VA applications. The MIC2310 incorporates high-side controller circuitry for an external N-channel MOSFET for which the MOSFET drain current rate of change is user-programmable via an external capacitor. The MIC2310 employs dual-speed, dual-level overcurrent fault protection. The primary overcurrent detector response time is programmable via an external current sense resistor and the secondary overcurrent detector is 2-bit user-programmable and exhibits a very fast (default) response to faults to ensure that the system power supplies are protected against catastrophic load current and short-circuit faults. Additionally, an analog output (voltage) signal is provided that is proportional to the steady-state load current to allow monitoring of the system's power. A PWRGD signal is provided to indicate a valid output voltage that can be used to enable a DC-DC power module.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

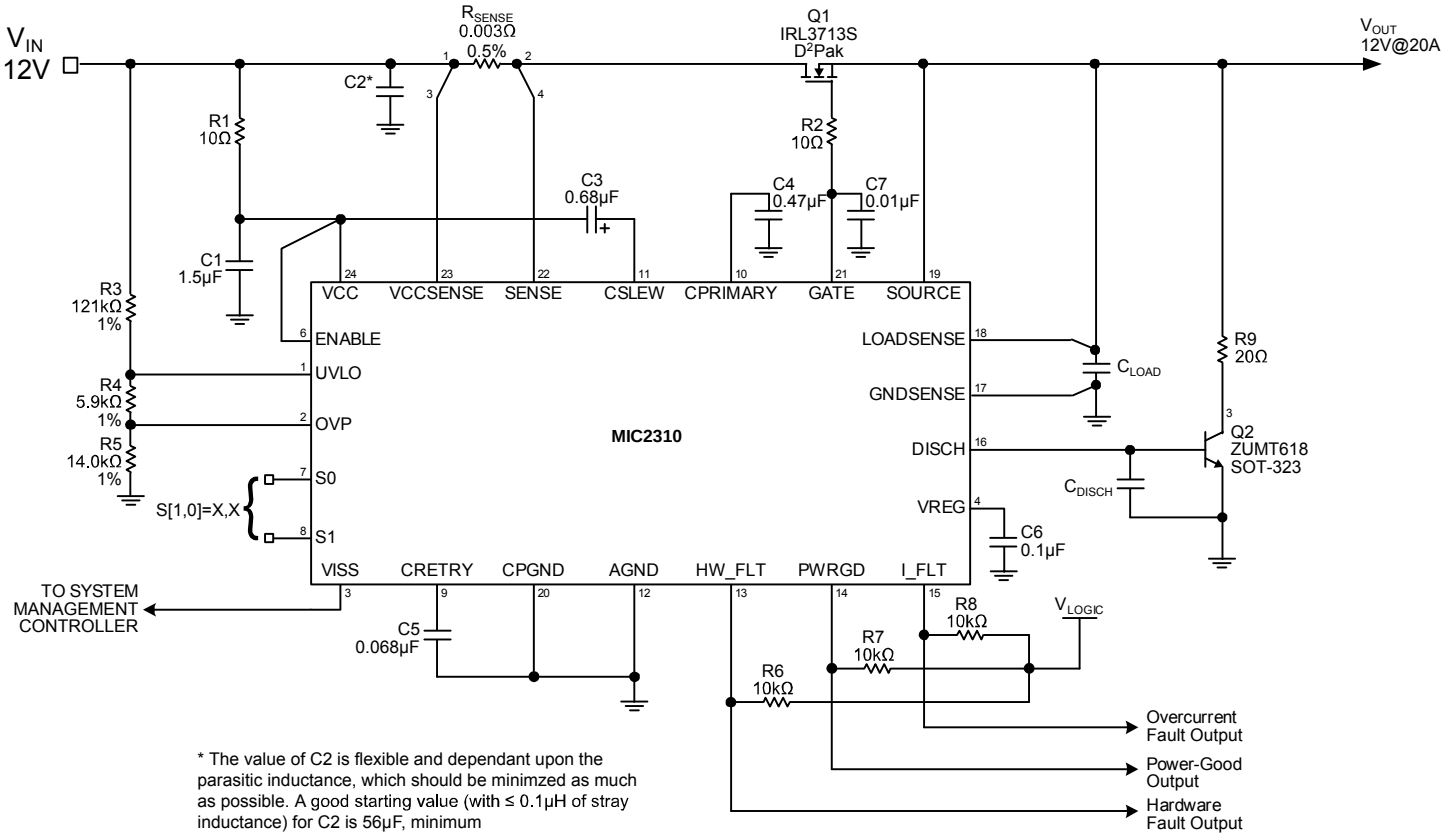
Features

- Provides safe PCB insertion and removal from live +12V backplanes
- Patent-pending, adaptive circuit breaker threshold control
  - Maintains constant power product at output
  - Power-limit product (VA) is externally programmable for various power applications
- Dual-level, dual-speed overcurrent detection/protection
  - Programmable primary detector response time
  - Fast (< 1 μs) secondary detector response time to short circuit conditions
    - User-programmable threshold settings via (2) digital inputs
- Steady-state load current monitoring
- Programmable inrush current slew-rate control
- Electronic circuit breaker functions after fault
  - Latch off
  - Automatic retry
- Programmable input undervoltage lockout and overvoltage protection
- Fault reporting:
  - Open-drain 'Power-is-Good' output
  - Open-drain 'I_FLT' output signaling for all current faults
  - Shorted R_{SENSE} and Damaged MOSFET detection (D-G and D-S shorts)

Applications

- UL60950, EN60950, and CSA1950 systems (240-VA)
- General Power-limiting Applications
- Base stations
- Enterprise servers
- High-reliability servers
- Enterprise switch networks
- +12V backplanes

Typical Application



* The value of C2 is flexible and dependant upon the parasitic inductance, which should be minimzed as much as possible. A good starting value (with ≤ 0.1µH of stray inductance) for C2 is 56µF, minimum

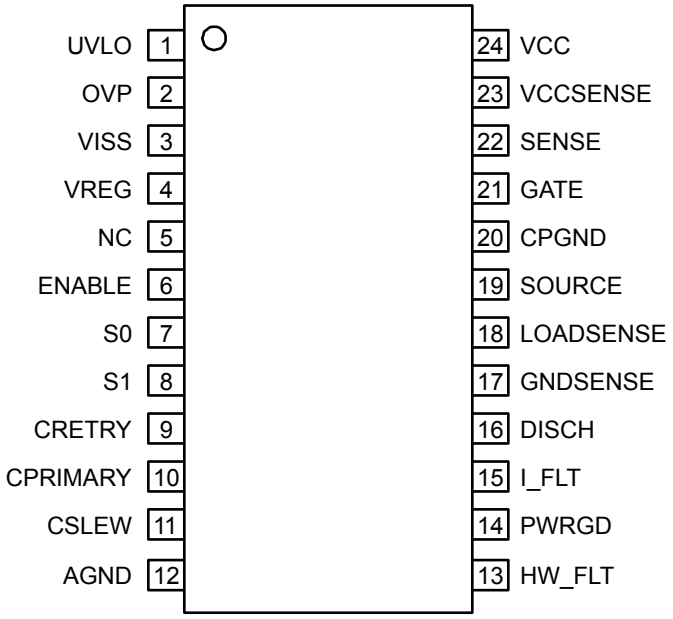
Ordering Information

Part Number	PWRGD State	I_FLT State	Fault Condition Status	Package	Lead Finish
MIC2310-1ZTS	Active-HIGH	Active-HIGH	Latched/Auto-retry	24-pin TSSOP	Pb-Free
MIC2310-2ZTS	Active-LOW	Active-LOW	Latched/Auto-retry	24-pin TSSOP	Pb-Free

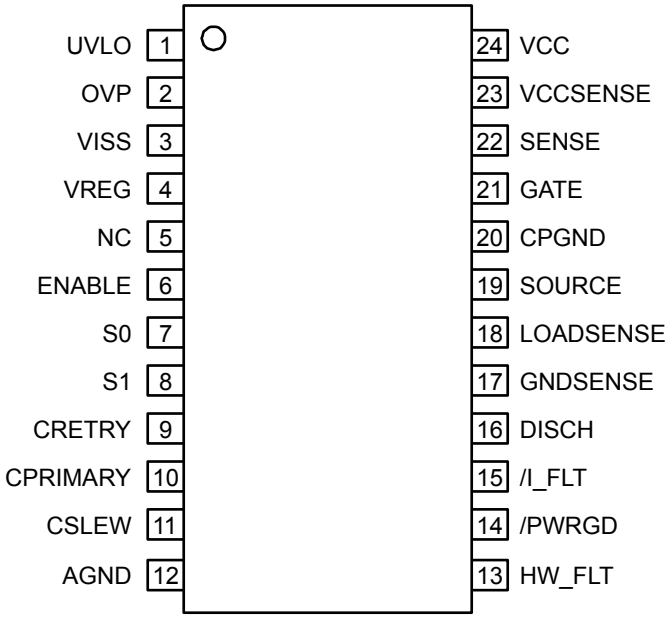
Note:

1. Other Voltage available. Contact Micrel for details.

Pin Configuration



24-pin TSSOP (TS)
MIC2310-1ZTS



24-pin TSSOP (TS)
MIC2310-2ZTS

Pin Description

Pin Number	Pin Name	Pin Function
1	UVLO	Undervoltage Lockout Input. When the applied voltage at the UVLO pin is higher than the controller's V_{UVLOH} threshold voltage, the GATE drive circuits are active when ENABLE= HIGH. If the applied voltage at the UVLO pin falls below the controller's V_{UVLOL} threshold voltage, the GATE drive circuits are disabled to turn the external MOSFET OFF. In addition, the DISCH circuit is activated to drive an optional, external discharge transistor alone (illustrated in the Typical Application circuit) or in combination with an SCR for a very fast discharge circuit configuration.
2	OVP	Overvoltage Protection Input. When the applied voltage at the OVP pin is higher than the controller's V_{OVPH} threshold voltage, the GATE drive circuit is disabled to turn the external MOSFET OFF. In addition, the DISCH circuit is activated to drive an optional, external discharge transistor alone (illustrated in the Typical Application circuit) or in combination with an SCR for a very fast discharge circuit configuration. Using an external resistor divider, the UVLO and the OVP pins form a window comparator that defines the supply voltage range within which the load may be safely powered.
3	VISS	Steady-state Output Current Monitor. This output signal provides an analog voltage that is proportional to the steady-state load current. This signal is provided as an input to the system supervisor/processor to monitor the dc current/power level of the application circuit.
4	VREG	Internal +5V Regulator Bypass. Connect a 0.1-µF, 16V ceramic capacitor from this pin to AGND.
5	NC	No connection
6	ENABLE	ENABLE Input. An active asserted-HIGH digital input that controls the operation of the MIC2310. Activated after the internal POR timer has terminated, a LOW-to-HIGH transition on this pin commences a start-up sequence if the applied V_{CC} is above the V_{UVLOH} and below the V_{OVPH} threshold voltages. While ENABLE = LOW, the GATE pin is held to 0V and the DISCH output is activated. The ENABLE input can be used to reset the internal circuit breaker by applying a HIGH-to-LOW-to-HIGH transition as defined by t_{ENLPW} following either a load current fault, an open LOADSENSE fault, an open GNDSENSE fault, or a shorted RSENSE fault.
7	S0	Secondary OC Detector Current Threshold Digital Inputs – S1 is the MSB and S0 is the LSB. When used together, S[1:0] sets the overcurrent threshold for the secondary overcurrent detection circuit to one of four levels relative to the primary overcurrent detector nominal threshold. For example, S[1:0] = L, L sets the secondary overcurrent threshold at 1.3X; S[1:0] = L, H sets a 1.5X threshold; S[1:0] = H, L sets a 2X threshold, and S[1:0] = H, H sets a 1.75X threshold. If the S[1:0] pins are not connected or left NC, the default setting is S[1:0] = L, L or 1.3X. The permissible voltage range on these inputs is AGND ≤ S[1:0] ≤ V_{CC}.
8	S1	
9	CRETRY	Auto-retry Timing Capacitor. A capacitor connected from the CRETRY pin to AGND configures the MIC2310 to re-start automatically with ENABLE = HIGH after the circuit breaker trips and latches off. It also sets the "cool-off" time delay before a new load current start-up sequence is initiated. To configure the MIC2310's circuit breaker to latch off after fault, connect this pin to AGND. The circuit breaker latches OFF and remains latched OFF unless the ENABLE input is toggled HIGH-to-LOW-to-HIGH as defined by t_{ENLPW} or the V_{CC} supply voltage is turned OFF then ON.
10	CPRIMARY	Primary Overcurrent Detector Timing Capacitor. Connecting a capacitor from the CPRIMARY pin to AGND sets the response time of the controller's primary overcurrent detection circuit to GATE OFF in the event of an overcurrent condition. If the CPRIMARY pin is not connected, the primary overcurrent detection response time defaults to $t_{POCSENSE}$, typically 250µs as specified in the Electrical Characteristics Table. The controller incorporates a patent-pending built-in test for a faulty CPRIMARY capacitor.

Pin Description (continued)

Pin Number	Pin Name	Pin Function
11	CSLEW	Inrush Current Slew Rate Control Input. To adjust the inrush load current profile (controlled dI_{DRAIN}/dt), connect a capacitor from this pin to VCC. To adjust the MOSFET GATE voltage profile (controlled dV_{GATE}/dt), leave this pin OPEN (floating) and connect a capacitor from GATE to AGND. For additional information on the operation of this function, please refer to the Functional Description section.
12	AGND	Analog Ground. Connect this pin to the system analog ground plane.
13	HW_FLT	External MOSFET Hardware Fault Digital Output. This output is an open-drain, active-HIGH signal that should be connected to a +3.3V logic supply by a 10kΩ resistor. This digital output is active after the internal POR timer has terminated and becomes asserted (HIGH) due to a fault under the following conditions: a) a shorted DG MOSFET with ENABLE = LOW; b) a shorted DS MOSFET with ENABLE = LOW; c) a shorted R_{SENSE}; d) a shorted DS MOSFET after steady-state operation with ENABLE = HIGH-to-LOW; or e) a shorted DG or DS while EN = HIGH and DISCH = HIGH; or f) a shorted $C_{PRIMARY}$ to AGND. The HW_FLT output is latched and is reset when VCC is brought low such that $V_{REG} < V_{VREG(UVLO)}$.
14	PWRGD /PWRGD	Power Good Digital Output. This output is an open-drain, active-HIGH (PWRGD) or active-LOW (/PWRGD) signal that should be connected to a +3.3-V logic supply by a 10kΩ resistor. This digital output is active after the internal POR timer has terminated and becomes asserted when the voltage between the LOADSENSE and the GNDSENSE pins is higher than the controller's V_{PGH} threshold voltage. It is de-asserted when the voltage between the LOADSENSE and the GNDSENSE pins is less than the controller's V_{PGL} threshold voltage.
15	I_FLT /I_FLT	Load Current Fault Digital Output. This output is an open-drain, active-HIGH (I_FLT) or active-LOW (/I_FLT) signal that should be connected to a +3.3V logic supply by a 10kΩ resistor. This digital output is active after the internal POR timer has terminated and becomes asserted whenever the primary or secondary overcurrent detection circuits cause the internal circuit breaker to latch OFF. The digital output remains asserted unless the ENABLE input is toggled HIGH-to-LOW-to-HIGH as defined by t_{ENLPW} or the V_{CC} supply voltage is turned OFF then ON or if the auto-retry mode is enabled.
16	DISCH	Discharge External Transistor Drive Output. When ENABLE = LOW or after a fault condition (either an overcurrent fault or hardware fault such as a shorted MOSFET) that causes either the primary and secondary overcurrent detectors to trip the internal circuit breaker, the DISCH circuit is activated to provide gate drive to optional, external transistors (and SCR, for very fast load discharge). These transistors serve as auxiliary gate pull-down or load voltage pull-down switches. A load voltage pull-down is illustrated in the Typical Application circuit.
17	GNDSENSE	These input pins (when used together) sense the load voltage and provide feedback to the controller's adaptive VA limit and Power-Good circuits. The voltage across these two pins also sets the controller's Power-Is-Good status output as defined by the specified V_{PGH} or the V_{PGL} threshold voltages. Internal circuit monitors are included if either or both LOADSENSE and GNDSENSE connections are severed or not connected to the load.
18	LOADSENSE	
19	SOURCE	External Power MOSFET Source Pin Monitor. To protect external circuits downstream of the controller, internal monitor circuits are included to sense a shorted drain-source condition of the external power MOSFETs.
20	CPGND	Internal charge pump power ground. Connect this pin directly to the system's analog ground plane.
21	GATE	External N-channel MOSFET GATE Drive Output. The GATE output signal uses an internal charge pump to charge the gate of an external N-channel MOSFET pass transistor.

Pin Description (continued)

Pin Number	Pin Name	Pin Function
22	SENSE	By connecting a very low value (mΩ) current sense resistor between these two pins, the MIC2310's internal primary and secondary overcurrent detection circuits monitor the load current. The VCCSENSE pin is the positive (+) input terminal and the SENSE pin is the negative (-) input terminal of the overcurrent detection circuits. If the voltage across the sense resistor exceeds either the primary overcurrent threshold for a time (t_{POC}) or the secondary primary overcurrent threshold for any duration, the MIC2310 electronic circuit breaker is tripped, the GATE is turned OFF, the DISCH circuit is activated, and the I_FLT digital output is asserted. The controller also incorporates a patent-pending built-in test for shorted current-sense resistors. Because of this built-in self test, the MIC2310's electronic circuit breaker cannot be disabled by connecting together the VCCSENSE and SENSE pins.
23	VCCSENSE	
24	VCC	Positive supply input to the MIC2310. The MIC2310 is specified to operate from +10.8V ≤ V_{CC} ≤ +13.2V and the supply current with ENABLE = HIGH is less than 10mA.

Absolute Maximum Ratings[1]

VCC, VCCSENSE, SENSE, LOADSENSE, ENABLE, CSLEW, S1, S0, SOURCE ..... –0.3V to +18V
GATE ..... –0.3V to +30V
UVLO, OVP, VISS, CRETRY, CPRIMARY, HW_FLT, PWRGD, I_FLT, DISCH, GNDSENSE .... –0.3V to +6V
Output Current
HW_FLT, PWRGD, I_FLT pins 10mA
ESD Rating (All pins)
Human Body Model ..... 2kV[3]
Machine Model 200V
Lead Temperature (Soldering) Pb-free package
IR Reflow ..... +260°C +0°C/-5°C
Storage Temperature ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +10.8V to +13.2V
Ambient Temperature Range (T_A) ..... 0 °C to +70 °C
Junction Temperature (T_J) ..... +125 °C
Package Thermal Resistance (θ_{JA})
24-pin TSSOP ..... 83.8 °C/W

DC Electrical Characteristics[4]

V_{CC} = +12V, C_{REG} = 0.1µF, T_A = +25 ºC unless otherwise noted. **Bold** indicates specification applies over the full operating temperature range of 0 ºC to +70 ºC. All voltages are measured with respect to AGND unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Operating Supply Voltage (Constant Output Power)		**10.8**		**13.2**	V
I_{CC}	Supply Current	ENABLE = LOW,HIGH			**10**	mA
$V_{VREG(UVLOH)}$	Internal VREG Undervoltage Lockout High Threshold Voltage	V_{REG} Low-to-High Transition	**3.95**	4.25	**4.5**	V
$V_{VREG(UVLOL)}$	Internal V_{REG} Undervoltage Lockout Low Threshold Voltage		**3.70**		**4.25**	V
V_{UVLOH}	UVLO High Threshold Voltage	Low-to-High Transition	**0.96**	1.00	**1.04**	V
V_{UVLOL}	UVLO Low Threshold Voltage	High-to-Low Transition	**0.91**	0.941	**0.97**	V
I_{UVLO}	UVLO Pin Input Current	UVLO = 6V			**5**	µA
V_{OVPH}	OVP High Threshold Voltage	Low-to-High Transition	**1.35**	1.407	**1.45**	V
V_{OVPL}	OVP Low Threshold Voltage	High-to-Low Transition	**1.295**	1.339	**1.395**	V
I_{OVP}	OVP Pin Input Current	OVP = 6V			**5**	µA
V_{GSPGH}	"Power-is-Good" GATE-SOURCE Threshold	(V_{GATE} – V_{SOURCE})	**4.25**	5		V
V_{PGH}	"Power-is-Good" High Threshold ($V_{LOADSENSE}$ – $V_{GNDSENSE}$)	Low-to-High Transition, (V_{GATE} – V_{SOURCE}) ≥ V_{GSPGH} Measured with respect to GNDSENSE = AGND	**9.3**	9.7	**10.1**	V
V_{PGL}	"Power-not-Good" Low Threshold ($V_{LOADSENSE}$ – $V_{GNDSENSE}$)	High-to-Low Transition, (V_{GATE} – V_{SOURCE}) ≥ V_{GSPGH} Measured with respect to GNDSENSE = AGND	**8.4**	9	**9.6**	V
V_{REG}	V_{REG} Output Voltage	R_{REG} > 1 MΩ	**4.5**	5	**5.5**	V

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{CBP}	Primary OC Circuit Breaker Threshold Voltage $V_{VCCSENSE} – V_{SENSE}$	$(V_{LOADSENSE} – V_{GNDSENSE})$ = +12V		**54.7**	57.2	**59.7**	mV
		$(V_{LOADSENSE} – V_{GNDSENSE})$ = +10.8V		**60.7**	63.5	**66.3**	mV
		$(V_{LOADSENSE} – V_{GNDSENSE})$ = +13.2V		**49.6**	51.9	**54.2**	mV
V_{CBS}	Secondary OC SENSE Voltage $V_{VCCSENSE}$ - V_{SENSE}	Secondary OC Detector Circuit Breaker Trips, $V_{LOADSENSE} – V_{GNDSENSE}$ = 10.8V to 13.2V	S[1:0] = L, L	**64**	75.5	**87**	mV
			S[1:0] = L, H	**75**	87.5	**99**	mV
			S[1:0] = H, L	**100**	116.6	**130**	mV
			S[1:0] = H,H	**85**	102	**116**	mV
$I_{VCCSENSE}$	VCCSENSE Pin Input Current	$V_{VCCSENSE} = V_{CC}$				**1**	µA
I_{SENSE}	SENSE Pin Input Current	$V_{SENSE} = V_{CC}$				**3**	µA
V_{RETRYH}	CRETRY Pin High Threshold Voltage			**1.21**	1.25	**1.28**	V
V_{RETRYL}	CRETRY Pin Low Threshold Voltage			**0.25**	0.3	**0.35**	V
$I_{RETRYUP}$	CRETRY Pin Charging Current	TIMER ON, V_{RETRY} = 0V		**-4.25**	-3	**-1.65**	µA
$I_{RETRYDN}$	CRETRY Pin Pull-down Current	TIMER OFF, V_{RETRY} = 1.5V			3		mA
V_{PRIL}	CPRIMARY Pin Low Threshold Voltage	During OC response; ENABLE = HIGH; $V_{CC(SENSE)} – V_{SENSE} > V_{CBP}$ Measured relative to V_{REG}		**-1.3**	-1.25	**-1.2**	V
V_{PRIL}	CPRIMARY Pin Low Threshold Voltage	During shorted $C_{PRIMARY}$ detection; Measured relative to V_{REG}	ENABLE = HIGH; $V_{CC(SENSE)} – V_{SENSE} < V_{CBP}$	**-1.3**	-1.25	**-1.2**	V
			ENABLE = LOW				
I_{PRI}	CPRIMARY Pin Charging Current	During Primary OC Fault $V_{CPRIMARY} = V_{REG}$; ENABLE = HIGH $V_{CC(SENSE)} – V_{SENSE} > V_{CBP}$		**2.4**	3	**3.6**	µA
		During nominal and reset operation $V_{PRIMARY} = V_{REG} – 1.25V$; ENABLE = HIGH $V_{CC(SENSE)} – V_{SENSE} < V_{CBP}$		**-4.5**	-3	**-1.5**	mA
		During disable; $V_{CPRIMARY} = V_{REG} – 1.25V$ ENABLE = LOW		**-4.5**	-3	**-1.5**	mA
ΔV_{GATE}	GATE Output Voltage	$(V_{GATE}-V_{CC})$: V_{CC} > 10.5V Internally clamped		**8**		**15**	V
ΔV_{CP}	$V_{CSLEW} – V_{SENSE}$ Differential	Charge pump to OFF			50		mV
I_{SLEW}	Inrush Current slew Charging current	$V_{CSLEW} = V_{CC} – 50mV$		**5**	10	**15**	µA

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{GATEUP}	GATE Pin Pull-up Current	Charge pump ON, $V_{GATE} = V_{SOURCE} = +13.2V$	**-60**	-30	**-15**	µA
I_{GATEDN}	Normal GATE Pin Pull-down Current	ENABLE = LOW, $V_{GATE} = 2V$	**1.0**	2.7	**4.5**	mA
	Fault-mode GATE Pin Pull-down current	I_FLT Latched and OC Detector Trip or in UVLO, $V_{GATE} = 2V$	**45**	120		mA
$V_{GATEFT(EXT)}$	GATE-to-AGND Fault Threshold ENABLE = LOW			5		V
$V_{SRCFT(EXT)}$	SOURCE-to-AGND Fault Threshold ENABLE = LOW			5		V
$V_{THLOADSENSE}$	Open LOADSENSE Threshold	$V_{SOURCE} - V_{LOADSENSE}$		4		V
$V_{THGNDSENSE}$	Open GNDSENSE Threshold	$V_{GNDSENSE}$		4		V
I_{SOURCE}	SOURCE Pin Input Current	EN = LOW, 0V ≤ SOURCE ≤ V_{CC}			**18**	µA
		EN = HIGH, SOURCE = V_{CC}			**1.5**	µA
		EN = HIGH, /FAULT Condition 0V ≤ SOURCE ≤ V_{CC}			**18**	µA
$I_{LOADSENSE}$	LOADSENSE Pin Input Current	+10.8V ≤ $V_{LOADSENSE}$ ≤ +13.2V			**300**	µA
		$V_{LOADSENSE}$ = 0V DISCH = HIGH			**300**	µA
$I_{GNDSENSE}$	GNDSENSE Pin Input Current	$V_{GNDSENSE}$ = 0V	**-400**			µA
$\Delta V_{DS(FET)}$	Shorted R_{SENSE} Threshold Voltage at SOURCE ($V_{SENSE} – V_{SOURCE}$)	$V_{CC(SENSE)} – V_{SENSE}$ = 0V, $V_{GATE} – V_{SOURCE} > V_{GSPGH}$		7		mV
ΔV_{RSENSE}	Shorted R_{SENSE} Threshold Voltage ($V_{VCCSENSE} – V_{SENSE}$)	$V_{SENSE} – V_{SOURCE}$ = 30mV, $V_{GATE} – V_{SOURCE} > V_{GSPGH}$		12		mV
V_{DISCH}	DISCH Pin Drive Voltage	I_{DISCH} = 12mA			**0.4**	V
I_{DISCH}	DISCH Pin Drive Current	V_{DISCH} = 2.5V			**-400**	µA
$V_{ISS(LIN)}$	Linear Sensing Range	$V_{VCC(SENSE)} - V_{SENSE}$	**0**		**90**	mV
$V_{ISS(Q)}$	Zero Voltage VISS Output Voltage	$V_{VCC(SENSE)} - V_{SENSE}$ = 0mV	**7**	55	**103**	mV
R_{VISS}	VISS DC Output Resistance	$[VISS_{(20µA)} - VISS_{(10µA)}]/10µA$		100		kΩ
$V_{ISS(SENS)}$	VISS Analog Signal Sensitivity	$\Delta V_{VISS}/\Delta(V_{VCC(SENSE)} - V_{SENSE})$	**28**	30	**32**	V/V
E_{TOT}	VISS Total Error % (240 VA)	$V_{VCC(SENSE)} - V_{SENSE}$ = 60mV			**±10**	%

Symbol	Parameter	Condition	Min	Typ	Max	Units
E_{LIN}	VISS Analog Nonlinearity	$V_{VCC(SENSE)}$ - V_{SENSE} = 0mV to 90mV			**±6.5**	%
V_{OL}	LOW-Level Output Voltage I_FLT, PWRGD, HW_FLT	I_{OUT} = 1.6mA			**0.4**	V
V_{IL}	LOW-Level Input Voltage ENABLE, S1, S0				**0.8**	V
V_{IH}	HIGH-Level Input Voltage ENABLE, S1, S0		**2**			V
I_{IH}	Input Pull-down Current ENABLE, S1, S0	V_{IH} = +0.8V	**55**	80	**120**	µA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Specification for packaged product only.

AC Electrical Characteristics[4]

V_{CC} = +12V, C_{REG} = 0.1µF, T_A = +25 ºC unless otherwise noted. **Bold** indicates specification applies over the full operating temperature range of 0 ºC to +70 ºC.

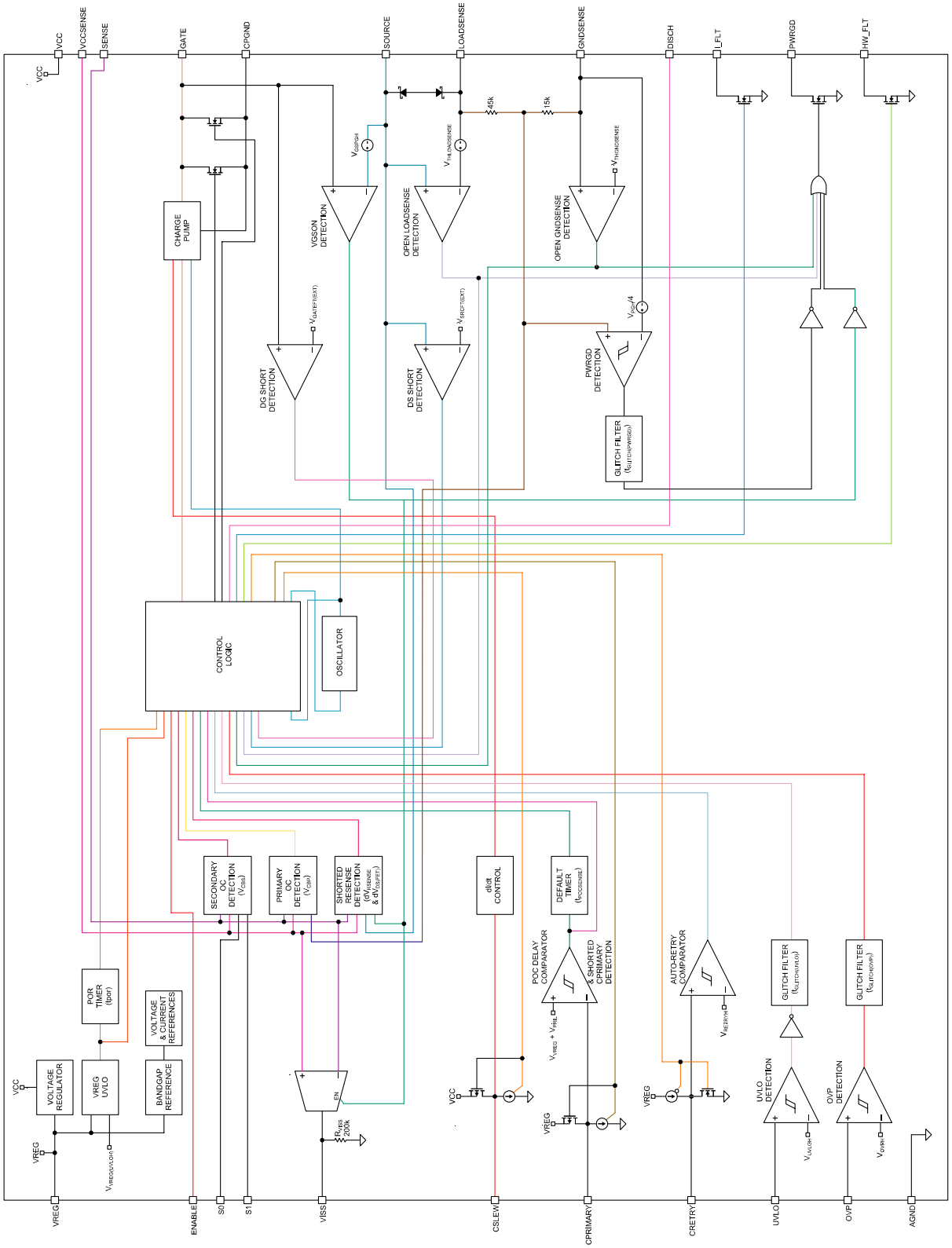
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{POR}	Power-on-Reset Delay	$V_{VREG} \geq V_{VREG(UVLOH)}$			**6.5**	ms
$t_{POCSENSE}$	Primary OC Detector Default Response Time to GATE pin Discharge	($V_{VCCSENSE}$ -V_{SENSE}) = 70-mV step; PRIMARY Pin Floating; and S[1:0] = H,L C_{GATE} = 100pF	**200**	300	**420**	µs
$t_{SOCSENSE}$	Secondary OC Detector Response Time to GATE Pin Discharge	($V_{VCCSENSE}$ -V_{SENSE}) = 200-mV step		0.25	**0.5**	µs
$t_{CBRESET}$	Circuit Breaker Reset Delay Time	ENABLE Low to I_FLT Low			**5**	µs
t_{ENLPW}	ENABLE Low Pulse Width		**200**			µs
$t_{SCPDETECT}$	Shorted $C_{PRIMARY}$ Detection Time to HW_FLT Latched	ENABLE = LOW or HIGH;		0.25		µs
$t_{SCPDETPOR}$	Shorted $C_{PRIMARY}$ Detection Delay after Primary OC Detection	$V_{VCCSENSE}$ -V_{SENSE} ≤ V_{CBP}			**6.5**	ms
$t_{DG(FET)}$	MOSFET DG Short to HW_FLT Latched	ENABLE = LOW; GATEFT(EXT) Asserts HW_FLT		10		µs
$t_{DS(FET)}$	MOSFET DS Short to HW_FLT Latched	ENABLE = LOW; SRCFT(EXT) Asserts HW_FLT		10		µs
$t_{DS\text{-}SSFAULT}$[2]	MOSFET DS Short to HW_FLT Latched	ENABLE = HIGH-to-LOW after steady-state operation		250		µs
		ENABLE = HIGH DISCH = LOW-to-HIGH				

Symbol	Parameter	Condition	Min	Typ	Max	Units
$t_{GLITCH(UVLO)}$	UVLO & OVP Glitch Filter Delay Time	Overdrive = 50mV		10		µs
$t_{VISS(PROP)}$	VISS Propagation Delay Time	$V_{VCCSENSE}$ - V_{SENSE} = 0mV to 60mV Capacitance from VISS to GND is 100pF		7		µs
$t_{VISS(RISE)}$	VISS Rise Time	$V_{VCCSENSE}$ - V_{SENSE} = 0mV to 60mV Capacitance from VISS to GND is 100pF V_{VISS} 10% to 90%		25		µs
$t_{GLITCH(PWRGD)}$	PWRGD Glitch Filter Delay Time	Overdrive = 250mV		30		µs
$t_{DLY(DISCH)}$	GATE OFF to DISCH Delay Time			0.25		µs

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Block Diagram



Functional Description

Basic Startup Cycle

The basic operation of the MIC2310 is illustrated below in Figure 2 from a cold-start condition. With the applied V_{CC} supply low such that the internal V_{REG} voltage is less than the MIC2310's internal $V_{VREG(UVLOH)}$ threshold voltage, all state machines are reset, all voltage and current monitor subcircuits are OFF, and the GATE drive circuit is disabled. Digital inputs and all open-drain digital outputs are inactive. When the applied V_{CC} supply rises such that the internal V_{REG} voltage is above the controller's $V_{VREG(UVLOH)}$ threshold voltage, the t_{POR} counter circuit commences. Once the timer terminates, all internal state machines are activated, the CPRIMARY short detection circuit is ON and the DG & DS MOSFET short detection circuits are ON if ENABLE is LOW. The I_FLT, PWRGD, and HW_FLT outputs are valid.

Upon the application of an ENABLE LOW-to-HIGH transition after the t_{POR} delay, or at the end of the t_{POR} delay if ENABLE is already HIGH, a nominal start-up commences where the dI_D/dt-controlled inrush current (by $dI_D/dt = 17.6x10^{-3} \times I_{SLEW} / (R_{SENSE} \times C_{SLEW})$) is permitted to exceed the I_{POC} threshold for t_{POC}, until there is sufficient charge stored on the load capacitor as evidenced by the output load voltage profile. Note that the secondary overcurrent detection threshold (I_{SOC}) is set externally at the controller's S[1:0] pins. Once the inrush current exceeds the I_{SOC} threshold, the circuit breaker trips without delay and the MIC2310 controller shuts down the output. If the inrush current profile does not cause either of the OC detection circuits to trip the circuit breaker and assert the I_FLT digital output, the controller will assert the PWRGD digital output when the output load voltage is higher than the controller's V_{PGH} threshold voltage and the V_{GS} of the external MOSFET is higher than the controller's V_{GSPGH} threshold voltage. Due to the low $R_{DS(ON)}$ of the external MOSFET, the output load voltage rises with the GATE voltage as the V_{GS} of the MOSFET reaches its threshold voltage. Once the output load voltage stabilizes near the V_{CC} supply voltage, the V_{GS} of the external MOSFET increases above its threshold voltage and eventually exceeds V_{GSPGH}. The PWRGD output asserts to signal that the external MOSFET is fully enhanced and ready for the application of the full load.

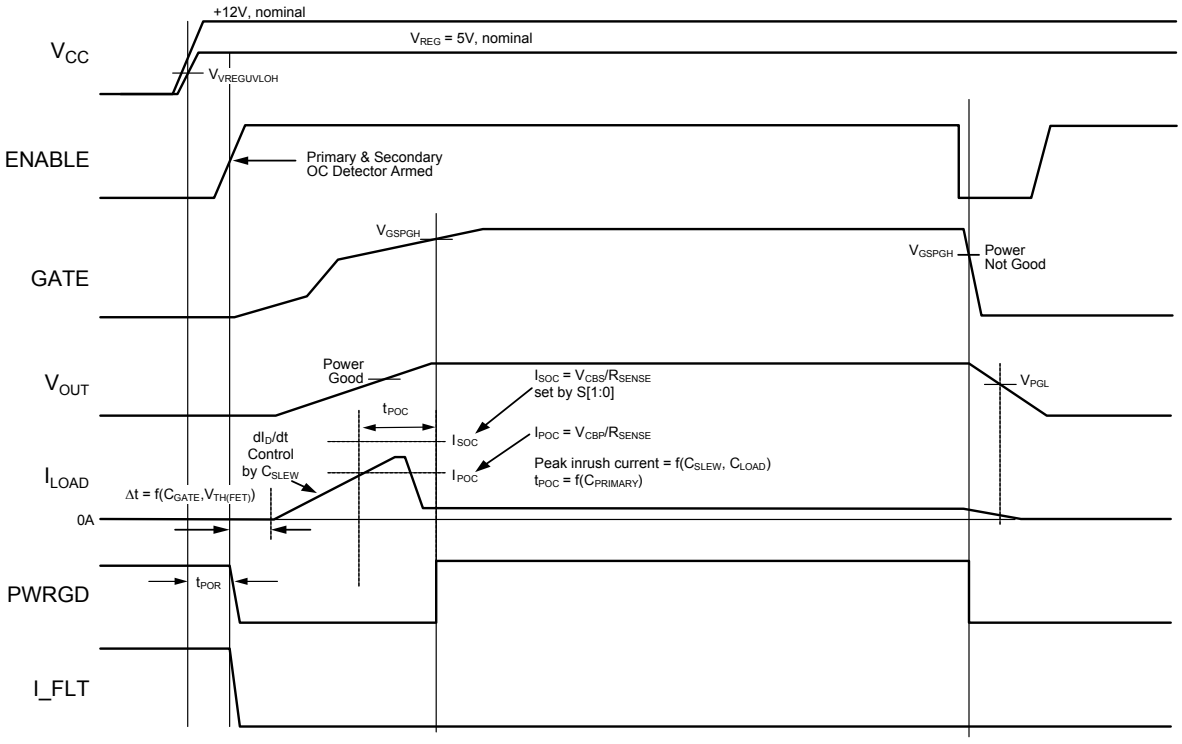


Figure 2. Basic Startup Cycle

Primary Overcurrent (OC) Detector Trips Circuit Breaker and Asserts I_FLT

Figure 3 below illustrates the behavior of the controller to an OC event after the primary and secondary OC detection circuits have been armed (upon the application of an ENABLE LOW-to-HIGH transition and after t_{POR}) and steady-state operation has been achieved. Note that the assertion of the controller's PWRGD digital output occurs when the output load voltage profile is higher than the controller's V_{PGH} threshold voltage and the V_{GS} of the external MOSFET is higher than the controller's V_{GSPGH} threshold voltage.

The use of an external $C_{PRIMARY}$ capacitor sets the response time, t_{POC}, of the primary OC detector according to the internal V_{PRIL} threshold voltage and the CPRIMARY pin discharging current, I_{PRI}, where $t_{POC} = t_{POCSENSE} + C_{PRIMARY} * (V_{PRIL}/I_{PRI})$. Prior to triggering the primary OC detector (i.e., when $V_{VCCSENSE} - V_{SENSE} < V_{CBP}$), a 3mA current source is enabled to hold the CPRIMARY pin voltage to the internally-generated V_{REG} voltage. When the primary OC detector has been triggered, the 3mA current source is first disabled and a 3µA current sink is enabled to discharge the external $C_{PRIMARY}$. When $C_{PRIMARY}$ has discharged below V_{PRIL}, a default timer is enabled. Once the default timer ($t_{POCSENSE}$) times out, the circuit breaker is tripped, the 3µA current sink is disabled, and the 3mA current source is enabled to discharge $C_{PRIMARY}$ back to V_{REG} quickly. Concurrently, the GATE drive circuit is disabled and a higher current, fault-mode pull-down current sink is enabled at the GATE pin. The DISCH output goes high to (optionally) drive external pull-down circuitry.

In the event that the CPRIMARY pin is left NC (intentionally or otherwise), the overcurrent timer default value is $t_{POCSENSE}$ (250µs typical), as specified in the ac specification table. Once the circuit breaker is latched, the I_FLT digital output is asserted and the PWRGD digital output becomes de-asserted when the output voltage profile falls below the controller's V_{PGL} threshold voltage or the V_{GS} of the external MOSFET falls below the controller's V_{GSPGH} threshold voltage.

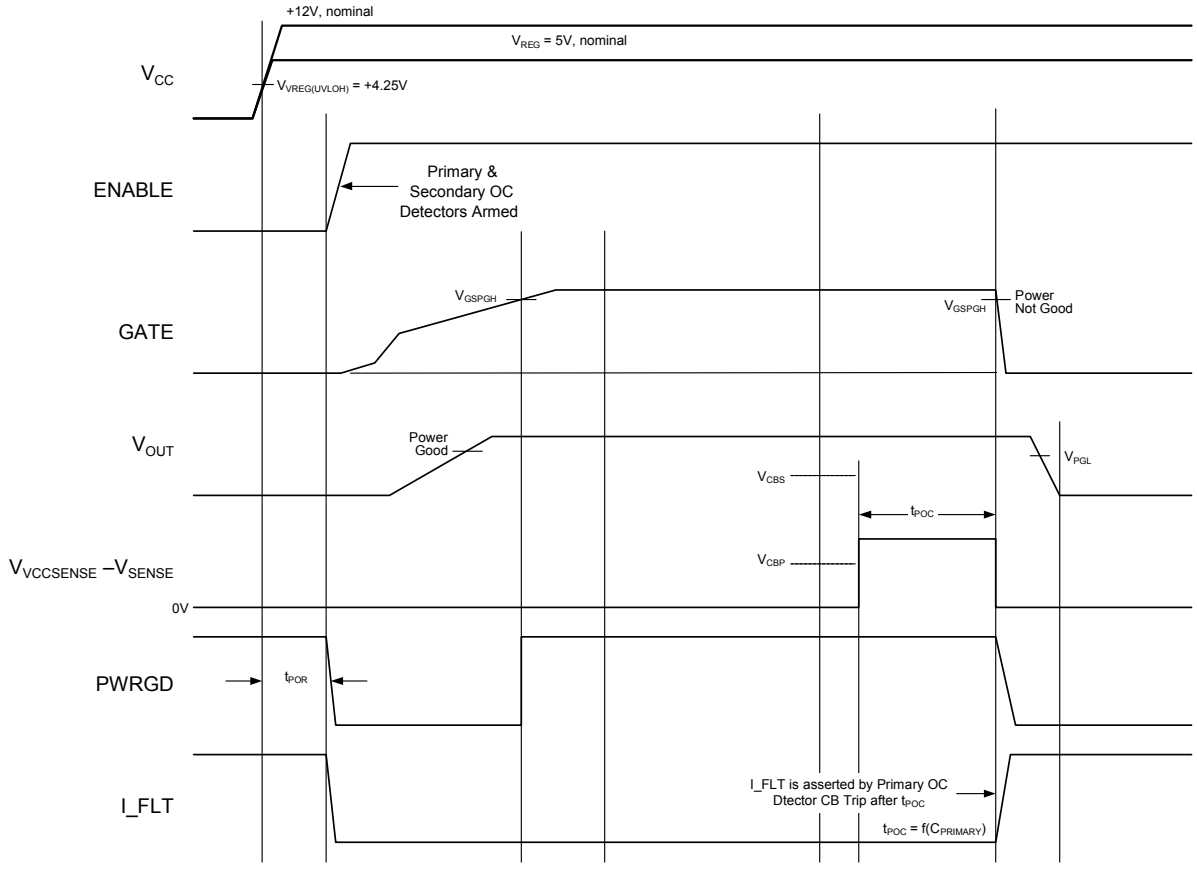


Figure 3. Primary OC Detector Trips Circuit Breaker

Secondary OC Detector Trips Circuit Breaker and Asserts I_FLT

Figure 4 illustrates the behavior of the controller to an OC event after the primary and secondary OC detection circuits have been armed (upon the application of an ENABLE LOW-to-HIGH transition and after t_{POR}) and steady-state operation has been achieved. Note that the assertion of the controller's PWRGD digital output occurs when the output load voltage profile is higher than the controller's V_{PGH} threshold voltage and the V_{GS} of the external MOSFET is higher than the controller's V_{GSPGH} threshold voltage.

The controller's secondary OC detection threshold is set by the status of the controller's S[1:0] pins and its response time is internally set at $t_{SOCSENSE}$ as shown in the ac specification table. When the secondary OC detector has sensed a very large current surge ($V_{CCSENSE} - V_{SENSE} \geq V_{CBS}$), the circuit breaker is tripped within $t_{SOCSENSE}$. Concurrently, the GATE drive circuit is disabled and a higher current, fault-mode pull-down current sink is enabled at the GATE pin. The DISCH output goes high to (optionally) drive external pull-down circuitry.

Once the circuit breaker is latched, the I_FLT digital output is asserted and the PWRGD digital output becomes de-asserted when the output voltage profile falls below the controller's V_{PGL} threshold voltage or the V_{GS} of the external MOSFET falls below the controller's V_{GSPGH} threshold voltage.

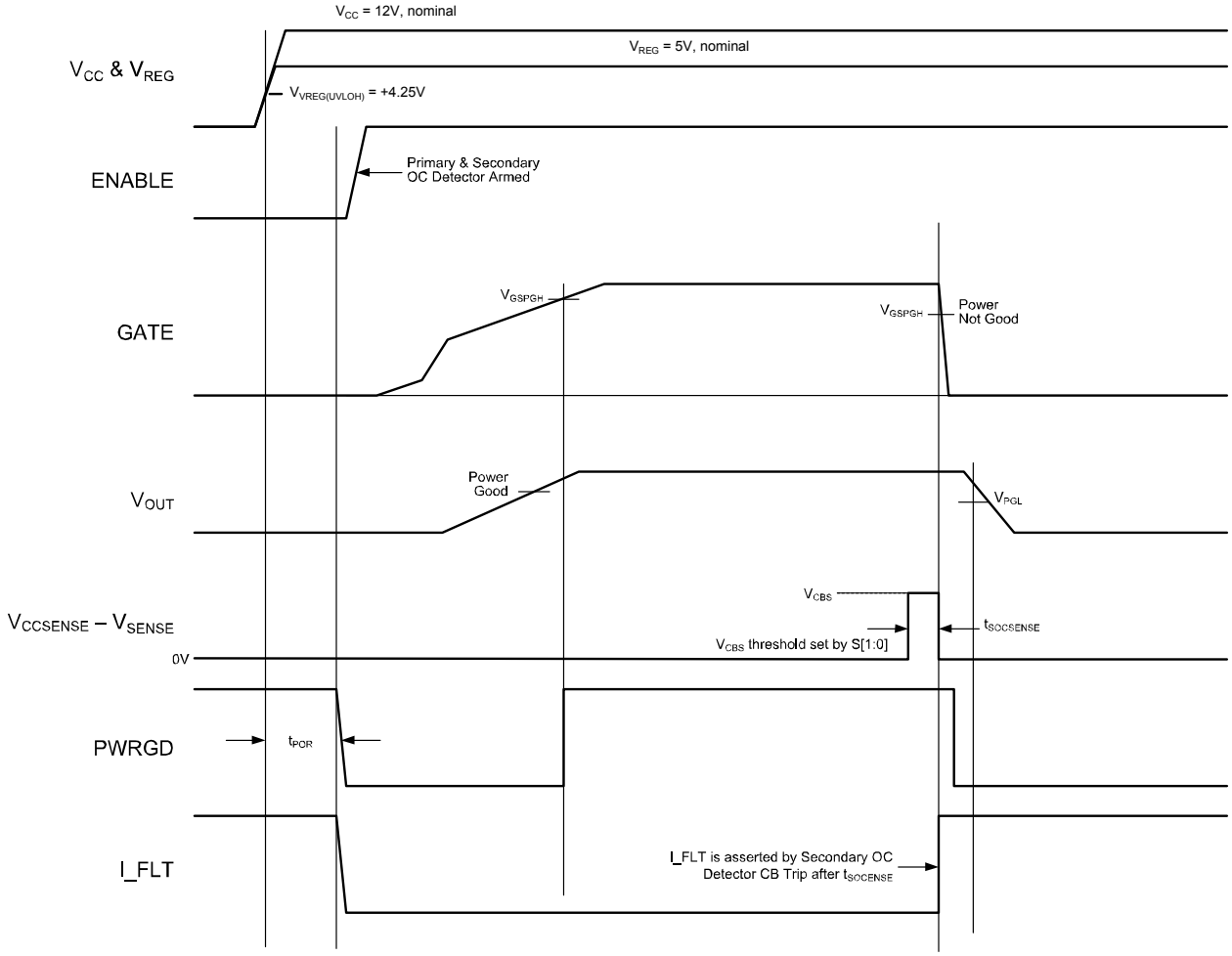


Figure 4. Secondary OC Detector Trips Circuit Breaker

Charging Load by dI_D/dt – Primary OC Trips CB after t_{POC} and CB Reset by Toggling ENABLE HIGH-to-LOW

Figure 5 illustrates the behavior of the controller to an OC event after the primary and secondary OC detection circuits have been armed (upon the application of an ENABLE LOW-to-HIGH transition and after t_{POR}). In this example, the load capacitor is charged at a controlled dI_D/dt rate. Steady-state operation is not achieved as the controlled inrush profile causes the primary OC detector to trigger at I_{POC} and continues charging when the $t_{POCSENSE}$ timer terminates. Note that the controller's PWRGD digital output does not assert because the output load voltage profile at no time rises higher than the controller's V_{PGH} threshold voltage and the V_{GS} of the external MOSFET does not rise higher than the controller's V_{GSPGH} threshold voltage.

Once the circuit breaker has latched, the I_FLT digital output is asserted. When the circuit breaker is tripped by either the primary OC or secondary OC detectors), applying a HIGH-to-LOW transition on the ENABLE pin will reset the circuit breaker. At a delay defined by $t_{CBRESET}$, the internal circuit breaker is reset and is indicated when the I_FLT digital output becomes de-asserted. The earliest a LOW-to-HIGH transition at ENABLE is permitted to initiate a new start-up sequence is defined by the t_{ENLPW} timing specification.

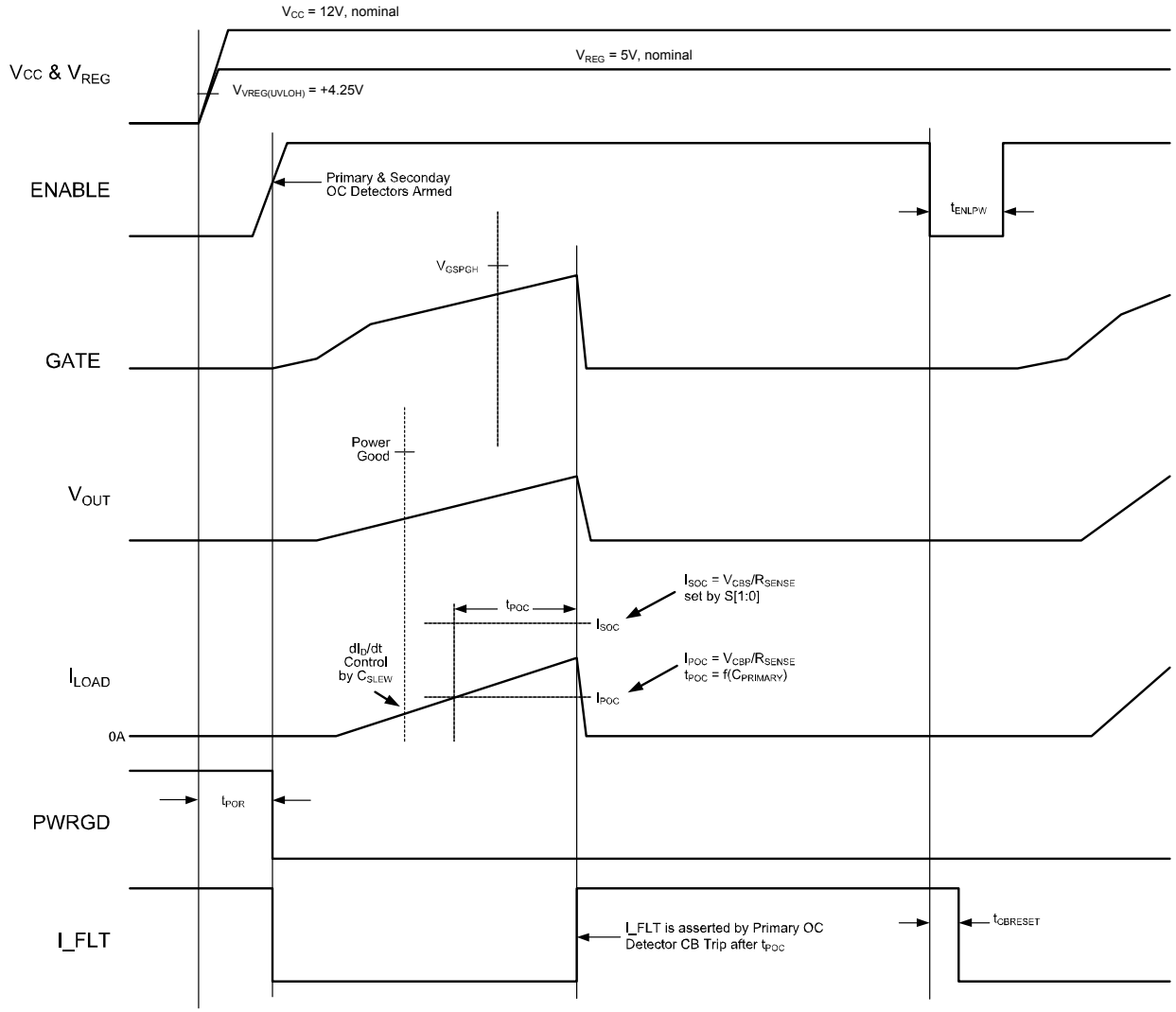


Figure 5. dI_D/dt Load Charge Profile w/ Primary OC Circuit Breaker (CB) Trip w/ CB Reset

Primary OC Trips Circuit Breaker (CB) and CB Resets with C_{RETRY} (Auto-Retry Timing Capacitor)

Figure 6 illustrates the behavior of the controller to a primary OC event when a C_{RETRY} capacitor is used to automatically reset the circuit breaker. The automatic reset operation is the same for the case of a secondary OC event. In this example, the primary and secondary OC detection circuits have been armed (upon the application of an ENABLE LOW-to-HIGH transition and after t_{POR}) and the load capacitor is charged at a controlled dI_D/dt rate. Note that in this diagram, ENABLE is tied to V_{CC} and rises with V_{CC}. Steady-state operation is achieved as the controller's PWRGD digital output is asserted when the output load voltage profile is higher than the controller's V_{PGH} threshold voltage and the V_{GS} of the external MOSFET is higher than the controller's V_{GSPGH} threshold voltage.

When the primary OC detector has been triggered by an output current exceeding I_{POC} for a time t_{POC}, the circuit breaker is tripped, the GATE drive circuit is disabled, the fault-mode pull-down current sink is enabled at the GATE pin, the DISCH output goes high, and the I_FLT digital output becomes asserted. The use of an external C_{RETRY} capacitor sets the auto-retry time, t_{RETRY}, according to the internal V_{RETRYH} threshold voltage and the CRETRY pin charging current, $I_{RETRYUP}$ [$t_{RETRY} = C_{RETRY} * (V_{RETRYH}/I_{RETRYUP})$]. Prior to the tripping of the OC circuit breaker, a 3mA current sink is enabled holding the CRETRY pin voltage at 0V. When the OC circuit breaker has been tripped, the 3mA current sink is disabled and a 3µA current source is enabled to charge the external C_{RETRY} capacitor. When C_{RETRY} has charged above V_{RETRYH}, the circuit breaker is reset such that the I_FLT digital output is de-asserted. Additionally, the 3µA current source is disabled and the 3mA current sink is enabled to discharge the CRETRY pin voltage back to 0V. When C_{RETRY} has discharged below V_{RETRYL}, the GATE drive circuit is re-enabled and the DISCH output returns low. For the case of a persistent overcurrent load, the controller will continuously cycle between starting up into an OC condition that trips the circuit breaker and the auto-retry time before the circuit breaker is reset.

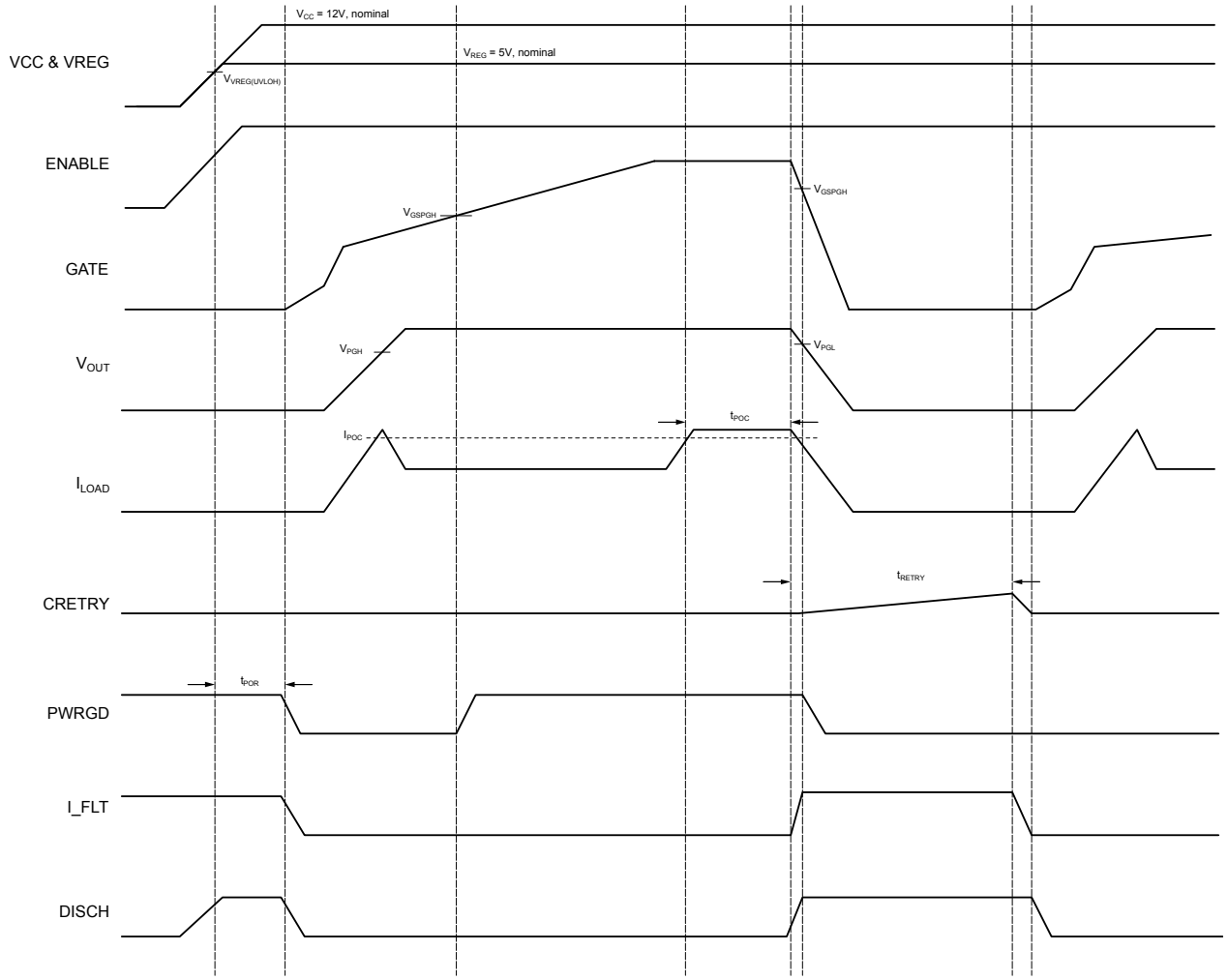


Figure 6. Primary Overcurrent Fault with Auto-Retry to Reset the Circuit Breaker

HW_FLT Digital Output Asserted by a MOSFET DG Short with ENABLE = LOW

In order to protect the system from the result of the installation of a damaged MOSFET on the PCB, the controller incorporates a MOSFET shorted DG detection scheme whose operation is described in Figure 7. With the applied V_{CC} supply high such that the internal V_{REG} voltage is above the controller's $V_{VREG(UVLOH)}$ threshold voltage, an elapsed POR timer, and with the ENABLE input LOW, a weak current sink at the GATE pin attempts to hold the GATE voltage at 0V. If there is a DG short on the MOSFET, the weak current sink is not capable of holding the voltage at 0V as the GATE voltage tracks the MOSFET's DRAIN voltage. The voltage monitor circuit at the controller's GATE pin will be triggered once the GATE voltage crosses the $V_{GATEFT(EXT)}$ threshold voltage. The HW_FLT digital output is subsequently asserted within a delay approximately equal to the delay in the logic circuits – no additional timing circuit is required. To clear the latched GATE voltage monitor circuit and to reset the HW_FLT digital output, the applied V_{CC} supply voltage must fall such that V_{REG} is below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

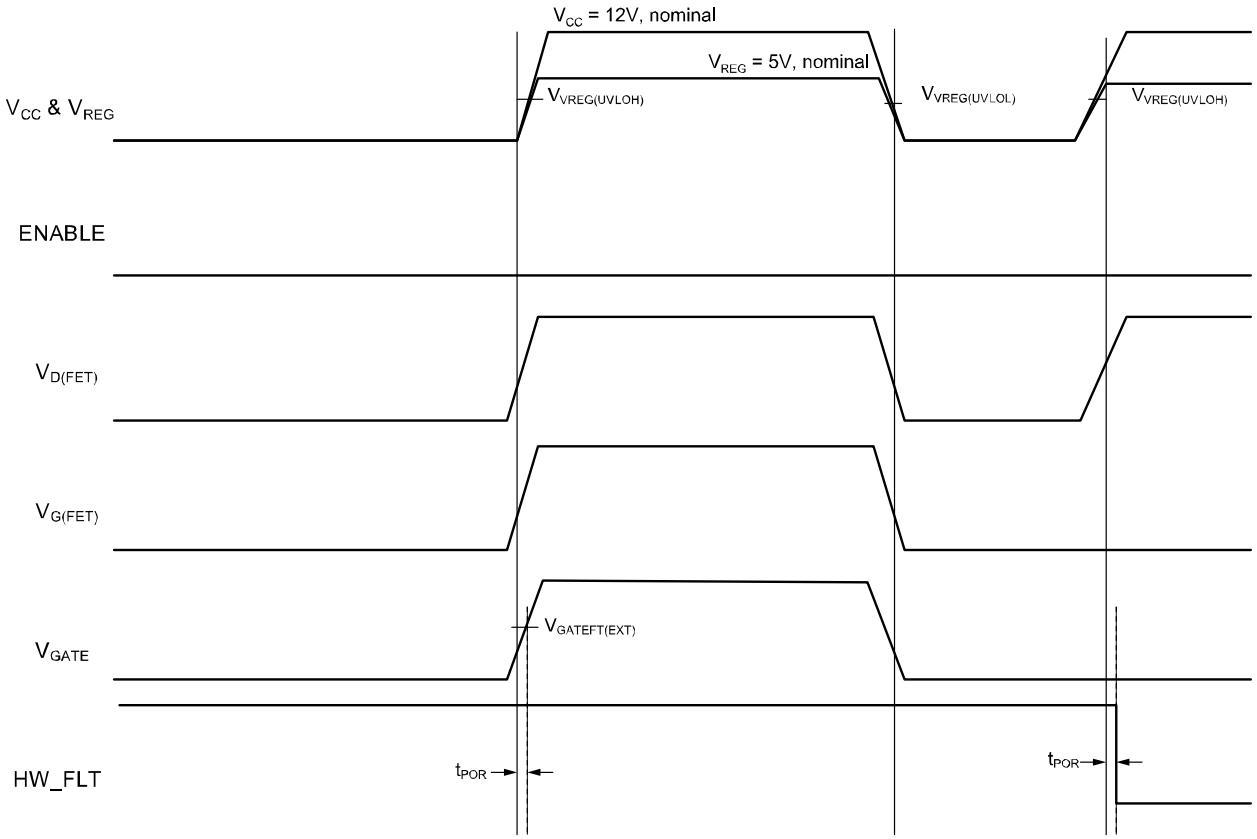


Figure 7. Hardware Fault Detection of a MOSFET DG Short with ENABLE = LOW

HW_FLT Digital Output Asserted by MOSFET DS Short with ENABLE = LOW

In order to protect the system from the result of the installation of a damaged MOSFET on the PCB, the controller incorporates a MOSFET shorted DS detection scheme whose operation is described in Figure 8. With the applied V_{CC} supply high such that the internal V_{REG} voltage is above the controller's $V_{VREG(UVLOH)}$ threshold voltage, an elapsed POR timer, and with the ENABLE input LOW, a voltage monitor circuit for the controller's SOURCE pin is enabled. If there is a DS short on the MOSFET, the external load on the MOSFET is not capable of holding the voltage at 0V as the SOURCE voltage tracks the MOSFET's DRAIN voltage. The voltage monitor circuit at the controller's SOURCE pin will be triggered once the SOURCE voltage crosses the $V_{SRCFT(EXT)}$ threshold voltage. The HW_FLT digital output is subsequently asserted within a delay approximately equal to the delay in the logic circuits – no additional timing circuit is required. To clear the latched source voltage monitor circuit and to reset the HW_FLT digital output, the applied V_{CC} supply voltage must fall such that V_{REG} is below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

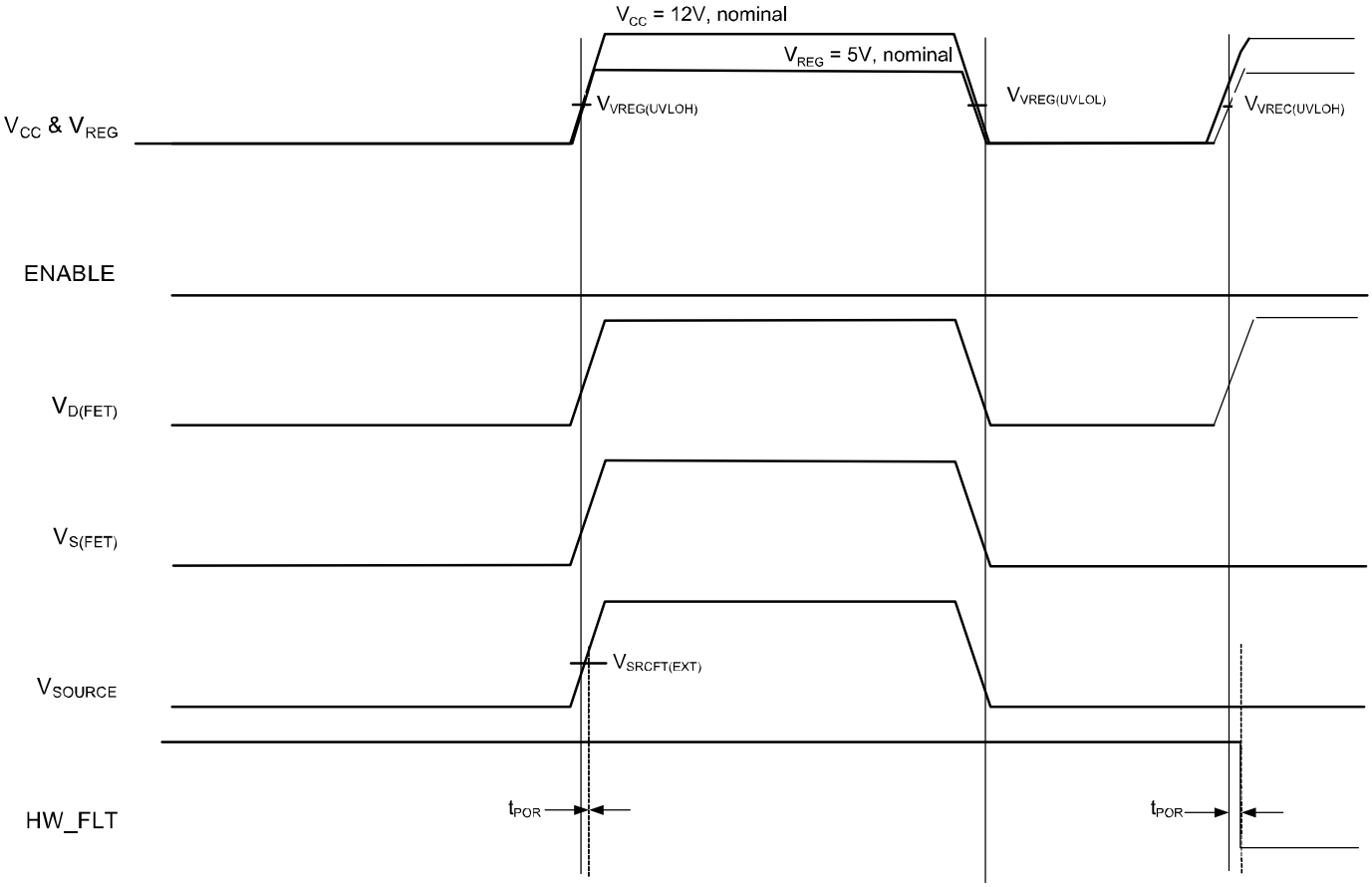


Figure 8. Hardware Fault Detection of a MOSFET DS Short with ENABLE = LOW

HW_FLT Asserted by MOSFET DS Short after Steady-state Operation then ENABLE = HIGH-to-LOW

Figure 9 illustrates the behavior of the controller to a shorted DS MOSFET condition after steady-state operation is achieved via a nominal start-up. Note that the load capacitor at start-up was charged in a controlled dI_D/dt mode and assertion of the controller's PWRGD digital output occurs when the output load voltage profile is higher than the controller's V_{PGH} threshold voltage and the V_{GS} of the external MOSFET is higher than the controller's V_{GSPGH} threshold voltage. Upon the application of a HIGH-to-LOW transition on ENABLE by the service processor, the GATE drive circuit is disabled, the weak GATE current sink is enabled, the DISCH output goes high, and the $t_{DS-SSFAULT}$ timer is started. With the ENABLE input LOW, a voltage monitor circuit for the controller's SOURCE pin (i.e., V_{OUT}) is enabled. If there is a DS short, the voltage at the source will not drop to 0V even though the GATE is OFF. If the output voltage at the SOURCE pin remains higher than the controller's $V_{SRCFT(EXT)}$ threshold voltage when the $t_{DS-SSFAULT}$ timer terminates, the HW_FLT digital output is asserted. To repair the damaged MOSFET and to reset the HW_FLT digital output and the controller, the service processor instructs the main supply to turn off the V_{CC} supply voltage to the controller such that V_{REG} falls below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

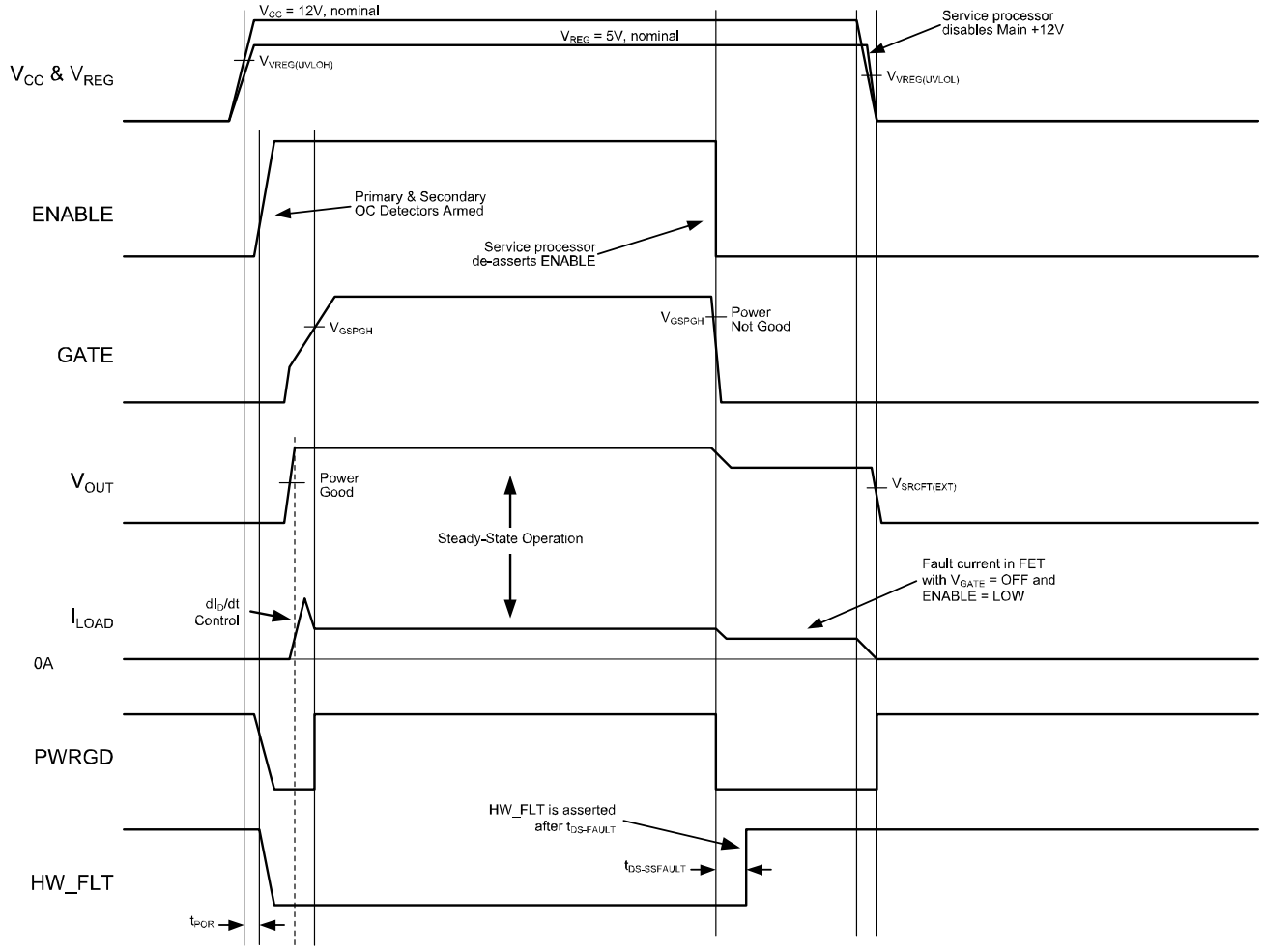


Figure 9. Hardware Fault by a MOSFET DS Short after Steady-State Operation (ENABLE = HIGH-to-LOW)

HW_FLT Asserted by MOSFET DS Short after Steady-state Operation then a Fault Condition

Figure 10 illustrates the behavior of the controller to a shorted DS MOSFET condition after steady-state operation is achieved via a nominal start-up. With the occurrence of one of the following fault conditions – UVLO, OVP, primary OC, secondary OC, open LOADSENSE, or open GNDSENSE - the GATE drive circuit is disabled, the GATE fault-mode pull-down current sink is enabled, the DISCH output goes high, and the $t_{DS-SSFAULT}$ timer is started. The occurrence of a primary OC fault condition is shown here. The voltage monitor circuit for the controller's SOURCE pin is also enabled. If there is a DS short, the voltage at the source will not drop to 0V even though the GATE is OFF. If the output voltage at the SOURCE pin remains higher than the controller's $V_{SRCFT(EXT)}$ threshold voltage when the $t_{DS-SSFAULT}$ timer terminates, the HW_FLT digital output is asserted. To repair the damaged MOSFET and to reset the HW_FLT digital output and the controller, the service processor instructs the main supply to turn off the V_{CC} supply voltage to the controller such that V_{REG} falls below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

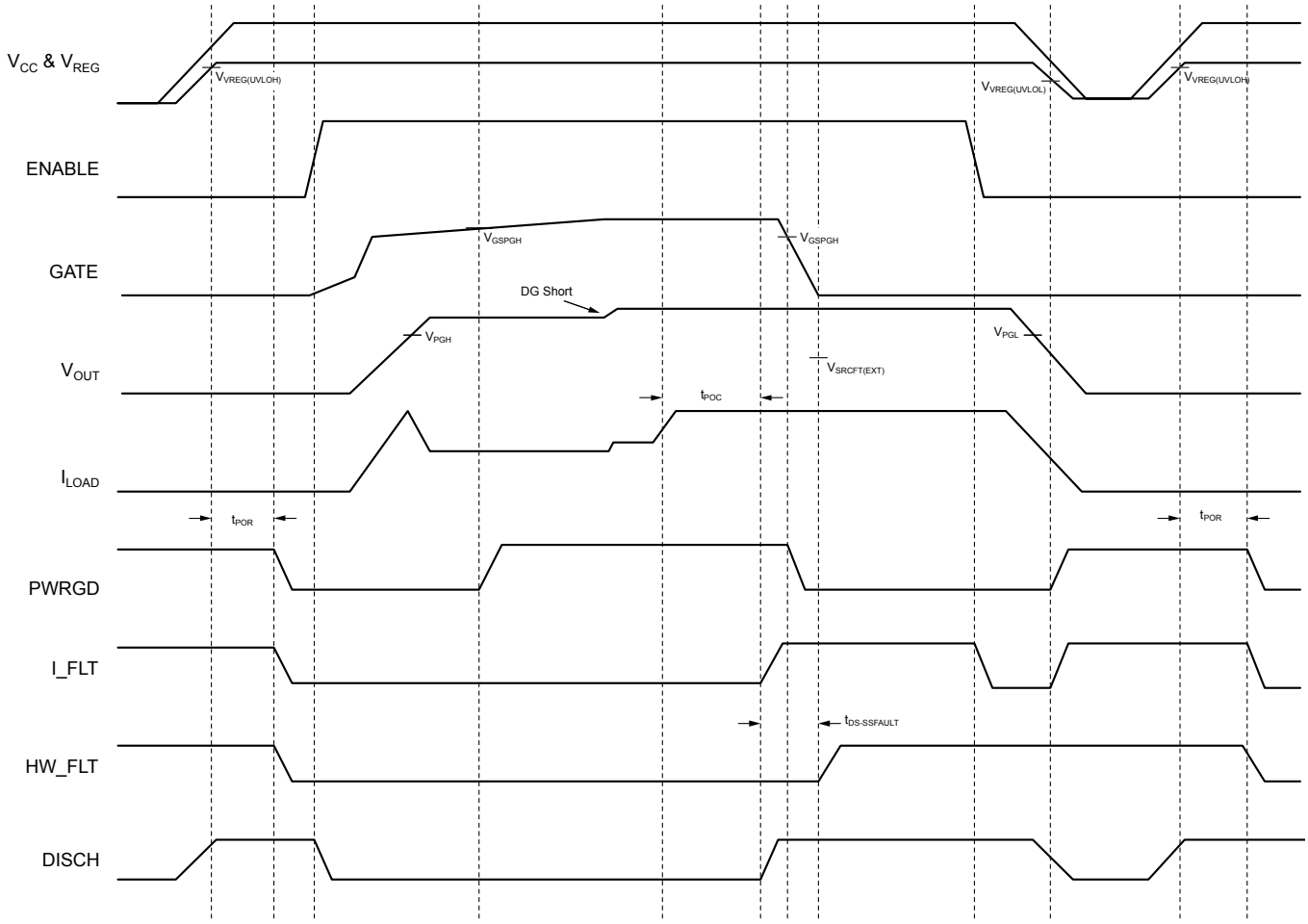


Figure 10. HW_FLT Asserted by a MOSFET DS Short after Steady-State Operation then a Fault Condition

Shorted R_{SENSE} Detector Trips CB and Asserts HW_FLT

In order to protect the system from the result of the installation of a shorted sense resistor on the PCB, which would increase the effective OC detection thresholds to unsafe levels, the controller incorporates a shorted R_{SENSE} detection scheme whose operation is described in Figure 11. The R_{SENSE} detection circuitry is enabled upon the application of an ENABLE LOW-to-HIGH transition, an elapsed POR timer, and the V_{GS} of the external MOSFET being higher than the controller's V_{GSPGH} threshold voltage. Note that for the case of a shorted sense resistor, dI_D/dt control of the inrush current is disabled and the controller defaults to dV_{GATE}/dt control of the GATE voltage.

An R_{SENSE} short is detected by comparing the V_{RS} voltage drop across the sense resistor

($V_{CCSENSE}$-V_{SENSE}) to the V_{DS} voltage drop across the external MOSFET (V_{SENSE}-V_{SOURCE}). To avoid a false R_{SENSE} short detection at low current, a minimum V_{DS} of $\Delta V_{DS(FET)}$ must exist across the external MOSFET for a shorted sense resistor to be detected. For larger values of V_{DS} across the external MOSFET generated by higher load currents, the ΔV_{RSENSE} threshold voltage for the detection of an R_{SENSE} short follows the equation $\Delta V_{RSENSE} = 0.5 * (V_{DS} - \Delta V_{DS(FET)})$. If there exists a short across the sense resistor such that V_{RS} drops below the ΔV_{RSENSE} threshold voltage, then an internal circuit breaker is tripped, the GATE drive circuit is disabled, the GATE fault-mode pull-down current sink is enabled, the DISCH output goes high, and the HW_FLT digital output is asserted. To repair the damaged sense resistor and reset the HW_FLT digital output, the service processor instructs the main supply to turn off the V_{CC} supply voltage to the controller such that V_{REG} falls below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

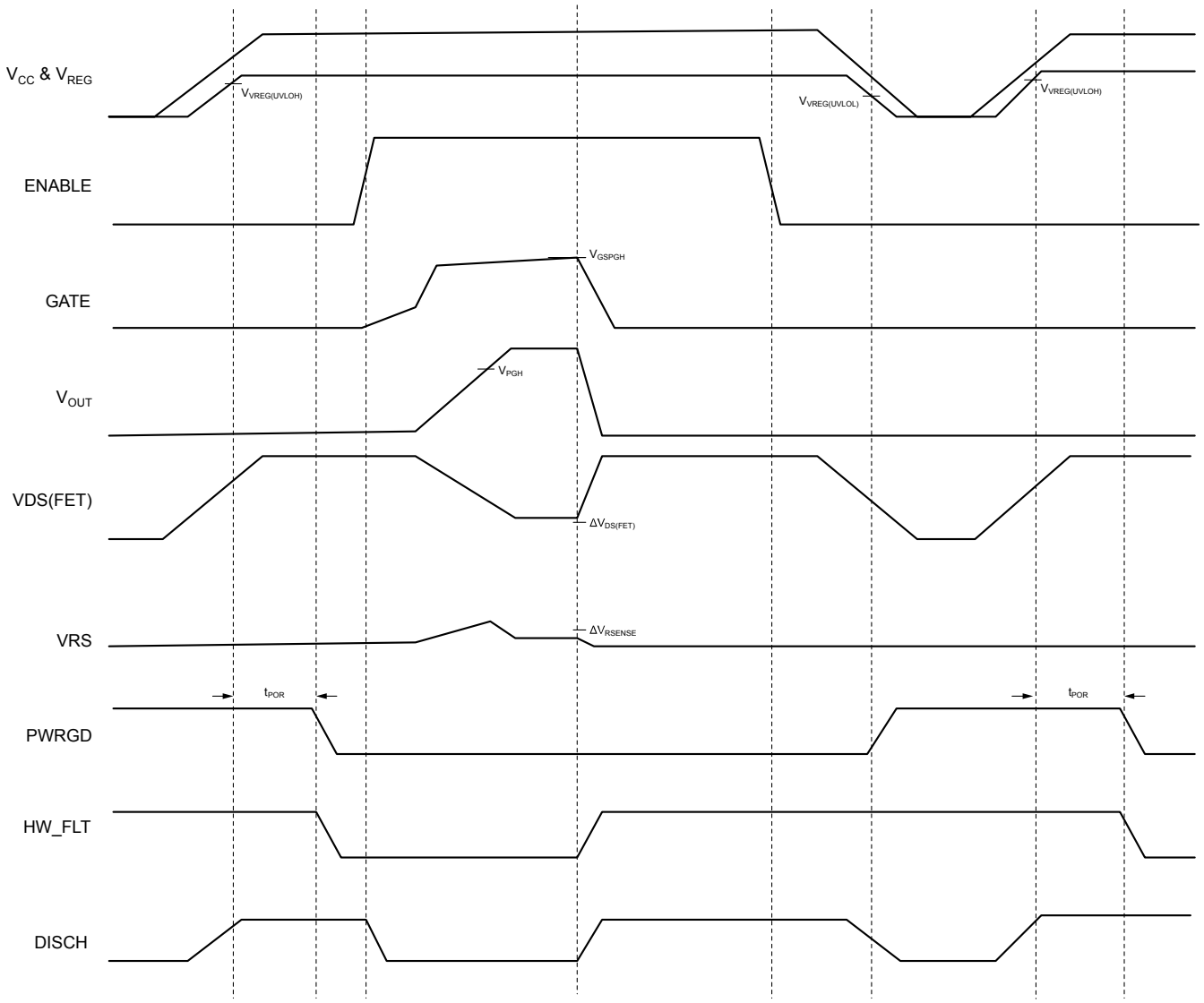


Figure 11. Shorted R_{SENSE} Trips Circuit Breaker and Asserts HW_FLT

Shorted $C_{PRIMARY}$ Detector Asserts HW_FLT at Start-up

In order to protect the system from the result of the installation of a shorted or excessively large $C_{PRIMARY}$ capacitor on the PCB, the controller incorporates a shorted $C_{PRIMARY}$ detection scheme. A shorted CPRIMARY pin or an excessively large $C_{PRIMARY}$ capacitor will impact the primary OC detection time, t_{POC}. The operation of the shorted $C_{PRIMARY}$ detection scheme at start-up is described in Figure 12. Prior to power-up, the CPRIMARY pin is discharged to 0V. As the applied V_{CC} supply and the internal V_{REG} voltage rise, a 3mA current source is applied to the CPRIMARY pin to charge $C_{PRIMARY}$ to V_{REG}. When the internal V_{REG} voltage is above the controller's $V_{VREG(UVLOH)}$ threshold voltage, the t_{POR} timer is initiated. For the case of a reasonable $C_{PRIMARY}$ capacitor value, one which keeps the primary OC response time, t_{POC}, less than 0.5s, $C_{PRIMARY}$ charges above V_{PRIH} before the POR timer terminates and normal operation commences. However, if the CPRIMARY pin is shorted to GND or $C_{PRIMARY}$ is too large, as in this timing diagram, the POR timer terminates before $C_{PRIMARY}$ charges above V_{PRIH} and a shorted $C_{PRIMARY}$ is detected. When a $C_{PRIMARY}$ short is detected, the GATE drive circuit and the DISCH output are not affected, however, the HW_FLT digital output is asserted. To repair the damaged $C_{PRIMARY}$ capacitor and reset the HW_FLT digital output, the service processor instructs the main supply to turn off the V_{CC} supply voltage to the controller such that V_{REG} falls below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

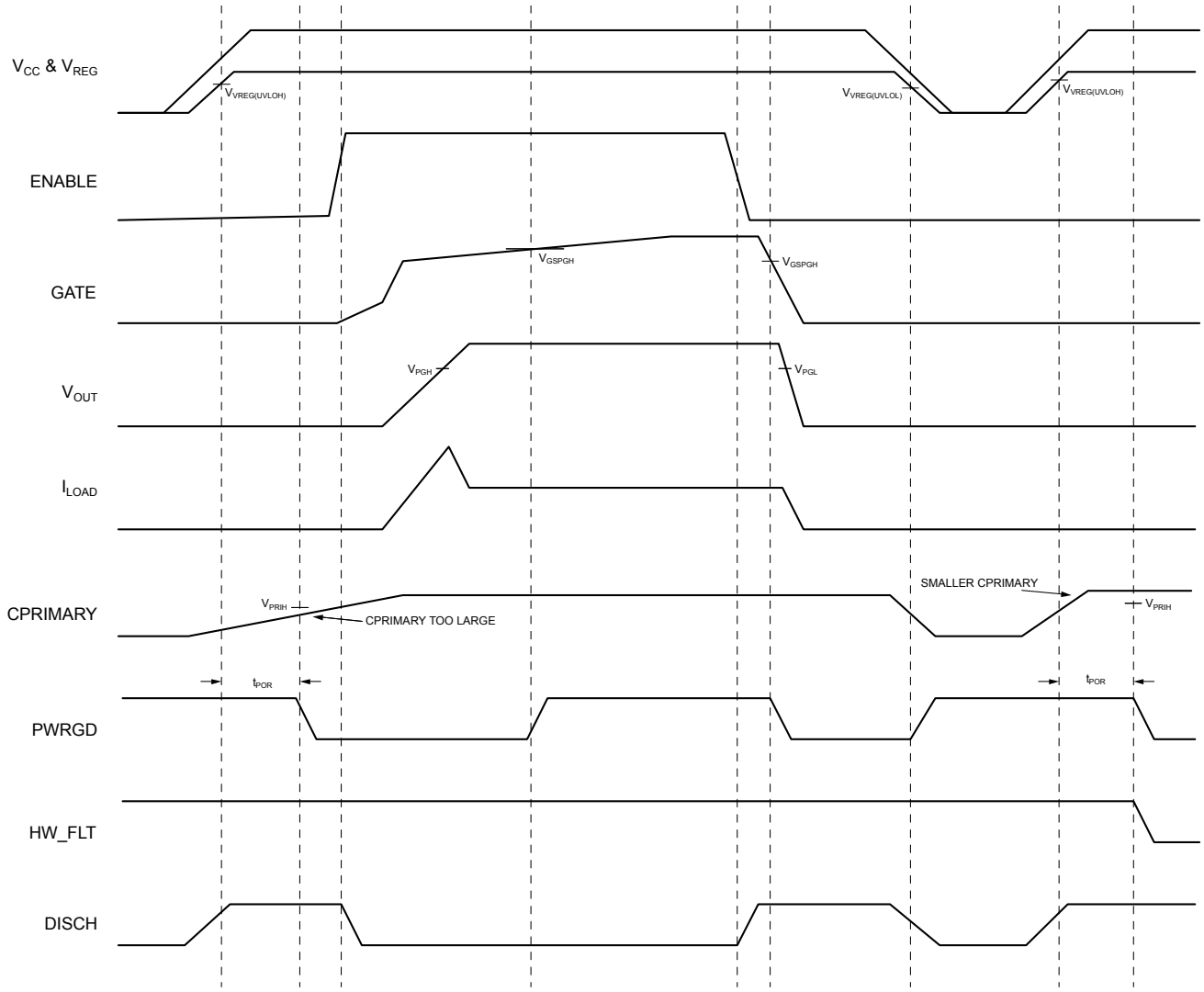


Figure 12. Shorted $C_{PRIMARY}$ Detector Asserts HW_FLT at Start-up

Shorted $C_{PRIMARY}$ Detector Asserts HW_FLT during Steady-state

Figure 13 illustrates the behavior of the controller to a shorted $C_{PRIMARY}$ capacitor condition after steady-state operation is achieved via a nominal start-up. If a $C_{PRIMARY}$ short occurs during steady-state operation, the CPRIMARY pin voltage will drop below the V_{PRIL} threshold voltage and a shorted $C_{PRIMARY}$ is detected. When a $C_{PRIMARY}$ short is detected, the GATE drive circuit remains enabled and the DISCH output remains low such that the external MOSFET remains ON, however, the HW_FLT digital output is asserted. To repair the damaged $C_{PRIMARY}$ capacitor and reset the HW_FLT digital output, the service processor instructs the main supply to turn off the V_{CC} supply voltage to the controller such that V_{REG} falls below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

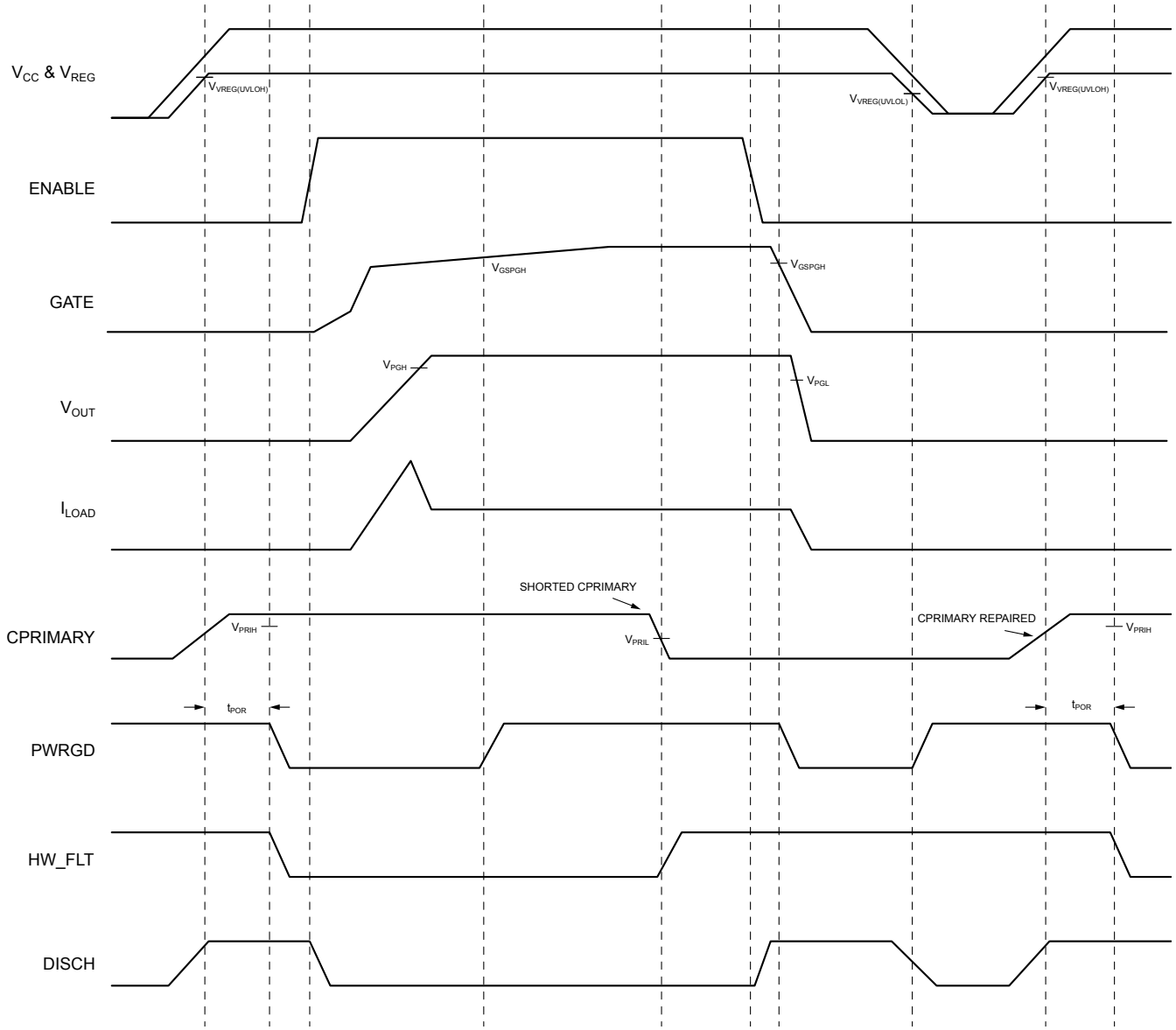


Figure 13. Shorted $C_{PRIMARY}$ Detector Asserts HW_FLT During Steady-State

Shorted $C_{PRIMARY}$ Detector Asserts HW_FLT After Primary OC Event

The diagram in Figure 14 illustrates the behavior of the controller to a shorted $C_{PRIMARY}$ capacitor condition after steady-state operation is achieved via a nominal start-up and after a primary OC event has occurred. As described previously, during a primary OC event, the $C_{PRIMARY}$ capacitor is discharged as part of setting the primary OC detector response time, t_{POC}. In order to prevent a false $C_{PRIMARY}$ short detection from occurring while the CPRIMARY pin is being intentionally discharged, the $C_{PRIMARY}$ short detection circuit is disabled when the primary OC detector detects an overcurrent. In addition, the $C_{PRIMARY}$ short detection circuit is not re-enabled until after a time delay, $t_{SCPDETPOR}$, once the primary OC detector no longer detects an overcurrent. This delay time should allow a capacitor of reasonable size to be charged back up above V_{PRIH}, even if it has been discharged to 0V, such that a false $C_{PRIMARY}$ short is not indicated when the $C_{PRIMARY}$ short detection circuitry is re-enabled.

In the timing diagram, $C_{PRIMARY}$ becomes shorted during the primary OC event. When the CPRIMARY pin voltage falls below V_{PRIL}, the $t_{POCSENSE}$ timer is enabled. Once this timer times out, the circuit breaker is tripped, I_FLT is asserted, the GATE drive circuitry is disabled, the GATE fault-mode pull-down current sink is enabled, and the DISCH output goes high. As the external MOSFET is turned OFF, the output current drops and an overcurrent condition is no longer detected. This initiates the $t_{SCPDETPOR}$ timer. Since $C_{PRIMARY}$ does not charge back up above V_{PRIH} before this timer expires, HW_FLT is asserted after the $t_{SCPDETPOR}$ time. To repair the damaged $C_{PRIMARY}$ capacitor and reset the HW_FLT digital output, the service processor instructs the main supply to turn off the V_{CC} supply voltage to the controller such that V_{REG} falls below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

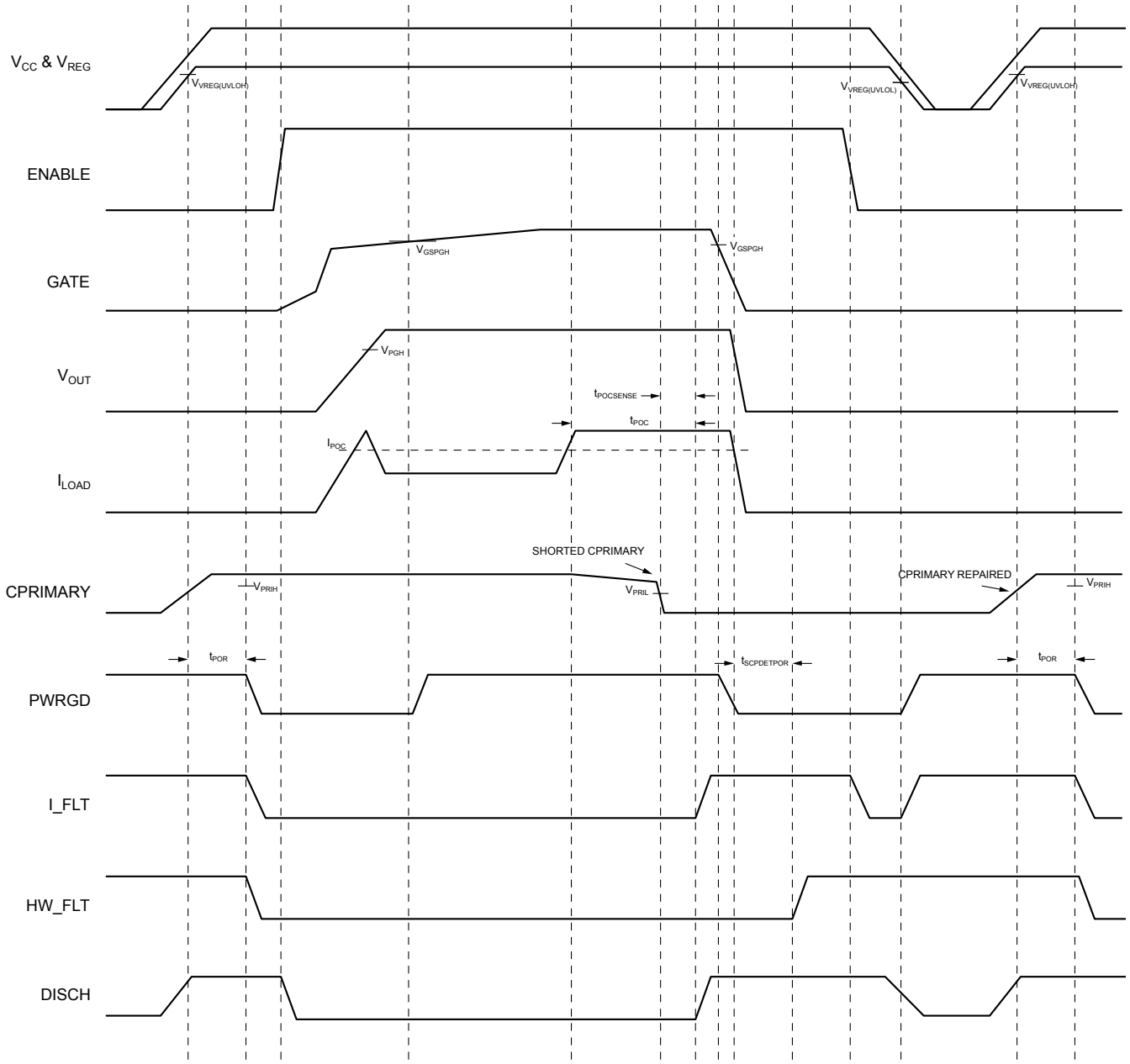


Figure 14. Shorted $C_{PRIMARY}$ Detector Asserts HW_FLT after Primary OC Event

Open LOADSENSE Detector Trips CB

In order to protect the system from the result of an open LOADSENSE pin, the controller incorporates an open LOADSENSE detection scheme. An open LOADSENSE pin could result in the effective primary OC detection threshold being at an unsafe level. The timing diagram in Figure 15 describes the operation of this function. With the applied V_{CC} supply high such that the internal V_{REG} voltage is above the controller's $V_{VREG(UVLOH)}$ threshold voltage, an elapsed POR timer, and with the application of an ENABLE LOW-to-HIGH transition, the GATE drive circuitry is enabled and the GATE voltage begins to rise. As the external MOSFET turns ON, the SOURCE voltage begins to rise also. Normally, the LOADSENSE voltage would rise with the SOURCE voltage. However, if the LOADSENSE pin is open, the LOADSENSE voltage will remain at a lower voltage due to the load of other internal circuitry. An open LOADSENSE pin is detected by comparing the voltage at the SOURCE pin to the voltage at the LOADSENSE pin. Once the voltage at the SOURCE pin differs from the voltage at the LOADSENSE pin by $V_{THLOADSENSE}$, a circuit breaker is tripped, the GATE drive circuitry is disabled, the GATE fault-mode pull-down current sink is enabled, and the DISCH output goes high. This circuit breaker can be reset, such that the GATE drive circuitry can be re-enabled, by either a HIGH-to-LOW transition on ENABLE or turning off the V_{CC} supply voltage to the controller such that V_{REG} falls below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

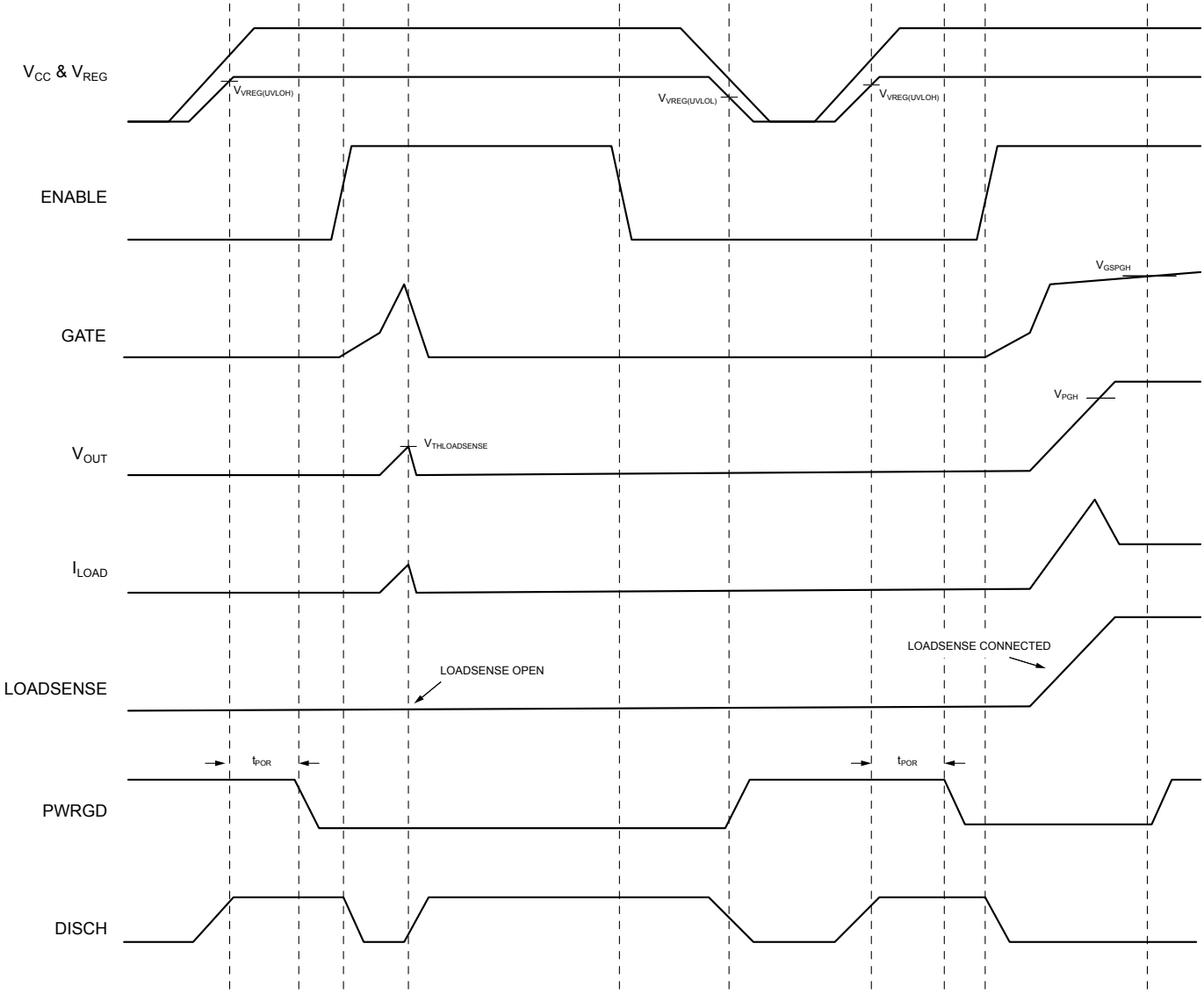


Figure 15. Open LOADSENSE Detector Trips CB

Open GNDSENSE Detector Trips CB

In order to protect the system from the result of an open GNDSENSE pin, the controller incorporates an open GNDSENSE detection scheme. An open GNDSENSE pin could result in the effective primary OC detection threshold being at an unsafe level. The timing diagram in Figure 16 describes the operation of this function. With the applied V_{CC} supply high such that the internal V_{REG} voltage is above the controller's $V_{VREG(UVLOH)}$ threshold voltage, an elapsed POR timer, and with the application of an ENABLE LOW-to-HIGH transition, the GATE drive circuitry is enabled and the GATE voltage begins to rise. As the external MOSFET turns ON, the SOURCE voltage begins to rise also and the LOADSENSE voltage follows the SOURCE voltage. Normally, the GNDSENSE pin would remain at 0V. However, if the GNDSENSE pin is open, the GNDSENSE voltage will rise due to the load of other internal circuitry. An open GNDSENSE pin is detected by comparing the voltage at the GNDSENSE pin to the voltage at the AGND pin. Once the voltage at the GNDSENSE pin differs from the voltage at the AGND pin by $V_{THGNDSENSE}$, a circuit breaker is tripped, the GATE drive circuitry is disabled, the GATE fault-mode pull-down current sink is enabled, and the DISCH output goes high. This circuit breaker can be reset, such that the GATE drive circuitry can be re-enabled, by either a HIGH-to-LOW transition on ENABLE or turning off the V_{CC} supply voltage to the controller such that V_{REG} falls below the controller's $V_{VREG(UVLOL)}$ threshold voltage.

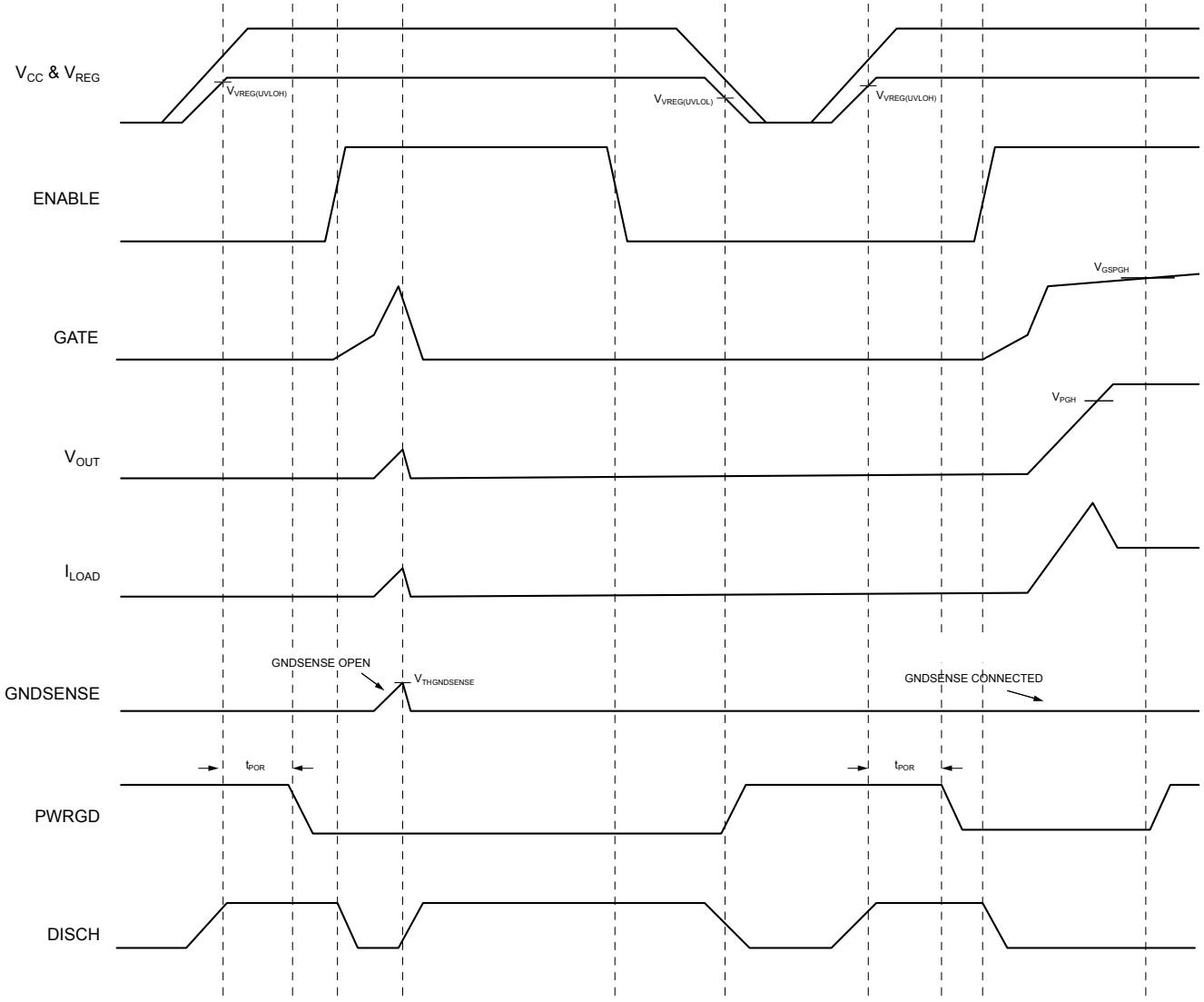


Figure 16. Open GNDSENSE Detector Trips CB

UVLO and OVP Operation

The system can be protected against an under-voltage condition or an over-voltage condition on the V_{CC} supply by using an external resistor divider and the UVLO and OVP pins, respectively. Figure 17 illustrates the timing of the GATE and digital pin outputs when the input supply crosses the UVLO and OVP thresholds. When the voltage applied to the UVLO pin is less than the V_{UVLOL} threshold voltage or the voltage applied to the OVP pin is greater than the V_{OVPH} threshold voltage, the GATE drive circuitry is disabled, the GATE fault-mode pull-down current sink is enabled, and the DISCH output goes high. Increasing V_{CC} such that the voltage applied to the UVLO pin increases above V_{UVLOH} or decreasing V_{CC} such that the voltage applied to the OVP decreases below V_{OVPL} re-enables the GATE drive circuit and forces the DISCH output low, allowing the controller to return to normal operation.

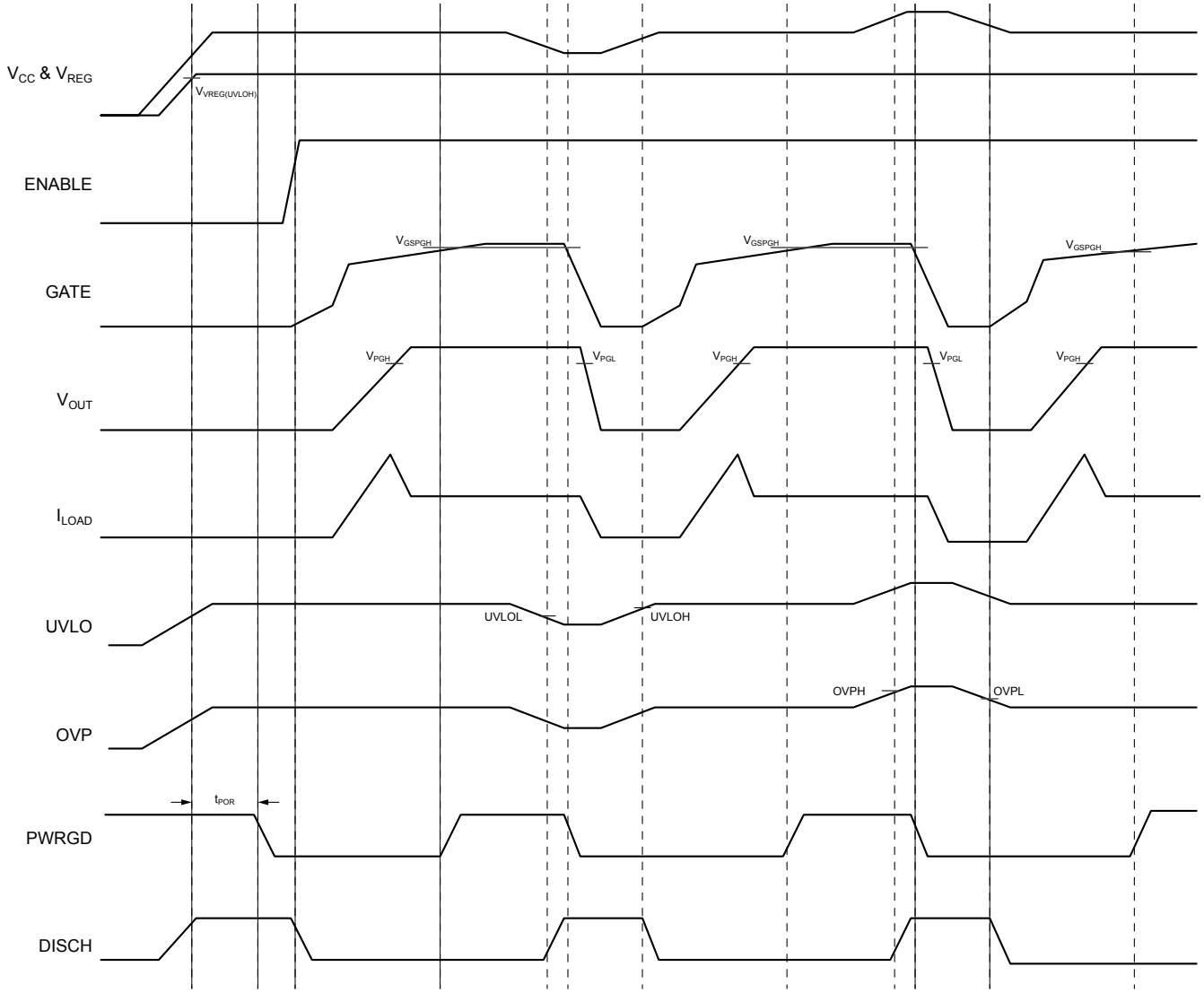


Figure 17. UVLO and OVP Operation

VISS Output Operation

The VISS output provides a voltage which is proportional to the output current flowing in the external sense resistor. Figure 18 illustrates the operation of this output. With the applied V_{CC} supply high such that the internal V_{REG} voltage is above the controller's $V_{VREG(UVLOH)}$ threshold voltage, an elapsed POR timer, and with the application of an ENABLE LOW-to-HIGH transition, the GATE drive circuitry is enabled. When the output load voltage profile is higher than the controller's V_{PGH} threshold voltage and the V_{GS} of the external MOSFET is higher than the controller's V_{GSPGH} threshold voltage, the PWRGD digital output is asserted and the VISS output becomes active. The current flowing in the external sense resistor is determined by sensing the voltage across the sense resistor ($V_{CCSENSE}$-V_{SENSE}). As the output current varies under changing load conditions, $V_{CCSENSE}$-V_{SENSE} also varies and the VISS output voltage changes proportionally according to $V_{ISS(SENS)}$. When the external MOSFET is disabled, either by a HIGH-to-LOW transition on ENABLE or due to a fault condition, the V_{GS} of the external MOSFET falls below the controller's V_{GSPGH} threshold voltage. This causes the PWRGD digital output to be de-asserted and the VISS output to be disabled.

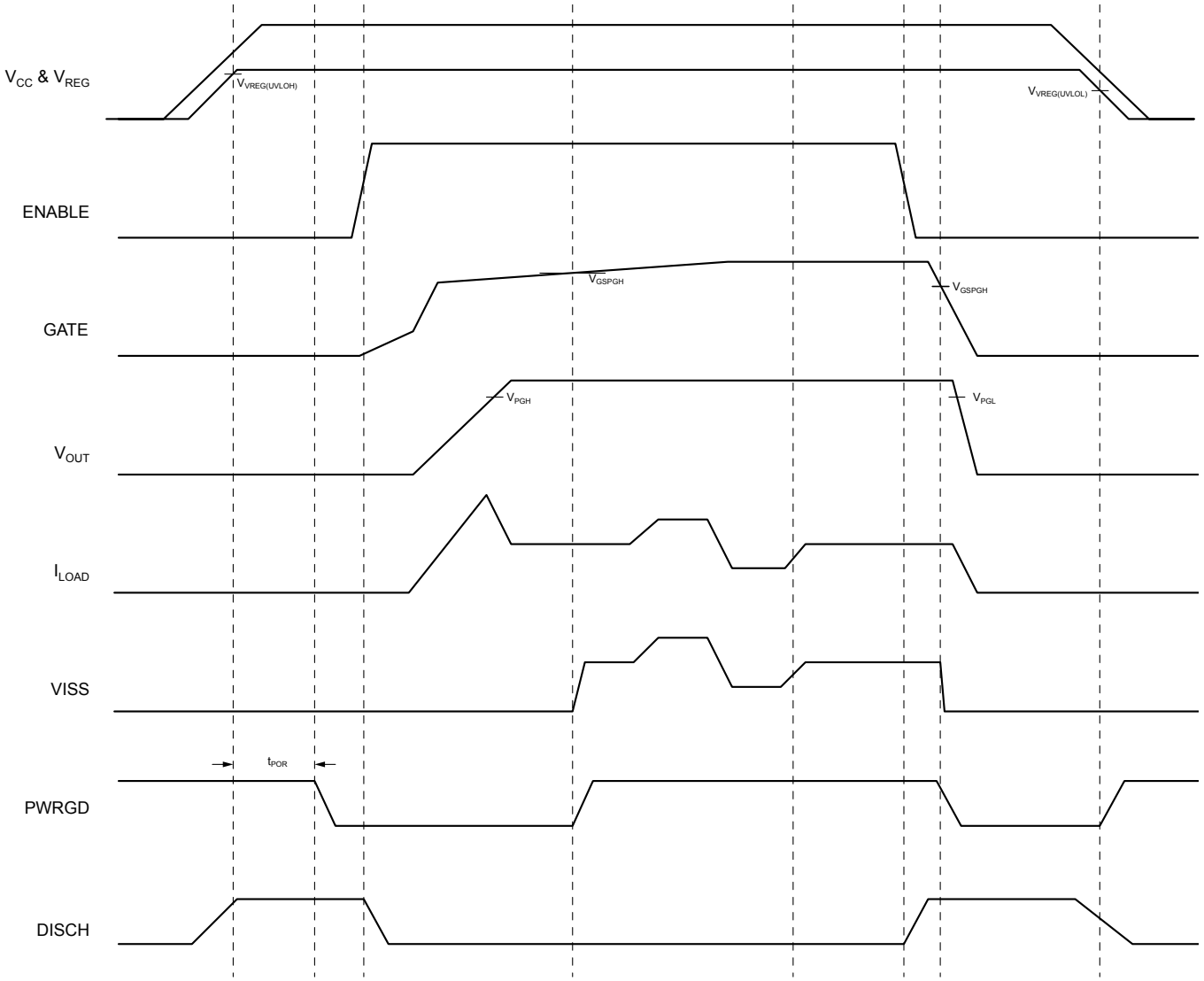
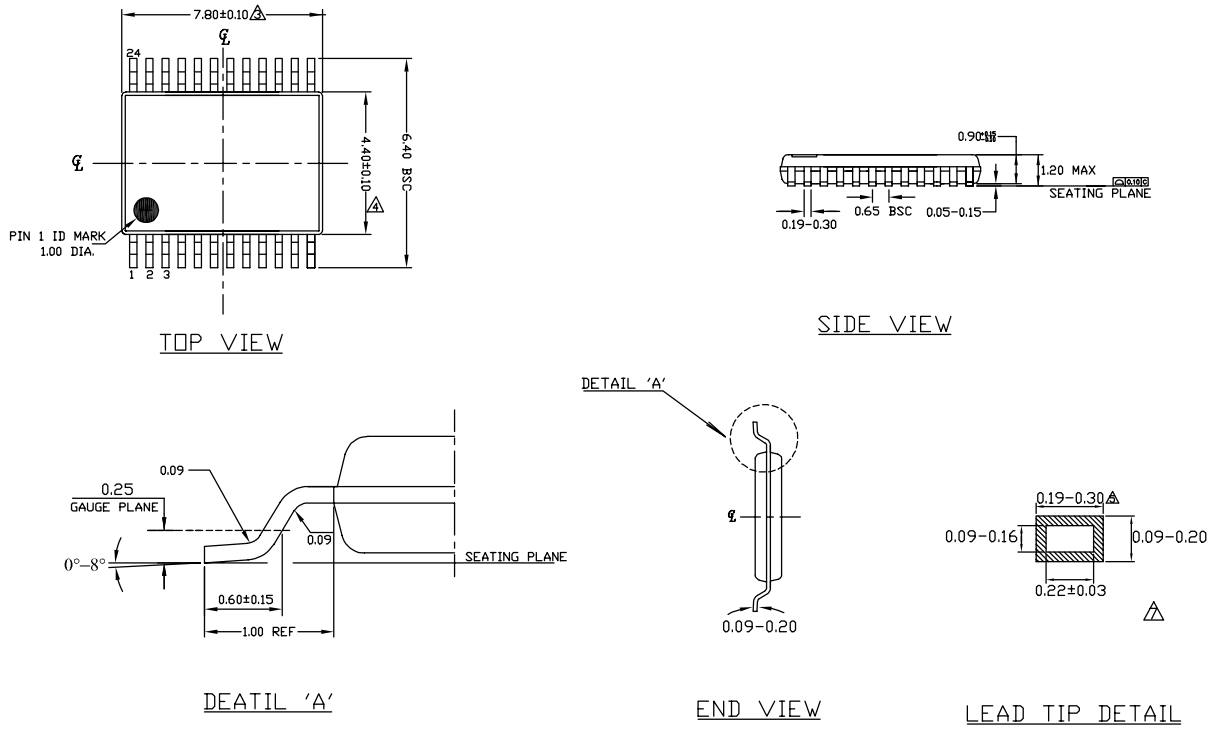


Figure 18. VISS Operation

Applications Information

The MIC2310 can be configured to address power-limiting applications other than the 240-VA power control (UL60950 Safe Power Handling Systems). There are two key requirements to consider in selecting the external components for use in various power-limit applications: 1) The value (and tolerance) of the R_{SENSE} current sensing resistor; and 2) The $R_{DS(ON)}$ of the external Power MOSFET. These two components are vital with regards to the shorted R_{SENSE} detection scheme such that the values of each need to be chosen such that variations in $R_{DS(ON)}$ and R_{SENSE} over process, supply, and temperature does not result in a false R_{SENSE} short detection. In short, the value of $R_{DS(ON)}$ of the external MOSFET should be selected to not exceed twice the value of R_{SENSE} over process, supply, and temperature, to avoid the generation of a false R_{SENSE} short detection.

Package Information



Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH ,PROTRUSIONS OR GATE BURRS.
4. DIMENSION DOES NOT INCLUDE INTERNAL FLASH OR PROTRUSION.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
6. CROSS SECTION TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.

24-Pin TSSOP (TS)

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