

## 1.8-V to 5-V DUAL UART WITH 64-BYTE FIFOS

### FEATURES

- Larger FIFOs Reduce CPU Overhead
- Programmable Auto-RTS and Auto-CTS
- In Auto-CTS Mode, CTS Controls the Transmitter
- In Auto-RTS Mode, RCV FIFO Contents, and Threshold Control RTS
- Serial and Modem Control Outputs Drive a RJ11 Cable Directly When Equipment is on the Same Power Drop
- Capable of Running With All Existing TL16C450 Software
- After Reset, All Registers Are Identical to the TL16C450 Register Set
- Up to 48-MHz Clock Rate for up to 3-Mbps (Standard 16× Sampling) Operation, or up to 6-Mbps (Optional 8× Sampling) Operation With  $V_{CC} = 5\text{ V}$  Nominal
- Up to 32-MHz Clock Rate for up to 2-Mbps (Standard 16× Sampling) Operation, or up to 4-Mbps (Optional 8× Sampling) Operation With  $V_{CC} = 3.3\text{ V}$  Nominal
- Up to 24-MHz Clock Rate for up to 1.5-Mbps (Standard 16× Sampling) Operation, or up to 3-Mbps (Optional 8× Sampling) Operation With  $V_{CC} = 2.5\text{ V}$  Nominal
- Up to 16-MHz Clock Rate for up to 1-Mbps (Standard 16× Sampling) Operation, or up to 2-Mbps (Optional 8× Sampling) Operation With  $V_{CC} = 1.8\text{ V}$  Nominal
- In TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data
- Programmable Baud-Rate Generator Allows Division of Any Input Reference Clock by 1 to  $(2^{16} - 1)$  and Generates an Internal 16× Clock
- Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream
- 5-V, 3.3-V, 2.5-V, and 1.8-V Operation
- Independent Receiver Clock Input
- Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled
- Fully Programmable Serial Interface Characteristics
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 = -, or 2-Stop Bit Generation
  - Baud Generation (DC to 1 Mbit/s)
- False-Start Bit Detection
- Complete Status Reporting Capabilities
- 3-State Output TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, and Framing Error Simulation
- Fully Prioritized Interrupt System Controls
- Modem Control Functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Available in 44-Pin PLCC (FN) or 32-Pin QFN (RHB) Packages
- Each UART's Internal Register Set May Be Written Concurrently to Save Setup Time
- Multifunction (MF) Output Allows Users to Select Among Several Functions, Saving Package Pins

### APPLICATIONS

- Point-of-Sale Terminals
- Gaming Terminals
- Portable Applications
- Router Control
- Cellular Data
- Factory Automation



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## DESCRIPTION

The TL16C2752 is a speed and functional upgrade of the TL16C2552. Since they are pinout and software compatible, designs can easily migrate from the TL16C2552 to the TL16C2752 if needed. The additional functionality within the TL16C2752 is accessed via an extended register set. Some of the key new features are larger receive and transmit FIFOs, embedded IrDA encoders and decoders, RS-485 transceiver controls, software flow control (Xon/Xoff) modes, programmable transmit FIFO thresholds, extended receive and transmit threshold levels for interrupts, and extended receive threshold levels for flow control halt/resume operation.

The TL16C2752 is a dual universal asynchronous receiver and transmitter (UART). It incorporates the functionality of two independent UARTs: each UART having its own register set and transmit and receive FIFOs. The two UARTs share only the data bus interface and clock source, otherwise they operate independently. Another name for the UART function is asynchronous communications element (ACE), and these terms will be used interchangeably. The bulk of this document describes the behavior of each ACE, with the understanding that two such devices are incorporated into the TL16C2752.

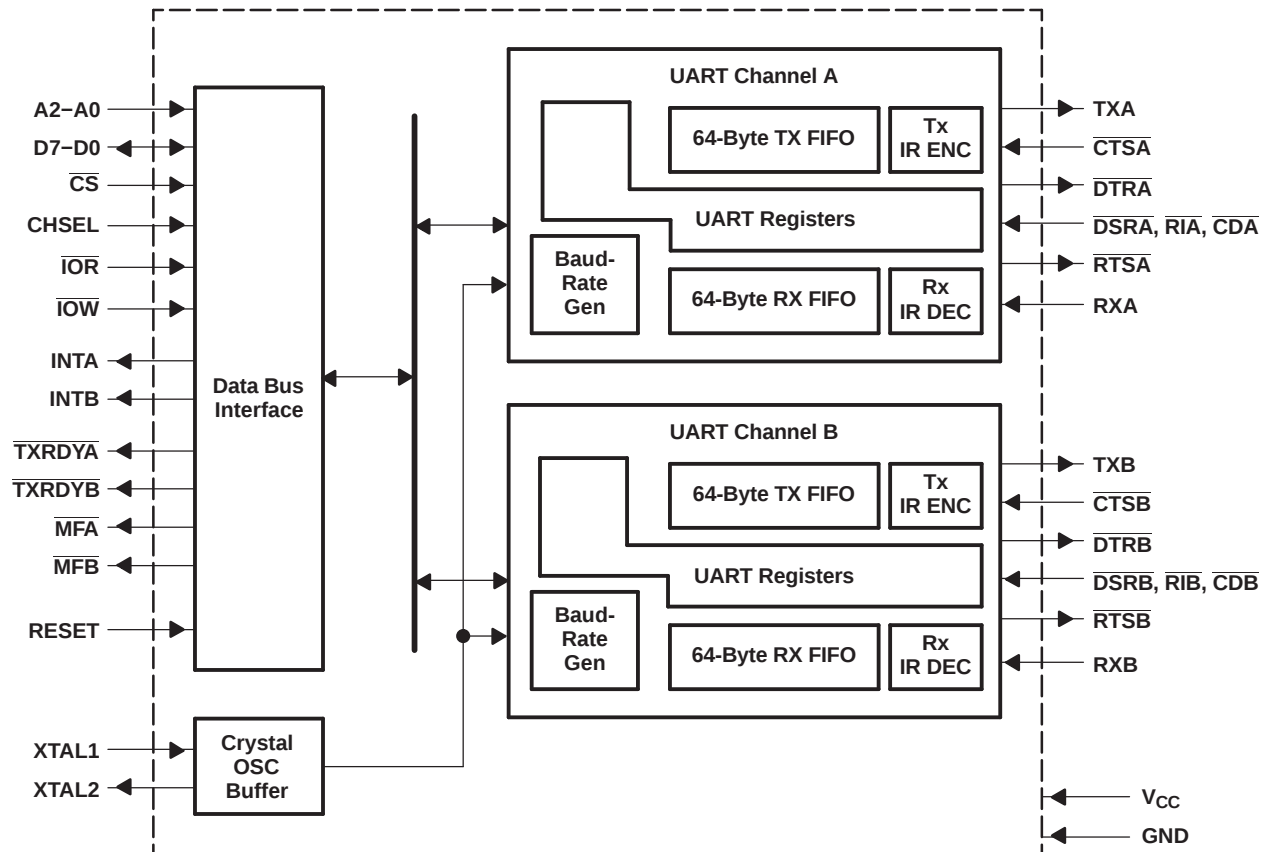
Functionally equivalent to the TL16C450 on power up or reset (single character or TL16C450 mode), each ACE can be placed in an alternate FIFO mode. This relieves the CPU of excessive software overhead by buffering received and to-be-transmitted characters. Each receiver and transmitter store up to 64 bytes in their respective FIFOs, with the receive FIFO including three additional bits per byte for error status. In the FIFO mode, selectable hardware or software autoflow control features can significantly reduce program overload and increase system efficiency by automatically controlling serial data flow.

Each ACE performs serial-to-parallel conversions on data received from a peripheral device or modem and stores the parallel data in its receive buffer or FIFO, and each ACE performs parallel-to-serial conversions on data sent from its CPU after storing the parallel data in its transmit buffer or FIFO. The CPU can read the status of either ACE at any time. Each ACE includes complete modem control capability and a processor interrupt system that can be tailored to the application.

Each ACE includes a programmable baud rate generator capable of dividing a reference clock with divisors of from 1 to 65535, thus producing a 16× or 8× internal reference clock for the transmitter and receiver logic. Each ACE accommodates up to a 3-Mbaud serial data rate (48-MHz input clock). As a reference point, that speed would generate a 333-ns bit time and a 3.33-μs character time (for 8,N,1 serial data), with the internal clock running at 48 MHz and 16× sampling.

Each ACE has a  $\overline{\text{TXRDY}}$  and  $\overline{\text{RXRDY}}$  (via  $\overline{\text{MF}}$ ) output that can be used to interface to a DMA controller.

## TL16C2752 Block Diagram



A.  $\overline{MF}$  output allows selection of  $\overline{OP}$ ,  $\overline{BAUDOUT}$ , or  $\overline{RXRDY}$  per channel.

### TERMINAL FUNCTIONS

| TERMINAL                                               |            |                   | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------------------------------------|------------|-------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                   | FN NO.     | RHB NO.           |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| A0                                                     | 10         | 3                 | I   | Address 0 select bit. Internal registers address selection.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| A1                                                     | 14         | 6                 | I   | Address 1 select bit. Internal registers address selection.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| A2                                                     | 15         | 7                 | I   | Address 2 select bit. Internal registers address selection.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| $\overline{\text{CDA}}$ ,<br>$\overline{\text{CDB}}$   | 42,<br>30  | —                 | I   | Carrier detect (active low). These inputs are associated with individual UART channels A and B. A low on these pins indicates that a carrier has been detected by the modem for that channel. The state of these inputs is reflected in the modem status register (MSR). These inputs should be pulled high if unused.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| CHSEL                                                  | 16         | 8                 | I   | Channel select. UART channel A or B is selected by the state of this pin when $\overline{\text{CS}}$ is a logic 0. A logic 0 on the CHSEL selects the UART channel B, while a logic 1 selects UART channel A. CHSEL could just be an address line from the user CPU such as A3. Bit 0 of the alternate function register (AFR) can temporarily override CHSEL function, allowing the user to write to both channel register simultaneously with one write cycle when $\overline{\text{CS}}$ is low. It is especially useful during the initialization routine.                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| $\overline{\text{CS}}$                                 | 18         | 10                | I   | UART chip select (active low). This pin selects channel A or B in accordance with the state of the CHSEL pin. This allows data to be transferred between the user CPU and the TL16C2752.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| $\overline{\text{CTSA}}$ ,<br>$\overline{\text{CTSB}}$ | 40,<br>28  | 25,<br>17         | I   | Clear to send (active low). These inputs are associated with individual UART channels A and B. A logic low on the CTS pins indicates the modem or data set is ready to accept transmit data from the TL16C2752. Status can be tested by reading MSR bit 4. These pins only affect the transmit and receive operations when auto CTS function is enabled through the enhanced feature register (EFR) bit 7, for hardware flow control operation. These inputs should be pulled high if unused.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| D0–D4<br>D5–D7                                         | 2–6<br>7–9 | 27–31<br>32, 1, 2 | I/O | Data bus (bidirectional). These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit (LSB) and the first data bit in a transmit or receive serial data stream.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| $\overline{\text{DSRA}}$ ,<br>$\overline{\text{DSRB}}$ | 41,<br>29  | —                 | I   | Data set ready (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem or data set is powered on and is ready for data exchange with the UART. The state of these inputs is reflected in the modem status register (MSR). These inputs should be pulled high if unused.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| $\overline{\text{DTRA}}$ ,<br>$\overline{\text{DTRB}}$ | 37,<br>27  | —                 | O   | Data terminal ready (active low). These outputs are associated with individual UART channels A and B. A logic low on these pins indicates that the TL16C2752 is powered on and ready. These pins can be controlled through the modem control register. Writing a 1 to MCR bit 0 sets the $\overline{\text{DTR}}$ output to low, enabling the modem. The output of these pins is high after writing a 0 to MCR bit 0, or after a reset.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| GND                                                    | 12, 22     | 20                |     | Signal and power ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| INTA,<br>INTB                                          | 34,<br>17  | 21,<br>9          | O   | Interrupt A and B (active high). These pins provide individual channel interrupts, INTA and INTB. INTA and INTB are enabled when MCR bit 3 is set to a logic 1, interrupt sources are enabled in the interrupt enable register (IER). Interrupt conditions include receiver errors, available receiver buffer data, available transmit buffer space, or when a modem status flag is detected. INTA and INTB are in the high-impedance state after reset.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| $\overline{\text{IOR}}$                                | 24         | 14                | I   | Read input (active-low strobe). A high-to-low transition on $\overline{\text{IOR}}$ loads the contents of an internal register defined by address bits A0–A2 onto the TL16C2752 data bus (D0–D7) for access by an external CPU.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| $\overline{\text{IOW}}$                                | 20         | 11                | I   | Write input (active-low strobe). A low-to-high transition on $\overline{\text{IOW}}$ transfers the contents of the data bus (D0–D7) from the external CPU to an internal register that is defined by address bits A0–A2 and CSA and CSB.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| NC                                                     | —          | 18, 19            |     | No internal connection                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| $\overline{\text{MFA}}$ ,<br>$\overline{\text{MFB}}$   | 35,<br>19  | —                 | O   | Multifunction. This output pin can function as the $\overline{\text{OP}}$ , $\overline{\text{BAUDOUT}}$ , or $\overline{\text{RXRDY}}$ pin. One of these output signal functions can be selected by the user-programmable bits 1–2 of the alternate function register (AFR). These signal functions are described as follows: <ol style="list-style-type: none"> <li><math>\overline{\text{OP}}</math>—When <math>\overline{\text{OP}}</math> (active low) is selected, the <math>\overline{\text{MF}}</math> pin is a logic 0 when MCR bit 3 is set to a logic 1 (see MCR bit 3). MCR bit 3 defaults to a logic 1 condition after a reset or powerup.</li> <li><math>\overline{\text{BAUDOUT}}</math>—When <math>\overline{\text{BAUDOUT}}</math> function is selected, the 16× baud rate clock output is available at this pin.</li> <li><math>\overline{\text{RXRDY}}</math>—<math>\overline{\text{RXRDY}}</math> (active low) is intended for monitoring DMA data transfers. If it is not used, leave it unconnected.</li> </ol> |

### TERMINAL FUNCTIONS (continued)

| TERMINAL                                                   |           |           | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------------------------------------------------------------|-----------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                       | FN NO.    | RHB NO.   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| RESET                                                      | 21        | 12        | I   | Reset. RESET will reset the internal registers and all the outputs. The UART transmitter output and the receiver input are disabled during reset time. See TL16C2752 external reset conditions for initialization details. RESET is an active-high input.                                                                                                                                                                                                                                                                        |
| $\overline{\text{RIA}}$ ,<br>$\overline{\text{RIB}}$       | 43,<br>31 | –         | I   | Ring indicator (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem has received a ringing signal from the telephone line. A low-to-high transition on these input pins generates a modem status interrupt, if enabled. The state of these inputs is reflected in the modem status register (MSR). These inputs should be pulled high if unused.                                                                                                       |
| $\overline{\text{RTSA}}$ ,<br>$\overline{\text{RTSB}}$     | 36,<br>23 | 22,<br>13 | O   | Request to send (active low). These outputs are associated with individual UART channels A and B. A low on the RTS pin indicates the transmitter has data ready and waiting to send. Writing a 1 in the modem control register (MCR bit 1) sets these pins to low, indicating data is available. After a reset, these pins are set to high. These pins only affects the transmit and receive operation when auto RTS function is enabled through the enhanced feature register (EFR) bit 6, for hardware flow control operation. |
| RXA,<br>RXB                                                | 39,<br>25 | 24,<br>15 | I   | Receive data input. These inputs are associated with individual serial channel data to the TL16C2752. During the local loopback mode, these RX input pins are disabled and TX data is internally connected to the UART RX input internally.                                                                                                                                                                                                                                                                                      |
| TXA,<br>TXB                                                | 38,<br>26 | 23,<br>16 | O   | Transmit data. These outputs are associated with individual serial transmit channel data from the TL16C2752. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX input.                                                                                                                                                                                                                                                                                              |
| $\overline{\text{TXRDYA}}$ ,<br>$\overline{\text{TXRDYB}}$ | 1,<br>32  | –         | O   | Transmit ready (active low). $\overline{\text{TXRDY}}$ A and B go low when there are at least a trigger-level number of spaces available. They go high when the TX buffer is full.                                                                                                                                                                                                                                                                                                                                               |
| V <sub>CC</sub>                                            | 33, 44    | 26        | I   | Power-supply inputs                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| XTAL1                                                      | 11        | 4         | I   | Crystal or external clock. XTAL1 functions as a crystal input or as an external clock input. A crystal can be connected between XTAL1 and XTAL2 to form an internal oscillator circuit (see Figure 4). Alternatively, an external clock can be connected to XTAL1 to provide custom data rates.                                                                                                                                                                                                                                  |
| XTAL2                                                      | 13        | 5         | O   | Crystal oscillator or buffered clock (see also XTAL1). XTAL2 is used as a crystal oscillator output or buffered a clock output.                                                                                                                                                                                                                                                                                                                                                                                                  |

## Detailed Description

### Hardware Autoflow Control (see Figure 1)

Hardware autoflow control is comprised of auto- $\overline{\text{CTS}}$  and auto- $\overline{\text{RTS}}$ . With auto- $\overline{\text{CTS}}$ , the  $\overline{\text{CTS}}$  input must be active before the transmitter FIFO can emit data. With auto- $\overline{\text{RTS}}$ , RTS becomes active when the receiver needs more data and notifies the sending serial device. When RTS is connected to CTS, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using ACE1 and ACE2 from a TLC16C2752 with the autoflow control enabled. If not, overrun errors can occur when the transmit data rate exceeds the receiver FIFO read latency.

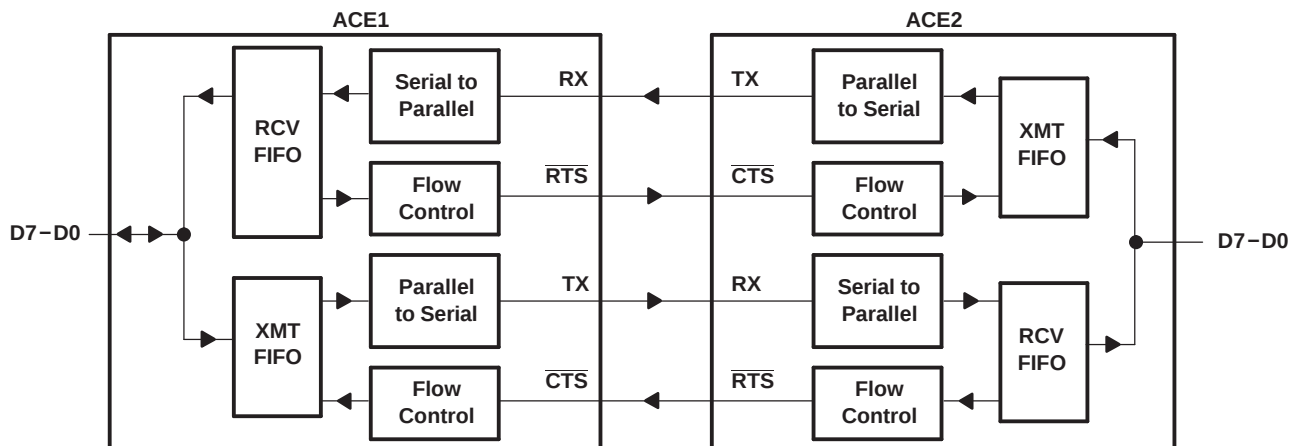


Figure 1. Autoflow Control (Auto- $\overline{\text{RTS}}$  and Auto- $\overline{\text{CTS}}$ ) Example

## Auto-RTS

Auto-RTS data flow control originates in the receiver timing and control block (see Figure 4) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches the defined halt trigger level 8 (see Figure 3), RTS is deasserted. The sending ACE may send an additional byte after the trigger level is reached (assuming the sending ACE has another byte to send) because it may not recognize the deassertion of RTS until after it has begun sending the additional byte. RTS is automatically reasserted once the defined resume trigger level is reached.

## Auto-CTS

The transmitter circuitry checks CTS before sending the next data byte. When CTS is active, it sends the next byte. To stop the transmitter from sending the following byte, CTS must be released before the middle of the last stop bit that is currently being sent (see Figure 2). The auto-CTS function reduces interrupts to the host system. When flow control is enabled, CTS level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTS, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.

## Auto-RTS and Auto-CTS Functional Timing

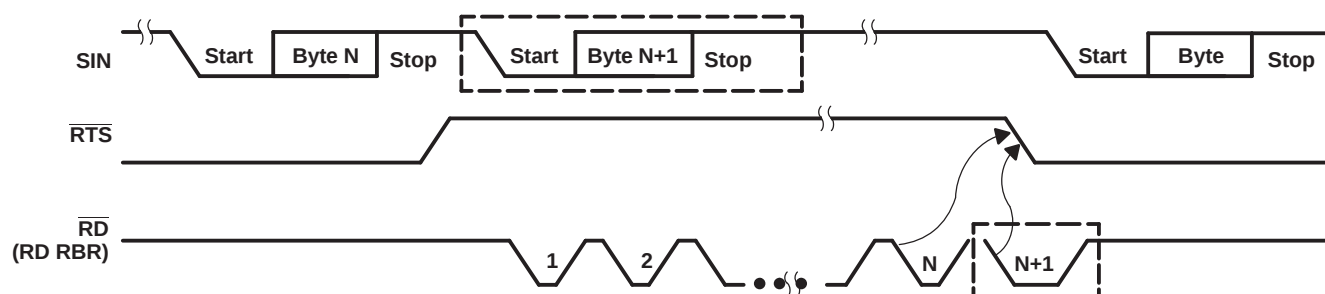


Figure 2. RTS Functional Timing Waveforms



Figure 3. CTS Functional Timing Waveforms

A. Pin numbers shown are for 44-pin PLCC FN package.

## Figure 4. Functional Block Diagram

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |                                                        |            | MIN  | MAX | UNIT |
|------------------|--------------------------------------------------------|------------|------|-----|------|
| V <sub>CC</sub>  | Supply voltage range <sup>(2)</sup>                    |            | −0.5 | 7   | V    |
| V <sub>I</sub>   | Input voltage range at any input                       |            | −0.5 | 7   | V    |
| V <sub>O</sub>   | Output voltage range                                   |            | −0.5 | 7   | V    |
| T <sub>A</sub>   | Operating free-air temperature range                   | TL16C2752  | 0    | 70  | °C   |
|                  |                                                        | TL16C2752I | −40  | 85  |      |
| T <sub>stg</sub> | Storage temperature range                              |            | −65  | 150 | °C   |
|                  | Lead temperature 1,6 mm (1/16 inch) from case for 10 s |            |      | 260 | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V<sub>SS</sub>.

## RECOMMENDED OPERATING CONDITIONS

**1.8 V = 10%**

over operating free-air temperature range (unless otherwise noted)

|                 |                                         | MIN  | NOM | MAX             | UNIT |
|-----------------|-----------------------------------------|------|-----|-----------------|------|
| V <sub>CC</sub> | Supply voltage                          | 1.62 | 1.8 | 1.98            | V    |
| V <sub>I</sub>  | Input voltage                           | 0    |     | V <sub>CC</sub> | V    |
| V <sub>IH</sub> | High-level input voltage                | 1.4  |     | 1.98            | V    |
| V <sub>IL</sub> | Low-level input voltage                 | −0.3 |     | 0.4             | V    |
| V <sub>O</sub>  | Output voltage                          | 0    |     | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current (all outputs) |      |     | 0.5             | mA   |
| I <sub>OL</sub> | Low-level output current (all outputs)  |      |     | 1               | mA   |
|                 | Oscillator/clock speed                  |      |     | 10              | MHz  |

## RECOMMENDED OPERATING CONDITIONS

**2.5 V = 10%**

over operating free-air temperature range (unless otherwise noted)

|                 |                                         | MIN  | NOM | MAX             | UNIT |
|-----------------|-----------------------------------------|------|-----|-----------------|------|
| V <sub>CC</sub> | Supply voltage                          | 2.25 | 2.5 | 2.75            | V    |
| V <sub>I</sub>  | Input voltage                           | 0    |     | V <sub>CC</sub> | V    |
| V <sub>IH</sub> | High-level input voltage                | 1.8  |     | 2.75            | V    |
| V <sub>IL</sub> | Low-level input voltage                 | −0.3 |     | 0.6             | V    |
| V <sub>O</sub>  | Output voltage                          | 0    |     | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current (all outputs) |      |     | 1               | mA   |
| I <sub>OL</sub> | Low-level output current (all outputs)  |      |     | 2               | mA   |
|                 | Oscillator/clock speed                  |      |     | 16              | MHz  |

**RECOMMENDED OPERATING CONDITIONS****3.3 V = 10%**

over operating free-air temperature range (unless otherwise noted)

|                 |                                         | MIN                   | NOM | MAX                   | UNIT |
|-----------------|-----------------------------------------|-----------------------|-----|-----------------------|------|
| V <sub>CC</sub> | Supply voltage                          | 3                     | 3.3 | 3.6                   | V    |
| V <sub>I</sub>  | Input voltage                           | 0                     |     | V <sub>CC</sub>       | V    |
| V <sub>IH</sub> | High-level input voltage                | 0.7 × V <sub>CC</sub> |     |                       | V    |
| V <sub>IL</sub> | Low-level input voltage                 |                       |     | 0.3 × V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                          | 0                     |     | V <sub>CC</sub>       | V    |
| I <sub>OH</sub> | High-level output current (all outputs) |                       |     | 1.8                   | mA   |
| I <sub>OL</sub> | Low-level output current (all outputs)  |                       |     | 3.2                   | mA   |
|                 | Oscillator/clock speed                  |                       |     | 20                    | MHz  |

**RECOMMENDED OPERATING CONDITIONS****5 V = 10%**

over operating free-air temperature range (unless otherwise noted)

|                 |                                         |                         | MIN                   | NOM | MAX                   | UNIT |
|-----------------|-----------------------------------------|-------------------------|-----------------------|-----|-----------------------|------|
| V <sub>CC</sub> | Supply voltage                          |                         | 4.5                   | 5   | 5.5                   | V    |
| V <sub>I</sub>  | Input voltage                           |                         | 0                     |     | V <sub>CC</sub>       | V    |
| V <sub>IH</sub> | High-level input voltage                | All except XTAL1, XTAL2 | 2                     |     |                       | V    |
|                 |                                         | XTAL1, XTAL2            | 0.7 × V <sub>CC</sub> |     |                       |      |
| V <sub>IL</sub> | Low-level input voltage                 | All except XTAL1, XTAL2 |                       |     | 0.8                   | V    |
|                 |                                         | XTAL1, XTAL2            |                       |     | 0.3 × V <sub>CC</sub> |      |
| V <sub>O</sub>  | Output voltage                          |                         | 0                     |     | V <sub>CC</sub>       | V    |
| I <sub>OH</sub> | High-level output current (all outputs) |                         |                       |     | 4                     | mA   |
| I <sub>OL</sub> | Low-level output current (all outputs)  |                         |                       |     | 4                     | mA   |
|                 | Oscillator/clock speed                  |                         |                       |     | 24                    | MHz  |

**ELECTRICAL CHARACTERISTICS****1.8 V Nominal**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS                                                                                                                                                                                           | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------|-----|------|
| V <sub>OH</sub>     | High-level output voltage <sup>(2)</sup><br>I <sub>OH</sub> = −0.5 mA                                                                                                                                     |     | 1.3                |     | V    |
| V <sub>OL</sub>     | Low-level output voltage <sup>(2)</sup><br>I <sub>OL</sub> = 1 mA                                                                                                                                         |     |                    | 0.5 | V    |
| I <sub>I</sub>      | Input current<br>V <sub>CC</sub> = 1.98 V, V <sub>SS</sub> = 0, V <sub>I</sub> = 0 to 1.98 V,<br>All other terminals floating                                                                             |     |                    | 10  | μA   |
| I <sub>OZ</sub>     | High-impedance-state output current<br>V <sub>CC</sub> = 1.98 V, V <sub>SS</sub> = 0, V <sub>I</sub> = 0 to 1.98 V,<br>Chip selected in write mode or chip deselected                                     |     |                    | ±20 | μA   |
| I <sub>CC</sub>     | Supply current<br>V <sub>CC</sub> = 1.98 V, T <sub>A</sub> = 0°C, RXA, RXB, DSRA, DSRB, CDA,<br>CDB, CTSA, CTSB, RIA, and RIB at 1.4 V, All other inputs at<br>0.4 V, XTAL1 at 16 MHz, No load on outputs |     |                    |     | mA   |
| C <sub>I(CLK)</sub> | Clock input impedance                                                                                                                                                                                     |     | 15                 | 20  | pF   |
| C <sub>O(CLK)</sub> | Clock output impedance<br>V <sub>CC</sub> = 0, V <sub>SS</sub> = 0, f = 1 MHz,<br>T <sub>A</sub> = 25°C, All other terminals grounded                                                                     |     | 20                 | 30  | pF   |
| C <sub>I</sub>      | Input impedance                                                                                                                                                                                           |     | 6                  | 10  | pF   |
| C <sub>O</sub>      | Output impedance                                                                                                                                                                                          |     | 10                 | 20  | pF   |

(1) All typical values are at V<sub>CC</sub> = 1.8 V and T<sub>A</sub> = 25°C.

(2) These parameters apply for all outputs except XTAL2.

## ELECTRICAL CHARACTERISTICS

### 2.5 V Nominal

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                                          | TEST CONDITIONS                                                                                                                                                                         | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|---------------------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------|-----|------|
| V <sub>OH</sub>     | High-level output voltage <sup>(2)</sup> | I <sub>OH</sub> = –1 mA                                                                                                                                                                 | 1.8 |                    |     | V    |
| V <sub>OL</sub>     | Low-level output voltage <sup>(2)</sup>  | I <sub>OL</sub> = 2 mA                                                                                                                                                                  |     |                    | 0.5 | V    |
| I <sub>I</sub>      | Input current                            | V <sub>CC</sub> = 2.75 V, V <sub>SS</sub> = 0, V <sub>I</sub> = 0 to 2.75 V,<br>All other terminals floating                                                                            |     |                    | 10  | = A  |
| I <sub>OZ</sub>     | High-impedance-state output current      | V <sub>CC</sub> = 2.75 V, V <sub>SS</sub> = 0, V <sub>I</sub> = 0 to 2.75 V,<br>Chip selected in write mode or chip deselected                                                          |     |                    | ±20 | = A  |
| I <sub>CC</sub>     | Supply current                           | V <sub>CC</sub> = 2.75 V, T <sub>A</sub> = 0°C, RXA, RXB, DSRA, DSRB, CDA,<br>CDB, CTSA, CTSB, RIA, and RIB at 1.8 V, All other<br>inputs at 0.6 V, XTAL1 at 24 MHz, No load on outputs |     |                    |     | mA   |
| C <sub>I(CLK)</sub> | Clock input impedance                    |                                                                                                                                                                                         |     | 15                 | 20  | pF   |
| C <sub>O(CLK)</sub> | Clock output impedance                   | V <sub>CC</sub> = 0, V <sub>SS</sub> = 0, f = 1 MHz,<br>T <sub>A</sub> = 25°C, All other terminals grounded                                                                             |     | 20                 | 30  | pF   |
| C <sub>I</sub>      | Input impedance                          |                                                                                                                                                                                         |     | 6                  | 10  | pF   |
| C <sub>O</sub>      | Output impedance                         |                                                                                                                                                                                         |     | 10                 | 20  | pF   |

(1) All typical values are at V<sub>CC</sub> = 2.5 V and T<sub>A</sub> = 25°C.

(2) These parameters apply for all outputs except XTAL2.

## ELECTRICAL CHARACTERISTICS

### 3.3 V Nominal

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                                          | TEST CONDITIONS                                                                                                                                                                      | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|---------------------|------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------|-----|------|
| V <sub>OH</sub>     | High-level output voltage <sup>(2)</sup> | I <sub>OH</sub> = –1.8 mA                                                                                                                                                            | 2.4 |                    |     | V    |
| V <sub>OL</sub>     | Low-level output voltage <sup>(2)</sup>  | I <sub>OL</sub> = 3.2 mA                                                                                                                                                             |     |                    | 0.5 | V    |
| I <sub>I</sub>      | Input current                            | V <sub>CC</sub> = 3.6 V, V <sub>SS</sub> = 0, V <sub>I</sub> = 0 to 3.6 V,<br>All other terminals floating                                                                           |     |                    | 10  | = A  |
| I <sub>OZ</sub>     | High-impedance-state output current      | V <sub>CC</sub> = 3.6 V, V <sub>SS</sub> = 0, V <sub>I</sub> = 0 to 3.6 V,<br>Chip selected in write mode or chip deselected                                                         |     |                    | ±20 | = A  |
| I <sub>CC</sub>     | Supply current                           | V <sub>CC</sub> = 3.6 V, T <sub>A</sub> = 0°C, RXA, RXB, DSRA, DSRB, CDA,<br>CDB, CTSA, CTSB, RIA, and RIB at 2 V, All other inputs<br>at 0.8 V, XTAL1 at 32 MHz, No load on outputs |     |                    |     | mA   |
| C <sub>I(CLK)</sub> | Clock input impedance                    |                                                                                                                                                                                      |     | 15                 | 20  | pF   |
| C <sub>O(CLK)</sub> | Clock output impedance                   | V <sub>CC</sub> = 0, V <sub>SS</sub> = 0, f = 1 MHz,<br>T <sub>A</sub> = 25°C, All other terminals grounded                                                                          |     | 20                 | 30  | pF   |
| C <sub>I</sub>      | Input impedance                          |                                                                                                                                                                                      |     | 6                  | 10  | pF   |
| C <sub>O</sub>      | Output impedance                         |                                                                                                                                                                                      |     | 10                 | 20  | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C.

(2) These parameters apply for all outputs except XTAL2.

## ELECTRICAL CHARACTERISTICS

### 5 V Nominal

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                                          | TEST CONDITIONS                                                                                                                                                                         | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|---------------------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------|-----|------|
| V <sub>OH</sub>     | High-level output voltage <sup>(2)</sup> | I <sub>OH</sub> = −4 mA                                                                                                                                                                 | 4   |                    |     | V    |
| V <sub>OL</sub>     | Low-level output voltage <sup>(2)</sup>  | I <sub>OL</sub> = 4 mA                                                                                                                                                                  |     |                    | 0.4 | V    |
| I <sub>I</sub>      | Input current                            | V <sub>CC</sub> = 5.5 V, V <sub>SS</sub> = 0, V <sub>I</sub> = 0 to 5.5 V,<br>All other terminals floating                                                                              |     |                    | 10  | μA   |
| I <sub>OZ</sub>     | High-impedance-state output current      | V <sub>CC</sub> = 3.6 V, V <sub>SS</sub> = 0, V <sub>I</sub> = 0 to 3.6 V,<br>Chip selected in write mode or chip deselected                                                            |     |                    | 20  | μA   |
| I <sub>CC</sub>     | Supply current                           | V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = 0°C, RXA, RXB, DSRA, DSRB, CDA,<br>CDB, CTSA, CTSB, RIA, and RIB at 2 V,<br>All other inputs at 0.8 V, XTAL1 at 32 MHz,<br>No load on outputs |     |                    |     | mA   |
| C <sub>I(CLK)</sub> | Clock input impedance                    |                                                                                                                                                                                         |     | 15                 | 20  | pF   |
| C <sub>O(CLK)</sub> | Clock output impedance                   | V <sub>CC</sub> = 0, V <sub>SS</sub> = 0, f = 1 MHz,<br>T <sub>A</sub> = 25°C, All other terminals grounded                                                                             |     | 20                 | 30  | pF   |
| C <sub>I</sub>      | Input impedance                          |                                                                                                                                                                                         |     | 6                  | 10  | pF   |
| C <sub>O</sub>      | Output impedance                         |                                                                                                                                                                                         |     | 10                 | 20  | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C.

(2) These parameters apply for all outputs except XTAL2.

## TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER        |                                                                                                    | ALT.<br>SYMBOL     | FIGURE | TEST<br>CONDITIONS     | LIMITS |     |       |     |       |     |     |     | UNIT |
|------------------|----------------------------------------------------------------------------------------------------|--------------------|--------|------------------------|--------|-----|-------|-----|-------|-----|-----|-----|------|
|                  |                                                                                                    |                    |        |                        | 1.8 V  |     | 2.5 V |     | 3.3 V |     | 5 V |     |      |
|                  |                                                                                                    |                    |        |                        | MIN    | MAX | MIN   | MAX | MIN   | MAX | MIN | MAX |      |
| t <sub>w8</sub>  | Pulse duration, RESET                                                                              | t <sub>RESET</sub> |        |                        | 1      |     | 1     |     | 1     |     | 1   |     | = S  |
| t <sub>w1</sub>  | Pulse duration, clock high                                                                         | t <sub>XH</sub>    | 6      |                        | 25     |     | 16    |     | 12    |     | 8   |     | ns   |
| t <sub>w2</sub>  | Pulse duration, clock low                                                                          | t <sub>XL</sub>    |        |                        |        |     |       |     |       |     |     |     |      |
| t <sub>cR</sub>  | Cycle time, read (t <sub>w7</sub> + t <sub>d8</sub> + t <sub>h7</sub> )                            | RC                 | 8      |                        | 115    |     | 80    |     | 62    |     | 57  |     | ns   |
| t <sub>cW</sub>  | Cycle time, write (t <sub>w6</sub> + t <sub>d5</sub> + t <sub>h4</sub> )                           | WC                 | 7      |                        | 115    |     | 80    |     | 62    |     | 57  |     | ns   |
| t <sub>w6</sub>  | Pulse duration, $\overline{\text{IOW}}$ or $\overline{\text{CS}}$                                  | t <sub>IOW</sub>   | 7      |                        | 80     |     | 55    |     | 45    |     | 40  |     | ns   |
| t <sub>w7</sub>  | Pulse duration, $\overline{\text{IOR}}$ or $\overline{\text{CS}}$                                  | t <sub>IOR</sub>   | 8      |                        | 80     |     | 55    |     | 45    |     | 40  |     | ns   |
| t <sub>SU3</sub> | Setup time, data valid before $\overline{\text{IOW}}\uparrow$ or $\overline{\text{CS}}\uparrow$    | t <sub>DS</sub>    | 7      |                        | 25     |     | 20    |     | 15    |     | 15  |     | ns   |
| t <sub>h4</sub>  | Hold time, address valid after $\overline{\text{IOW}}\uparrow$ or $\overline{\text{CS}}\uparrow$   | t <sub>WA</sub>    | 7      |                        | 20     |     | 15    |     | 10    |     | 10  |     | ns   |
| t <sub>h5</sub>  | Hold time, data valid after $\overline{\text{IOW}}\uparrow$ or $\overline{\text{CS}}\uparrow$      | t <sub>DH</sub>    | 7      |                        | 15     |     | 10    |     | 5     |     | 5   |     | ns   |
| t <sub>h7</sub>  | Hold time, data valid after $\overline{\text{IOR}}\uparrow$ or $\overline{\text{CS}}\uparrow$      | t <sub>RA</sub>    | 8      |                        | 20     |     | 15    |     | 10    |     | 10  |     | ns   |
| t <sub>d5</sub>  | Delay time, address valid before $\text{IOW}\downarrow$ or $\text{CS}\downarrow$                   | t <sub>AW</sub>    | 7      |                        | 15     |     | 10    |     | 7     |     | 7   |     | ns   |
| t <sub>d8</sub>  | Delay time, address valid to $\overline{\text{IOR}}\downarrow$ or $\overline{\text{CS}}\downarrow$ | t <sub>AR</sub>    | 8      |                        | 15     |     | 10    |     | 7     |     | 7   |     | ns   |
| t <sub>d10</sub> | Delay time, $\overline{\text{IOR}}\downarrow$ or $\overline{\text{CS}}\downarrow$ to data valid    | t <sub>RVD</sub>   | 8      | C <sub>L</sub> = 30 pF | 55     |     | 35    |     | 25    |     | 20  |     | ns   |
| t <sub>d11</sub> | Delay time, $\overline{\text{IOR}}\uparrow$ or $\overline{\text{CS}}\uparrow$ to floating data     | t <sub>HZ</sub>    | 8      | C <sub>L</sub> = 30 pF | 40     |     | 30    |     | 20    |     | 20  |     | ns   |
| t <sub>d12</sub> | Write cycle to write cycle delay                                                                   |                    | 7      |                        | 100    |     | 75    |     | 60    |     | 50  |     | ns   |
| t <sub>d13</sub> | Read cycle to read cycle delay                                                                     |                    | 8      |                        | 100    |     | 75    |     | 60    |     | 50  |     | ns   |

## BAUD GENERATOR SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 30$  pF (for FN package only)

| PARAMETER       |                                                    | ALT. SYMBOL      | FIGURE | TEST CONDITION S | LIMITS |     |       |     |       |     |     |     | UNIT |
|-----------------|----------------------------------------------------|------------------|--------|------------------|--------|-----|-------|-----|-------|-----|-----|-----|------|
|                 |                                                    |                  |        |                  | 1.8 V  |     | 2.5 V |     | 3.3 V |     | 5 V |     |      |
|                 |                                                    |                  |        |                  | MIN    | MAX | MIN   | MAX | MIN   | MAX | MIN | MAX |      |
| t <sub>w3</sub> | Pulse duration, $\overline{\text{BAUDOUT}}$ low    | t <sub>LW</sub>  | 6      | CLK ÷ 2          | 50     |     | 35    |     | 27    |     | 16  |     | ns   |
| t <sub>w4</sub> | Pulse duration, $\overline{\text{BAUDOUT}}$ high   | t <sub>HW</sub>  | 6      | CLK ÷ 2          | 50     |     | 35    |     | 27    |     | 16  |     | ns   |
| t <sub>d1</sub> | Delay time, XIN↑ to $\overline{\text{BAUDOUT}}$ ↑  | t <sub>BLD</sub> | 6      |                  |        | 35  |       | 25  |       | 20  |     | 15  | ns   |
| t <sub>d2</sub> | Delay time, XIN↑↓ to $\overline{\text{BAUDOUT}}$ ↓ | t <sub>BHD</sub> | 6      |                  |        | 35  |       | 25  |       | 20  |     | 15  | ns   |

## RECEIVER SWITCHING CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER        |                                                                            | ALT. SYMBOL       | FIGURE           | TEST CONDITIONS        | LIMITS |     |       |     |       |     |     |     | UNIT                          |
|------------------|----------------------------------------------------------------------------|-------------------|------------------|------------------------|--------|-----|-------|-----|-------|-----|-----|-----|-------------------------------|
|                  |                                                                            |                   |                  |                        | 1.8 V  |     | 2.5 V |     | 3.3 V |     | 5 V |     |                               |
|                  |                                                                            |                   |                  |                        | MIN    | MAX | MIN   | MAX | MIN   | MAX | MIN | MAX |                               |
| t <sub>d12</sub> | Delay time, RCLK to sample                                                 | t <sub>SCD</sub>  | 9                |                        | 20     |     | 15    |     | 10    |     | 10  |     | ns                            |
| t <sub>d13</sub> | Delay time, stop to set INT or read RBR to LSI interrupt or stop to RXRDY↓ | t <sub>SINT</sub> | 8, 9, 10, 11, 12 |                        | 1      |     | 1     |     | 1     |     | 1   |     | RCLK cycle                    |
| t <sub>d14</sub> | Delay time, read RBR/LSR to reset INT                                      | t <sub>RINT</sub> | 8, 9, 10, 11, 12 | C <sub>L</sub> = 30 pF | 100    |     | 90    |     | 80    |     | 70  |     | ns                            |
| t <sub>d26</sub> | Delay time, RCV threshold byte to RTS↑                                     |                   | 19               | C <sub>L</sub> = 30 pF |        |     |       |     |       |     | 2   |     | baudout cycles <sup>(2)</sup> |
| t <sub>d27</sub> | Delay time, read of last byte in receive FIFO to RTS↓                      |                   | 19               | C <sub>L</sub> = 30 pF |        |     |       |     |       |     | 2   |     | baudout cycles                |
| t <sub>d28</sub> | Delay time, first data bit of 16th character to RTS↑                       |                   | 20               | C <sub>L</sub> = 30 pF |        |     |       |     |       |     | 2   |     | baudout cycles                |
| t <sub>d29</sub> | Delay time, RBRD low to RTS↓                                               |                   | 20               | C <sub>L</sub> = 30 pF |        |     |       |     |       |     | 2   |     | baudout cycles                |

(1) In the FIFO mode, the read cycle (RC) = 1 baud clock (min) between reads of the receive FIFO and the status registers (interrupt identification register or line status register).

(2) A baudout cycle is equal to the period of the input clock divided by the programmed divider in DLL, DLM.

## TRANSMITTER SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

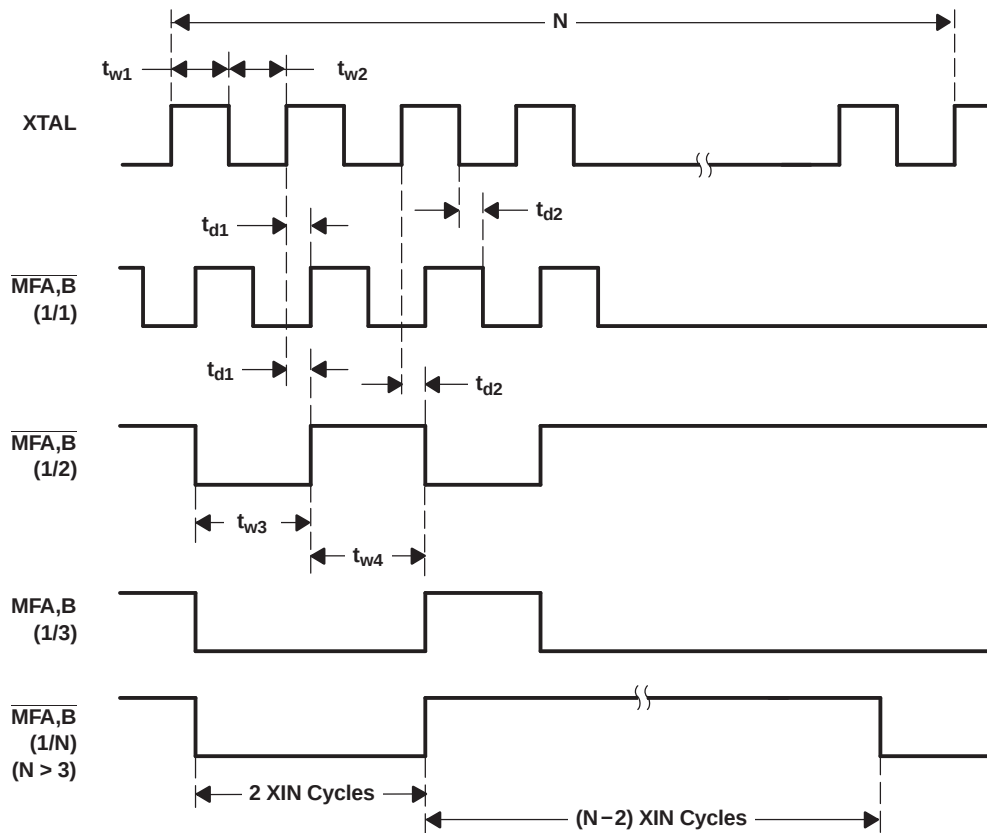
| PARAMETER        | ALT. SYMBOL                                                                          | FIGURE           | TEST CONDITIONS | LIMITS                 |     |       |     |       |     |     |     | UNIT |                |
|------------------|--------------------------------------------------------------------------------------|------------------|-----------------|------------------------|-----|-------|-----|-------|-----|-----|-----|------|----------------|
|                  |                                                                                      |                  |                 | 1.8 V                  |     | 2.5 V |     | 3.3 V |     | 5 V |     |      |                |
|                  |                                                                                      |                  |                 | MIN                    | MAX | MIN   | MAX | MIN   | MAX | MIN | MAX |      |                |
| t <sub>d15</sub> | Delay time, initial write to transmit start                                          | t <sub>IRS</sub> | 14              |                        | 8   | 24    | 8   | 24    | 8   | 24  | 8   | 24   | baudout cycles |
| t <sub>d16</sub> | Delay time, start to INT                                                             | t <sub>STI</sub> | 14              |                        | 8   | 10    | 8   | 10    | 8   | 10  | 8   | 10   | baudout cycles |
| t <sub>d17</sub> | Delay time, $\overline{\text{IOW}}$ (WR THR) to reset INT                            | t <sub>HR</sub>  | 14              | C <sub>L</sub> = 30 pF |     | 70    |     | 60    |     | 50  |     | 50   | ns             |
| t <sub>d18</sub> | Delay time, initial write to INT (THRE <sup>(1)</sup> )                              | t <sub>SI</sub>  | 14              |                        | 16  | 34    | 16  | 34    | 16  | 34  | 16  | 34   | baudout cycles |
| t <sub>d19</sub> | Delay time, read $\overline{\text{IOR}}\uparrow$ to reset INT (THRE <sup>(1)</sup> ) | t <sub>IR</sub>  | 14              | C <sub>L</sub> = 30 pF |     | 70    |     | 50    |     | 35  |     | 35   | ns             |
| t <sub>d20</sub> | Delay time, write to $\overline{\text{TXRDY}}$ inactive                              | t <sub>WXI</sub> | 15, 16          | C <sub>L</sub> = 30 pF |     | 60    |     | 45    |     | 35  |     | 35   | ns             |
| t <sub>d21</sub> | Delay time, start to $\overline{\text{TXRDY}}$ active                                | t <sub>SXA</sub> | 15, 16          | C <sub>L</sub> = 30 pF |     | 9     |     | 9     |     | 9   |     | 9    | baudout cycles |
| t <sub>SU4</sub> | Setup time, $\overline{\text{CTS}}\uparrow$ before midpoint of stop bit              |                  | 18              |                        | 30  |       | 20  |       | 10  |     | 10  |      | ns             |
| t <sub>d25</sub> | Delay time, $\overline{\text{CTS}}$ low to TX $\downarrow$                           |                  | 18              | C <sub>L</sub> = 30 pF |     | 24    |     | 24    |     | 24  |     | 24   | baudout cycles |

(1) THRE = Transmitter holding register empty; IIR = interrupt identification register

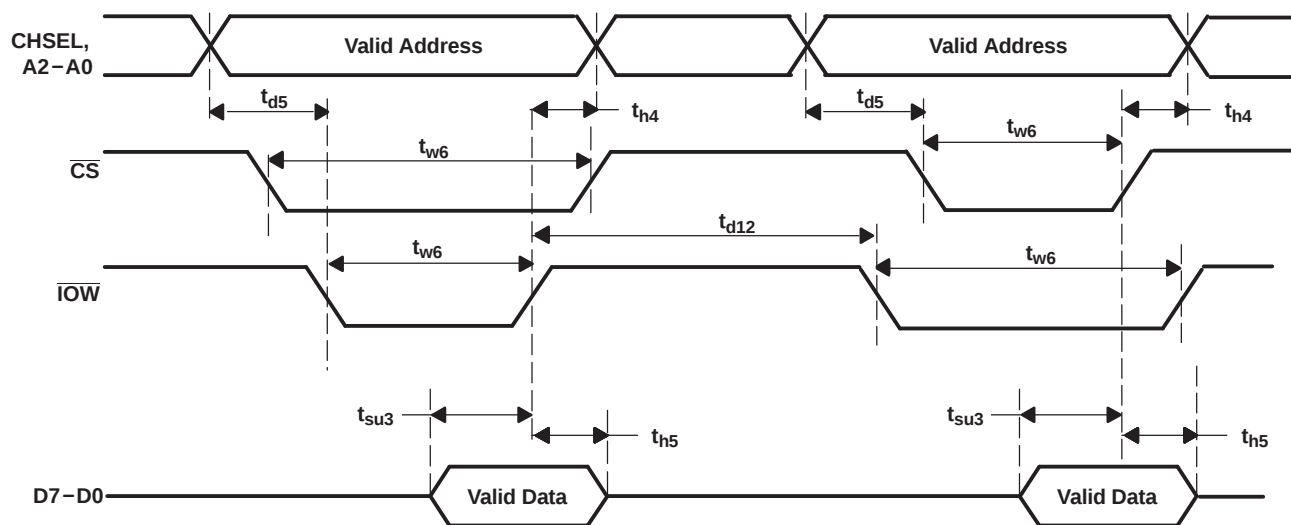
## MODEM CONTROL SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

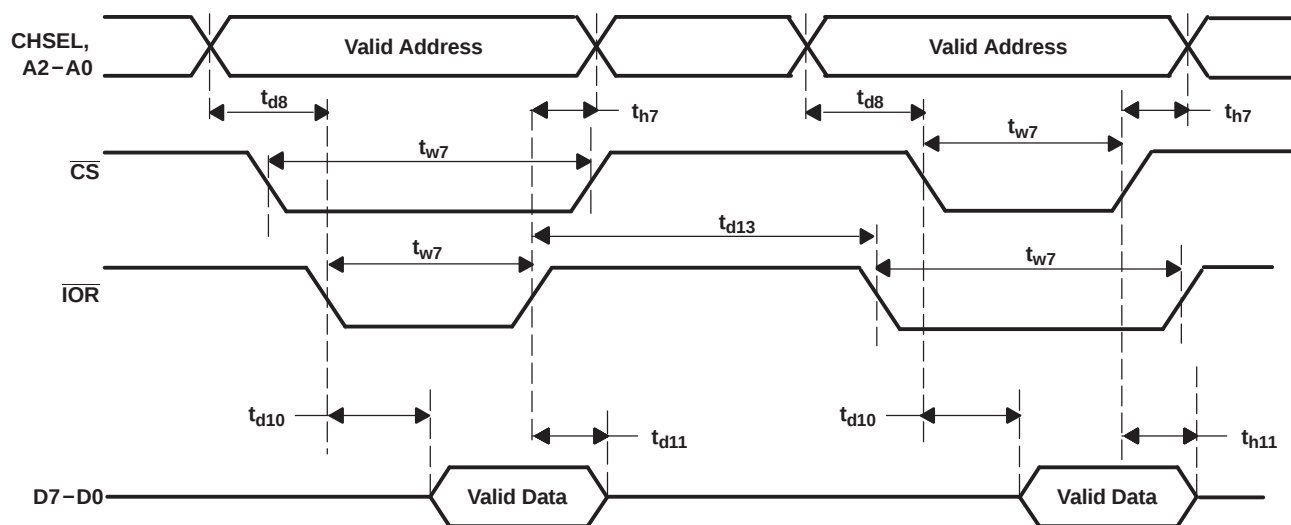
| PARAMETER        |                                        | ALT. SYMBOL      | FIGURE | TEST CONDITIONS        | LIMITS |     |       |     |       |     |     |     | UNIT |
|------------------|----------------------------------------|------------------|--------|------------------------|--------|-----|-------|-----|-------|-----|-----|-----|------|
|                  |                                        |                  |        |                        | 1.8 V  |     | 2.5 V |     | 3.3 V |     | 5 V |     |      |
|                  |                                        |                  |        |                        | MIN    | MAX | MIN   | MAX | MIN   | MAX | MIN | MAX |      |
| t <sub>d22</sub> | Delay time, WR MCR to output           | t <sub>MDO</sub> | 17     | C <sub>L</sub> = 30 pF | 90     |     | 70    |     | 60    |     | 50  |     | ns   |
| t <sub>d23</sub> | Delay time, modem interrupt to set INT | t <sub>SIM</sub> | 17     | C <sub>L</sub> = 30 pF | 60     |     | 50    |     | 40    |     | 35  |     | ns   |
| t <sub>d24</sub> | Delay time, RD MSR to reset INT        | t <sub>RIM</sub> | 17     | C <sub>L</sub> = 30 pF | 80     |     | 60    |     | 50    |     | 40  |     | ns   |



**Figure 5. Input Clock and Baud Generator Timing Waveforms  
(for FN Package Only) (When AFR2:1 = 01)**



**Figure 6. Write Cycle Timing Waveforms**



**Figure 7. Read Cycle Timing Waveforms**

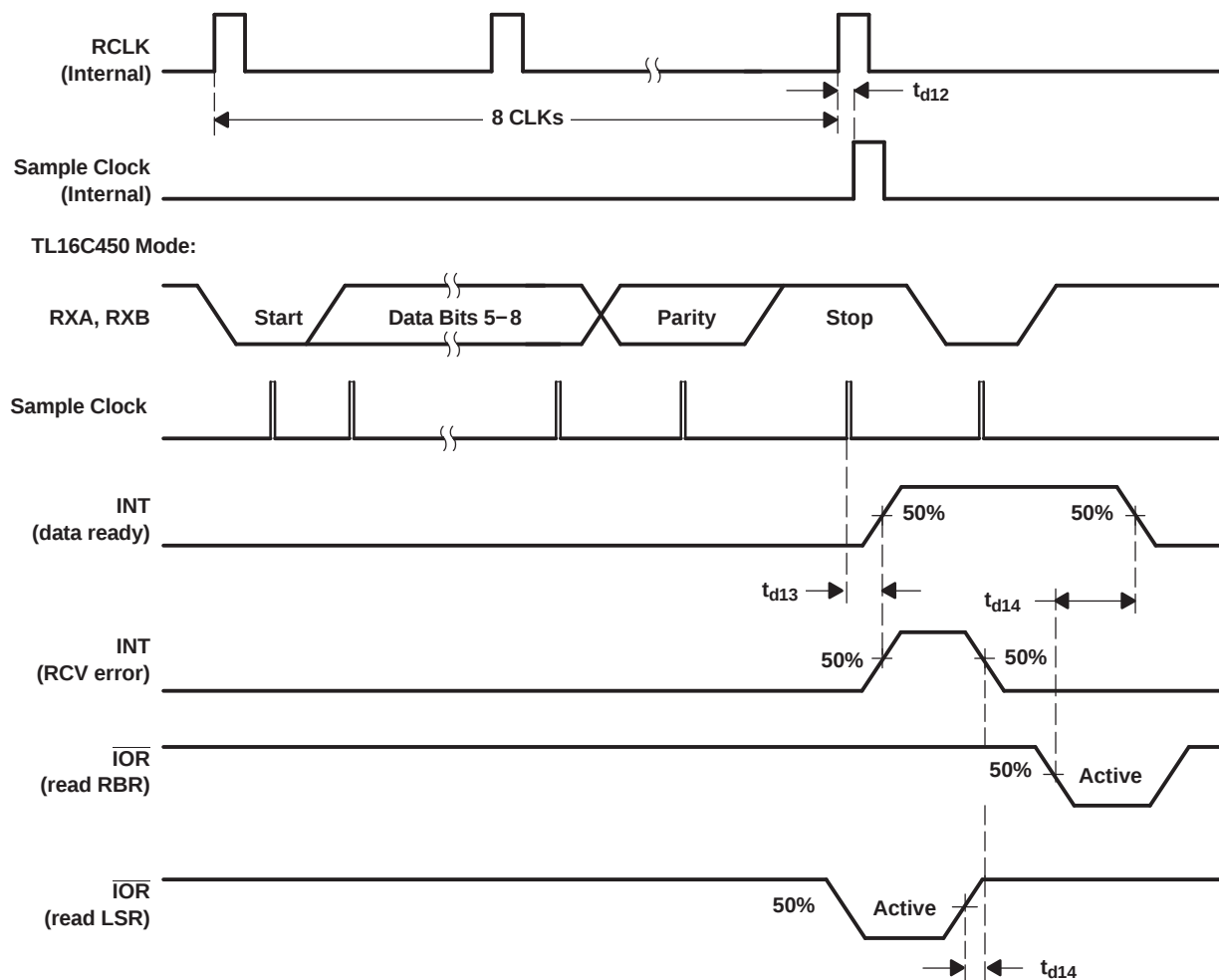
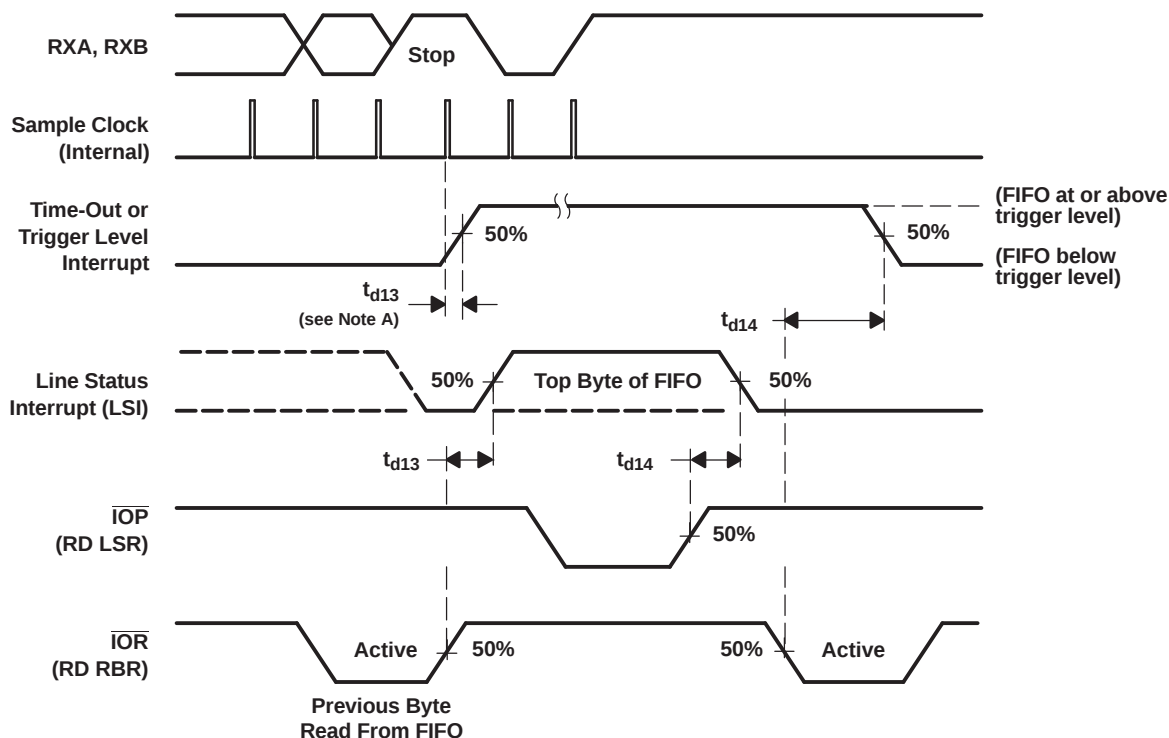
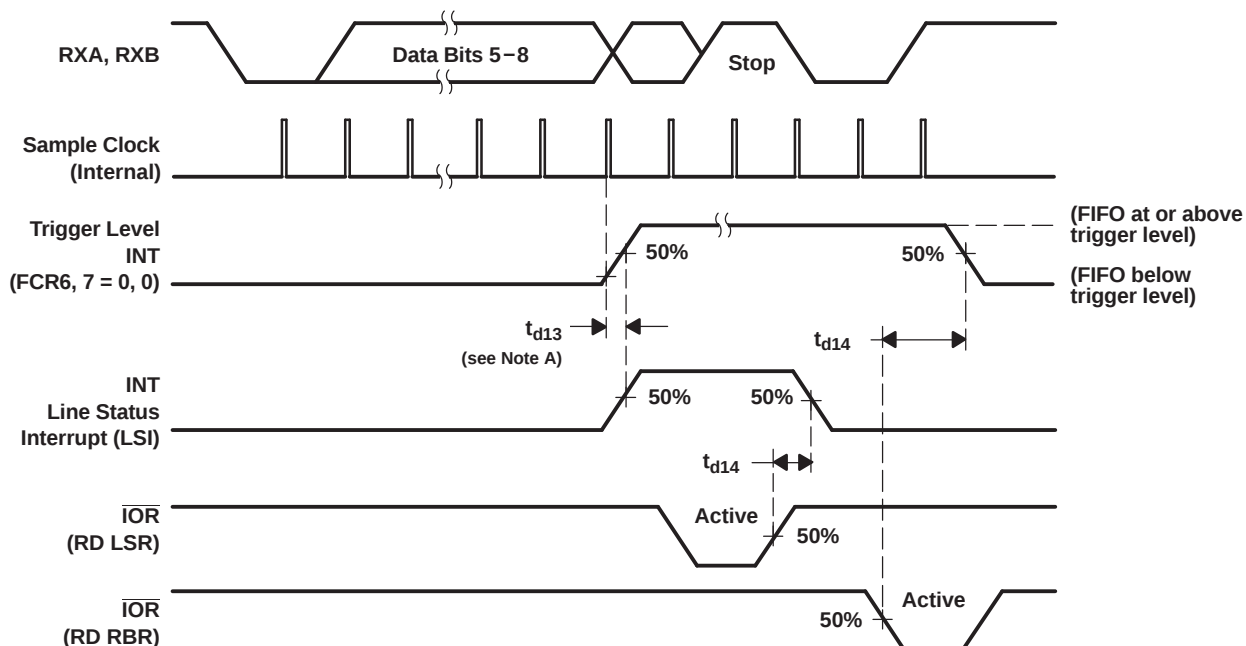


Figure 8. Receiver Timing Waveforms



**Figure 10. Receive FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms**

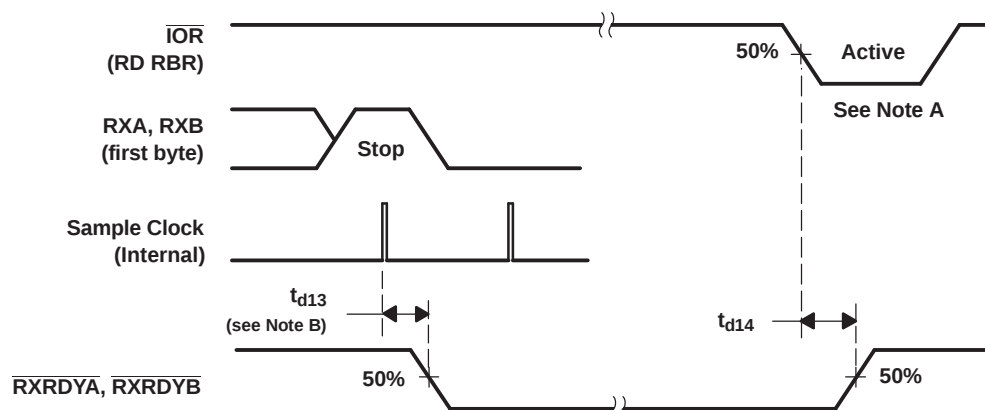
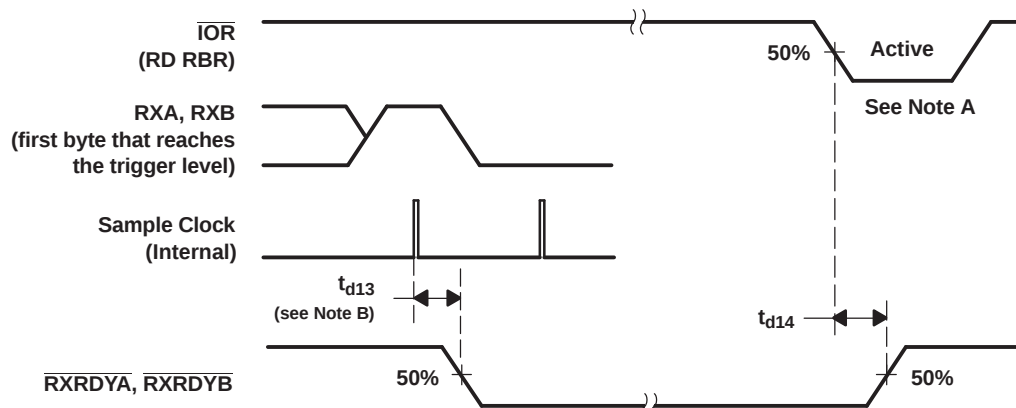
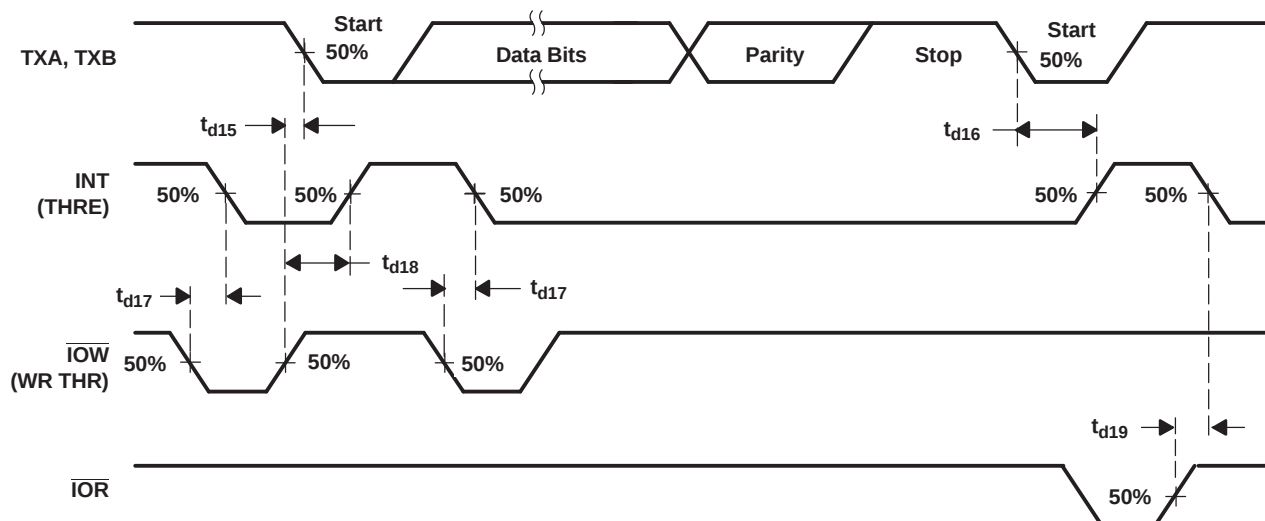
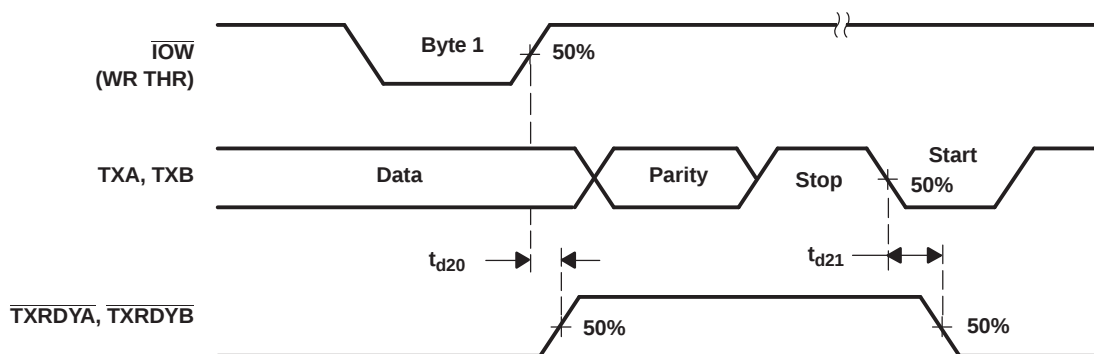
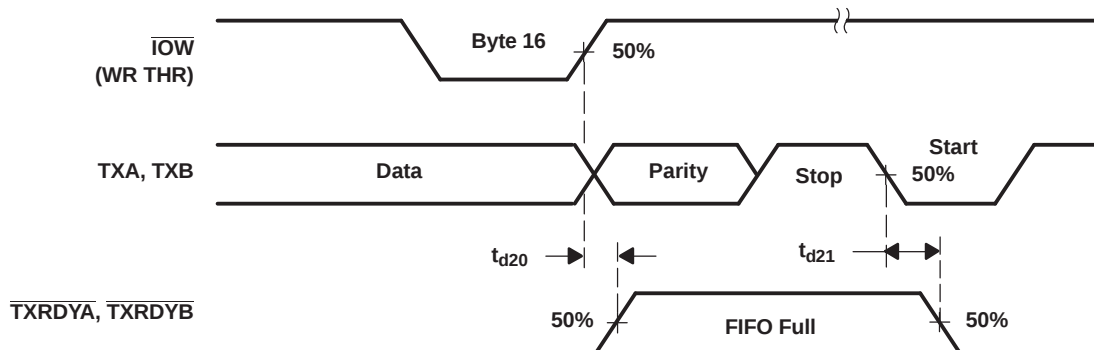
Figure 11. Receiver Ready ( $\overline{\text{RXRDY}}$ ) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)Figure 12. Receiver Ready ( $\overline{\text{RXRDY}}$ ) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

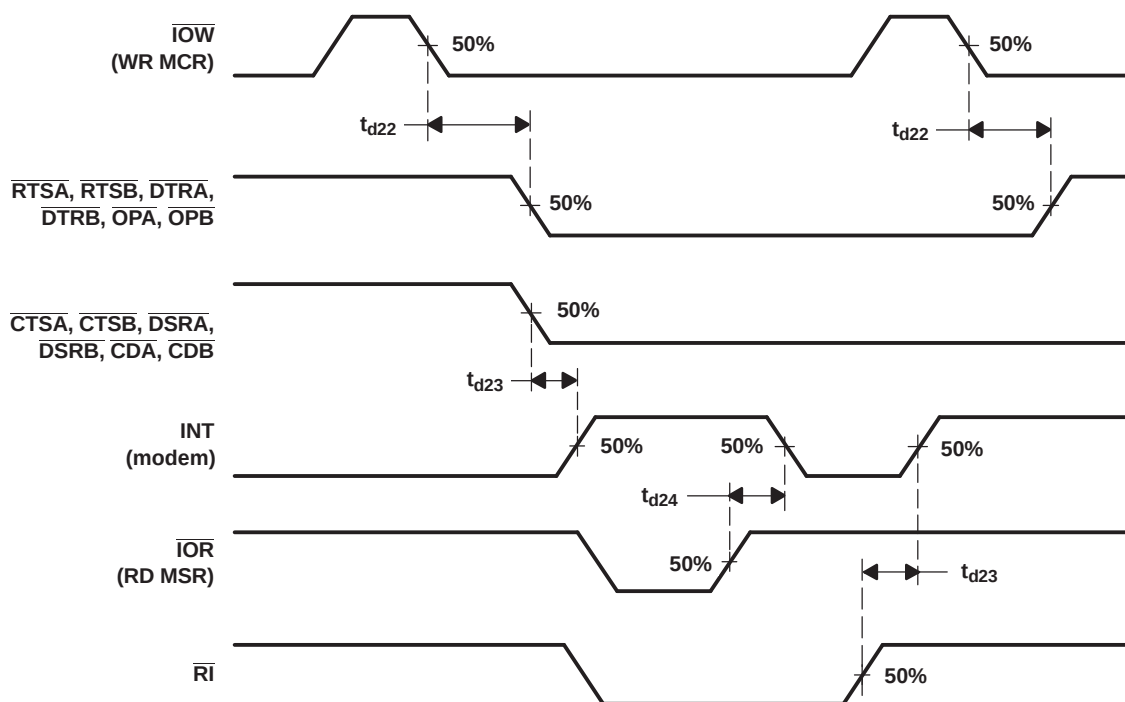
Figure 13. Transmitter Timing Waveforms



**Figure 14. Transmitter Ready ( $\overline{\text{TXRDY}}$ ) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)**



**Figure 15. Transmitter Ready ( $\overline{\text{TXRDY}}$ ) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)**



**Figure 16. Modem Control Timing Waveforms**

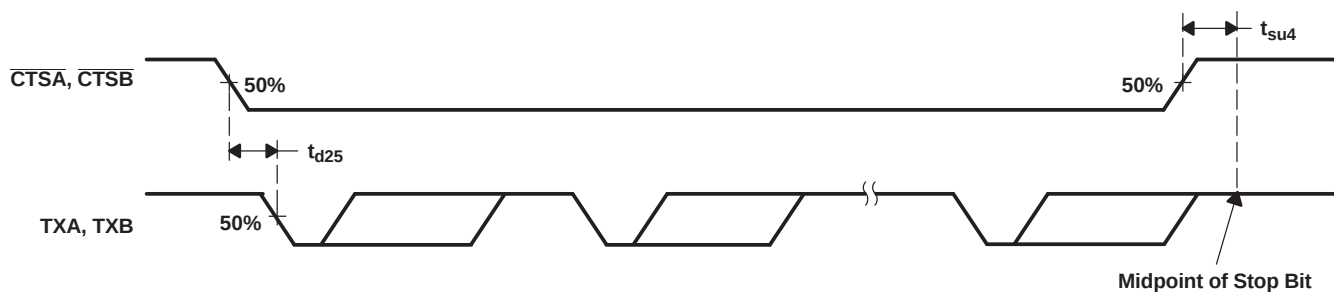


Figure 17.  $\overline{\text{CTS}}$  and TX Autoflow Control Timing (Start and Stop) Waveforms

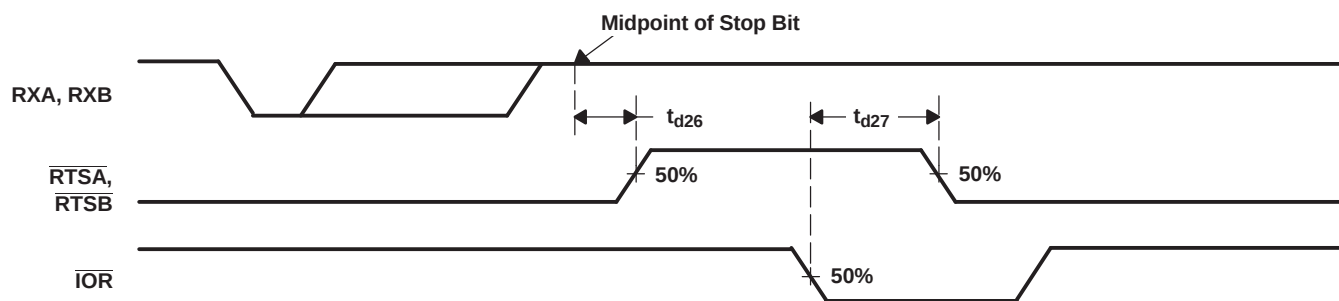


Figure 18. Auto- $\overline{\text{RTS}}$  Timing

## APPLICATION INFORMATION

- A. Pin numbers shown are for 44-pin PLCC FN package.

**Figure 19. Typical TL16C2752 Connection**

## PRINCIPLES OF OPERATION

### UART Internal Registers

Each of the UART channel in the TL16C2752 has its own set of configuration registers selected by address lines A0, A1, and A2 with  $\overline{CS}$  and CHSEL selecting the channel. The complete register set is shown in [Table 1](#) and [Table 2](#).

**Table 1. UART Channel A and B UART Internal Registers**

| ADDRESS                     | RESET<br>(HEX)<br>VALUE | COMMENTS                                   | REGISTER                                                                      | READ/WRITE              |
|-----------------------------|-------------------------|--------------------------------------------|-------------------------------------------------------------------------------|-------------------------|
| A2–A0                       |                         |                                            |                                                                               |                         |
| 16C550 Compatible Registers |                         |                                            |                                                                               |                         |
| 0 0 0                       | XX<br>XX                | LCR[7] = 0                                 | RHR—Receive Holding Register<br>THR—Transmit Holding Register                 | Read only<br>Write only |
| 0 0 0                       | XX                      | LCR[7] = 1, LCR ≠ 0xBF                     | DLL—Div Latch Low Byte                                                        | Read/Write              |
| 0 0 1                       | XX                      |                                            | DLM—Div Latch High Byte                                                       | Read/Write              |
| 0 1 0                       | 00                      |                                            | AFR—Alternate Function Register                                               | Read/Write              |
| 0 0 0                       | 00                      | DLL, DLM = 0x00,<br>LCR[7] = 1, LCR ≠ 0xBF | DREV—Device Revision Code                                                     | Read only               |
| 0 0 1                       | 0A                      |                                            | DVID—Device Identification Code                                               | Read only               |
| 0 0 1                       | 00                      | LCR[7] = 0                                 | IER—Interrupt Enable Register                                                 | Read/Write              |
| 0 1 0                       | 01<br>00                | LCR[7] = 0                                 | ISR—Interrupt Status Register<br>FCR—FIFO Control Register                    | Read only<br>Write only |
| 0 1 1                       | 00                      |                                            | LCR—Line Control Register                                                     | Read/Write              |
| 1 0 0                       | 00                      | LCR ≠ 0xBF                                 | MCR—Modem Control Register                                                    | Read/Write              |
| 1 0 1                       | 60                      |                                            | LSR—Line Status Register<br>Reserved                                          | Read only<br>Write only |
| 1 1 0                       | X0                      |                                            | MSR—Modem Status Register<br>Reserved                                         | Read only<br>Write only |
| 1 1 1                       | FF                      | LCR ≠ 0xBF, FCTR[6] = 0                    | SPR—Scratch Pad Register                                                      | Read/Write              |
| 1 1 1                       | 00                      | LCR ≠ 0xBF, FCTR[6] = 1                    | FLVL—RX/TX FIFO Level Counter Register                                        | Read only               |
| 1 1 1                       | 80                      |                                            | EMSR—Enhanced Mode Select Register                                            | Write only              |
| Enhanced Registers          |                         |                                            |                                                                               |                         |
| 0 0 0                       | 00<br>00                | LCR = 0xBF                                 | TRG—RX/TX FIFO Trigger Level Register<br>FC—RX/TX FIFO Level Counter Register | Write only<br>Read only |
| 0 0 1                       | 00                      |                                            | FCTR—Feature Control Register                                                 | Read/Write              |
| 0 1 0                       | 00                      |                                            | EFR—Enhanced Function Register                                                | Read/Write              |
| 1 0 0                       | 00                      |                                            | Xon-1—Xon Character 1                                                         | Read/Write              |
| 1 0 1                       | 00                      |                                            | Xon-2—Xon Character 2                                                         | Read/Write              |
| 1 1 0                       | 00                      |                                            | Xoff-1—Xoff Character 1                                                       | Read/Write              |
| 1 1 1                       | 00                      |                                            | Xoff-2—Xoff Character 2                                                       | Read/Write              |

**Table 2. Internal Registers Description<sup>(1)</sup>**

| Address<br>A2-A0            | Register<br>Name | Read/<br>Write | Comments                                             | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
|-----------------------------|------------------|----------------|------------------------------------------------------|------------------------------|------------------------------------|---------------------------|-----------------------------------------------------------|------------------------------------|------------------------------|-----------------------------|-----------------------------|-------------------------|-------------------------|--------------------|---------------------|------------------|--------------|
| 16C550 Compatible Registers |                  |                |                                                      |                              |                                    |                           |                                                           |                                    |                              |                             |                             |                         |                         |                    |                     |                  |              |
| 0 0 0                       | RHR              | RD             | LCR[7] = 0                                           | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 0 0 0                       | THR              | WR             |                                                      | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 0 0 1                       | IER              | RD/WR          |                                                      | 0/<br>CTS Int.<br>Enable     | 0/<br>RTS Int.<br>Enable           | 0/<br>Xoff Int.<br>Enable | 0/<br>Sleep Mode<br>Enable                                | Modem Stat.<br>Int. Enable         | RX Line Stat.<br>Int. Enable | TX Empty Int.<br>Enable     | RX Data Int.<br>Enable      |                         |                         |                    |                     |                  |              |
| 0 1 0                       | ISR              | RD             |                                                      | FIFOs<br>Enabled             | FIFOs<br>Enabled                   | 0/<br>INT Source Bit<br>5 | 0/<br>INT Source<br>Bit 4                                 | INT Source Bit<br>3                | INT Source Bit<br>2          | INT Source Bit<br>1         | INT Source Bit<br>0         |                         |                         |                    |                     |                  |              |
| 0 1 0                       | FCR              | WR             |                                                      |                              |                                    | RXFIFO<br>Trigger         | RXFIFO<br>Trigger                                         |                                    |                              |                             |                             | 0/<br>TXFIFO<br>Trigger | 0/<br>TXFIFO<br>Trigger | DMA Mode<br>Enable | TX FIFO<br>Reset    | RX FIFO<br>Reset | FIFOs Enable |
| 0 1 1                       | LCR              | RD/WR          |                                                      |                              |                                    | Divisor<br>Enable         | Set TX Break                                              |                                    |                              |                             |                             | Set Parity              | Even Parity             |                    |                     |                  |              |
| 1 0 0                       | MCR              | RD/WR          |                                                      | 0/<br>BRG<br>Prescaler       | 0/<br>IR Mode<br>Enable            | 0/<br>XonAny              | Internal<br>Loopback<br>Enable                            | OP2# Output<br>Control             | Rsrvd (OP1#)                 | RTS# Output<br>Control      | DTR# Output<br>Control      |                         |                         |                    |                     |                  |              |
| 1 0 1                       | LSR              | RD             |                                                      | RX FIFO<br>Global Error      | THR & TSR<br>Empty                 | THR Empty                 |                                                           |                                    |                              |                             |                             | RX Break                | RX Framing<br>Error     | RX Parity<br>Error | RX Overrun<br>Error | RX Data<br>Ready |              |
| 1 1 0                       | MSR              | RD             |                                                      | CD# Input                    | RI# Input                          | DSR# Input                | CTS# Input                                                | Delta CD#                          | Delta RI#                    | Delta DSR#                  | Delta CTS#                  |                         |                         |                    |                     |                  |              |
| 1 1 1                       | SPR              | RD/WR          | LCR ≠ 0xBF<br>FCTR Bit 6 = 0                         | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 1 1 1                       | EMSR             | WR             | LDR ≠ 0xBF<br>FCTR Bit 6 = 1                         | 16X<br>Sampling<br>Rate Mode | LSR Error<br>Interrupt<br>Imd/Dly# | Auto RTS<br>Hyst. Bit 3   | Auto RTS<br>Hyst Bit 2                                    | Auto RS485<br>Output<br>Inversion  | Rsrvd                        | Rx/Tx FIFO<br>Count         | Rx/Tx FIFO<br>Count         |                         |                         |                    |                     |                  |              |
| 1 1 1                       | FLVL             | RD             |                                                      | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| Baud-Rate Generator Divisor |                  |                |                                                      |                              |                                    |                           |                                                           |                                    |                              |                             |                             |                         |                         |                    |                     |                  |              |
| 0 0 0                       | DLL              | RD/WR          | LCR[7] = 1 LCR<br>≠ 0xBF                             | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 0 0 1                       | DLM              | RD/WR          |                                                      | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 0 1 0                       | AFR              | RD/WR          |                                                      | Rsrvd                        | Rsrvd                              | Rsrvd                     | Rsrvd                                                     | Rsrvd                              | RXRDY#<br>Select             | Baudout#<br>Select          | Concurrent<br>Write         |                         |                         |                    |                     |                  |              |
| 0 0 0                       | DREV             | RD             | LCR[7] = 1 LCR<br>≠ 0xBF DLL =<br>0x00 DLM =<br>0x00 | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 0 0 1                       | DVID             | RD             |                                                      | 0                            | 0                                  | 0                         | 0                                                         | 1                                  | 0                            | 1                           | 0                           |                         |                         |                    |                     |                  |              |
| Enhanced Registers          |                  |                |                                                      |                              |                                    |                           |                                                           |                                    |                              |                             |                             |                         |                         |                    |                     |                  |              |
| 0 0 0                       | TRG              | WR             | LCR = 0xBF                                           | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 0 0 0                       | FC               | RD             |                                                      | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 0 0 1                       | FCTR             | RD/WR          |                                                      | RX/TX<br>Mode                | SCPAD Swap                         | Trig Table Bit<br>1       | Trig Table<br>Bit 0                                       | Auto RS485<br>Direction<br>Control | RX IR Input<br>Inv.          | Auto RTS<br>Hyst Bit 1      | Auto RTS<br>Hyst Bit 0      |                         |                         |                    |                     |                  |              |
| 0 1 0                       | EFR              | RD/WR          |                                                      | Auto CTS<br>Enable           | Auto RTS<br>Enable                 | Special Char<br>Select    | Enable<br>IER[7:4],<br>ISR[5:4],<br>FCT[5:4],<br>MCR[7:5] | Software Flow<br>Cntl Bit 3        | Software Flow<br>Cntl Bit 2  | Software Flow<br>Cntl Bit 1 | Software Flow<br>Cntl Bit 0 |                         |                         |                    |                     |                  |              |
| 1 0 0                       | XON1             | RD/WR          |                                                      | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 1 0 1                       | XON2             | RD/WR          |                                                      | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 1 1 0                       | XOFF1            | RD/WR          |                                                      | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |
| 1 1 1                       | XOFF2            | RD/WR          |                                                      | Bit 7                        | Bit 6                              | Bit 5                     | Bit 4                                                     | Bit 3                              | Bit 2                        | Bit 1                       | Bit 0                       |                         |                         |                    |                     |                  |              |

(1) Shaded bits are accessible when EFR Bit 4 = 1.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL16C2752FN      | ACTIVE        | PLCC         | FN                 | 44   | 26             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | 0 to 70      | 2752FN                  | <a href="#">Samples</a> |
| TL16C2752IFN     | ACTIVE        | PLCC         | FN                 | 44   | 26             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | 2752IFN                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

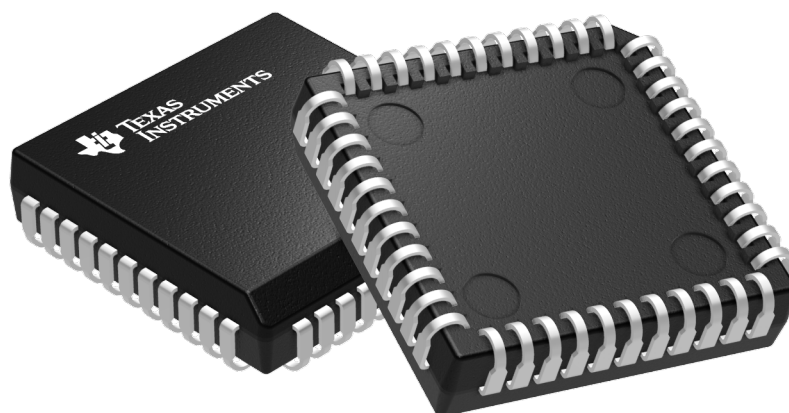
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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Refer to the product data sheet for package details.

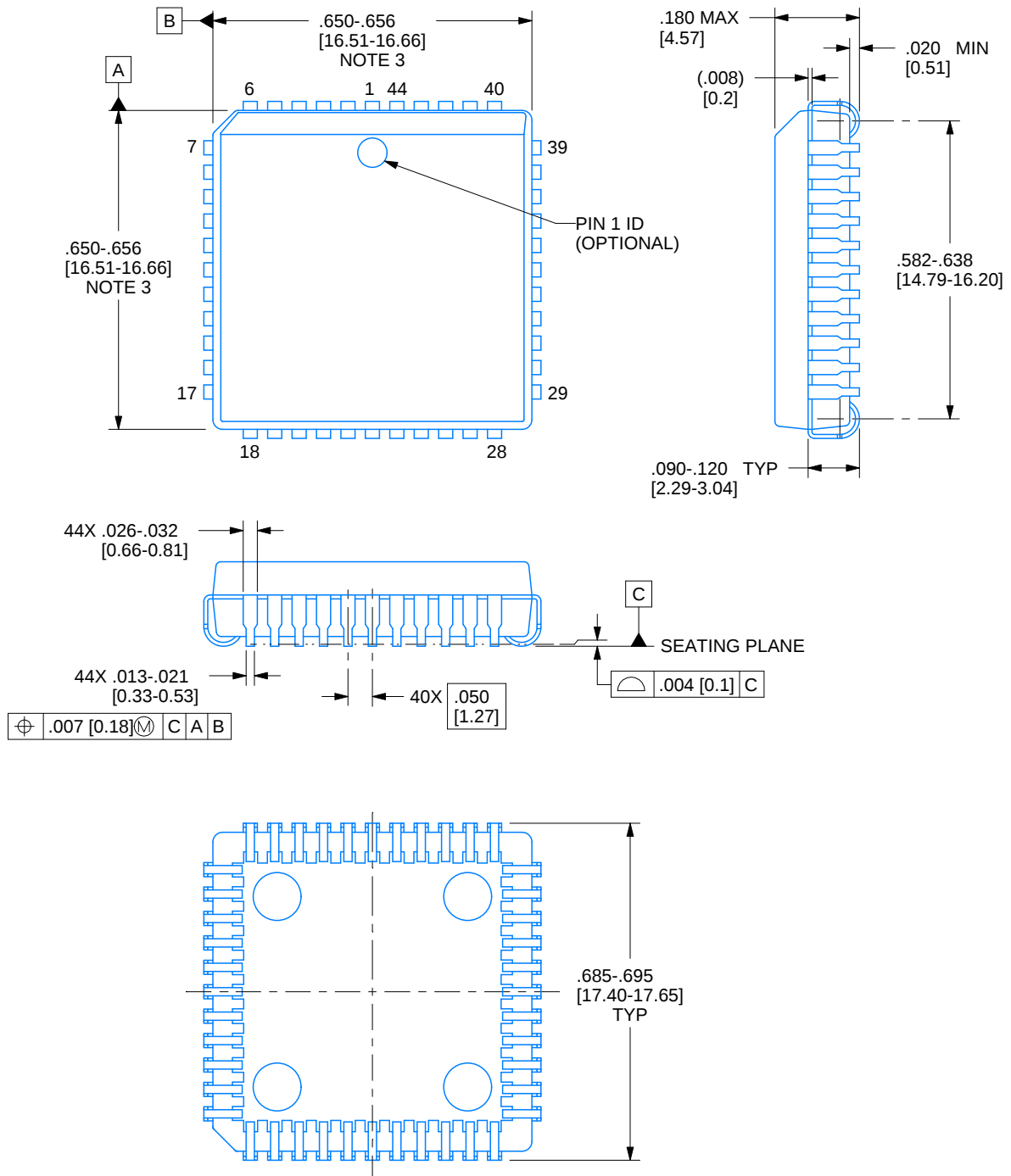
FN0044A



# PACKAGE OUTLINE

## PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



4215154/A 04/2017

### NOTES:

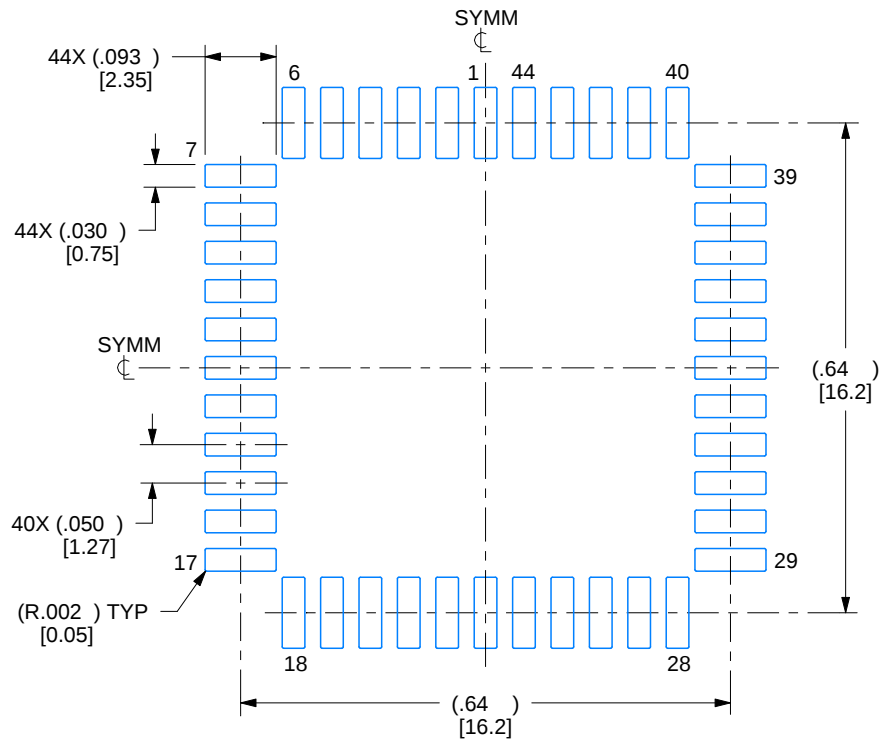
1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion  $.01$  in [ $0.25$  mm] per side.
4. Reference JEDEC registration MS-018.

# EXAMPLE BOARD LAYOUT

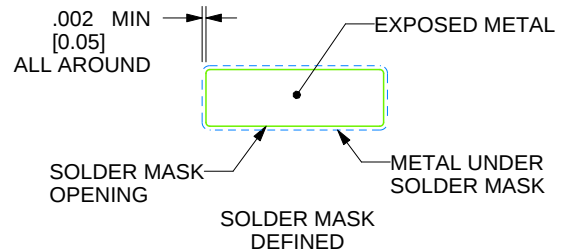
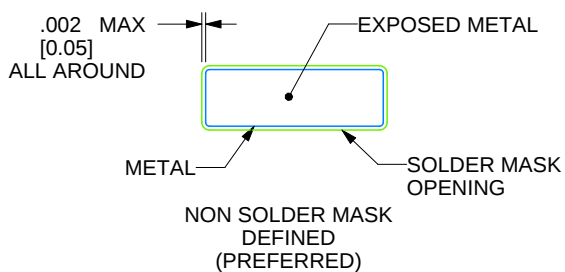
FN0044A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:4X



SOLDER MASK DETAILS

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NOTES: (continued)

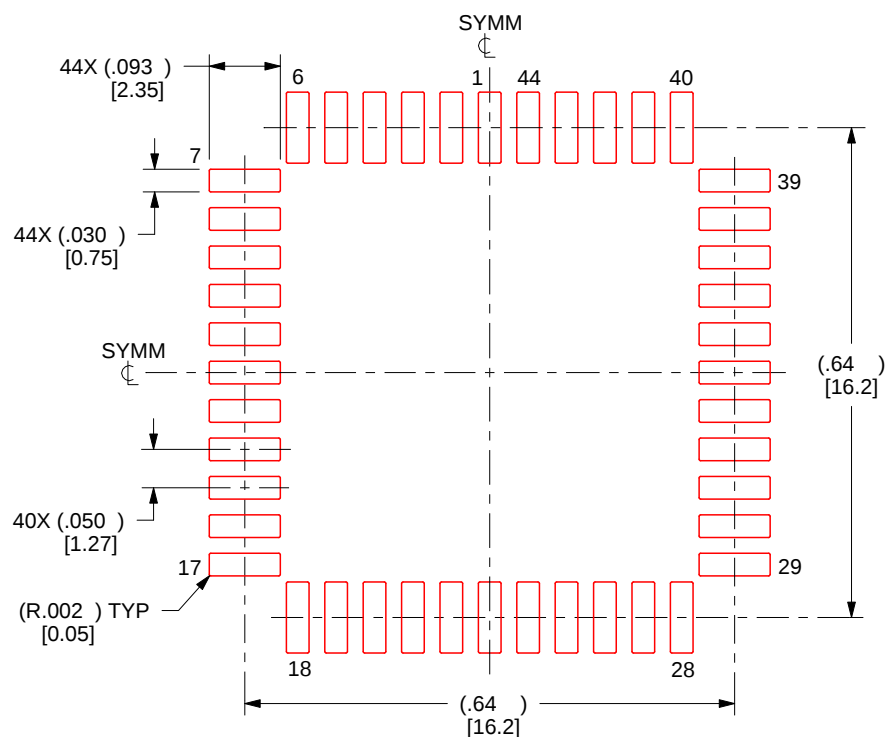
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

FN0044A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:4X

4215154/A 04/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

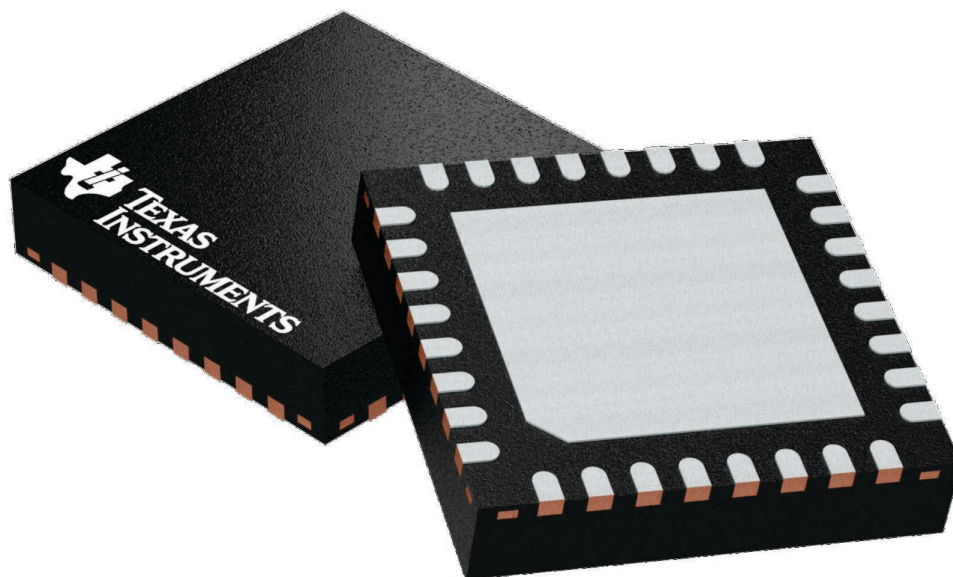
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A

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