dsPIC33EPXXGS50X FAMILY

dsPIC33EPXXGS50X Family
Silicon Errata and Data Sheet Clarification

The dsPIC33EPXXGS50X family devices that you have received conform functionally to the current Device Data Sheet (DS70005127**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of dsPIC33EPXXGS50X family silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**C0**).

Data Sheet clarifications and corrections start on Page 22, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select _Programmer > Reconnect_.
   b) For MPLAB X IDE, select _Window > Dashboard_ and click the **Refresh Debug Tool Status** icon (🔃).
5. Depending on the development tool used, the part number _and_ Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various silicon revisions of the dsPIC33EPXXGS50X family are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID[1]	Revision ID for Silicon Revision[2]		
		B2	**B3**	**C0**
dsPIC33EP16GS502	0x4E01			
dsPIC33EP16GS504	0x4E02			
dsPIC33EP16GS505	0x4E02			
dsPIC33EP16GS506	0x4E03			
dsPIC33EP32GS502	0x4E11			
dsPIC33EP32GS504	0x4E12	0x4005	0x4006	0x4007
dsPIC33EP32GS505	0x4E12			
dsPIC33EP32GS506	0x4E13			
dsPIC33EP64GS502	0x4E21			
dsPIC33EP64GS504	0x4E22			
dsPIC33EP64GS505	0x4E22			
dsPIC33EP64GS506	0x4E23			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the _"dsPIC33EPXXGS50X Family Flash Programming Specification"_ (DS70005160) for detailed information on Device and Revision IDs for your specific device.

dsPIC33EPXXGS50X FAMILY

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				B2	B3	C0
Auxiliary PLL	APLL Lock	1.	The APLL lock bit is asserted directly after enabling the APLL.	X	X	X
CPU	`div.sd`	2.	When using the signed 32-by-16-bit division instruction, `div.sd`, the Overflow bit is not getting set when an overflow occurs.	X	X	X
CPU	`DO` Loop	3.	PSV access, including Table Reads or Writes in the first or last instruction of a `DO` loop, is not allowed.	X	X	X
—	—	4.	—			
Comparator	EXTREF	5.	The comparator does not function when the external reference is used as the DAC reference voltage.	X	X	
I²C	Slave Mode	6.	Bus data can get corrupted when they match with one of the slave addresses connected to the bus.	X	X	
PWM	PWM Module Enabled	7.	A glitch may be observed on the PWM pins when the PWM module is enabled after assignment of pin ownership to the PWM module.	X	X	X
Input Capture	Cascade Mode	8.	When ICx is used in Cascaded mode, the even timer does not increment immediately when the odd timer rolls over, but instead, increments one cycle after the rollover.	X	X	X
PWM	Push-Pull Mode	9.	When EIPU = 0, a period update may produce back-to-back pulses.	X	X	
Input Capture	Synchronous Cascade Mode	10.	An even numbered timer does not reset on a source clock rollover in a synchronous cascaded operation.	X	X	X
Output Compare	PWM Mode	11.	In the scaled down timer source for the output compare module, the first PWM pulse may not appear on the OCx pin.	X	X	X
Output Compare	Interrupt	12.	Under certain circumstances, an output compare match may cause the Output Compare x Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin.	X	X	X
PWM	Redundant/ Push-Pull Output Mode	13.	Changing the duty cycle value from a non-zero value to zero will produce a glitch pulse equal to one PWM clock.	X	X	X
PWM	Trigger Compare Match	14.	The first PWM/ADC trigger event on a TRIGx/STRIGx match may not occur under certain conditions.	X	X	X
UART	Break Character Generation	15.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.	X	X	X
ADC	ADC Sampling	16.	Under specific conditions, multi-core ADC sampling crosstalk noise might be present.	X	X	X
PWM	Push-Pull Mode	17.	When EIPU = 1, Period register writes may produce back-to-back pulses under certain conditions.	X	X	X
I²C	Slave Mode	18.	In 10-Bit Addressing Slave mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence.	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				B2	B3	C0
I^{2}C	Slave Receive Mode	19.	The Acknowledge Time Status bit (ACKTIM) is asserted only if Address Hold Enable (AHEN) or Data Hold Enable (DHEN) is enabled.	X	X	
PWM	Master Time Base Mode	20.	Changes to the PHASEx register after enabling the PWM module may result in abnormal PWM switching waveforms.	X	X	X
ADC	DNL	21.	DNL is out of specification at the mid-code boundary in Single-Ended mode.	X	X	X
PWM	Center-Aligned Complementary	22.	Dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when SWAP mode is disabled.	X	X	X
ADC	Single-Ended Offset Error	23.	Offset error is out of specification in Single-Ended mode.	X		
CPU	Variable Interrupt Latency	24.	When Variable Interrupt Latency is selected (VAR = 1), an address error trap or incorrect application behavior may occur.	X	X	X
CPU	Context Switching	25.	When nesting more than one interrupt (without the Alternate Working register set) within the interrupts which are using Alternate Working register sets, there will be an unexpected change in the CCTXI[2:0] bits in the CTXTSTAT register while returning from the highest priority interrupt.	X	X	X
I^{2}C	Address Hold	26.	In Slave mode when AHEN = 1 (Address Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.	X	X	
I^{2}C	Data Hold	27.	In Slave mode when DHEN = 1 (Data Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of data reception, then a slave interrupt will not occur after the 8th clock.	X	X	
SPI	SPI Enable	28.	When SPI is enabled for the first time, there may be a spurious clock on the SCK which causes mismatch between the clock and data lines.	X	X	X
Comparator	Comparator Output Jitter	29.	The comparator module may generate erroneous triggers/interrupts.	X	X	
I/O	5V Tolerant	30.	Limited input current to I/O pins that support 5V operation.	X	X	X
I/O	Schmitt Trigger	31.	Schmitt Trigger output may produce glitches.	X	X	
I^{2}C	Bus Collisions	32.	In Slave mode, false bus collision triggers are generated when bus collision is enabled (SBCDE = 1).	X	X	
I^{2}C	Hold Time	33.	Minimum hold time of 300 ns is not achieved when the Data Hold Time bit (SDAHT) is set.	X	X	
ADC	Oversampling Filter	34.	Parallel operation of the two oversampling filters results in missing data writes to the lower priority ADC Digital Filter x Control register.	X	X	X
I^{2}C	Slave Mode	35.	In Slave mode, false bus collision triggers are generated when the bus collision is enabled (SBCDE = 1) and a Stop bit is received.			X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2:   SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				B2	B3	C0
I^{2}C	Slave Mode	36.	In Slave mode, the Bus Collision bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).	X	X	X
I^{2}C	Slave Mode	37.	In Slave mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, a slave interrupt is asserted at the 9th falling edge of the clock.			X
I^{2}C	Slave Mode	38.	In Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).	X	X	X
SPI	Master Mode	39.	Received data are shifted by one bit when the Clock Polarity Select bit is set (CKP = 1) and the Clock Edge Select bit is cleared (CKE = 0).	X	X	X
CPU	Data Flash Reads	40.	Given a specific set of preconditions, when two or more data Flash read instructions (via Program Space Visibility (PSV) read or table read) are executed back-to-back, one or more subsequent instructions will be misexecuted.	X	X	X
PWM	Push-Pull Mode	41.	PWM generators may exhibit an incorrect phase relationship when configured in Push-Pull mode.			X
I^{2}C	I/O Voltage Threshold	42.	With SMBus disabled, the I^{2}C V$_{ILMAX}$ threshold may be lower than 0.3 V$_{DD}$.	X	X	X
PLL	PLL	43.	The PLL may temporarily be out of specification during the oscillator switchover event.	X	X	X

Note 1:   Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**C0**).

1. Module: Auxiliary PLL

The Auxiliary PLL Lock bit (ACLKCON[14]) is asserted directly after enabling the APLL module (ACLKCON[15]).

Work around

Add a 50 µs delay routine after enabling the APLL lock bit.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

2. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the Overflow bit does not always get set when an overflow occurs.

This erratum only affects operations in which at least one of the following conditions is true:

a) Dividend and divisor differ in sign,

b) Dividend > 0x3FFFFFFF or

c) Dividend < 0xC0000000.

Work around

The application software must perform both the following actions in order to handle possible undetected overflow conditions:

a) The value of the dividend must always be constrained to be in the following range: $0xC0000000 \leq$ Dividend $\leq 0x3FFFFFFF$.

b) If the dividend and divisor differ in sign (e.g., dividend is negative and divisor is positive), then after executing the `div.sd` instruction or the compiler built-in function, `__builtin_divsd()`, inspect the sign of the resultant quotient.

If the quotient is found to be a positive number, then treat it as an overflow condition.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

3. Module: CPU

Table Write (`TBLWTx`), Table Read (`TBLRDx`) and PSV Flash read instructions should not be used in the first or last instruction locations of a `DO` loop.

Work around

None.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

4. Module: —

Silicon errata issue 4 has been corrected and does not apply to the current silicon revision.

Affected Silicon Revisions

B2	B3	C0					

5. Module: Comparator

When the External Voltage Reference bit is enabled (EXTREF = 1) in the CMPxCON[5] register, the dedicated Digital-to-Analog Converter (DAC) will not be connected to the respective analog comparators' inverting/negative input terminals.

Work around

Configure the External Reference bit, EXTREF = 0 in the CMPxCON[5] register, to select AV$_{DD}$ as the reference for the respective Digital-to-Analog Converter (DAC).

Affected Silicon Revisions

B2	B3	C0					
X	X						

6. Module: I²C

In applications with multiple I²C slaves, bus data can become corrupted when the data payload sent to an addressed slave device matches the bus address of another (unaddressed) slave device.

Work around

Keep track of the bus address and data phases in software. When Address Hold Enable is used (the AHEN bit is set), the application can assert a NACK for any of the received bytes (invalid addresses and data bytes for other slave devices) until a Stop bit is received.

Affected Silicon Revisions

B2	B3	C0					
X	X						

7. Module: PWM

The PENH and PENL bits in the IOCONx register are used to assign ownership of the pins to either the PWM module or the GPIO module. The correct procedure to configure the PWM module is to first assign pin ownership to the PWM module and then enable it using the PTEN bit in the PTCON register.

If the PWM module is enabled using the above sequence, then a glitch may be observed on the PWM pins before the actual switching of the PWM outputs begins. This glitch may cause a momentary turn-on of power MOSFETs that are driven by the PWM pins and may cause damage to the application hardware.

Work around

Perform the following steps to avoid any glitches from appearing on the PWM outputs at the time of enabling:

1. Configure the respective PWM pins to digital inputs using the TRISx registers. This step will put the PWM pins in a high-impedance state. The PWM outputs must be maintained in a safe state by using pull-up or pull-down resistors.

2. Assign pin ownership to the GPIO module by configuring the PENH bit (IOCONx[15] = 0) and the PENL bit (IOCONx[14] = 0).

3. Specify the PWM override state to the desired safe state for the PWM pins using the OVRDAT[1:0] bits field in the IOCONx register.

4. Override the PWM outputs by setting the OVRENH bit (IOCONx[9] = 1) and the OVRENL bit (IOCONx[8] = 1).

5. Enable the PWM module by setting the PTEN bit (PTCON[15] = 1).

6. Remove the PWM overrides by making the OVRENH bit (IOCONx[9] = 0) and the OVRENL bit (IOCONx[8] = 0).

7. Ensure a delay of at least one full PWM cycle.

8. Assign pin ownership to the PWM module by setting the PENH bit (IOCONx[15] = 1) and the PENL bit (IOCONx[14] = 1).

The code in Example 1 illustrates the use of this work around.

EXAMPLE 1: CONFIGURE PWM MODULE TO PREVENT GLITCHES ON PWM1H AND PWM1L PINS AT THE TIME OF ENABLING

```
TRISAbits.TRISA4 = 1;      // Configure PWM1H/RA4 as digital input
                           // Ensure output is in safe state using pull-up or pull-down resistors
TRISAbits.TRISA3 = 1;      // Configure PWM1L/RA3 as digital input
                           // Ensure output is in safe state using pull-up or pull-down resistors

IOCON1bits.PENH = 0;       // Assign pin ownership of PWM1H/RA4 to GPIO module
IOCON1bits.PENL = 0;       // Assign pin ownership of PWM1L/RA3 to GPIO module

IOCON1bits.OVRDAT = 0;     // Configure PWM outputs override state to the desired safe state

IOCON1bits.OVRENH = 1;     // Override PWM1H output
IOCON1bits.OVRENL = 1;     // Override PWM1L output

PTCONbits.PTEN = 1;        // Enable PWM module

IOCON1bits.OVRENH = 0;     // Remove override for PWM1H output
IOCON1bits.OVRENL = 0;     // Remove override for PWM1L output

Delay(x);                  // Introduce a delay greater than one full PWM cycle

IOCON1bits.PENH = 1;       // Assign pin ownership of PWM1H/RA4 to PWM module
IOCON1bits.PENL = 1;       // Assign pin ownership of PWM1L/RA3 to PWM module
```

Example 1 applies when the PWMLOCK Configuration bit is disabled. If the PWMLOCK bit is enabled, unlock/lock routines are required to write to the IOCONx registers.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

8. Module: Input Capture

When the IC is used in Cascaded mode, the even timer does not increment immediately when the odd timer rolls over, but instead, occurs one cycle after the rollover.

In the cascaded configuration, ICy:ICx (ICy represents the even numbered modules and ICx represents the odd numbered modules) form a single 32-bit module. In such a configuration, when ICx counts for a 16-bit value (65535 cycles) and rolls over to 0 during the next clock cycle (65536th cycle), ICy should immediately increment by 1. Instead, the ICy timer remains at 0, and during the next clock cycle (65537th cycle), both ICx and ICy timers increment by 1.

Work around

None.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

9. Module: PWM

When the PWM module is configured for Push-Pull mode (IOCONx[11:10] = 0b10) with the Enable Immediate Period Update bit disabled (PTCON[10] = 0), and when operating in (ITB = 0) Master Time Base mode (PWMCONx[9] = 0), a write to the Period register occurs on the PWMx cycle boundaries. This may cause the push-pull output logic to produce back-to-back pulses on the PWMx pins.

Work around

Work around 1: Ensure that the Enable Immediate Period Update bit (PTCON [10] = 1) is set.

Work around 2: Configure the PWM phase-shift value (PHASEx[15:0]) with a value more than 0x0007.

When multiple PWM generators are configured in Push-Pull mode, configure the PWM phase-shift value (PHASEx[15:0]) with a value more than 0x0007 for the respective PWM generators.

Affected Silicon Revisions

B2	B3	C0					
X	X						

10. Module: Input Capture

The even numbered timer does not reset on a source clock rollover in Synchronous Cascaded mode operation.

In the cascaded configuration, ICy:ICx (ICy represents the even numbered modules and ICx represents the odd numbered modules), ICy and ICx form a single 32-bit module. In Synchronous Cascaded mode (IC32 = 1, ICTRIG = 0 and the SYNCSEL[4:0] bits are not equal to 0h), both timers, ICyTMR:ICxTMR, must reset on a Sync_trig input from the 32-bit source timers, but only the odd timer (ICxTMR) is getting reset on a Sync Trigger input.

Work around

None.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

11. Module: Output Compare

The first PWM pulse may not appear on the OCx pin if the timer source of the Output Compare x module is scaled down.

The first pulse on the OCx pin is missed in PWM mode when the timer source for the Output Compare x module is scaled down (1:8, 1:64 or 1:256) using the Timerx Input Clock Prescale Select bits, TCKPS[1:0] (TxCON[5:4]).

Work around

- Configure the prescaler for the source timer to 1:1 for output compare.
- The scaled down timer (1:8, 1:64 or 1:256) can be used as a source for the output compare.

### Affected Silicon Revisions

B2	B3	C0					
X	X	X					

12. Module: Output Compare

Under certain circumstances, an output compare match may cause the Output Compare x Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin. This has been observed when all of the following are true:

- The module is in One-Shot mode (OCM[2:0] = 0b001, 0b010 or 0b100)
- One of the timer modules is being used as the time base
- A timer prescaler other than 1:1 is selected

If the module is re-initialized by clearing the OCM[2:0] bits after the One-Shot mode compare, the OCx pin may not be driven as expected.

Work around

After OCxIF is set, allow an interval (in CPU cycles) of at least twice the prescaler factor to elapse before clearing the OCM[2:0] bits. For example, for a prescaler value of 1:8, allow 16 CPU cycles to elapse after the interrupt.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

13. Module: PWM

In the Redundant Output mode (IOCONx[11:10] = 0b01) and Push-Pull Output mode (IOCONx[11:10] = 0b10), with the Immediate Update Enable bit disabled (PWMCONx[0] = 0), when the Duty Cycle register is updated from a non-zero value to zero, a glitch pulse of a width equal to one PWM clock will appear at the next PWM period boundary, as shown in Figure 1 (for the Redundant Output mode). The Duty Cycle register refers to the PDCx register if PWMCONx[8] = 0 or the MDC register if PWMCONx[8] = 1.

FIGURE 1: **EXAMPLE FOR REDUNDANT OUTPUT MODE**
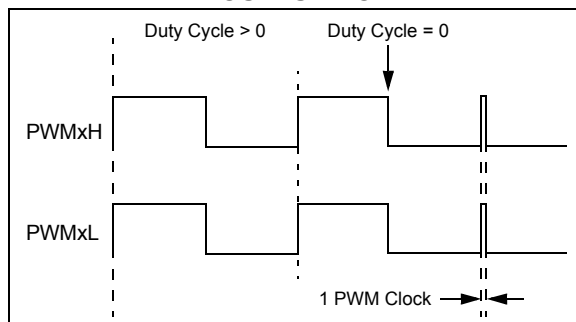
Work around

If the application requires a zero duty cycle output, there are two possible work around methods:

1. Use the PWM override feature to override the PWM output to a low state instead of writing to the Duty Cycle register. In order to switch back to a non-zero duty cycle output, turn off the PWM override. The override-on and override-off events must be timed close to the PWM period boundary if the IOCONx register has been configured with IOCONx[0] = 0 (i.e., output overrides through the OVDDAT[1:0] bits occur on the next CPU clock boundary).

2. Enable the Immediate Update Enable bit (PWMCONx[0] = 1) while configuring the PWMx module (i.e., before enabling the PWMx module, PTCON[15] = 1). With the Immediate Update enabled, writes to the Duty Cycle register can have an immediate effect on the PWM output. Therefore, the duty cycle write operations must be timed close to the PWM period boundary in order to avoid distortions in the PWM output.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

14. Module: PWM

The triggers generated by the PWMx Primary Trigger Compare Value register (TRIGx) and the PWMx Secondary Trigger Compare Value register (STRIGx) will not trigger at the point defined by the TRIGx/STRIGx register values on the first instance for the configurations listed below. Subsequent trigger instances are not affected.

- Trigger compare values for TRIGx, STRIGx are less than eight counts
- Trigger Output Divider bits, TRGDIV[3:0] (TRGCONx[15:12]), are greater than '0'
- Trigger Postscaler Start Enable Select bits, TRGSTRT[5:0] (TRGCONx[5:0]), are equal to '0'

Work around

Configure the PWMx Primary Trigger Compare Value Register (TRIGx) and PWMx Secondary Trigger Compare Value Register (STRIGx) values to be equal to or greater than eight.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

15. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.

For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA[11]), to be cleared instead of the TRMT bit (UxSTA[8]) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

16. Module: ADC

When using multiple ADC cores, if one of the ADC cores completes conversion while other ADC cores are still converting, the data in the ADC cores which are converting may be randomly corrupted.

Work around

Work around 1: When using multiple ADC cores, the ADC triggers are to be sufficiently staggered in time to ensure that the end of conversion of one or more cores doesn't occur during the conversion process of other cores.

Work around 2: For simultaneous conversion requirements, make sure the following conditions are met:

1. All the ADC cores for simultaneous conversion should have the same configurations.
2. Avoid shared ADC core conversion with any of the dedicated ADC cores. They can be sequential.
3. The trigger to initiate ADC conversion should be from the same source and at the same time.
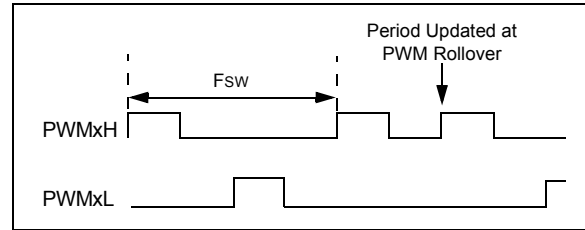
Affected Silicon Revisions

B2	B3	C0					
X	X	X					

17. Module: PWM

When the PWM module is configured for Push-Pull mode (IOCONx[11:10] = 0b10) with the Enable Immediate Period Update bit enabled (PTCON [10] = 1), a write to the Period register that coincides with the period rollover event may cause the push-pull output logic to produce back-to-back pulses on the PWMx pins (Figure 2).

FIGURE 2:

Work around

Ensure that the update to the PWM Period register occurs away from the PWM rollover event by setting the EIPU bit (PTCON[10] = 1). Use either the PWM Special Event Trigger (SEVTCMP) or the PWM Primary Trigger (TRIGx) to generate a PWM Interrupt Service Routine (ISR) near the start of the PWM cycle. This ISR will ensure that period writes do not occur near the PWM period rollover event.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

18. Module: I²C

In I²C Slave 10-Bit Addressing mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence. This issue is not seen during the reception of the lower address byte (A7 to A0) and data bytes.

The hardware asserts the ACKTIM on the falling edge of the eighth clock and deasserts on the rising edge of the ninth clock. In this case, ACKTIM is not asserted on the upper address byte reception. When AHEN = 1, the clock is stretched after the 8th falling edge and the ACKTIM bit is asserted until the clock is released. If AHEN = 0, the clock is not stretched and ACKTIM is asserted during the Acknowledgment sequence, which is of a short duration. Therefore, the user application can see this issue of the ACKTIM bit not getting asserted when AHEN = 1.

Work around

Instead of polling for ACKTIM to be asserted, poll for the RBF flag.

Affected Silicon Revisions

B2	B3	C0					
X	X						

19. Module: I²C

In I²C Slave Receive mode, the Acknowledge Time Status bit (ACKTIM) has no effect if Address Hold Enable (AHEN) and Data Hold Enable (DHEN) are disabled (AHEN = 0 and DHEN = 0). The Acknowledge Time Status bit (ACKTIM) is asserted only if Address Hold Enable (AHEN) or Data Hold Enable (DHEN) is enabled.

Work around

Instead of polling for the ACKTIM bit to be asserted, poll for the RBF flag.

Affected Silicon Revisions

B2	B3	C0					
X	X						

20. Module: PWM

In Edge-Aligned Complementary mode with master time base selected (PWMCONx[9] = 0), a reduction in phase shift, such that PHASEx becomes less than DTRx (or PDCx), will result in an abnormal PWM pulse at the next master period boundary.

Similarly, an increase in phase shift, such that PHASEx becomes greater than DTRx (or PDCx), will result in a reduced dead time for one PWM cycle at the next master period boundary. The amount of dead time is shown in Table 3.

In addition, dead time may also be impacted when updates to the PWMx Phase-Shift register occur while operating below the defined dead-time region.

With immediate updates disabled (PWMCONx[0] = 0), the abnormal pulse or reduced dead time may appear at the second master period boundary from when the write to PHASEx occurred.

Table 3 summarizes the expected PWM event that occurs at the master PWM period boundary when PHASEx is updated.

TABLE 3: EXPECTED PWM EVENTS

Condition	Event at Master Period Boundary	Result
$PHASEx < PHASEx_{(new)} < DTRx$	Reduced Dead Time	Dead Time = $DTRx - (PHASEx_{(new)} - PHASEx_{(old)})$
$PHASEx > PHASEx_{(new)} < DTRx$	Increased Dead Time	Dead Time = $DTRx + (PHASEx_{(old)} - PHASEx_{(new)})$
$PHASEx < DTRx, PHASEx_{(new)} > DTRx$	Reduced Dead Time	Dead Time = $PHASEx_{(old)}$
$PHASEx < PDCx, PHASEx_{(new)} > PDCx$	Reduced Dead Time	Dead Time = $PDCx + DTRx - PHASEx_{(new)}$
$PHASEx > DTRx, PHASEx_{(new)} < DTRx$	Abnormal PWM Pulse	Abnormal Pulse Width = $PHASEx_{(new)} - DTRx$
$PHASEx > PDCx, PHASEx_{(new)} < PDCx$	Abnormal PWM Pulse	Abnormal Pulse Width and Possibility for Reduced Dead Time (Zero Dead Time)

Work around

When modifying the PHASEx register on-the-fly, bound the PHASEx register to the following conditions: DTRx < PHASEx < PDCx.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

21. Module: ADC

When the ADC SAR core is configured to operate in Single-Ended mode, the core's DNL performance may be out of specification at the mid-code boundary.

Work around

None.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

22. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when SWAP is disabled under the following conditions:

• PWMx module is enabled (PTEN = 1)
• SWAP is enabled prior to this event

Work around

None.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

23. Module: ADC

When the ADC SAR core is configured to operate in Single-Ended mode, the core's offset error may be out of specification. The affected revisions have the following offset error specifications.

TABLE 4: ADC SAR CORE OFFSET ERROR

AD24b	E$_{OFF}$	Offset Error (Dedicated Core)	> 18	39	< 58	LSb	AV$_{SS}$ = 0V, AV$_{DD}$ = 3.3V
		Offset Error (Shared Core)	> 8	25	< 38	LSb	

Work around

None.

Affected Silicon Revisions

B2	B3	C0					
X							

24. Module: CPU

An address error trap or incorrect application behavior may occur if the variable exception processing latency is enabled by setting the VAR bit (CORCON[15] = 1).

Work around

Enable the Fixed Interrupt Latency mode by clearing the VAR bit (CORCON[15] = 0).

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

25. Module: CPU

When returning from an Interrupt Service Routine (ISR) by executing the RETFIE instruction, in the case of a nested interrupt, the Interrupt Priority Control bits (IPC[3:0]) associated with the lower priority interrupt are compared with the CTXTn bits field in the FLTREG Configuration register:

- If there is a match with either of the CTXTn bits field, then the corresponding Alternate Working Register Set is chosen and the Current Context Identifier bits (CCTXI[2:0]) in the CTXTSTAT register are updated to reflect the new Alternate Working Register Set.

- If there is no match with either of the CTXTn bits field, then the expected behavior is to keep the context (defined by the value of the Current Context Identifier bits, CCTXI[2:0] in the CTXTSTAT register) unchanged. However, the

context gets changed. A new context, corresponding to the value in the Manual Context Identifier bits (MCTXI[2:0]) in the CTXTSTAT register, is selected by the hardware and the CCTXI[2:0] bits in the CTXTSTAT register are modified to reflect this change.

When using interrupts with the Alternate Working Register Set (automatic context assignment), no more than one ISR without an Alternate Working Register Set must be nested within an ISR with an Alternate Working Register Set.

Issue and work around are illustrated in Figure 3 and Figure 4, respectively. The figures show the status bits, CCTXI[2:0] and MCTXI[2:0], after entering into an ISR from a lower priority ISR (left pane), and after returning to the same ISR from a higher priority ISR (right pane).

FIGURE 3: **MISMATCH OF WORKING REGISTER SET WHEN NESTING MORE THAN ONE INTERRUPT WITHIN INTERRUPTS THAT USE ALTERNATE WORKING REGISTER SETS**
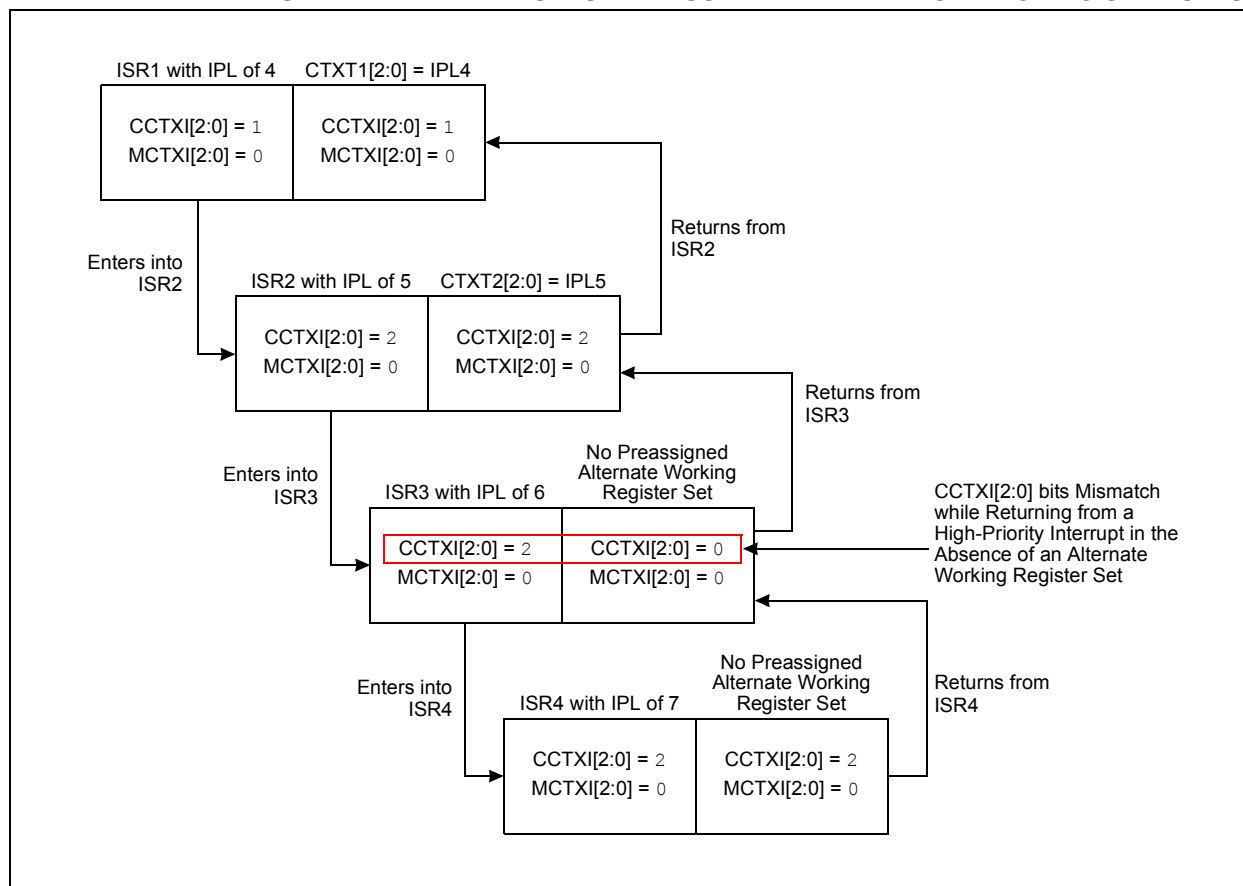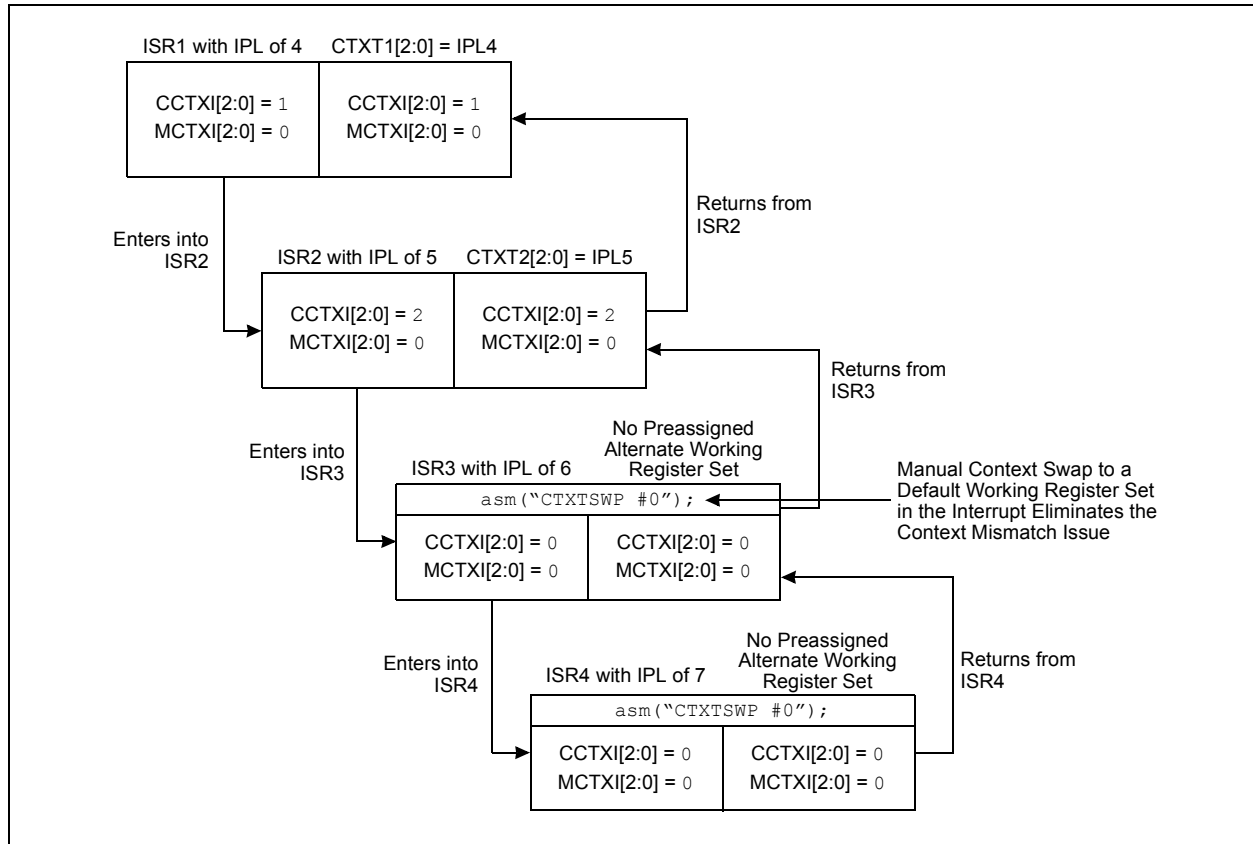
FIGURE 4: **WORK AROUND FOR MISMATCH OF WORKING REGISTER SET WHEN NESTING MORE THAN ONE INTERRUPT WITHIN INTERRUPTS THAT USE ALTERNATE WORKING REGISTER SETS**

Work around

Work around 1: When using interrupts with the Alternate Working Register Set, at the entry of all ISRs that do not have an Alternate Working Register Set and have a higher IPL level than the ISRs with an Alternate Working Register Set, perform a manual context swap to Context #0 as:

```
asm("CTXTSWP #0");
```

Note:	The application software must not perform a manual context swap (using the CTXTSWP instruction) to a context other than Context #0.

Work around 2: Always assign higher IPLs for the ISRs that use an Alternate Working Register Set than for the ISRs that do not use an Alternate Working Register Set.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

26. Module: I²C

In Slave mode, when AHEN = 1 (Address Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

B2	B3	C0					
X	X						

27. Module: I²C

In Slave mode, when DHEN = 1 (Data Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of data reception, then the slave interrupt will not occur after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

B2	B3	C0					
X	X						

28. Module: SPI

When SPI is enabled for the first time, there may be a spurious clock on the SCK. This may result in one bit of data shifted out on the data line, resulting in a mismatch between the clock and data lines.

This issue may also occur when the SPI is disabled during data transmission and enabled subsequently.

Work around

1. Disable the SPI module after two SPI cycles and then re-enable SPI; this will synchronize the clock and data.
2. If the SPI is configured on PPS pins, first enable the SPI without configuring the PPS, then allow two SPI clocks to pass and then configure the PPS to connect to the SPI module. This will prevent the spurious SPI clock going out on the pin. If the SPI module is turned off periodically, ensure to turn off the PPS as well.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

29. Module: Comparator

Analog comparator output may have a jitter when it is operating and this will generate erroneous triggers/interrupts. If the PWM module is configured to be controlled by an analog comparator, the output of the PWM generator may be affected by jitter in the analog comparator output.

Work around

Configure the Comparator Hysteresis Select bits, HYSSEL[1:0], as '0b11' (20 mV hysteresis) and set the Digital Filter Enable bit, FLTREN (CMPxCON[10]), to '1'.

Affected Silicon Revisions

B2	B3	C0					
X	X						

30. Module: I/O

Undesired pin failure may occur on the RC15, RD0, RD4, RD5, RD10, RD12 and RD15 5V tolerant I/O pins.

Work around

If 5V input operation is desired on I/O pins, RC15, RD0, RD4, RD5, RD10, RD12 and RD15, use a current-limiting resistor of at least 1 kOhm.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

31. Module: I/O

If the input signal rise or fall time is greater than 300 nS, the I/O Schmitt Trigger output may have glitches.

Work around

The rise/fall times must be less than 300 nS.

Affected Silicon Revisions

B2	B3	C0					
X	X						

32. Module: I²C

In Slave mode, false bus collision triggers are generated when bus collision is enabled (SBCDE = 1).

Work around

None.

Affected Silicon Revisions

B2	B3	C0					
X	X						

33. Module: I²C

Minimum hold time of 300 ns on SDAx after the falling edge of SCLx is not achieved when the Data Hold Time bit (SDAHT) is set.

Work around

None.

Affected Silicon Revisions

B2	B3	C0					
X	X						

34. Module: ADC

If both oversampling filters are configured identically and have different input channel selections (FLCHSEL[4:0] bits in the ADFLxCON register), and the channels start conversion from the same trigger source, then the lower priority filter result will not be written to the ADC Filter Output Data register. Both Data registers will contain the result from the higher priority filter (i.e., ADFL0DAT).

Work around

Ensure oversampling filters have input channels with different trigger sources and do not complete conversions simultaneously.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

35. Module: I²C

In Slave mode, false bus collision triggers are generated when the bus collision is enabled (SBCDE = 1) and a Stop bit is received.

Work around

Ignore the bus collision. Disable the I²C module and then re-enable the module.

Affected Silicon Revisions

B2	B3	C0					
		X					

36. Module: I²C

In Slave mode, the Bus Collision bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).

Work around

Disable the I²C module and then re-enable the module.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

37. Module: I²C

In Slave mode, with DHEN = 1 (Data Hold Enable), if software sends a NACK, a slave interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the slave interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

B2	B3	C0					
		X					

dsPIC33EPXXGS50X FAMILY

38. Module: I²C

In Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

39. Module: SPI

In Master mode, the SPI device reads the data on the SDIx line incorrectly; data are shifted by one bit (e.g., if 0x37 is transmitted, it is read as 0x1B).

The issue occurs for the following configuration: SMP = x, CKE = 0 and CKP = 1

Work around

When CKE = 0 and CKP = 1, use the following sequence to initiate SPI communication:

1. Set the slave select line to the Idle state.
2. Set the SCKx pin high.
3. Enable Master mode.
4. Enable the module.
5. Assert the slave select line.

If the SPI slave device does not use the $\overline{SSx}$ line, the SPI slave should be enabled only after the master clock line is made high.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

40. Module: CPU

> **Note:** This issue is deterministic based on the instruction sequence executed, and is not sensitive to manufacturing process, temperature, voltage or other application operating conditions that do not affect the instruction sequence.

When two or more data Flash read instructions (via Program Space Visibility (PSV) read or table read) are executed back-to-back, one or more subsequent instructions can be misexecuted when all of the conditions in Table 5 occur.

TABLE 5: REQUIRED CONDITIONS

1.	A PSV `MOV.D` instruction is executed with opcode at address ending in 0x0, 0x4, 0x8 or 0xC; and
2.	Some "connecting code" is executed (following the `MOV.D` of condition 1) with the properties:
	a) The connecting code does not include any program flow changes, including: taken branch instructions (including all versions of `BRA`, `CPBEQ`, `CPBGT`, `CPBLT`, `CPBNE`), `CALL`, `CALL.L`, `GOTO`, `GOTO.L`, `RCALL`, `RETLW`, `RETURN`, vectoring to an ISR, returning from an interrupt (`RETFIE`) and certain debug operations, such as `break` and `one-step`; and
	b) The connecting code does not include a `TBLRDx` or non-`MOV.D` PSV instruction located at a Flash memory address ending in 0x0, 0x4, 0x8 or 0xC; and
	c) The connecting code is at least two instruction words in length; and
	d) The connecting code does not end with a `REPEAT` instruction with count > 0; and
3.	≥ 2 back-to-back PSV or `TBLRDx` instructions are executed (following the code of condition 2), where the first of the back-to-back instructions is located at an address ending in 0x2, 0x6, 0xA or 0xE.

Figure 5 provides an example of the effective behavior.

FIGURE 5: SIMPLIFIED BEHAVIOR
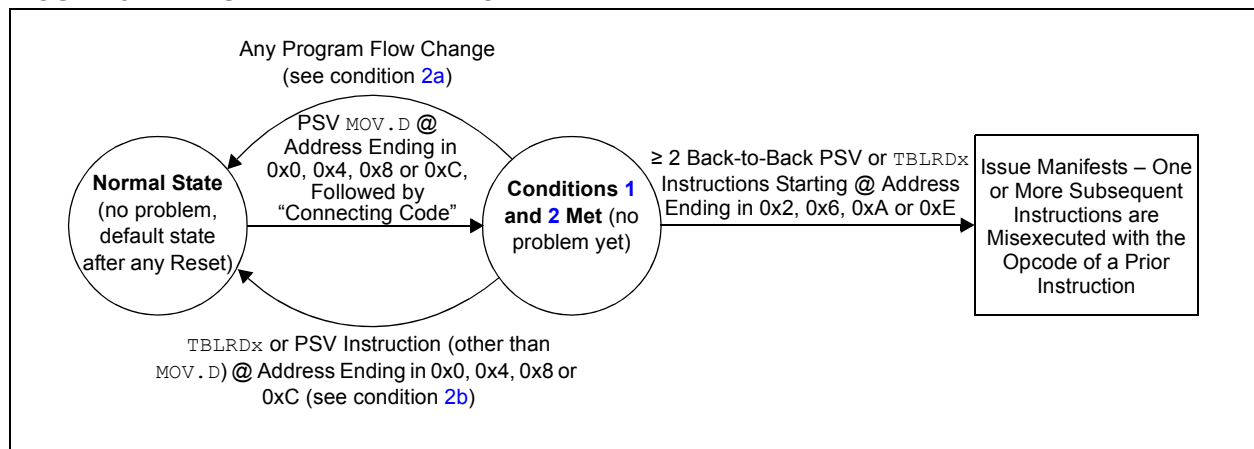
Work around

The issue can be avoided by ensuring any one or more of the requirements are not met. For example:

1. All instances of PSV `MOV.D` can be replaced with two PSV `MOV` instructions instead. Non-PSV `MOV.D` instructions acting on RAM/SFRs do not need to be modified; or

2. If not already present, a program flow change instruction (such as `BRA $+2`) can be inserted above back-to-back data Flash read sequences; or

3. Back-to-back data Flash read instruction sequences can be broken up by inserting a non-Flash read instruction (such as a `NOP`), in between the Flash read instructions; or

4. The alignment of the code can be shifted to avoid the required opcode location addresses.

C code built with MPLAB® XC16 Compiler Version 1.32, or later, implements the work around by default. However, if the application uses Assembly language routines, these should be manually modified to implement the work around. Additionally, if precompiled libraries are used, these should be built with XC16 Version 1.32 or later. For additional information, please visit: **www.microchip.com/erratum_psrd_psrd**

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

41. Module: PWM

When the PWMx Primary Phase-Shift register (PHASEx[15:0]) value is less than 0x0007 counts, PWM generators configured in Push-Pull mode (IOCONx[11:10] = `0b10`) may exhibit an incorrect phase relationship compared to other PWM generators.

Work around

Ensure that the PWMx Primary Phase-Shift register (PHASEx[15:0]) value is always greater than 0x0007 counts for all PWM generators configured in Push-Pull mode.

Affected Silicon Revisions

B2	B3	C0					
		X					

42. Module: I^{2}C

With SMBus disabled (SMEN (I2CxCONL[8]) = `0`), the I^{2}C V_{IL} maximum threshold may be lower than 0.3 V_{DD}.

With SMBus disabled as per the specification (DI18 parameter), the Maximum Input Low Voltage (V_{ILMAX}) specification for I/O pins with SDAx and SCLx should be 0.3 V_{DD}. However, for the I^{2}C to recognize low, the voltage should be driven to $\leq 0.8V$.

Work around

1. With SMBus disabled, the Maximum Input Low Voltage (V_{ILMAX}) threshold on SCLx and SDAx should be below 0.8V.

2. Enable SMBus (SMEN (I2CxCONL[8]) = `1`), then V_{ILMAX} will be 0.8V. This voltage is closer to 0.3 V_{DD}.

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

43. Module: PLL

When configuring the device to operate at or near maximum MIPS (55 < MIPS ≤ 70), using the on-chip PLL (Phase-Locked Loop), the PLL may temporarily be out of specification during the oscillator switchover event. This incorrect operating frequency may violate Flash access read times, which can result in instruction mis-execution, such as device Reset, address error trap or incorrect branching.

Work around

To avoid violating Flash access read times during the oscillator switchover event, the REPEAT instruction, followed by the NOP instruction, should be inserted immediately after initiating the clock switch, as shown in Example 2. This instruction sequence will ensure Flash is not being read during the clock switch event. The addition of the REPEAT/NOP instruction adds a few hundred microseconds (< 500 µs) to the overall oscillator switchover event (Parameter OS52 (T$_{LOCK}$), as mentioned in the data sheet).

EXAMPLE 2:   INSTRUCTION SEQUENCE CODE

```
// Initiate Clock Switch to Primary Oscillator with PLL (or Fast RC Oscillator with PLL, 0x01)
__builtin_write_OSCCONH(0x03);
__builtin_write_OSCCONL(OSCCON | 0x01);

// Immediately fetch repeat and NOP instructions. NOP executed during clock switch-over event,
// Flash read occurs only once ensuring no miss-execution of instructions
__asm__("REPEAT #0x7FFF \n NOP");

// Wait for Clock switch to occur (0x01 for FRC w/ PLL)
while (OSCCONbits.COSC != 0x03);

// Wait for PLL to lock
while (OSCCONbits.LOCK != 1);
```

Affected Silicon Revisions

B2	B3	C0					
X	X	X					

dsPIC33EPXXGS50X FAMILY

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005127**D**).

> **Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Pin Diagrams

A note has been added to the RB2 port pin, as shown below in **bold**. This note applies to RB2 on all available packages.

28-Pin SOIC

```
                ┌──────⌣──────┐
     MCLR ──█  1 │             │ 28  █── AVDD
      RA0 ──  2 │             │ 27   ── AVSS
      RA1 ──  3 │             │ 26  █── RA3
      RA2 ──  4 │   dsPIC33   │ 25  █── RA4
      RB0 ──  5 │  EPXXGS502  │ 24  █── RB14
      RB9 ──  6 │             │ 23  █── RB13
     RB10 ──  7 │             │ 22  █── RB12
      VSS ──  8 │             │ 21  █── RB11
      RB1 ──  9 │             │ 20   ── VCAP
  RB2(1) ── 10 │             │ 19   ── VSS
      RB3 ── 11 │             │ 18   ── RB7
      RB4 ──█ 12 │             │ 17   ── RB6
      VDD ── 13 │             │ 16   ── RB5
      RB8 ── 14 │             │ 15  █── RB15
                └─────────────┘
```
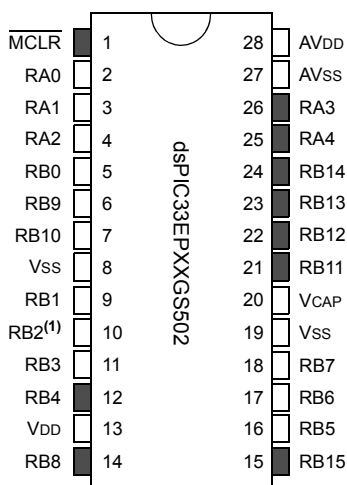
Pin	Pin Function	Pin	Pin Function
1	$\overline{\text{MCLR}}$	15	PGEC3/SCL2/RP47/RB15
2	AN0/PGA1P1/CMP1A/RA0	16	TDO/AN19/PGA2N2/RP37/RB5
3	AN1/PGA1P2/PGA2P1/CMP1B/RA1	17	PGED1/TDI/AN20/SCL1/RP38/RB6
4	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2	18	PGEC1/AN21/SDA1/RP39/RB7
5	AN3/PGA2P3/CMP1D/CMP2B/RP32/RB0	19	VSS
6	AN4/CMP2C/CMP3A/ISRC4/RP41/RB9	20	VCAP
7	AN5/CMP2D/CMP3B/ISRC3/RP42/RB10	21	TMS/PWM3H/RP43/RB11
8	VSS	22	TCK/PWM3L/RP44/RB12
9	OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/RP33/RB1	23	PWM2H/RP45/RB13
10	OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/RP34/RB2(1)	24	PWM2L/RP46/RB14
11	PGED2/AN18/DACOUT1/INT0/RP35/RB3	25	PWM1H/RA4
12	PGEC2/ADTRG31/EXTREF1/RP36/RB4	26	PWM1L/RA3
13	VDD	27	AVSS
14	PGED3/SDA2/FLT31/RP40/RB8	28	AVDD

Legend: Shaded pins are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.
Note 1: **At device power-up (POR), a pulse with an amplitude around 2V and a duration greater than 500 µs, may be observed on this device pin independent of pull-down resistors. It is recommended not to use this pin as an output driver unless the circuit being driven can endure this active duration.**

---

2. Module: Electrical Characteristics

The minimum value for Parameter DA01 External Voltage Reference has been changed from 0V to 1V, as shown below in **bold**.

TABLE 26-46: DACx MODULE SPECIFICATIONS

AC/DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Comments
DA01	EXTREF	External Voltage Reference	**1**	—	AV$_{DD}$	V	

3. Module: Electrical Characteristics

For Revision C0, the comparator hysteresis has been updated, as shown below in **bold**.

TABLE 26-45: HIGH-SPEED ANALOG COMPARATOR MODULE SPECIFICATIONS

AC/DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Comments
CM15	V$_{HYST}$	Input Hysteresis	**15**	**30**	**45**	mV	Depends on HYSSEL[1:0]

4. Module: Electrical Characteristics

For Table 26-5, the maximum filter capacitance is 10 µF, as shown below in **bold**.

TABLE 26-5: FILTER CAPACITOR (C$_{EFC}$) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Comments
	C$_{EFC}$	External Filter Capacitor Value[1]	4.7	—	**10**	µF	Capacitor must have a low series resistance ([1 ohm)

Note 1:   Typical V$_{CAP}$ Voltage = 1.8 volts when V$_{DD}$ ≥ V$_{DDMIN}$.

5. Module: Oscillator Configuration

The following notes have been added to **Figure 8-1: Oscillator System Diagram**:

Note 4:   The APLL module incorporates a new loss of lock feature that may generate a soft error trap at device power-up when the internal FRC is the reference clock. In the event the trap occurs, clearing the APLL bit (INTCON3[0]) will allow application firmware to continue executing. The APLL remains operational and within specified frequency limits. The APLL circuitry will automatically relock within 50 µs.

5:    If FRCSEL = 0 and the clock corresponding to POSCCLK is either not connected or has failed, then the FRC clock is selected as the clock source.

6.   **Module: High-Speed, 12-Bit Analog-to-Digital Converter (ADC)**

The following note has been added to **Register 19-26: ADTRIGxL: ADC Channel Trigger x Selection Register Low (x = 0 to 5)** and **Register 19-27: ADTRIGxH: ADC Channel Trigger x Selection Register High (x = 0 to 5)**:

Note 1:   The ADC module should be initialized and calibrated before the selected trigger source (PWM, output compare or timer) is enabled.

7.   **Module: High-Speed, 12-Bit Analog-to-Digital Converter (ADC)**

The following NRE bit has been added to **Register 19-1: ADCON1L: ADC Control Register 1 Low**:

bit 7   **NRE:** Noise Reduction Enable bit[2]

1 = Holds conversion process for 1 T_{ADCORE} when another core completes conversion to reduce noise between cores
0 = Noise reduction feature is disabled

   2:   Silicon Revision C0 and later support this feature.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2015)

Initial version of this document; issued for silicon revision B2.

Rev B Document (10/2015)

Adds silicon revision B3.

Adds new silicon issue 23 (ADC).

Rev C Document (3/2016)

Adds new silicon issues 24 (CPU), 25 (CPU), 26 (I^2C), 27 (I^2C), 28 (SPI) and 29 (Comparator).

Adds data sheet clarifications 1 (ADC), 2 (ADC Module Specifications) and 3 (Packaging Information).

Rev D Document (4/2017)

Adds new silicon issues 30 (I/O), 31 (I/O), 32 (I^2C) and 33 (I^2C).

Adds additional text following Example 1 in silicon issue 7 (PWM).

Removes silicon issue 4 (PWM) because the issue with dead time not being asserted when PDCx is updated has been corrected in the current silicon revision.

Rev E Document (8/2017)

Adds silicon revision C0.

Updates silicon issues 2 (CPU), 3 (CPU) and 20 (PWM).

Adds silicon issues 34 (ADC), 35 (I^2C), 36 (I^2C), 37 (I^2C), 38 (I^2C), 39 (SPI) and 40 (CPU).

Removes all previous data sheet clarifications because all issues have been corrected in the current device data sheet.

Adds data sheet clarification 1 (Pin Diagrams), 2 (Electrical Characteristics) and 3 (Electrical Characteristics).

Rev F Document (11/2017)

Adds data sheet clarifications 4 (Electrical Characteristics) and 5 (Oscillator Configuration).

Rev G Document (1/2018)

Adds silicon issue 41 (PWM).

Rev H Document (12/2018)

Adds silicon issue 42 (I^2C).

Rev J Document (6/2019)

Adds silicon issue 43 (PLL).

Adds data sheet clarifications 6 (High-Speed, 12-Bit Analog-to-Digital Converter (ADC)) and 7 (High-Speed, 12-Bit Analog-to-Digital Converter (ADC).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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