8-Channel Fault-Protected Analog Multiplexer

ADG528F

FEATURES

Low on resistance (300 Ω typical)
Fast switching times
  t_{ON}: 250 ns maximum
  t_{OFF}: 250 ns maximum
Low power dissipation (3.3 mW maximum)
Fault and overvoltage protection (−40 V to +55 V)
All switches off with power supply off
Analog output of on channel clamped within power supplies if an overvoltage occurs
Latch-up proof construction
Break-before-make construction
TTL and CMOS compatible inputs

APPLICATIONS

Existing multiplexer applications (both fault-protected and nonfault-protected)
New designs requiring multiplexer functions

FUNCTIONAL BLOCK DIAGRAM

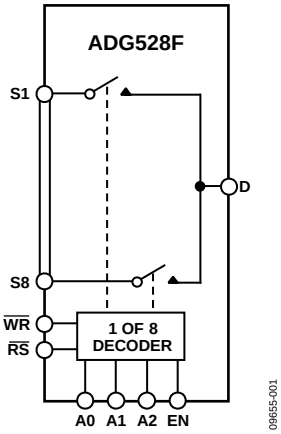

Figure 1.

GENERAL DESCRIPTION

The ADG528F[1] is a CMOS analog multiplexer, with the comprising eight single channels. This multiplexer provides fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs from −40 V to +55 V. During fault conditions, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources that drive the multiplexer.

The ADG528F switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The ADG528F has on-chip address and control latches that facilitate microprocessor interfacing. An EN input on the device is used to enable or disable the device. When disabled, all channels are switched off.

PRODUCT HIGHLIGHTS

1. Fault protection.
   The ADG528F can withstand continuous voltage inputs from −40 V to +55 V. When a fault occurs due to the power supplies being turned off, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. On channel turns off while fault exists.
3. Low R_{ON}.
4. Fast switching times.
5. Break-before-make switching.
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench isolation eliminates latch-up.
   A dielectric trench separates the p-channel and n-channel MOSFETs thereby preventing latch-up.

Rev. F
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REVISION HISTORY

7/11—Rev. E to Rev. F

Deleted ADG508F/ADG509F ... Universal
Changes to Table 3 ... 6
Added Table 4 ... 7
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 15

7/09—Rev. D to Rev. E

Updated Format ... Universal
Added TSSOP ... Universal
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 18

4/01—Data Sheet Changed from Rev. C to Rev. D.

Changes to Ordering Guide ... 1
Changes to Specifications Table ... 2
Max Ratings Changed ... 4
Deleted 16-Lead Cerdip from Outline Dimensions ... 11
Deleted 18-Lead Cerdip from Outline Dimensions ... 12

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	B Version +25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} + 3	V min	
		V_{DD} − 1.5	V max	
R_{ON}	300	350	Ω typ	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA; V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%
		400	Ω max	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA; V_{DD} = +15 V ± 5%, V_{SS} = −15 V ± 5%
R_{ON} Drift	0.6		%/°C typ	V_S = 0 V, I_S = 1 mA
R_{ON} Match	5		% max	V_S = 0 V, I_S = 1 mA
LEAKAGE CURRENTS				
Source Off Leakage I_S (Off)	±0.02		nA typ	V_D = ±10 V, V_S = ∓10 V;
	±1	±50	nA max	See Figure 19
Drain Off Leakage I_D (Off)	±0.04		nA typ	V_D = ±10 V, V_S = ∓10 V;
	±1	±60	nA max	See Figure 20
Channel On Leakage I_D, I_S (On)	±0.04		nA typ	V_S = V_D = ± 10 V;
	±1	±60	nA max	See Figure 21
FAULT				
Output Leakage Current	±0.02		nA typ	V_S = ±33 V, V_D = 0 V, see Figure 20
(With Overvoltage)	±2	±2	µA max	
Input Leakage Current	±0.005		µA typ	V_S = ±25 V, V_D = ∓10 V, see Figure 22
(With Overvoltage)	±2		µA max	
Input Leakage Current	±0.001		µA typ	V_S = ±25 V, V_D = V_{EN} = A0, A1, A2 = 0 V
(With Power Supplies Off)	±2		µA max	See Figure 23
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}		±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[1]				
$t_{TRANSITION}$	200		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	300	400	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; see Figure 24
t_{OPEN}	50		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	25	10	ns min	V_S = 5 V; see Figure 25
t_{ON} (EN, $\overline{WR}$)	200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	250	400	ns max	V_S = 5 V; see Figure 26
t_{OFF} (EN, $\overline{RS}$)	200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
t_{SETT}, Settling Time	250	400	ns max	V_S = 5 V; see Figure 26
0.1%		1	µs typ	R_L = 1 kΩ, C_L = 35 pF;
0.01%		2.5	µs typ	V_S = 5 V
t_W, Write Pulse Width	100	120	ns min	
t_S, Address, Enable Setup Time		100	ns min	
t_H, Address, Enable Hold Time		10	ns min	
t_{RS}, Reset Pulse Width		100	ns min	

Parameter	B Version +25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
Charge Injection	4		pC typ	V_S = 0 V, R_S = 0 Ω, C_L= 1 nF; see Figure 29
Off Isolation	68		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
	50		dB min	V_S = 7 V rms; see Figure 30
C_S (Off)	5		pF typ	
C_D (Off)	50		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.1	0.2	mA max	V_{IN} = 0 V or 5 V
I_{SS}	0.1	0.1	mA max	

[1] Guaranteed by design, not subject to production test.

TRUTH TABLE

Table 2. ADG528F Truth Table[1]

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
X	X	X	X	↑	1	Retains previous switch condition
X	X	X	X	X	0	None (address and enable latches cleared)
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

[1] X = don't care.

TIMING DIAGRAMS

Figure 2 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$. Figure 3 shows the reset pulse width, t_{RS}, and the reset turnoff time, t_{OFF} ($\overline{RS}$). Note that all digital input signals rise and fall times are measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.

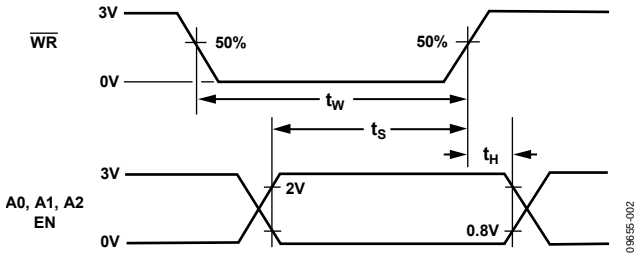


Figure 2. Timing Sequence for Latching the Switch Address and Enable Inputs

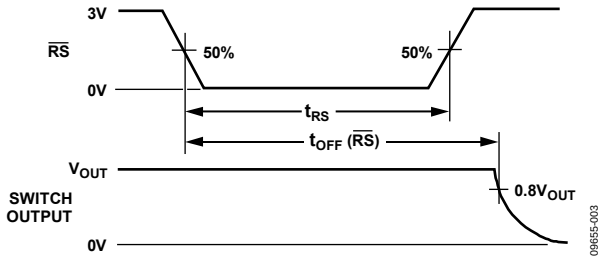


Figure 3. Reset Pulse Width

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Digital Input, EN, Ax	−0.3 V to V_{DD} + 2 V or 20 mA, whichever occurs first
V_S, Analog Input Overvoltage with Power On (V_{DD} = +15 V, V_{SS} = −15 V)	V_{SS} − 25 V to V_{DD} + 40 V
V_S, Analog Input Overvoltage with Power Off (V_{DD} = 0 V, V_{SS} = 0 V)	−40 V to +55 V
Continuous Current, S or D	20 mA
Peak Current, S or D	
(Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA}, Thermal Impedance	90°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

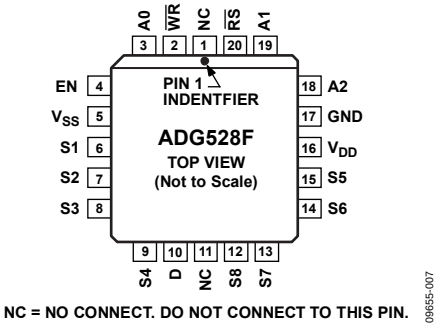


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. This pin is open.
2	$\overline{WR}$	Write. The $\overline{WR}$ signal latches the state of the address control lines and the enable line.
3	A0	Logic Control Input.
4	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
5	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
6	S1	Source Terminal 1. This pin can be an input or an output.
7	S2	Source Terminal 2. This pin can be an input or an output.
8	S3	Source Terminal 3. This pin can be an input or an output.
9	S4	Source Terminal 4. This pin can be an input or an output.
10	D	Drain Terminal. This pin can be an input or an output.
11	NC	No Connect. This pin is open.
12	S8	Source Terminal 8. This pin can be an input or an output.
13	S7	Source Terminal 7. This pin can be an input or an output.
14	S6	Source Terminal 6. This pin can be an input or an output.
15	S5	Source Terminal 5. This pin can be an input or an output.
16	V_{DD}	Most Positive Power Supply Potential.
17	GND	Ground (0 V) Reference.
18	A2	Logic Control Input.
19	A1	Logic Control Input.
20	$\overline{RS}$	Reset. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off).

TYPICAL PERFORMANCE CHARACTERISTICS

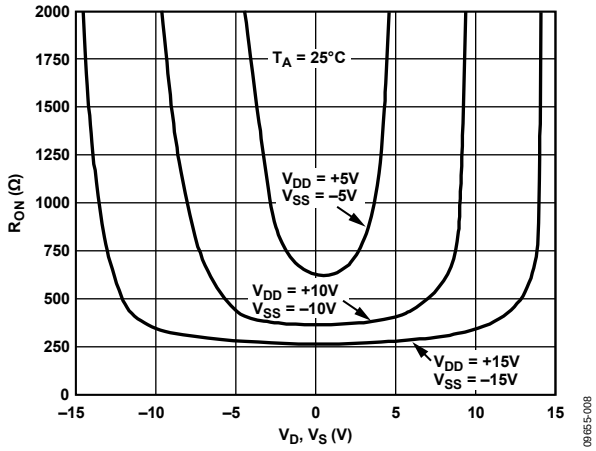


Figure 5. On Resistance as a Function of V_D (V_S)

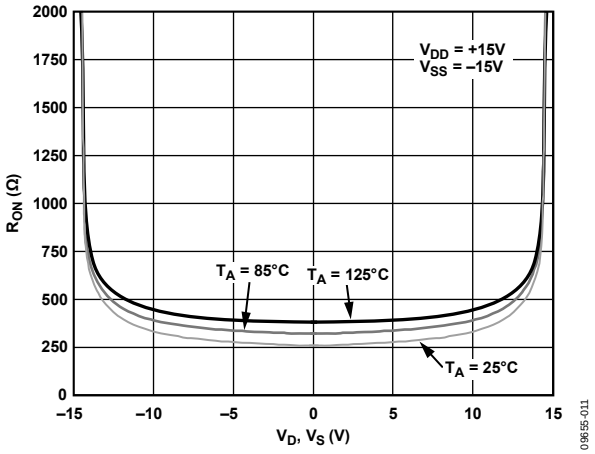


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures

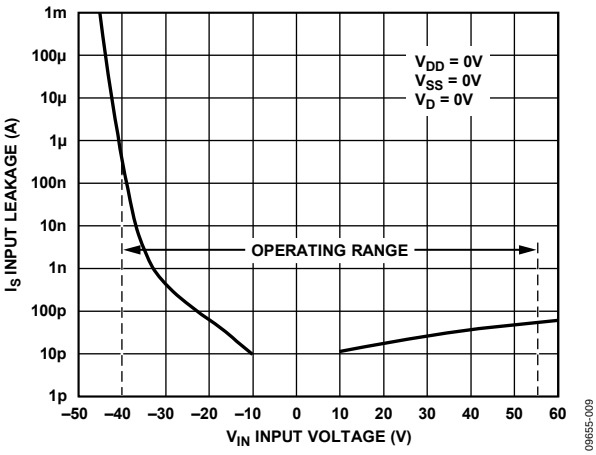


Figure 6. Input Leakage Current as a Function of V_S (Power Supplies Off) During Overvoltage Conditions

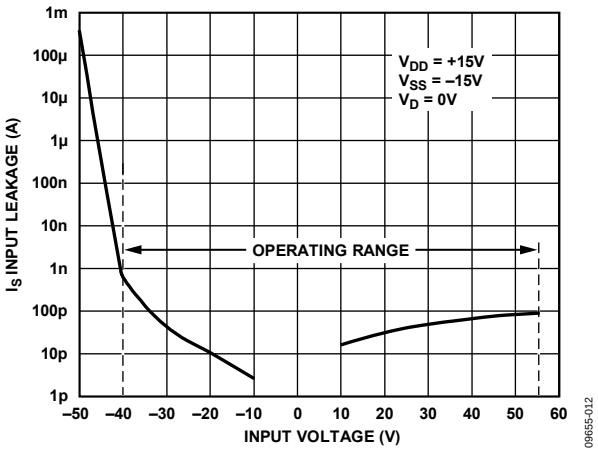


Figure 9. Input Leakage Current as a Function of V_S (Power Supplies On) During Overvoltage Conditions

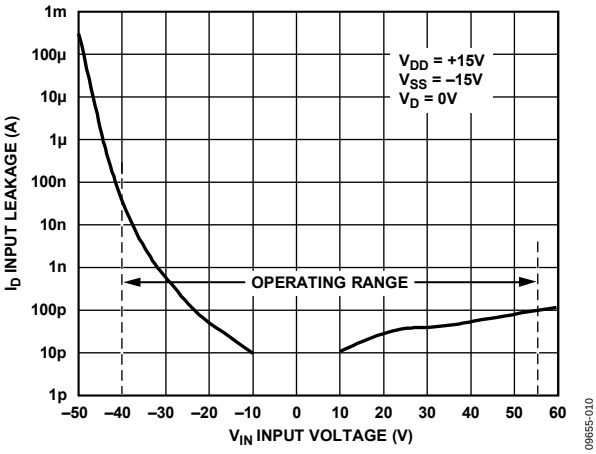


Figure 7. Output Leakage Current as a Function of V_S (Power Supplies On) During Overvoltage Conditions

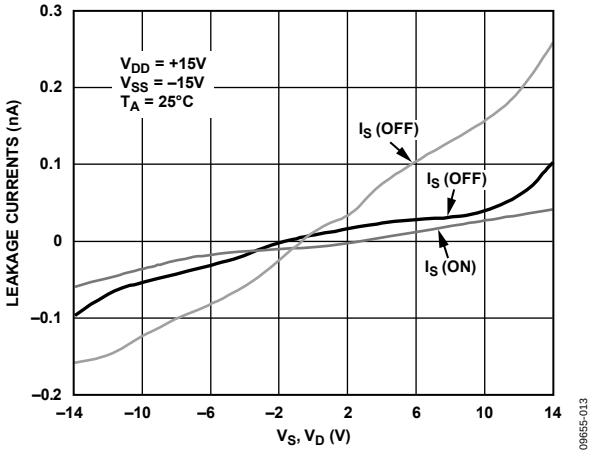


Figure 10. Leakage Currents as a Function of V_D (V_S)

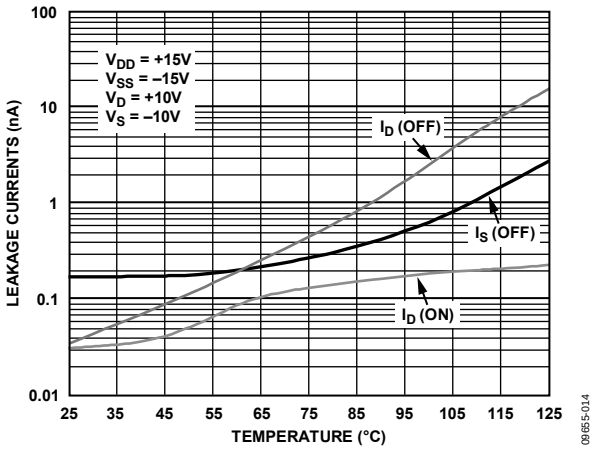


Figure 11. Leakage Currents as a Function of Temperature

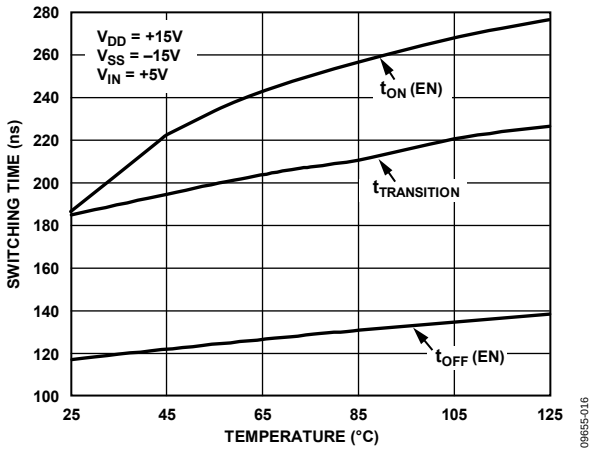


Figure 13. Switching Time vs. Temperature

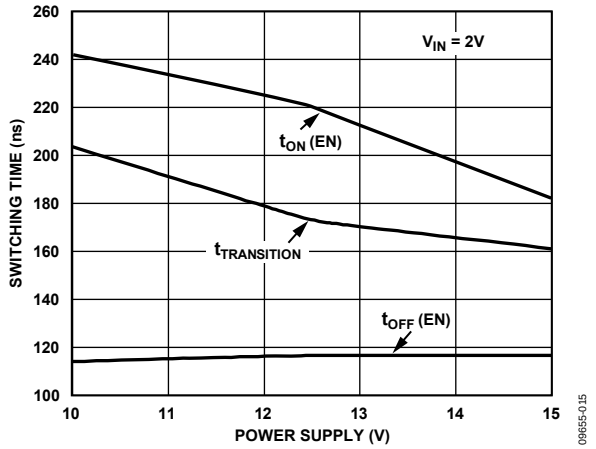


Figure 12. Switching Time vs. Power Supply

TERMINOLOGY

V_{DD}
Most positive power supply potential.

V_{SS}
Most negative power supply potential.

GND
Ground (0 V) reference.

R_{ON}
Ohmic resistance between D and S.

R_{ON} Drift
Change in R_{ON} when temperature changes by one degree Celsius.

R_{ON} Match
Difference between the R_{ON} of any two channels.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog Voltage on Terminal D and Terminal S.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{OPEN}
Off time measured between 80% points of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

THEORY OF OPERATION

The ADG528F multiplexer is capable of withstanding overvoltages from −40 V to +55 V, irrespective of whether the power supplies are present or not. Each channel of the multiplexer consists of an n-channel MOSFET, a p-channel MOSFET, and an n-channel MOSFET, connected in series. When the analog input exceeds the power supplies, one of the MOSFETs will switch off, limiting the current to submicroamp levels, thereby preventing the overvoltage from damaging any circuitry following the multiplexer. Figure 14 illustrates the channel architecture that enables these multiplexers to withstand continuous overvoltages.

When an analog input of V_{SS} + 3 V to V_{DD} − 1.5 V is applied to the ADG528F, the multiplexer behaves as a standard multiplexer, with specifications similar to a standard multiplexer, for example, the on-resistance is 400 Ω maximum. However, when an overvoltage is applied to the device, one of the three MOSFETs will turn off.

Figure 14 to Figure 17 show the conditions of the three MOSFETs for the various overvoltage situations. When the analog input applied to an on channel approaches the positive power supply line, the n-channel MOSFET turns off because the voltage on the analog input exceeds the difference between V_{DD} and the n-channel threshold voltage (V_{TN}). When a voltage more negative than V_{SS} is applied to the multiplexer, the p-channel MOSFET will turn off because the analog input is more negative than the difference between V_{SS} and the p-channel threshold voltage (V_{TP}). Because V_{TN} is nominally 1.5 V and V_{TP} is typically 3 V, the analog input range to the multiplexer is limited to −12 V to +13.5 V when a ±15 V power supply is used.

When the power supplies are present but the channel is off, again either the p-channel MOSFET or one of the n-channel MOSFETs will turn off when an overvoltage occurs.

Finally, when the power supplies are off, the gate of each MOSFET will be at ground. A negative overvoltage switches on the first n-channel MOSFET but the bias produced by the overvoltage causes the p-channel MOSFET to remain turned off. With a positive overvoltage, the first MOSFET in the series will remain off because the gate to source voltage applied to this MOSFET is negative.

During fault conditions, the leakage current into and out of the ADG528F is limited to a few microamps. This protects the multiplexer and succeeding circuitry from over stresses as well as protecting the signal sources, which drive the multiplexer. Also, the other channels of the multiplexer will be undisturbed by the overvoltage and will continue to operate normally.

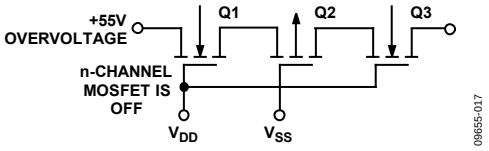


Figure 14. +55 V Overvoltage Input to the On Channel

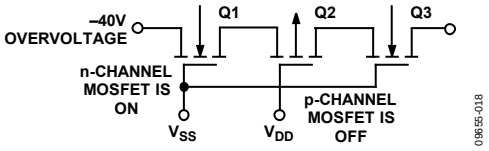


Figure 15. −40 V Overvoltage on an Off Channel with Multiplexer Power On

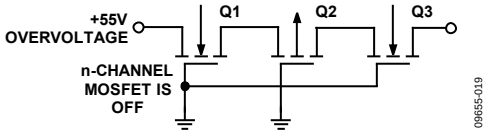


Figure 16. +55 V Overvoltage with Power Off

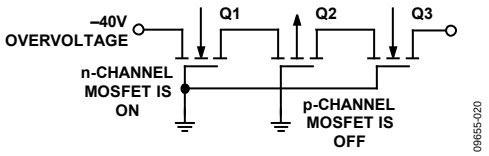


Figure 17. −40 V Overvoltage with Power Off

TEST CIRCUITS

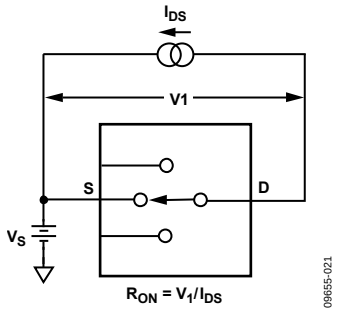


Figure 18. On Resistance

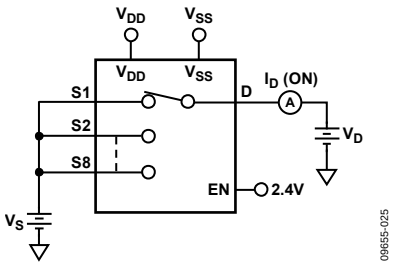


Figure 21. I_D (On)

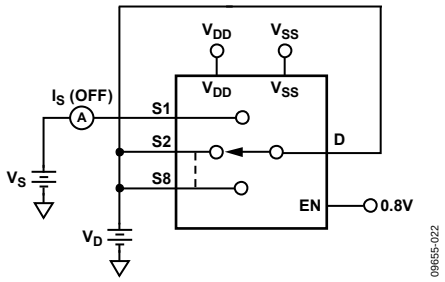


Figure 19. I_S (Off)

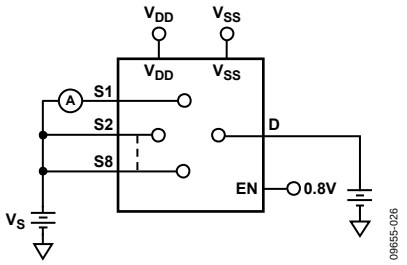


Figure 22. Input Leakage Current (with Overvoltage)

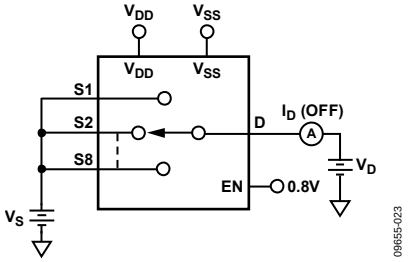


Figure 20. I_D (Off)

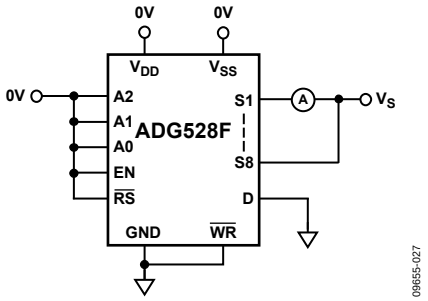


Figure 23. Input Leakage Current (with Power Supplies Off)

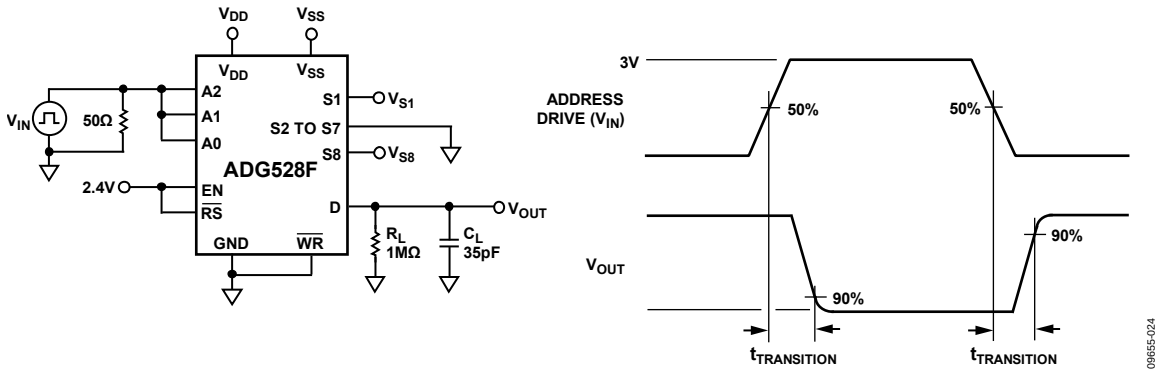


Figure 24. Switching Time of Multiplexer, $t_{TRANSITION}$

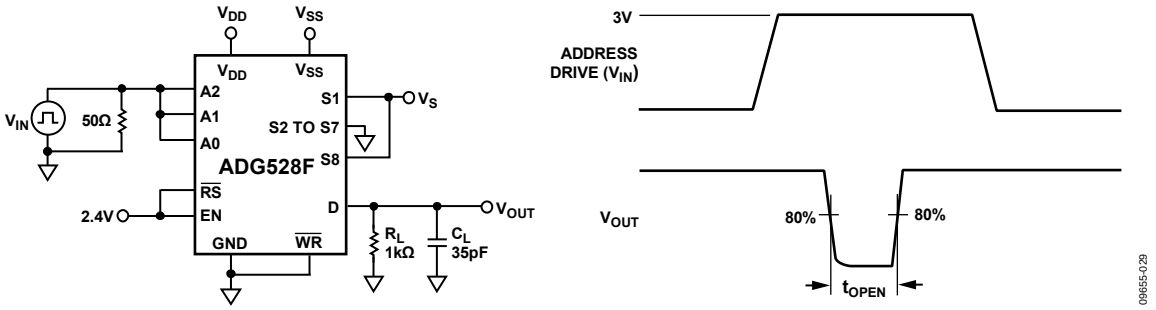


Figure 25. Break-Before-Make Delay, t_{OPEN}

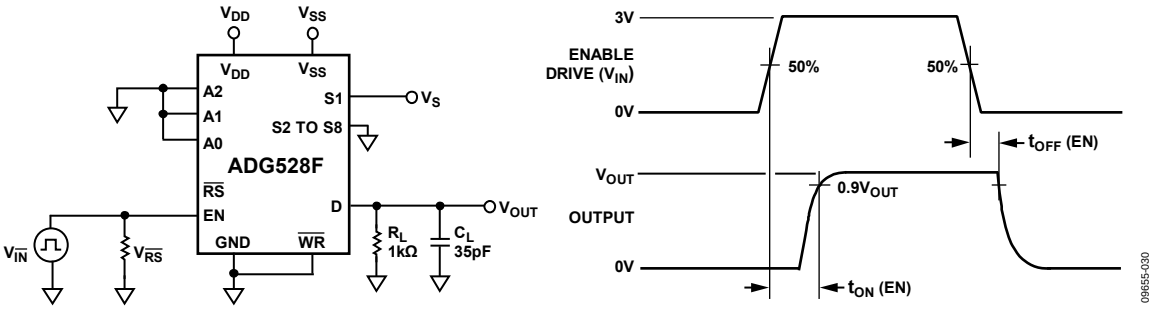


Figure 26. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

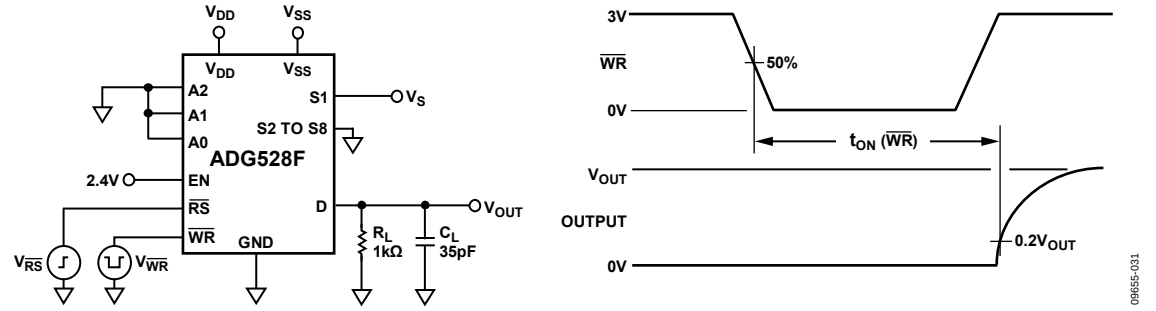


Figure 27. Write Turn-On Time, t_{ON} ($\overline{WR}$)

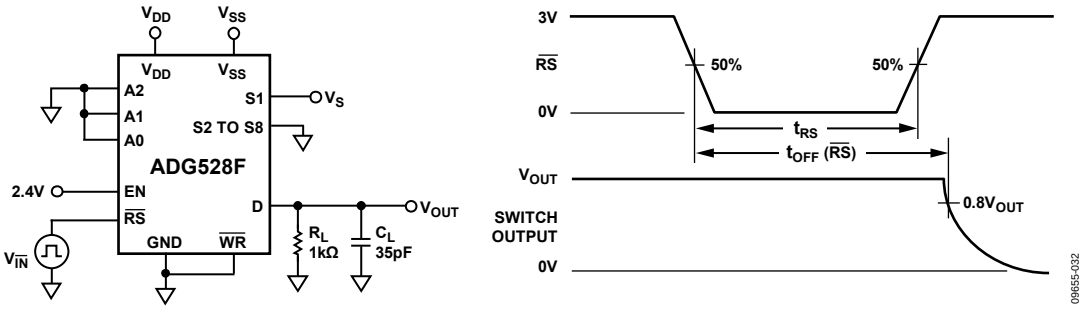


Figure 28. Reset Turn-Off Time, t_{OFF} ($\overline{RS}$)

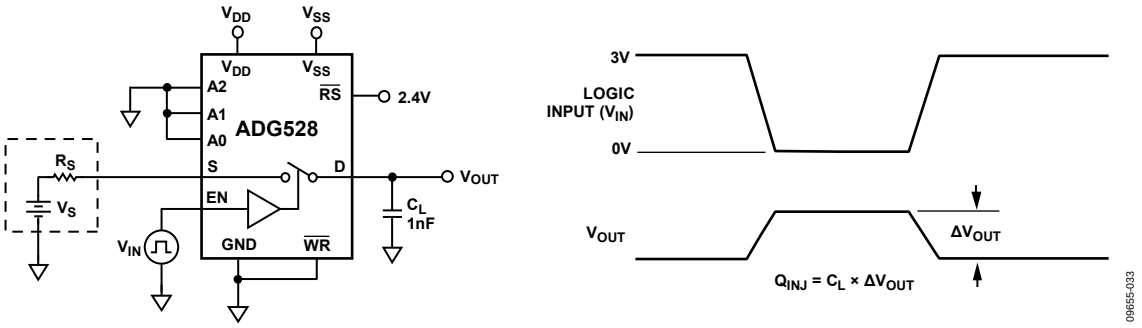


Figure 29. Charge Injection

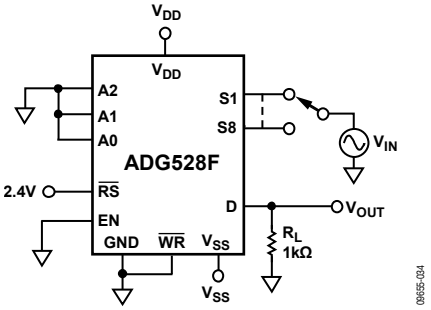
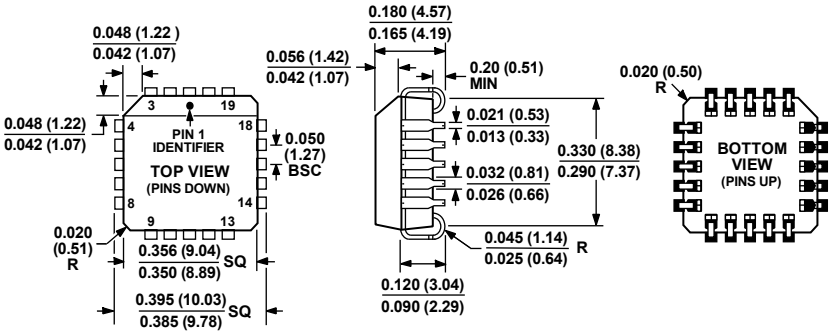


Figure 30. Off Isolation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-047-AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 31. 20-Lead Plastic Leaded Chip Carrier [PLCC] (P-20)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG528FBP	−40°C to +85°C	20-Lead PLCC	P-20
ADG528FBPZ	−40°C to +85°C	20-Lead PLCC	P-20

[1] Z = RoHS Compliant Part.

NOTES

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