IXYS

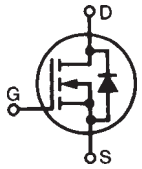
HiPerFET™ Power MOSFETs
ISOPLUS247™ Q CLASS

	V_{DSS}	I_{D25}	$R_{DS(on)}$
IXFR 12N100Q	1000 V	10 A	1.1 Ω
IXFR 10N100Q	1000 V	9 A	1.20 Ω

(Electrically Isolated Back Surface)

$t_{rr} \leq 300$ µs

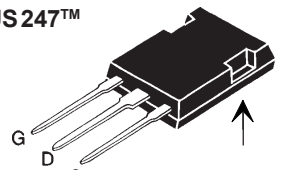
N-Channel Enhancement Mode
Avalanche Rated, High dV/dt
Low Gate Charge and Capacitances



Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		1000	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		1000	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	12N100	10	A
		10N100	9	A
I_{DM}	T_C = 25°C, Pulse width limited by T_{JM}	12N100	48	A
		10N100	40	A
I_{AR}	T_C = 25°C	12N100	12	A
		10N100	10	A
E_{AR}	T_C = 25°C		30	mJ
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \leq V_{DSS}$ $T_J \leq 150$°C, R_G = 2 Ω		5	V/ns
P_D	T_C = 25°C		250	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
T_L	1.6 mm (0.063 in.) from case for 10 s		300	°C
V_{ISOL}	50/60 Hz, RMS t = 1 min		2500	V~
Weight			5	g

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 3mA		1000			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4mA		2.5		5.5	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	V_{DS} = 0.8•V_{DSS}	T_J = 25°C			50	µA
	V_{GS} = 0 V	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = I_T$ Notes 1 & 2	12N100			1.1	Ω
		10N100			1.2	Ω

ISOPLUS 247™



Isolated back surface*

G = Gate D = Drain
S = Source

* Patent pending

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low drain to tab capacitance(<50pF)
- Low $R_{DS\ (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control

Advantages

- Easy assembly
- Space savings
- High power density

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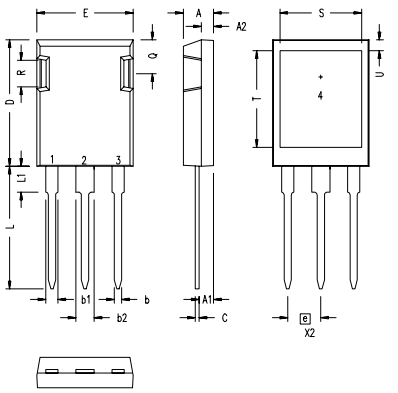
Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	min.	typ.	max.	
g_{fs}	V_{DS} = 15 V; $I_D = I_T$ Note 1	4	10		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2900		pF
C_{oss}			315		pF
C_{rss}			50		pF
$t_{d(on)}$	V_{GS} = 10 V, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = I_T$ R_G = 1 Ω (External),		20		ns
t_r			23		ns
$t_{d(off)}$			40		ns
t_f			15		ns
$Q_{g(on)}$	V_{GS} = 10 V, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = I_T$		90		nC
Q_{gs}			30		nC
Q_{gd}			40		nC
R_{thJC}				0.50	K/W
R_{thCK}			0.15		K/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	min.	typ.	max.	
I_S	V_{GS} = 0 V			12	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			48	A
V_{SD}	$I_F = I_S$, V_{GS} = 0 V, Note 1			1.3	V
t_{rr}	$I_F = I_s$, -di/dt = 100 A/μs, V_R = 100 V		200	300	ns
Q_{RM}			1.6		μC
I_{RM}			7		A

Note: 1. Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %
2. I_T test current: IXFR10N100 I_T = 5A
IXFR12N100 I_T = 6A

ISOPLUS 247 OUTLINE



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Note: Please see IXFH12N100Q Data Sheet for characteristic curves.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025



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